ATTACHMENT 1

STATEMENT FOR SECTION 15.37 OF THE RULES

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Date : January 20, 1999

Statement for Section 15.37 of the Rules

Equipment : Pager Receiver

FCC ID. : ODGBPX5ACL1

Concerning the FCC Part 15, section 15.37 transition provision, we, Hantel Co., Ltd., hereby confirm above referenced device as follows.

This device(Pager Receiver) subject to the regulations in FCC Part 15 that are manufactured on or after June 23, 1999 complies with new rules adopted under Docket 87-389.

This Device is not associated with a transmitter that could not have been authorized under regulations in effect prior to June 23, 1989. e.q., a transmitter operating under the provisions of section 15.209 or section 15.249 (below 960MHz).

This device is not scanning receivers or frequency converters designed or marketed for use with scanning receivers.

Best Regards

Hoe-Bum Kim, General Manager
Hantel Co., Ltd.

ATTACHMENT 2

PROPOSED FCC ID. LABEL AND MARKING

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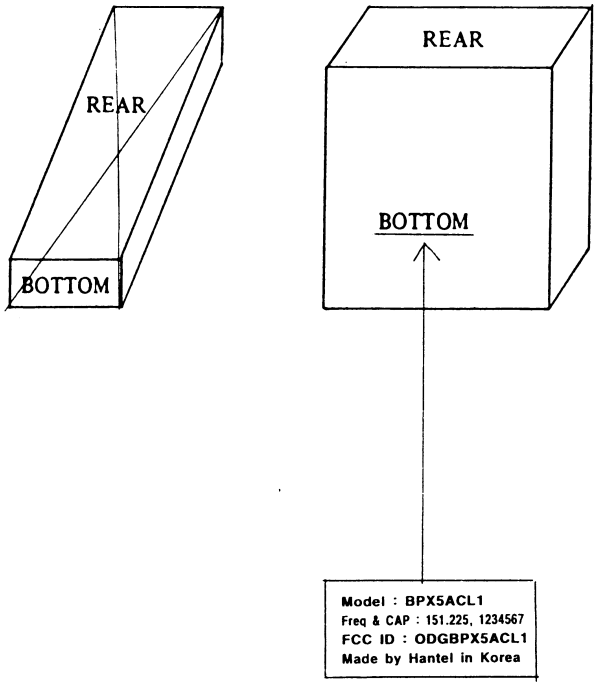


ATTACHMENT 3

MANUAL FOR INSTALLATION AND OPERATING INSTRUCTION

HANTEL POCSAG PAGER

Function button

Read button

Caution : Any changes or modifications in construction of this device which are not expressly approved by responsible for compliance could void the user's authority to operate the equipment.

This device complies with part 15 of the FCC Rules.
Operation is subject to the condition that this device dose not harmful interference

LCD display

LCD is consist of 8 icons, small clock display area and main 12 digits display.

Icons are;

: In range indication

: Licked message indication

: Sound alert / Vibration mode

: Unread message indication

: Alarm clock enable indication

: Duplicate message detection indication

: Low battery indication

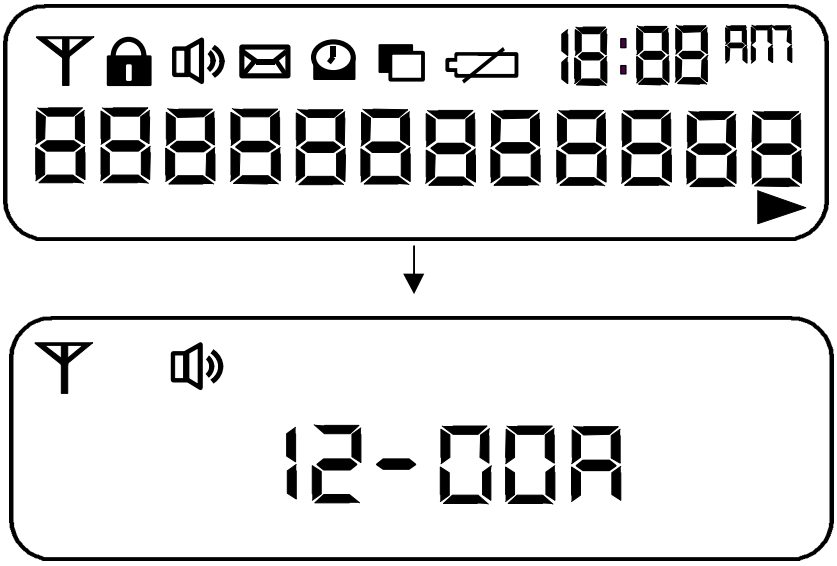
: Additional message indication for more than 13digits.

How to Operate

1. Power ON / OFF

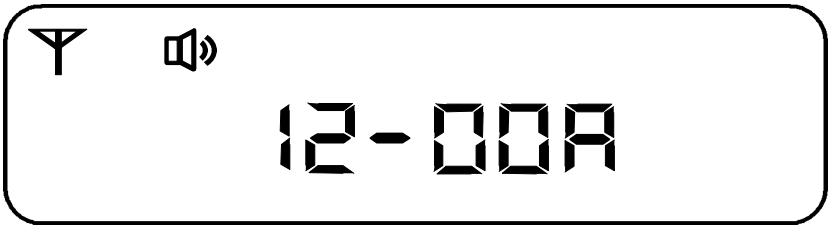
1) Power ON

When pressing any button for 2 seconds or longer while the receiver is in the OFF state. A ring tone is activated and at the same time the following is displayed. And then, power is turned on.



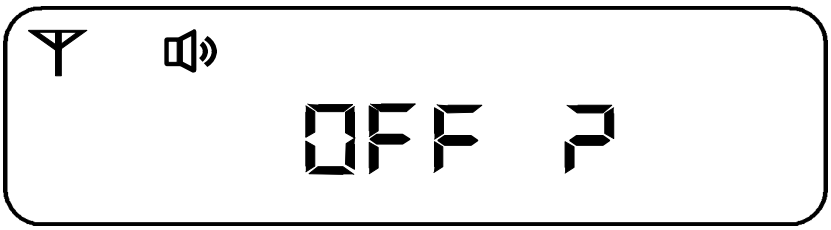
< Receive Waiting State >

2) Power OFF



< Receive Waiting State >

Press the function button three times.



↓ Press the read button.

< Power OFF State >

2. Initial Receive Waiting State

The following 1) and 2) show the initial receive waiting state in each mode.

1) Ring Tone Mode

< Initial State >

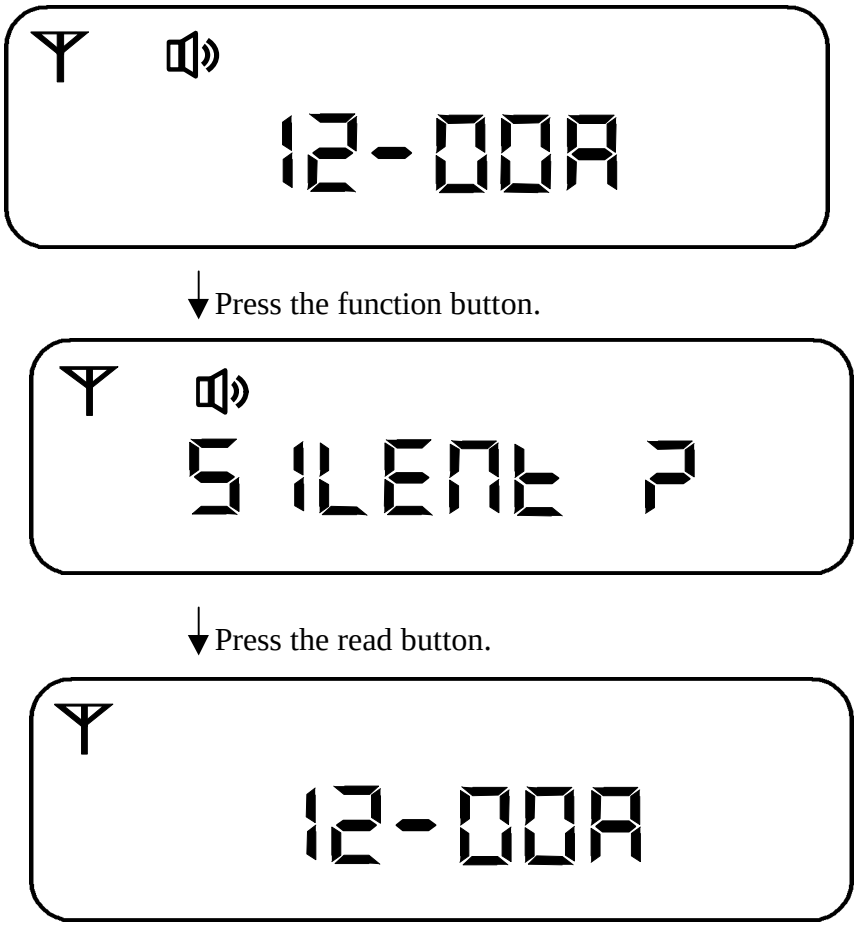
2) Vibration Mode

< Initial State >

¡ ØFor the time indication in the initial receive waiting state, arrange “ - “ indication between time and minute in the interval of 0.5 seconds. In addition, adjust the current time in accordance with the time adjustment order.

3. Switch of Alert Status

1) When switching from the ring tone mode to the vibration mode,

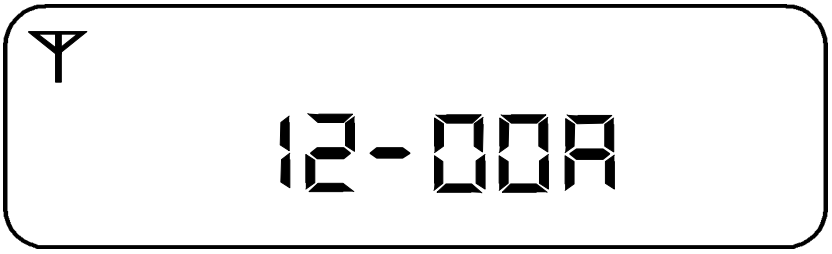


< Switching into the vibration mode >

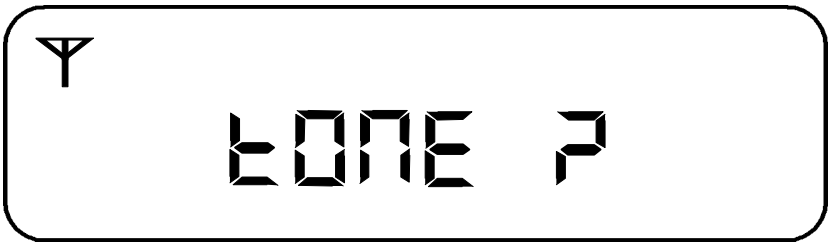
2) When switching from the vibration mode to the ring tone mode,

When pressing the read button once after pressing the function button, the status Changes into Tone1, Tone2, Tone3, and Tone4 sequentially.

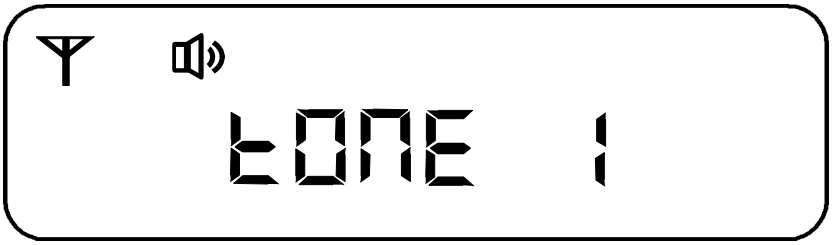
Then, When selecting your favorite tone and pressing the function button, the selected tone is designated as ring tone.



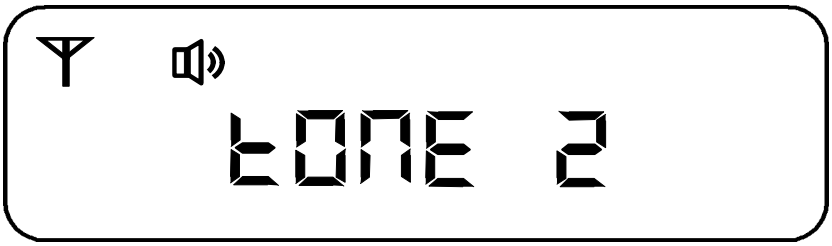
Press the function button.



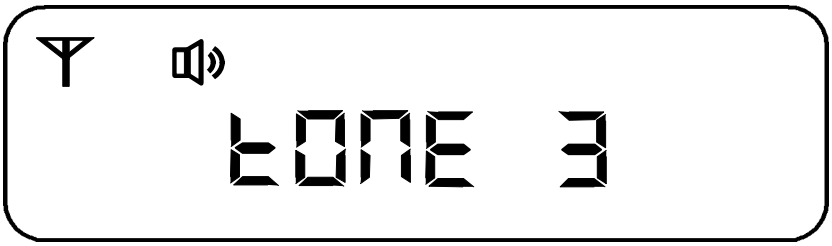
Press the read button.



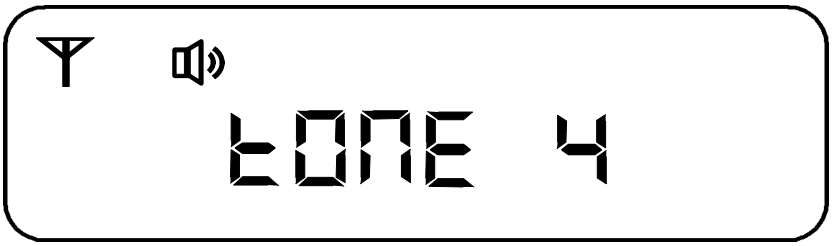
Press the read button.



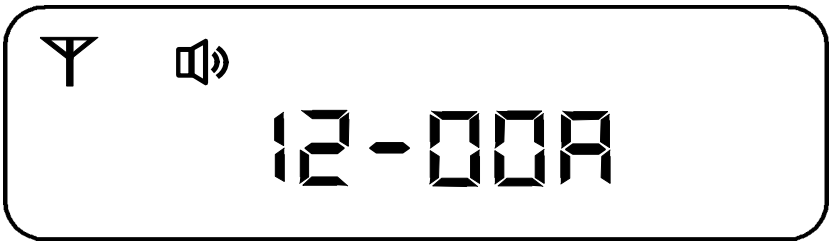
Press the read button.



Press the read button.



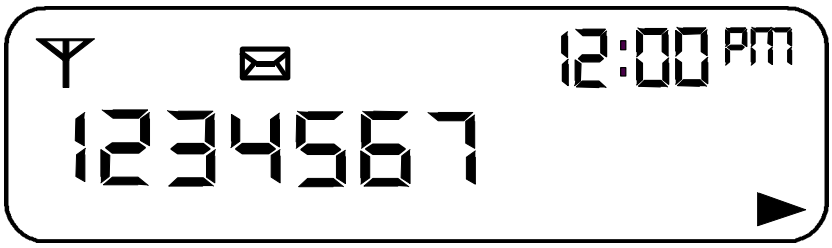
↓ Press the read button.



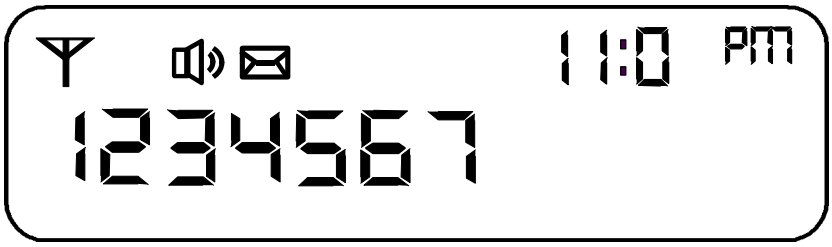
< Switching into the ring tone mode >

4. Message Receive

1) In case a call is made, the received message is displayed on the screen and the call alert is activated at the same time.

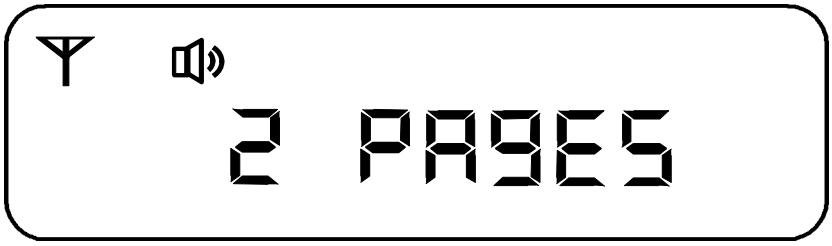


<Message receive while in the vibration mode >



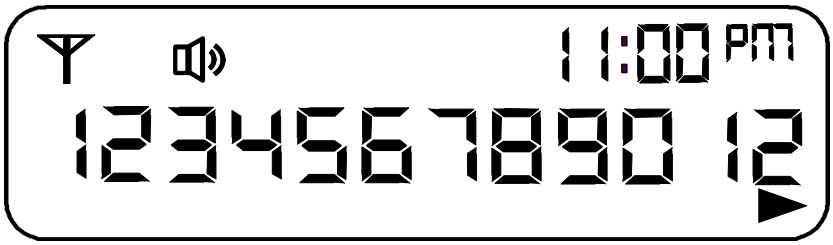
< Message receive while in the ring tone mode >

2) In the received messages are not read, the number of messages not red is displayed on the screen as follows (See “ Reading the Messages Not Read ”)



3) Displaying the message with 13 characters or more

In case the message with 13 characters or more received, the “ ► ” indication is displayed on the end part of the first screen to notify that the message continues on the next screen.



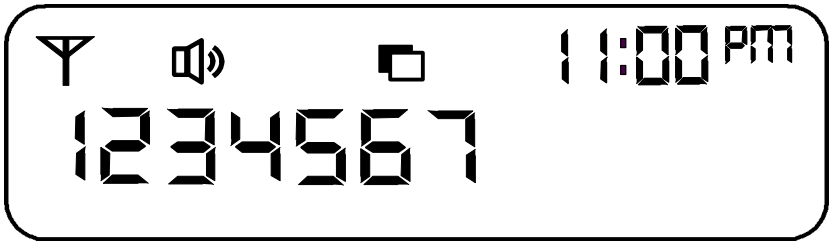
< First Screen >

↓ Press the read button.

< Next Screen >

4) Displaying Overlapped Message

In case the received message is the same to the memorized message, “ ⧉ ” which is The message overlap indication is displayed. Moreover, “ ⧉ ”is displayed over the Message when reading this message again.



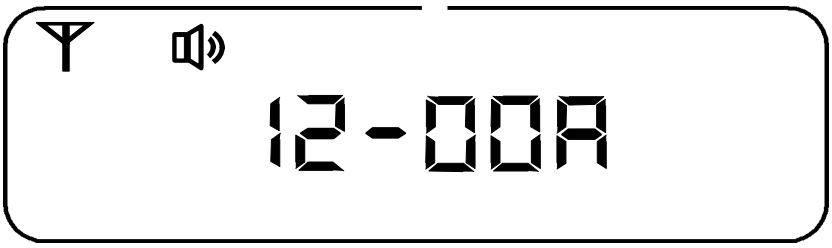
< Displaying the Message Overlap >

5.Reading the Message

1) Reading the received Message

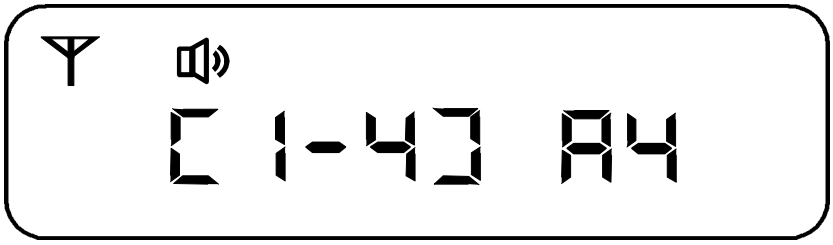
When receiving the message the alert (ring tone or vibration) can be deactivated within the automatic recovery time by pressing function or read button. At this time, if a message with 13 digits or longer or longer is received, continuity indication is displayed.

2) Reading the Stored Message



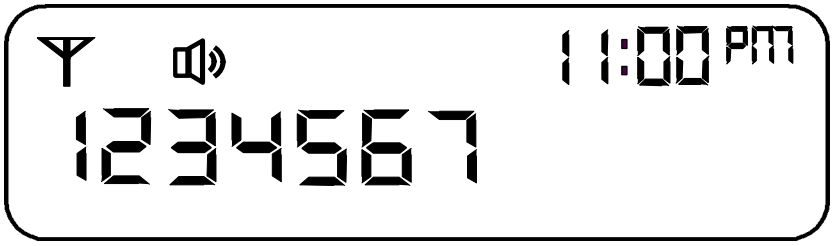
< Receive Waiting State >

Press the read button.



1 : This means the first message.

4 : This means the total number of messages received.

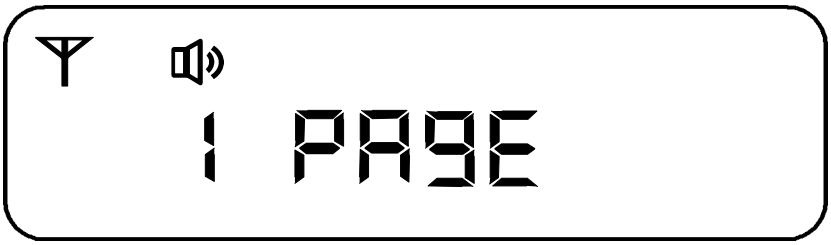


The message is displayed.

The next message is displayed sequentially whenever pressing the read button once. In case there are no more data received, the state is changed into the receive waiting state.

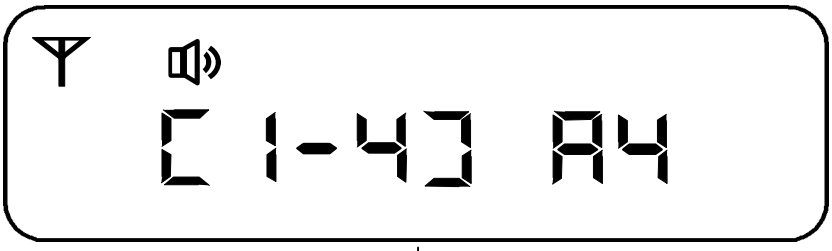
.3) Reading the Message Not Read

In case there are messages not read, the following is displayed on the screen.



Displays the total number of messages not read.

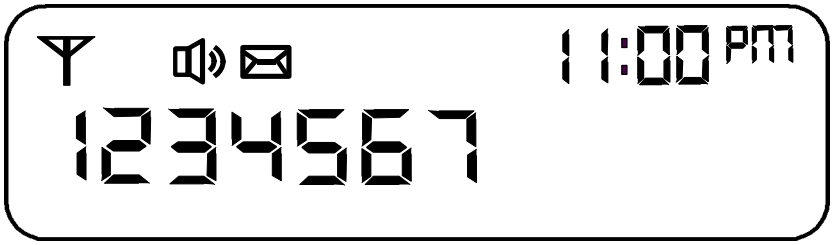
↓ Press the “ read ” button.



↓

1: this means the first message.

4: This means the total number of messages received.



✉ : Message not red.

The message is displayed.

¡ ØThe next message not read is displayed when pressing the read button after reading the current message.

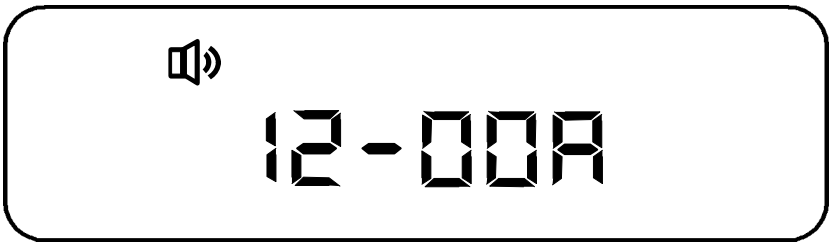
¡ ØIn case the power that has been turned off, while the messages not read exist, is turned on, it is indicated that there are the messages not read.

6. Memory Capacity

This receiver stores a total of 16 telephone numbers. When all the telephone numbers are stored, new messages are received. Since the messages are deleted sequentially, starting with the first memorized message, important telephone numbers can be prevented from being deleted by protecting them beforehand.

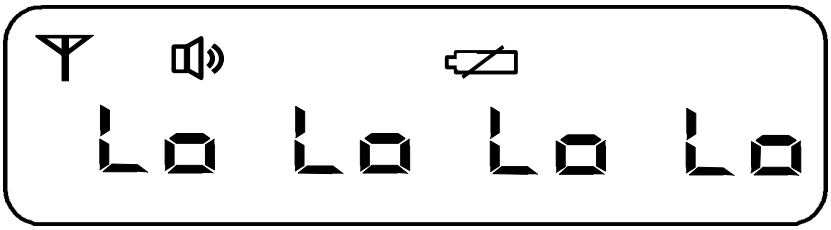
7. Erasing Signal Receiving Area Display

In case the receiver goes out of the receiving area for 4 minutes or longer , the “ ” indication on the screen disappears as follows. During this state, the message receive is impossible.



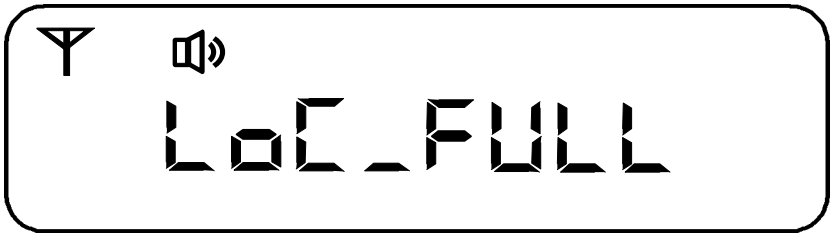
8. Displaying Low Voltage

In case the battery capacity falls below a tolerance value, the receive displays low voltage on the screen as follows and at the same tine low voltage alarm tone is activated.



9. Protection and Releasing of Received Message

A maximum of 12 messages can be protected in order to prevent the received message from being deleted when receiving a new message. The following is displayed during the message protection operation after 12 messages are protected.

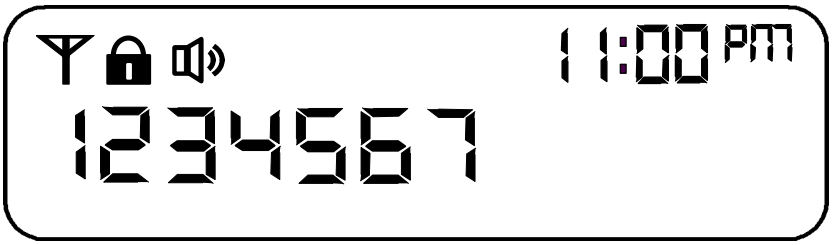


< All the 12 messages gave been protected >

¡ ØThe user should be careful since the message is not protected without batteries.

1) Message Protection

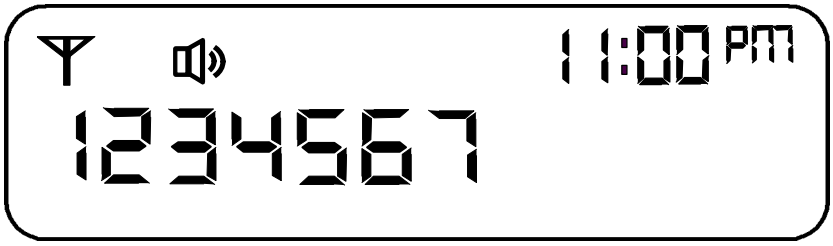
Select the message to be protected on the screen. Then, press the function button while pressing the read button, to display the "🔒" indication. This is used to indicate that the message on the screen is protected.



< Message Protection State >

2) Message Releasing

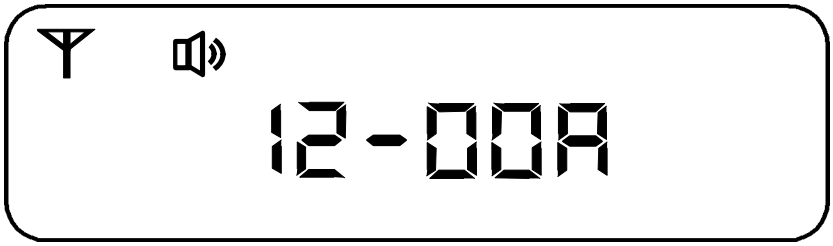
Select the message to be erased from the screen and then, press the function button while pressing the read button, then the "🔒" indication disappears. This is used to indicate that the message on the screen is released.



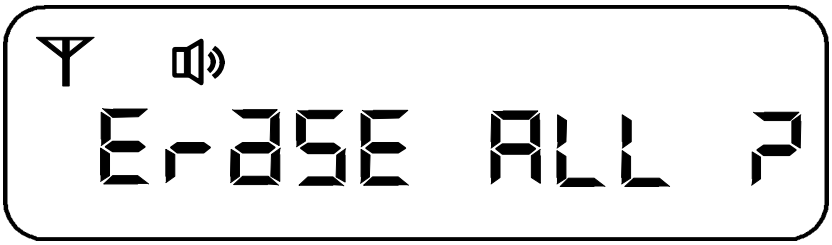
< Message Release State >

10. Message Deletion Method

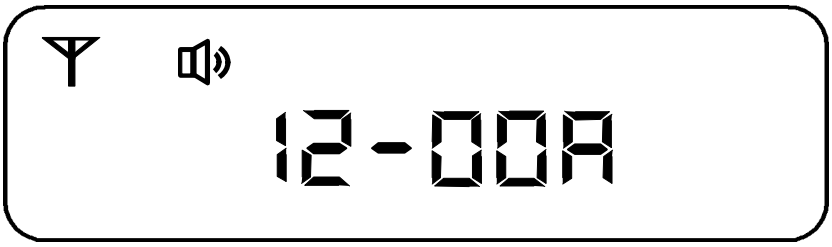
The method of deleting stored messages is as follows.



↓ Press the function button four times during the initial receive state.



↓ Press the read button.

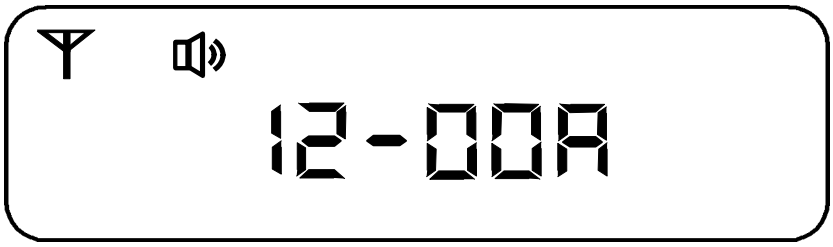


The state is changed into the initial receive state as the message is deleted.

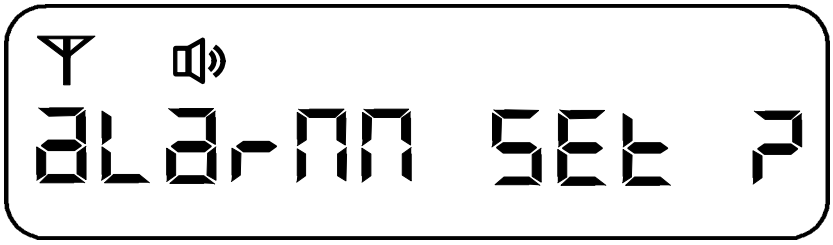
11. Alarm Adjustment Method

The alarm function is used to activate the alarm at the user desired time.

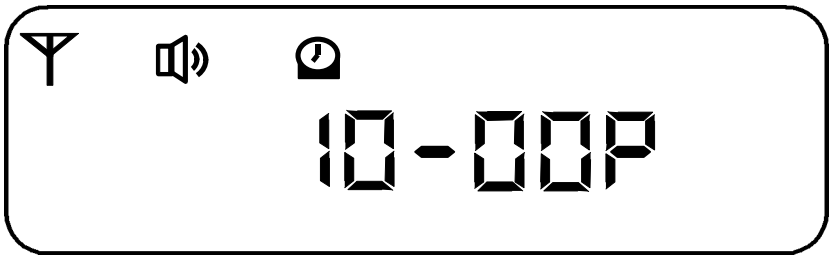
1) Alarm Set - Up



Press the function button two times in the initial receive state.



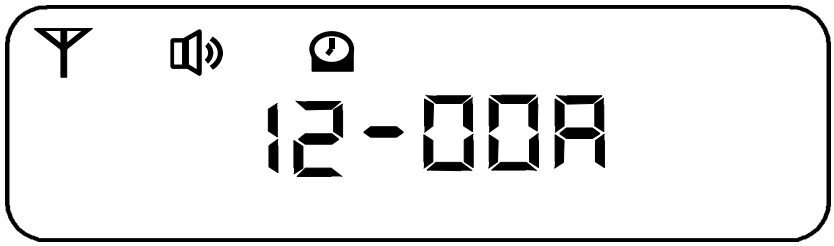
↓ Press the read button.



↓ “ ” and “ 10 ” start to blink.
“ Read button ” : Time Adjustment
“ Function button ” : Hour ¡ æMinute ¡ æAM / PM

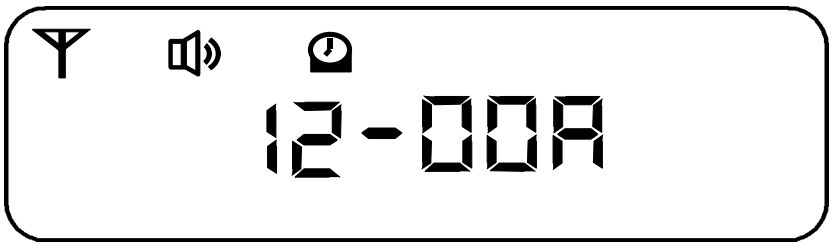
Press the function button after adjusting the changed time.

¡ ØIn case time adjustment has not been made in this state, the display starts to blink for 8 seconds and then, the alarm is set up to the pre - set time.

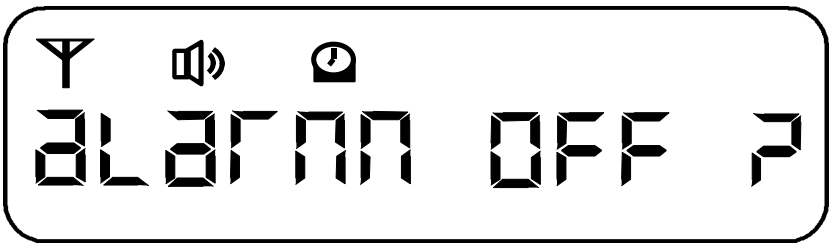


< Alarm Set - up Status >

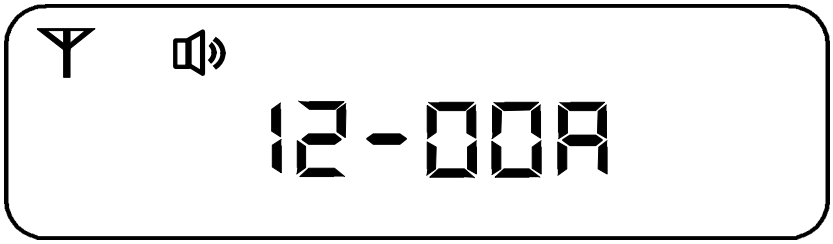
2) Alarm Releasing



Press the function button two tines while the alarm has been set up.



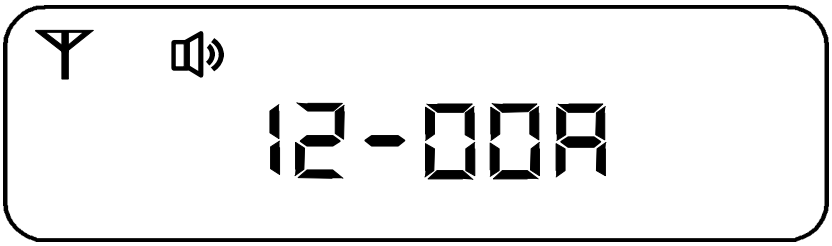
↓ Press the read button.



The state is changed into the initial screen as the alarm is released.

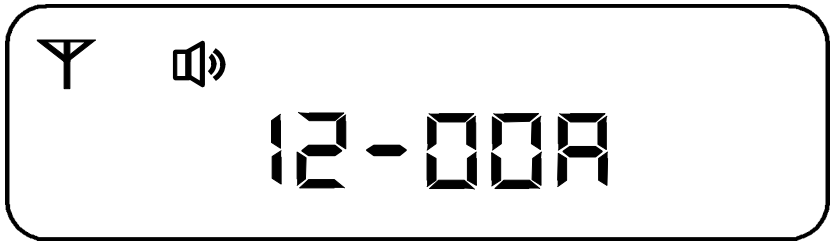
< Alarm Release State >

12. Time Adjustment Method



Press the function button five times in the initial receive state.

↓ Press the read button.



Current Time : The display starts to blink at the “ hour “

“ Read button ” : Time Adjustment

“ Function button ” : Hour - Minute - AM / PM

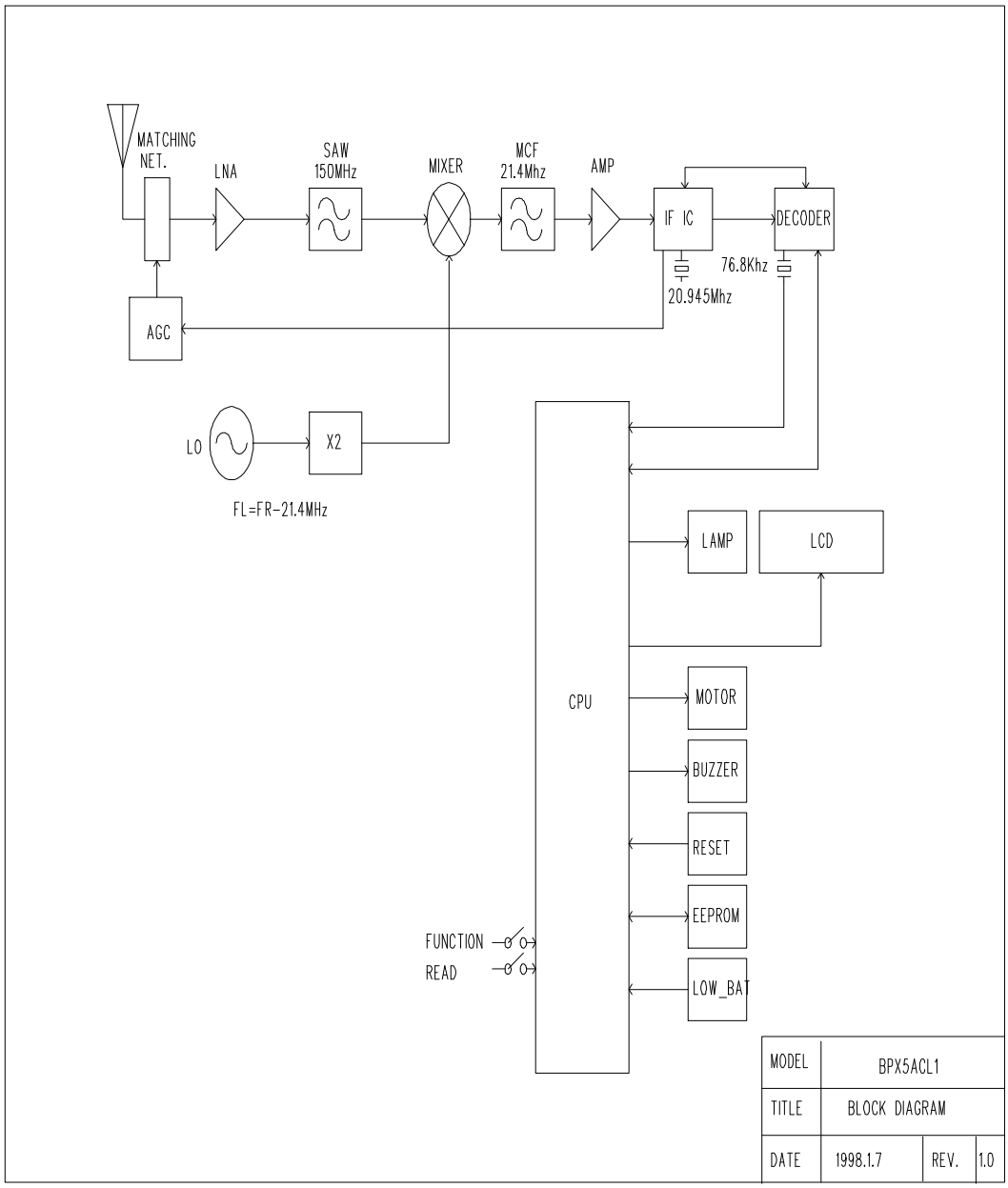
Press the function button after changed time adjustment.

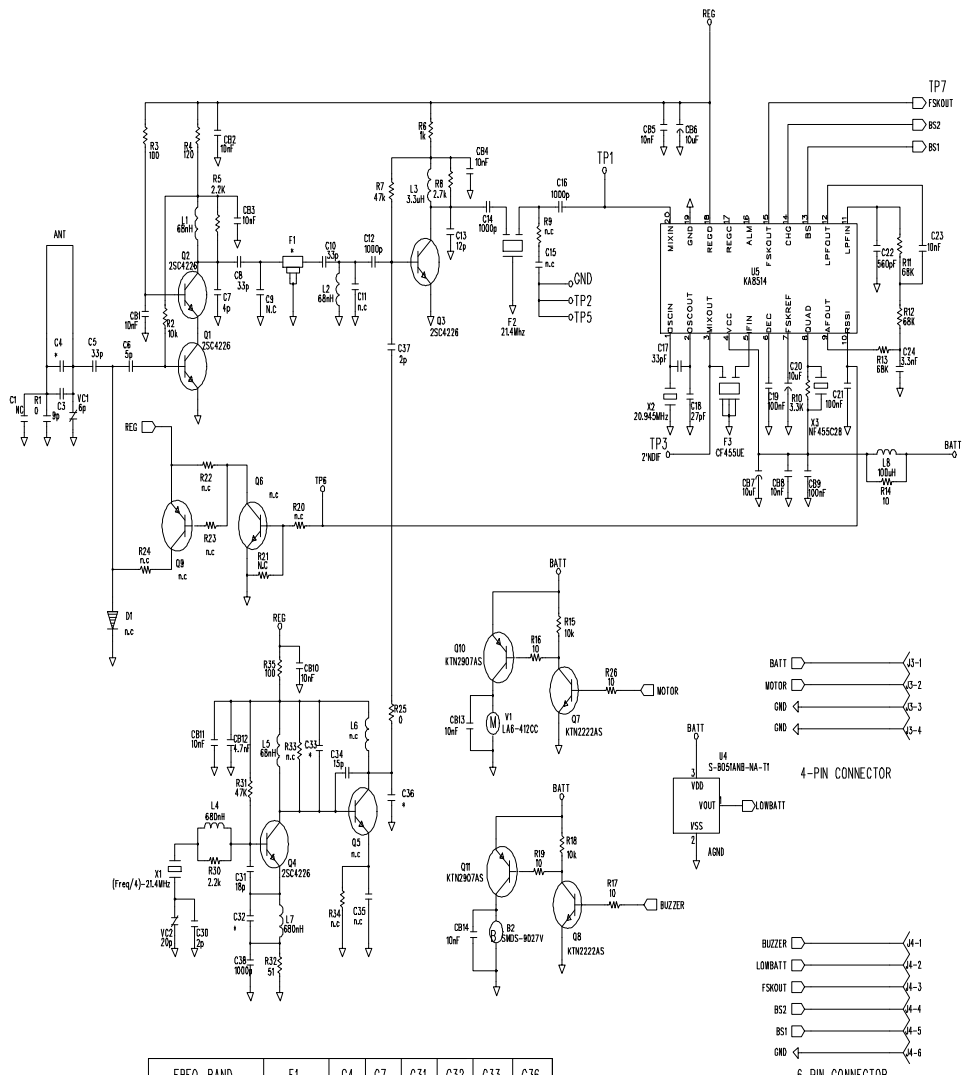
¡ ØIn case time adjustment has not been made in this state, the display starts to blink for 8 seconds and then, the alarm is set up to the pre - set time.

ATTACHMENT 4

BLOCK DIAGRAM & SCHEMATIC DIAGRAM

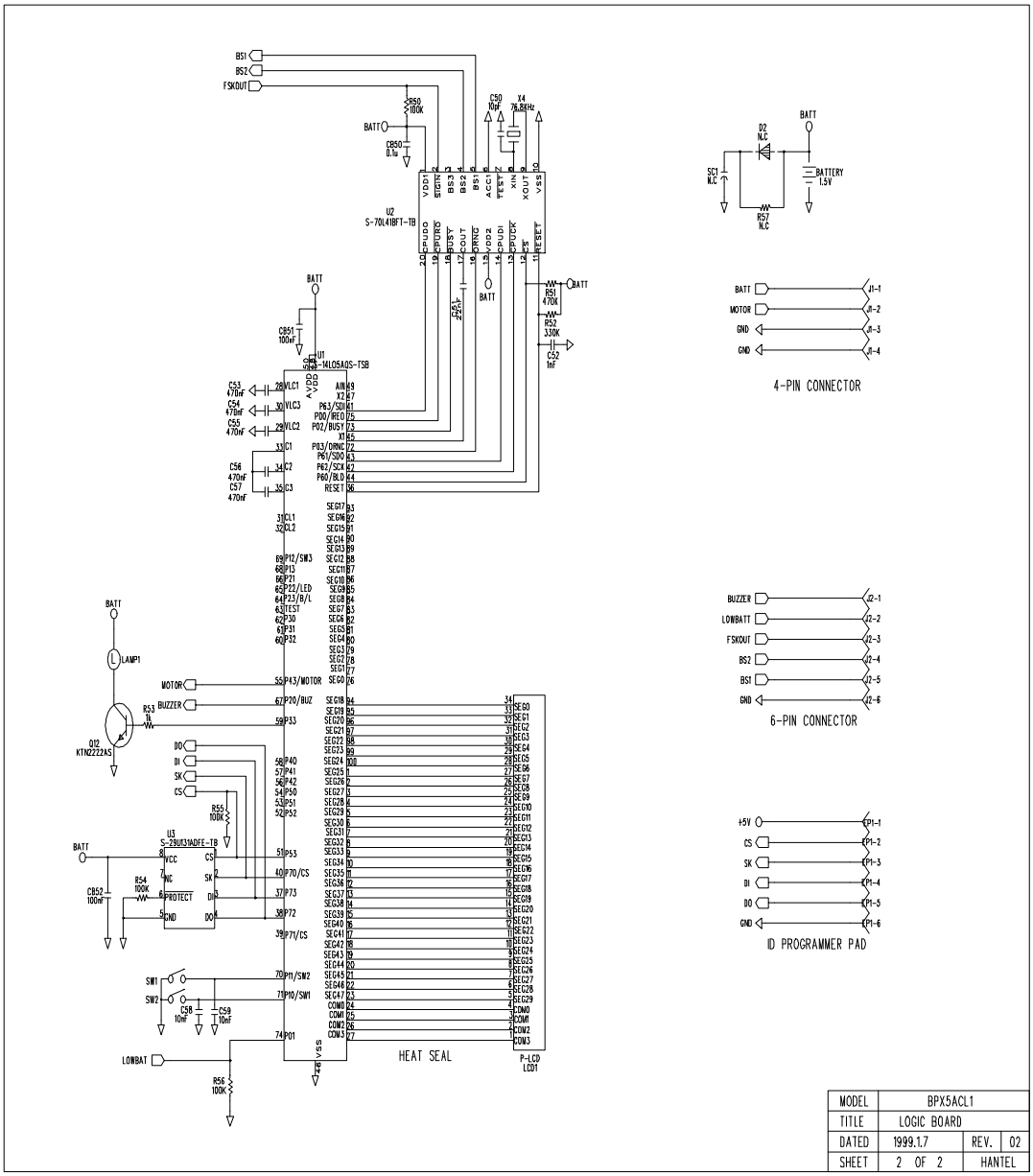
BLOCK DIAGRAM & SCHEMATIC DIAGRAM





FREQ. BAND	F1	C4	C7	C31	C32	C33	C36
A(135-143MHz)	DF139BC1	8p	4p	27p	22p	12p	33p
B(143-151MHz)	DF147BC1	8p	4p	27p	22p	8p	33p
D(151-159MHz)	DF155BC1	2p	4p	18p	18p	6p	33p
E(159-167MHz)	DF163BC1	NC	4p	18p	15p	3p	27p
F(167-174MHz)	DF171BC1	NC	4p	18p	15p	NC	27p

MODEL	BPX5ACL1		
TITLE	RF BOARD		
DATED	1999.1.7	REV.	02
SHEET	1 OF 2	HANTEL	



MODEL	BPX5ACL1		
TITLE	LOGIC BOARD		
DATED	1999.1.7	REV.	02
SHEET	2 OF 2	HANTEL	

ATTACHMENT 5

DESCRIPTION OF CIRCUIT FUNCTION

DESCRIPTION OF CIRCUIT FUNCTION

1. INTRODUCTION

The HANTEL POCSAG Numeric Display pager consists of a radio-frequency(rf) circuit board and a microcomputer-controlled circuit board. Typically, a page is received via an rf carrier that is frequency-modulated by a coded binary sequence. Basically, signal pattern consists of a preamble, start code, and address code which is followed by two blocks of data. These two blocks contain numeric data to be displayed.

The circuitry in the receiver performs the rf to intermediate-frequency conversion and the frequency demodulation. This information is passed to the decoder board which contains the logic circuits to decode the binary information. In addition, this board contains the logic control for the switches, the data filter components, and the output device.

2. POCSAG PAGING FORMAT, CODE, AND CODE CAPACITY

a. General

The basic signaling pattern used in this pager is a sequence of coded binary data using the Post Office code Standardization Advisory Group (POCSAG) code. The POCASG code is a synchronous paging format that allows pages to be transmitted in a simple batch structure. The code accommodates both tone-only and tone-and-data paging ; however, the pager use only tone-and-data paging. The POCSAG code also provides improved battery saving capability and an increased code capacity. The negative logic convention (“0”=high, “1”=low) is used in this system.

The POCSAG code format consists of a preamble and one or more batches of codewords. Each batch comprises a 32-bit frame synchronization code and idle codewords each. The frame synchronization code marks the start of the batch of codewordes.

b. Preamble structure

The preamble consists of 576 bits of a 101010 pattern transmitted at a bit rate of 512 or 1200 bps. The decoder uses the preamble both to determine if the data received is a POCSAG signal and for synchronization with the stream of data.

c. Batch structure

A batch consists of a frame synchronization code followed by eight frames of two address codewords per frame (16 address codewords per batch). In order to maintain the

proper batch structure, each frame is filled with two address codewords, or two idle codewords, or any appropriate combination of the two codeword types.

d. Frame Synchronization Code Structure.

The frame synchronization (FS) code is a unique, reserved word that is used to identify the beginning of each batch. Regulated B+volatage is produced for the duration of the FS code. The FS code comprises the 32 bits: 01111100110100100001010111011000.

e. Address Codeword Structure and Code Capacity.

An address codeword's first bit (bit1) us always a zero. Bits 2 through 19 are the address bits ; the pager looks at these bits to find its own unique address. Each POCSAG codeword is capable of providing address information for four different paging sources (Address 1 through Address 4). These values of bits 20 and 21 (the source-identifier bits). Bits 22 through 31 are the parity check bits, and bit 32 is the even parity bit.

Pre-coded into the code plug are three bits which designate the frame location, within each batch, at which the pager's address is to be received ; the decoder will look only at the codewords in this frame for its address.

Power is removed from the receiver during all frames other than the pre-coded one, thus extending pager battery life.

The combination of the code plug's three pre-coded frame location bits and the address codeword's 18 address bits provides over two million different assignable codes.

In this combination, the frame location bits are the lease-significants bits, and the address bits are the most-significant bits.

f. Message Codewords

A message codeword always starts with a 1 and always follows directly after the address. Each message codeword replaces an address codeword in the batch.

g. Idle Codeword Structure

The idle codeword is a unique, reserved codeword used to take the place of an address in any frame that would not otherwise be filled with 64 bits.

Thus, if a frame contains only one address, and idle codeword will be added to complete the 64-bit frame.

The idle codeword comprises the 32 bits :

01111010100010011100000110010111.

3. GENERAL CIRCUIT DESCRIPTIN

a. Power

Operating power for both the receiver and decoder boards is obtained from the battery. On the receiver board, a 1-volt regulator supplies the rf circuitry with power.

The regulator is turned on and off from the decoder via the battery-saver strobe. The decoder board receives its power from the battery and generates 1.5 volts, which is supplied to the microcomputer/LCD driver and code plug.

b. Standard receiver basic circuit description

The basic pager circuits consist of the following receiver board stages : antenna and amplifier/preselector to receive, amplify, and filter the RF paging signal. The mixer converts the RF signal to an intermediate frequency(IF). The crystal filter attenuates the signal above and below the RF paging signal to the correct IF demodulator amplifies, filters, and mixes with the first IF to produce a 455KHz second IF and demodulates the signal to recover the audio data.

The receiver board receives power from the main system battery. A 1 Volt regulator contained in the IF demodulator supplies the receiver circuits with power.

Control lines turn this regulator on and off as well as to select the IF demodulator model of operation.

c. Decoder basic circuit description

The basic decoder consists of the following functional module : Microcomputer module with LCD driver, LCD display module, user interface buttons, POCSAG decoder and EEPROM writing module. The POCSAG decoder is a signal processing module which communicates with the host microcomputer. Two switches provide user interface for the pager.

The code plug module includes an electrically erasable programmable read-only memory(EEPROM) integrated circuit. It is programmed with pager address codes, The microcomputer controls the major functions involving data decoding and control of the alert circuitry and the LCD.

4. OPERATING MODES

The are two modes of operation for the decoder : power-up and page search.

a. Power-up

The power-up condition starts when the primary battery is inserted into the pager.
The voltage management circuits activate and begin to regulate the system voltage.

b. Page search

When the pager powers up, the receiver turned on and the decoder begins to search for preamble. When preamble is detected, the pager synchronizes to the channel, and compare start code, address data with the incoming data from decoder, If the data corresponds to data held in the U01, then the U01 performs its decoding function and keys the appropriate alerting circuit.

Once the decoder detect its address, U01 state the alert tone and continues decoding.

If the detected preamble was inverted, the decoder will search for its address up to 16 address times detecting the start code.

During the absence of preamble, for approximately 217 msec of every 1.047 second(512bps) and 93 msec of every 1.047 second (1200bps). Battery saving strobe signal applied to U05, minimize the power consumption.

5. DETAILED CIRCUIT DESCRIPTION

a. Battery voltage, voltage regulator and battery-saver strobe circuits.

The negative side of the battery is connected to circuit common. The positive voltage from the battery is distributed throughout the decoder and receiver section. A voltage regulator on board the IF demodulator supplies 1.0 volt to sections of the receiver at discrete times, reducing current drain.

The battery voltage is applied to the microcomputer(U01) and decoder (U02)

b. POCSAG receiver circuit descriptions.

(1) Battery voltage and DC-DC converter.

The negative side of the battery is connected to circuit common. Positive voltage from the battery, B+, is distributed throughout the decoder and receiver sections.

BATT is applied to Microcomputer(U01), low battery detection IC(U04), Motor/Buzzer driver (Q7, Q8) and EEPROM(U03)

(2) Antenna and RF amplifier

The antenna system for the pager is the metal-looped type which resonates with the capacitors C05, C03 and VC1 trimming capacitor. Matching the antenna impedance to the input of RF amplifier(Q1,Q2) is performed by the fixed capacitor C05. By tuning the

VC1 capacitor, the antenna can be turned to pager's operating frequency.
The RF signal is coupled by C05 to the input of the RF amplifier, cascoded pair Q1 and Q2. Resistors R02, R03 and R04 provide DC bias stability. DC supply decoupling were performed by C33. The output of the RF amplifier is coupled to the mixer Q3 via a SAW filter(F1). The antenna circuitry, together with the SAW filter, provide image and spurious response protection.

(3) Two-pole crystal filter.

The two pole crystal filter is a very high Q bandpass filter, resonant at the IF frequency. The low-conversion output contained frequencies other than desire 21.4MHz. The very narrow bandpass filter out the signal above and below 21.4MHz.

(4) Low-conversion/Demodulation module.

The first IF signal from filter F2 couples to the second mixer at pin 20 of low conversion module U05. It mixes with the second oscillator frequency for an output of 455KHz.
The second oscillator is a crystal controlled unit X2. There are no peaking or tuning adjustments. Output of the second oscillator must be 455KHz below the first IF. Output of the second mixer(second IF) is routed through ceramic filter F3 and the two internal IF amplifier stages. This further reduces the unwanted signals and provide better adjacent channel selectivity. After the second IF amplifier, the signal is applied to the audio demodulator.

c. Decoder circuit description

(1) Microprocessor module

The microcomputer(U01) module controls the overall operation of the decoder section.
Each time the pager is turned on, the U01 reads the code-plug information and performs the necessary operations to produce a power-up alert(audio beeps). Basically, the U01 consists of a microprocessor and a read-only memory(ROM).

A program in the ROM instructs the U01 to decode the recovered data, store the data message, power the RF/IF circuits on and off, process display data, and interact with the user controls and switches.
The S-14L05AQS-TSA is an 80 pin MCU with highly sophisticated on-chip peripheral functions. The memory map includes 24K bytes of user ROM and 768bytes of RAM.
The MCU has eight parallel ports A, B, C, D, E, F, G, and J. ports A, B, C, and E has 8 I/O pins, port D has 7 I/O pins, port J has 2 I/O pins, port F has 8 input-only pins, and

port G has 8 output-only pins. The S-14L05AQS-TSA includes 16-bit and 8-bit timers, a COP Watch dog timer, LCD drivers, an 8 channel ADC, and two channel serial peripheral interface. The details features are as below.

. Low voltage operation
. Low average standby current
. ROM 4K step X 16 bit
. RAM 3K bit (768 X 4 bit)
. 8 bit synchronous serial interface
. 100 pin SQFP
. LCD driver (7 segments X 12 digits)

(2) Code plug module

The code plug module includes an electrically erasable programmable read only memory(EEPROM) integrated circuit. It is programmed with pager address codes, functions to which the pager will respond, and pager options.

(3) Decoder

It simplifies implementation if a POCSAG paging device by interfacing with any of several off-the-shelf paging receiver IC’s and any of several off-the-shelf host microcontroller/microprocessors. Its primary function is to process information received and demodulated from a POCSAG radio paging channel. Select messages addressed to the paging device and communicate the message information to the host. The host’s function is the interpret the message information in an appropriate manner. The POCSAG IC also operates the paging receiver in an efficient power consumption mode and enables the host to operate in a low power mode when monitoring a single channel for message information.

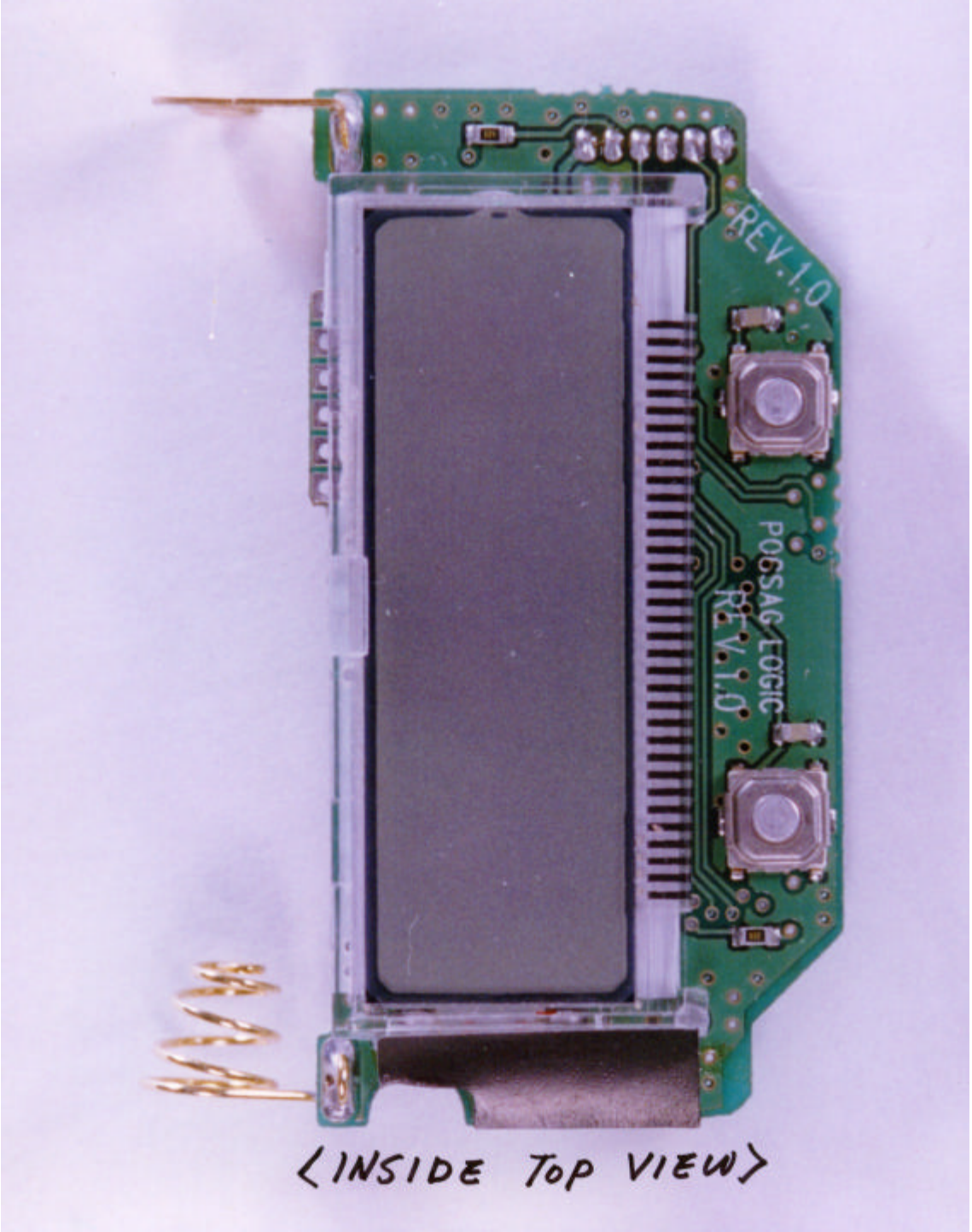
ATTACHMENT 6

PHOTOGRAPHS

<TOP VIEW>

Model : BPX5ACL1
Freq. & CAP. : 151.225, 1234567
FCC ID : ODGBPX5ACL1
Made by Hantel in Korea

<BOTTOM VIEW>



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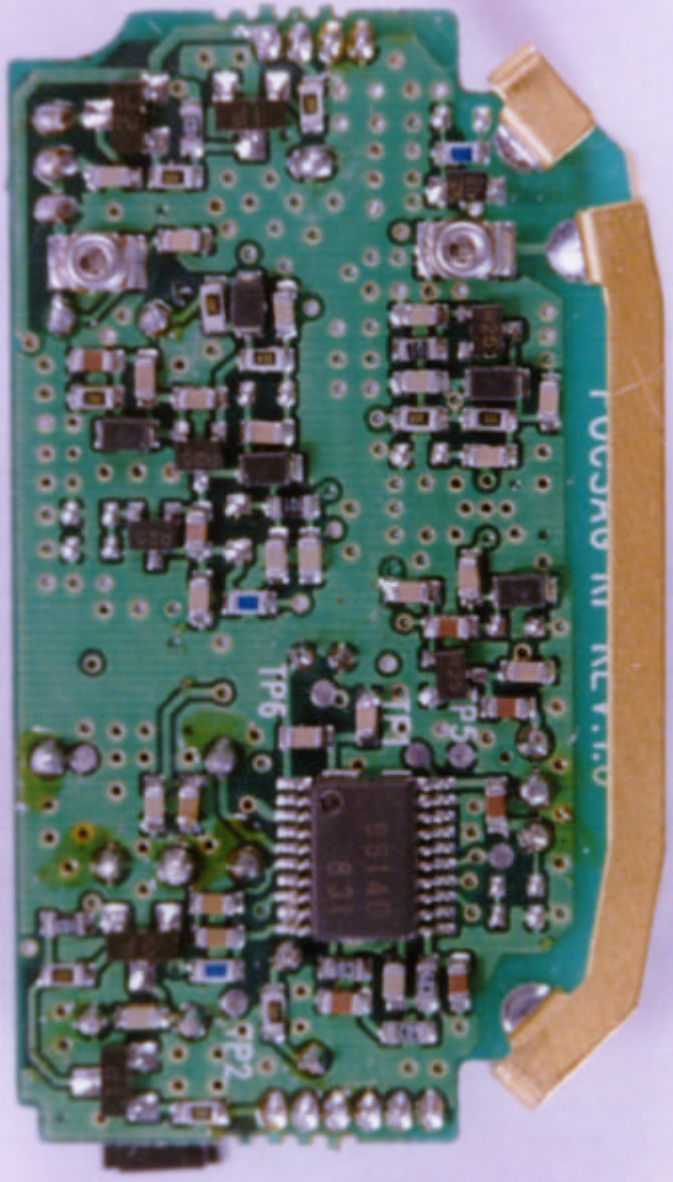

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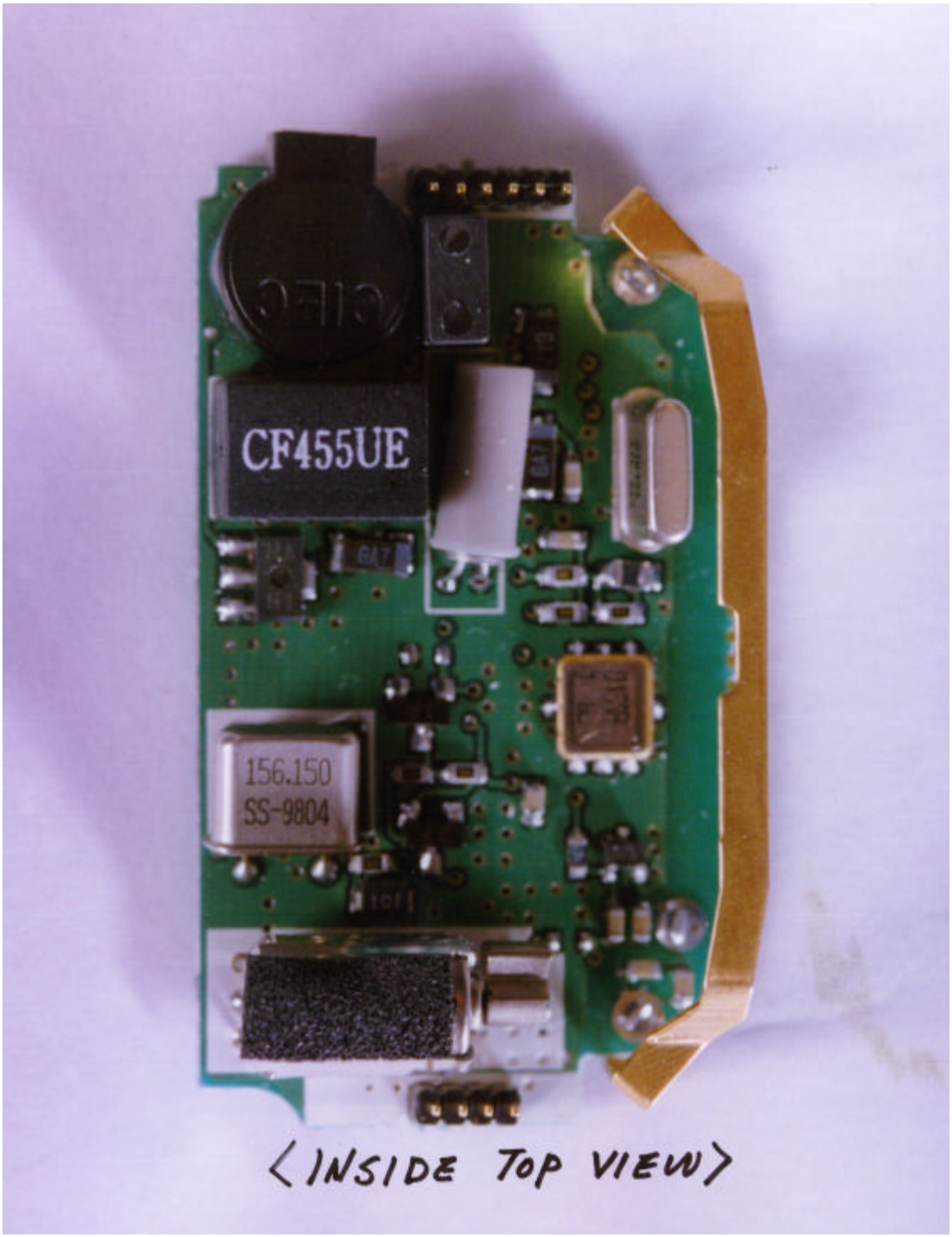

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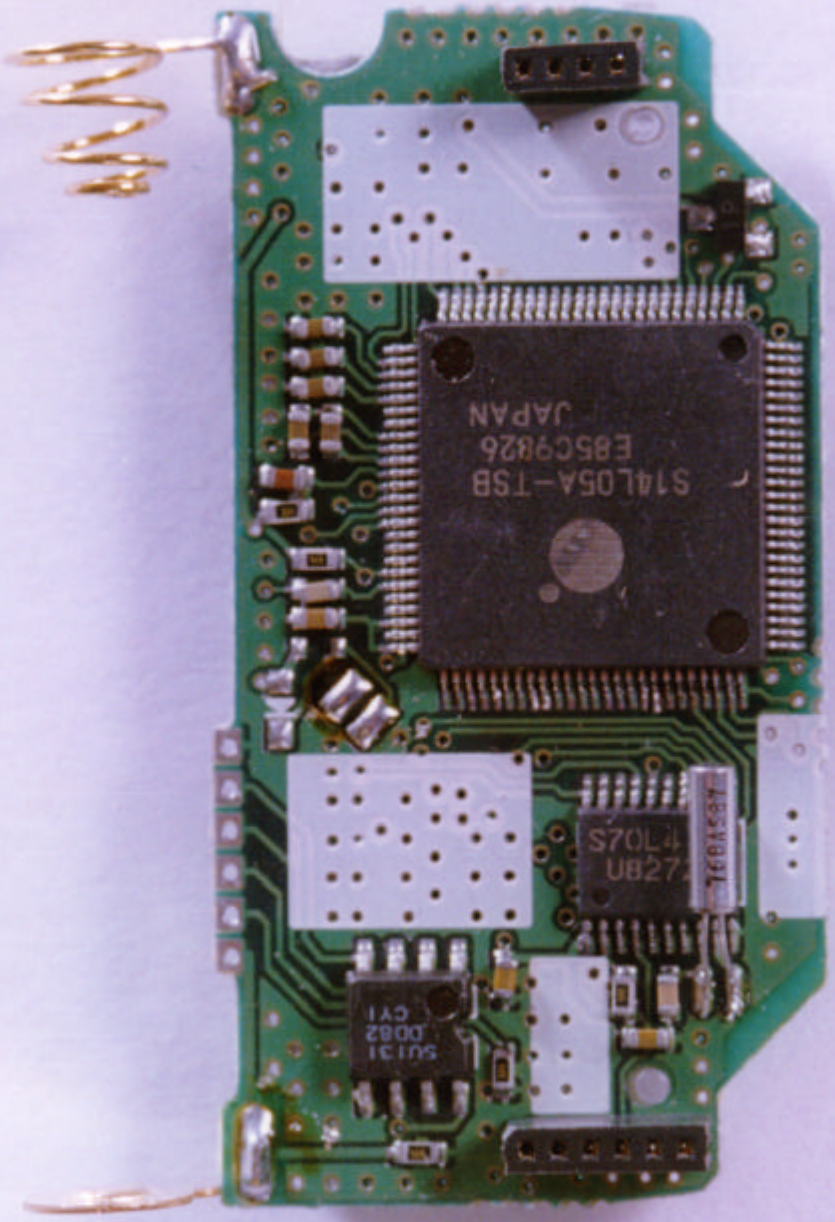

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