User Manual

Ver.0.9

Jan. 24, 2018

Release Record

Version	Release Date	Comments
0.9	Jan. 24, 2018	Draft Release

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Description:

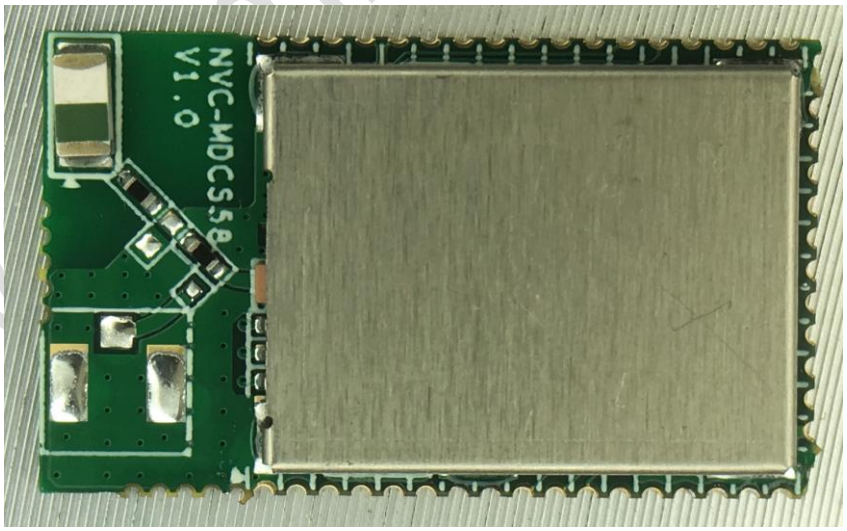
NVC-MDCS58 is a dual mode Bluetooth® 4.2 module. It is based on Qualcomm's QCC3007. With internal DSP and audio codec, it is a full solution for integrating Bluetooth® audio functions into various products with minima efforts. With NovaComm's iNova® stack, designers can easily customize their applications to support different Bluetooth profiles, such as HS/HF, A2DP, AVRCP, OPP, DUN, SPP, HID, GATT and etc. And with the build in firmware the module can also be connected with Apple's Authentication Coprocessor to build an iAP over Bluetooth application. Please contact NovaComm for more applications.

Typical Bluetooth audio applications:

- Home entertainment
- Office and mobile accessories

Features:

- Dual mode Bluetooth® v4.2
- Support Profiles: HFP, A2DP, AVRCP, SPP, OPP, DUN, iAP over Bluetooth for Apple, HID and etc.
- UART/I2C master
- 12 digital PIOs
- Support I2S interface
- Support Apt-X, SBC codec.
- Wakeup interrupt and watchdog timer
- 23.9mm x 14.3mm x 2.45mm
- Weight: 1g
- SMT pads for easy and reliable PCB mounting,
- QDID:
- FCC ID: OC3BM1858
- IC: 22104-BM1858
- CE NB 1313
- MSIP: MSIP-CRM-NAC-MDCS58
- RoHS compliant



Ordering Number	Package	Items in One Package	Comments
NVC-MDCS58	Plastic tray	100	

Table 1: Ordering Information

Please also supply the customer firmware code issued by NovaComm Technologies when you place the order.

1 Pinout and Description

1.1 Pin Assignments

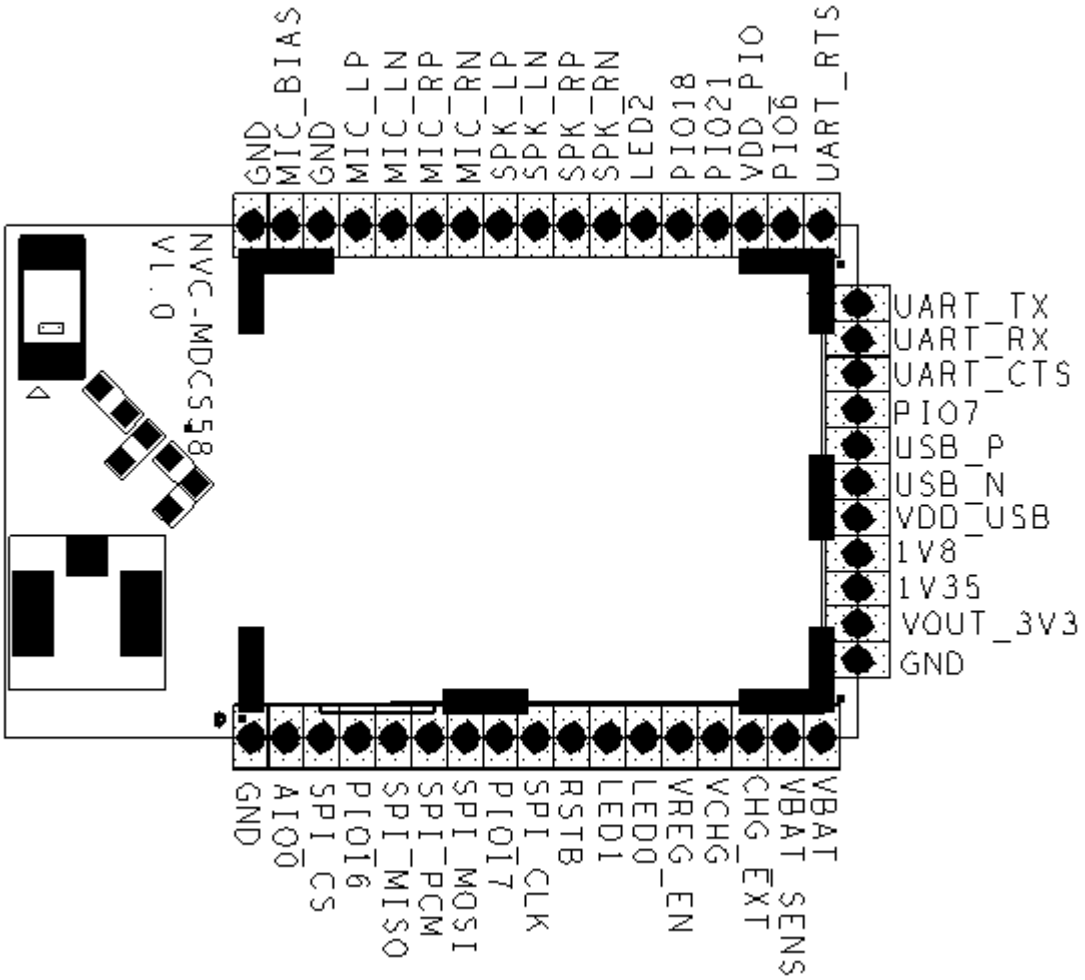


Figure 1: Pinout of NVC-MDCS58

1.2 Pin Descriptions

Pin	Symbol	I/O Type	Description
1	GND	Ground	Ground
2	AIO0	Bidirectional	Analog programmable input line 0
3	SPI_CS	Bidirectional with weak pull-down	When SPI_PCM is high, the IO is chip select for Debug SPI When SPI_PCM is low, the IO is I2S1 word select or general IO 4
4	PIO16	Bidirectional with strong	Programmable IO 16

		pull-up	
5	SPI_MISO	Bidirectional with weak pull-down	When SPI_PCM is high, the IO is Debug SPI data output When SPI_PCM is low, the IO is I2S1 synchronous data output or general IO 3
6	SPI_PCM	Input with weak pull-down	SPI/I2S select input, 0 select I2S/PIO, 1 select Debug SPI
7	SPI_MOSI	Bidirectional with weak pull-down	When SPI_PCM is high, the IO is Debug SPI data input When SPI_PCM is low, the IO is I2S1 synchronous data input (SPDIF input) or general IO 2
8	PIO17	Bidirectional with strong pull-down	Programmable IO 17
9	SPI_CLK	Input with weak internal pull-down	When SPI_PCM is high, the IO is Debug SPI clock When SPI_PCM is low, the IO is I2S1 synchronous data clock or general IO 5
10	RSTB	Input with strong pull-up	Active LOW reset, input debounced so must be low for >5ms to cause a reset
11	LED1	Bi-directional	Open drain output
12	LED0	Bi-directional	Open drain output
13	VREG_EN	Input	Regulator enable and multifunction button. A high input (tolerant to VBAT voltages) enables the on-chip regulators, which can then be latched on internally and the button used as a multifunction input.
14	VCHG	Charger input	Always connect to a USB VBUS
15	CHG_EXT	Output	External battery charger transistor base control when using external charger boost. Otherwise leave unconnected.
16	VBAT_SENS	Input	Battery charger sense input.
17	VBAT	Power Input	Battery positive terminal
18	GND	Ground	Ground
19	VOUT_3V3	Output	3.3 V regulator output.
20	1V35	Output	1.35 V regulator output.
21	1V8	Output	1.8V regulator output.
22	VDD_USB	Power Input	Positive supply for USB port.

23	USB_N	Bi-directional	USB data minus
24	USB_P	Bi-directional	USB data plus with selectable internal 1.5 k pull-up resistor
25	PIO7	Bidirectional with strong pull-down	Programmable IO 7
26	UART_CTS	Bidirectional with strong pull-down	UART clear to send, active low
27	UART_RX	Bidirectional with strong pull-up	UART data input
28	UART_TX	Bidirectional with strong pull-up	UART data output
29	UART_RTS	Bidirectional with strong pull-up	UART Request to send, active low
30	PIO6	Bidirectional with strong pull-down	Programmable IO 6
31	VDD_PIO	Power Input	Positive supply of IO ports.
32	PIO21	Bidirectional with weak pull-down	Programmable IO 21
33	PIO18	Bidirectional with weak pull-down	Programmable IO 18
34	LED2	Bi-directional	Open drain output
35	SPK_RN	Analogue output	Speaker output negative, right
36	SPK_RP	Analogue output	Speaker output positive, right
37	SPK_LN	Analogue output	Speaker output negative, left
38	SPK_LP	Analogue output	Speaker output positive, left
39	MIC_RN	Analog input	Line input negative, channel right
40	MIC_RP	Analog input	Line input positive, channel right
41	MIC_LN	Analog input	Line or microphone input negative, channel left
42	MIC_LP	Analog input	Line or microphone input positive, channel left
43	MIC_GND	Analog GND	GND for Microphone bias
44	MIC_BIAS	Analog output	Microphone bias
45	GND	Ground	Ground

Table 2: Pin Definition

2 Electrical Characteristics

2.1 Absolute Maximum Rating

Rating	Min	Max	Unit
Storage Temperature	-40	+105	℃
Operating Temperature	-40	+85	℃
VCHG Voltage	-0.4	6.5	V
VDD_USB/USB_DP/USB_DN Voltage	-0.4	+3.6	V
VBAT Voltage	-0.4	+4.4	V
PIO Voltage	-0.4	+3.6	V
AIO Voltage	-0.4	+1.95	V
Other Terminal Voltages except RF	-0.4	+3.6	V

Table 3: Absolute Maximum Rating

2.2 Recommended Operating Conditions

Operating Condition	Min	Typ	Max	Unit
Operating Temperature Range	-20	--	+85	℃
VCHG	4.75	5.0	6.5	V
VDD_USB/USB_DP/USB_DN Voltage	3.1	3.3	3.6	V
VBAT Voltage	2.5	3.7	4.4	V
PIO Voltage	+1.7	+3.3	+3.6	V
AIO Voltage	+1.7	+1.8	+1.95	V

Table 4: Recommended Operating Conditions

2.3 Input/output Terminal Characteristics

2.3.1 Digital Terminals

Supply Voltage Levels	Min	Typ	Max	Unit
Input Voltage Levels				
V_{IL} input logic level low	-0.4	-	+0.4	V

V_{IH} input logic level high	0.7 x VDD_PIO	-	VDD_PIO + 0.3	V
Tr/Tf	-	-	25	ns
Output Voltage Levels				
V_{OL} output logic level low, I_{OL} = 4.0mA	-	-	0.4	V
V_{OH} output logic level high, I_{OH} = -4.0mA	0.75 x VDD_PIO	-	-	V
Tr/Tf	-	-	5	ns
Input and Tri-state Current				
Strong pull-up	-150	-40	-10	uA
Strong pull-down	10	40	150	µA
Weak pull-up	-5	-1.0	-0.33	µA
Weak pull-down	0.33	+1.0	5.0	µA
CI Input Capacitance	1.0	-	5.0	pF

Table 5: Digital Terminal

2.3.2 USB

USB Terminals	Min	Typ	Max	Unit
Input Threshold				
V_{IL} input logic level low	-	-	0.3 x VDD_USB	V
V_{IH} input logic level high	0.7xVDD	-	-	V
Output Voltage Levels to Correctly Terminated USB Cable				
V_{OL} output logic level low	0.0	-	0.2	V
V_{OH} output logic level high	2.8	-	VDD_USB	V

Table 6: USB Terminal

2.3.3 Internal CODEC - Analogue to Digital Converter

Parameter	Conditions		Min	Typ	Max	Unit
Resolution			-	-	16	Bits
Input Sample Rate, F_{sample}			8	-	48	kHz
Signal to Noise Ratio, SNR	f_{in}=1kHz B/W=20Hz->20kHz A-Weighted	F_{sample}				
		8kHz	-	94.4	-	dB
		16kHz	-	92.4	-	

	THD+N<0.1% 1.6V Vpk-pk input	32kHz	-	92.5	-	
		44.1kHz	-	93.2	-	
		48kHz	-	91.9	-	
THD+N	f_{in}=1kHz B/W=20Hz->20kHz 1.6V Vpk-pk input	F_{sample}				
		8kHz	-	0.004	-	%
		48kHz	-	0.016	-	%
Digital Gain	Digital Gain Resolution = 1/32 dB		-24	-	21.5	dB
Analogue Gain	Pre-amplifier setting = 0dB, 9dB, 21dB or 30dB Analog setting = -3dB to 12dB in 3dB steps		-3	-	42	dB
Maximum ADC input signal amplitude 0dB=1600mv Vpk-pk			13	-	2260	mV Vpk-pk
Stereo separation (crosstalk)			-	-89.9	-	dB

Table 7: Analogue to Digital Converter

2.3.4 Internal CODEC - Digital to Analogue Converter

Parameter	Conditions		Min	Typ	Max	Unit
Resolution			-	-	16	Bits
Output Sample Rate, F_{sample}			8	-	48	kHz
Signal to Noise Ratio, SNR	f_{in}=1kHz B/W=20Hz->20kHz A-Weighted THD+N<0.1% 0dBFS signal	F_{sample} / Load				
		48kHz 100kΩ	-	95.4	-	dB
		48kHz 32Ω load	-	96.5	-	
		48kHz 16Ω load	-	95.8	-	
THD+N	f_{in}=1kHz B/W=20Hz->20kHz 0dBFS signal	F_{sample} / Load				
		8kHz 100kΩ	-	0.0021	-	%
		8kHz 32Ω	-	0.0031	-	%
		8kHz 16Ω	-	0.0034	-	%
		48kHz 100kΩ	-	0.0037	-	%
		48kHz 32Ω	-	0.0029	-	%
		48kHz 16Ω	-	0.0042	-	%
Digital Gain	Digital Gain Resolution = 1/32 dB		-24	-	21.5	dB
Analogue Gain	Analogue Gain Resolution = 3dB		-21	-	0	dB

Output voltage full swing (differential)	-	-	778	mV rms
Stereo separation (crosstalk)	-	-90.5	-	dB

Table 8: Digital to Analogue Converter

2.4 Power consumptions

Operating Condition	Discoverable	Connectable	Min	Typical	Max	Unit
Not connected	Yes	-				mA
Not connected	-	Yes				mA
Not connected	Yes	Yes				mA
Not connected deep sleep on	-	Yes		0.25		mA
Not connected deep sleep on	Yes	-		0.2		mA
Not connected deep sleep on	Yes	Yes		0.44		mA
Not connected deep sleep on	-	-		63		uA
Connected Idle (Sniff = 1280ms, 8 attempt, 1 timeout)	-	-		126		uA
Connected with audio streaming (A2DP)	-	-		10mA		mA
Connected with data transfer (SPP or iAP)	-	-		7mA		mA

Table 9: Power consumptions

Note :

Power consumption depends on the firmware used. Typical values are shown in the table.

(a)Sniff mode ----- In Sniff mode, the duty cycle of the slave's activity in the piconet may be reduced. If a slave is in active mode on an ACL logical transport, it shall listen in every ACL slot to the master traffic, unless that link is being treated as a scatternet link or is absent due to hold mode. With sniff mode, the time slots when a slave is listening are reduced, so the master shall only transmit to a slave in specified time slots. The sniff anchor points are spaced regularly with an interval of Tsniff.

3 Physical Interfaces

3.1 Power Supply

There are two power supply schemes available for the module. It can be powered by a Li-poly battery (3.7V) or a 3.3V DC. Please refer to the reference designs in 5.

3.2 Reset

The module may be reset from several sources: RESETB pin, power-on reset, USB charger attach reset and software configured watchdog timer.

The RSTB pin is an active low reset. It is recommended that RSTB be applied for a period greater than 5ms.

At reset the digital I/O pins are set to inputs for bi-directional pins and outputs are tri-state. The pull-down state is shown below.

Pin Name / Group	Pin Status on Reset
USB_DP	Tristate
USB_DN	Tristate
UART_RX	PUS
UART_TX	PUS
SPI_MOSI	PDW
SPI_MISO	PDW
SPI_CS	PDW
SPI_CLK	PDW
PIO6	PDS
PIO7	PDS
UART_RTS	PUS
UART_CTS	PDS
PIO16	PUS
PIO17	PDS
PIO18	PDW
PIO21	PDW

Table 10: Pin Status on Reset

Note: PUS – Strong pull-up, PDS – Strong pull-down, PUW – Weak pull-up, PDW – Weak pull-down.

If RSTB is held low for > 2.4 s and VCHG is not applied, the module turns off. A rising edge on VREG_EN or VCHG is then required to power on.

3.3 Audio Interfaces

The audio interface circuit consists of the following components:

Dual analog audio inputs

Dual analog audio outputs

1 digital microphone input

2 configurable I²S interfaces

Configurable SPDIF input interface

3.3.1 Audio Input and Output

The audio input circuitry consists of 2 independent 16 bit high quality ADC channels:

1. Programmable as either stereo or dual-mono inputs.
2. 1 input programmable as either microphone or line input, the other as line input only.
3. Each channel can be connected as either single-ended or fully differential.
4. Each channel has an analog and digital programmable gain stage.

The audio output circuitry consists of a dual differential class A-B output stage.

NOTE NVC-MDCS58 is designed for a differential audio output. If a single-ended audio output is required, use an external differential to single-ended converter.

3.3.2 Digital Audio Interface (I^2S)

The digital audio interface supports the industry standard formats for I2S, left-justified or right-justified. The interface shares the same pins of the SPI interface as Table 11.

Pin No.	SPI Interface (SPI_PCM=1)	I^2S Interface (SPI_PCM=0)
5	SPI_MISO	SD_OUT
7	SPI_MOSI	SD_IN
9	SPI_CLK	SCK
3	SPI_CS	WS

Table 11: Alternative Functions of the Digital Audio Bus Interface on the SPI Interface

The module is an I2S slave device with the default firmware. Contact with NovaComm for special firmware when use the module as an I2S master. The I2S support following formats:

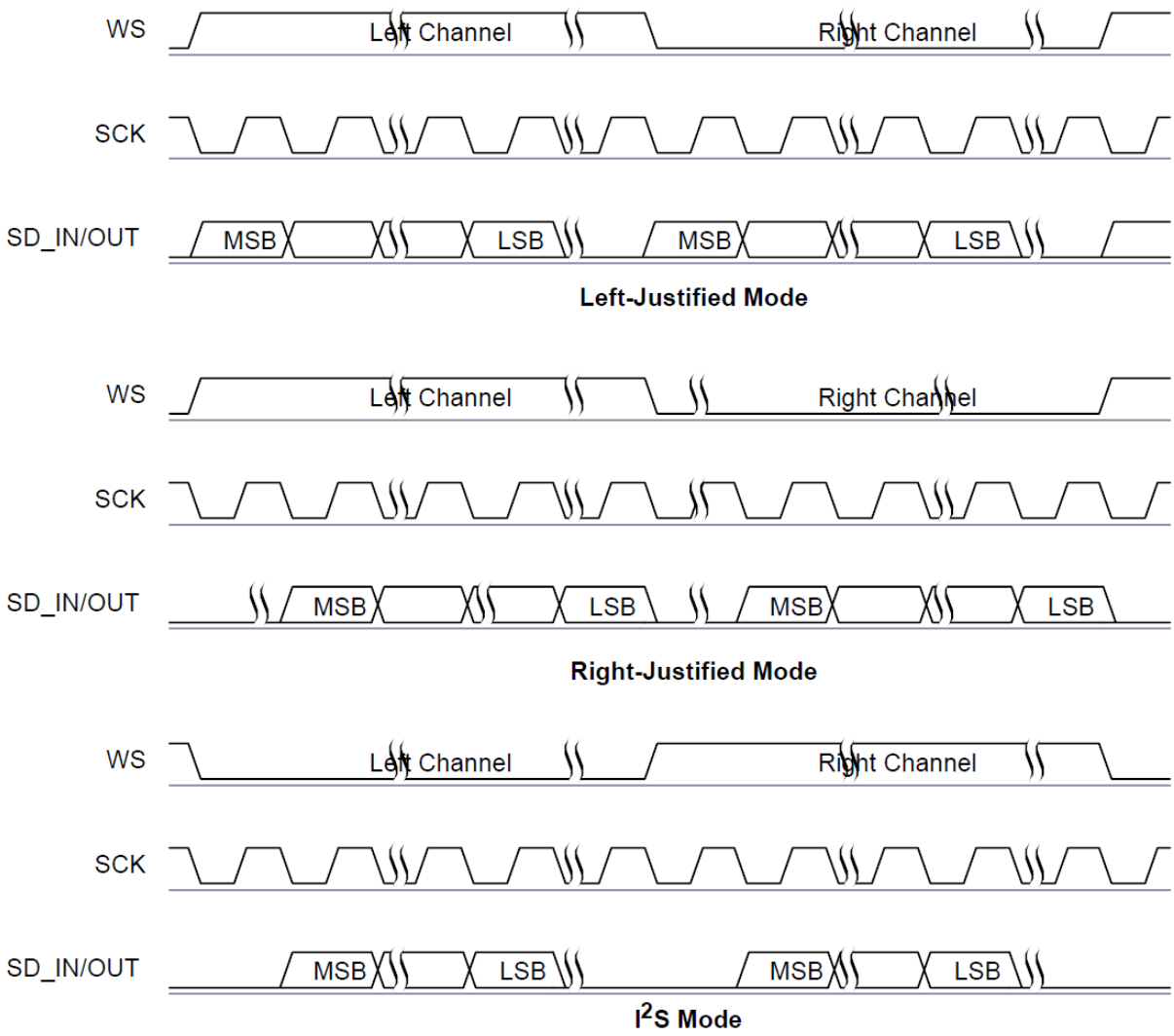


Figure 2 : Digital Audio Interface Modes

Symbol	Parameter	Min	Typical	Max	Unit
-	SCK Frequency	-	-	6.2	MHz
-	WS Frequency	-	-	96	kHz
t_{ch}	SCK high time	80	-	-	ns
t_{cl}	SCK low time	80	-	-	ns
t_{opd}	SCK to SD_OUT delay	-	-	20	ns
t_{ssu}	WS to SCK set up time	20	-	-	ns
t_{sh}	WS to SCK hold time	2.5	-	-	ns
t_{isu}	SD_IN to SCK set-up time	20	-	-	ns
t_{ih}	SD_IN to SCK hold time	2.5	-	-	ns

Table 12 : Digital Audio Interface Slave Timing

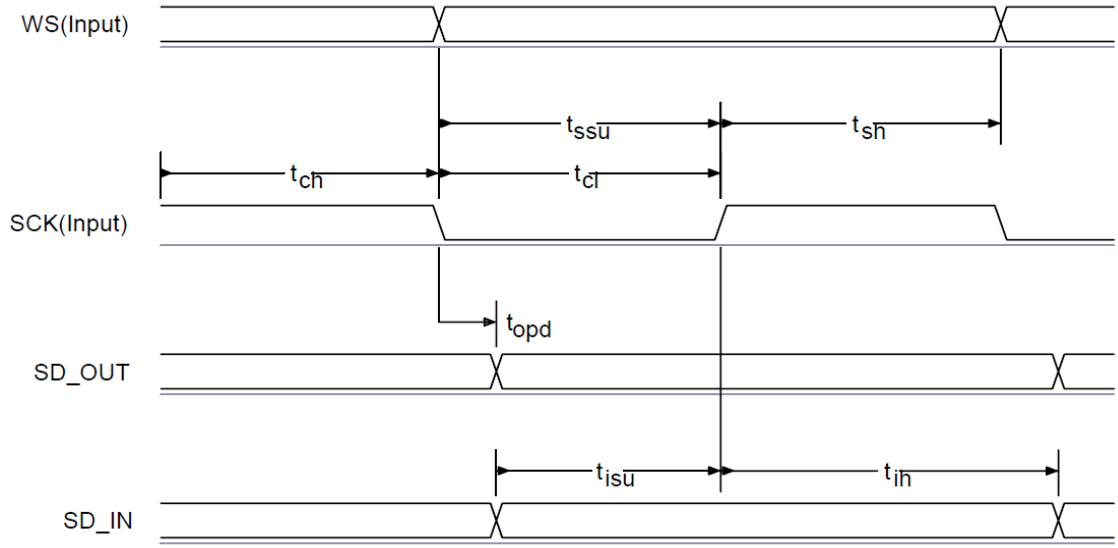


Figure 3 : Digital Audio Interface Slave Timing

Symbol	Parameter	Min	Typical	Max	Unit
-	SCK Frequency	-	-	6.2	MHz
-	WS Frequency	-	-	96	kHz
t_{opd}	SCK to SD_OUT delay	-	-	18.44	ns
t_{spd}	SCK to WS delay	-	-	39.27	ns
t_{isu}	SD_IN to SCK set-up time	18.44	-	-	ns
t_{ih}	SD_IN to SCK hold time	0	-	-	ns

Table 13 : Digital Audio Interface Master Timing

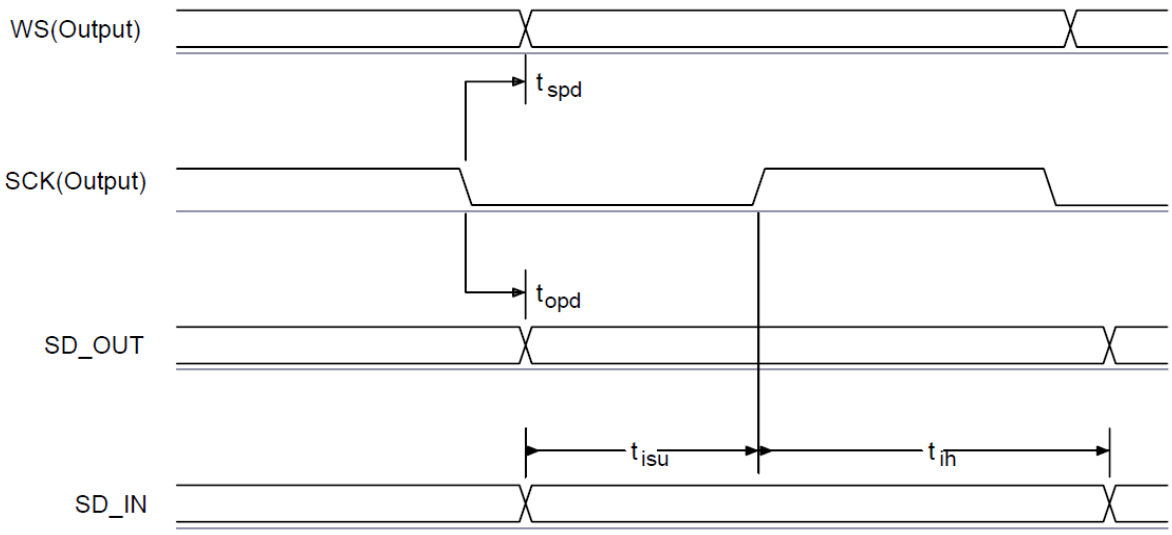


Figure 4 : Digital Audio Interface Master Timing

3.4 General Purpose Analog IO

The module has one general-purpose analogue interface pins, AIO0. In a Li+ battery application, it can be designed to monitor the temperature of the battery.

3.5 LED Drivers

The NVC-MDCS58 includes a 3-pad PWM LED driver for driving RGB LEDs for producing a wide range of colors.
All LEDs are controlled by application.
The terminals are open-drain outputs, so the LED must be connected from a positive supply rail to the pad in series with a current-limiting resistor.

3.6 Serial Interfaces

3.6.1 Bluetooth UART

The module has a standard UART serial interface that provides a simple mechanism for communicating using RS232 protocol.

Table 14 : Possible UART Settings

Parameter		Possible Values
Baud Rate	Minimum	1200 baud (≤2%Error)
		9600 baud (≤1%Error)
	Maximum	4M baud (≤1%Error)
Flow control		RTS/CTS or None
Parity		None, Odd or Even
Number of Stop Bits		1 or 2
Bits per Byte		8

3.6.2 USB

NVC-MDCS58 has a full-speed (12 Mbps) USB interface for communicating with other compatible digital devices. The USB interface on NVC-MDCS58 acts as a USB peripheral, responding to requests from a master host controller.
NVC-MDCS58 contains internal USB termination resistors and requires no external resistors.
NVC-MDCS58 supports the Universal Serial Bus Specification, Revision v2.0 (USB v2.0 Specification), supports USB standard charger detection, and fully supports the USB Battery Charging Specification v1.2.

3.6.3 I²C

PIO6 and PIO7 can be used to form a master I2C interface. PIO lines need to be pulled up through 2.2Kohm resistors.

3.6.4 SPI Interface

The synchronous serial port interface (SPI) is used for debug and testing purpose. It cannot be used for any user functionality. Please always design test points for this interface on the PCB for EMC testing requirement.

4 iNova Stack

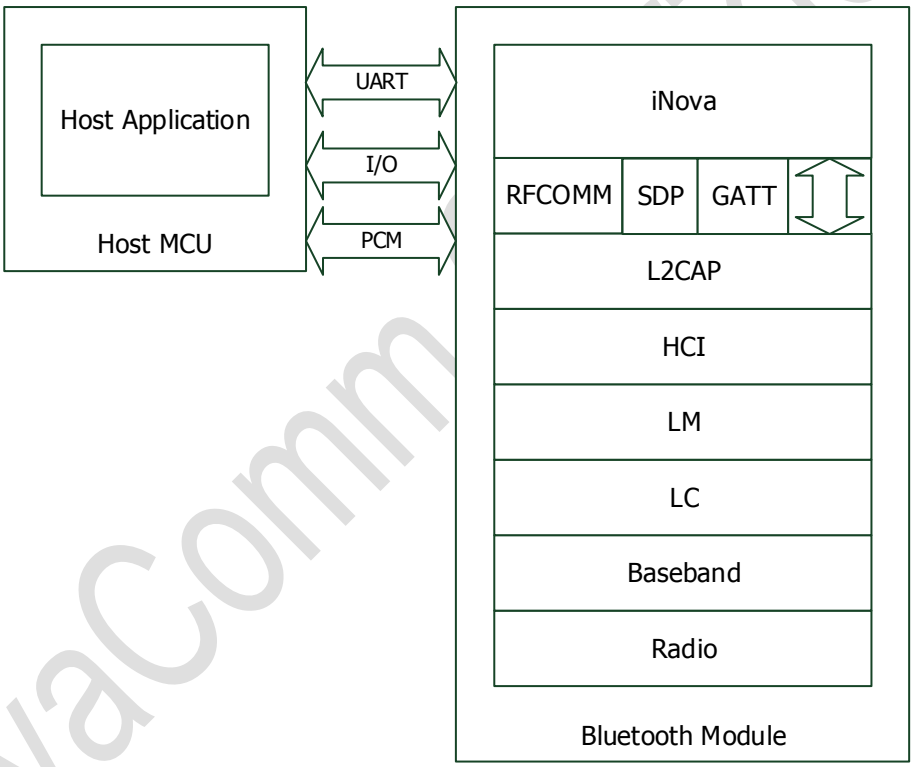


Figure 5: NVC-MDCS58 Stacks

NVC-MDCS58 is supplied with Bluetooth 4.2 compliant stack firmware. With NovaComm's iNova profile stacks, the host MCU can easily integrate HFP, A2DP, AVRCP, SPP, HID profiles and iAP over Bluetooth functions, it also supports GATT based profiles over BLE.

5 Reference Design

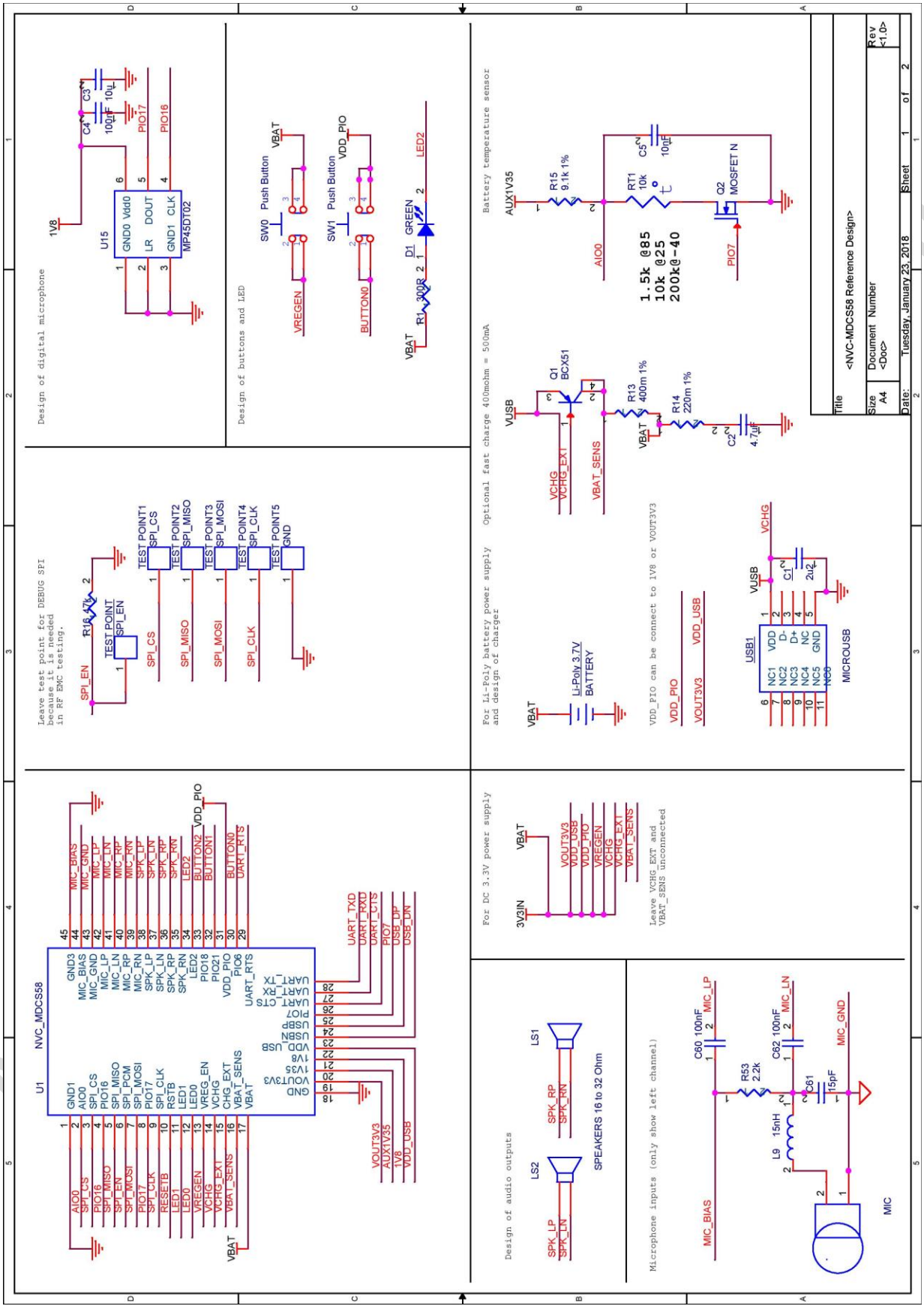


Figure 6: Schematics reference design

6 Mechanical Size and Recommended PCB Footprint

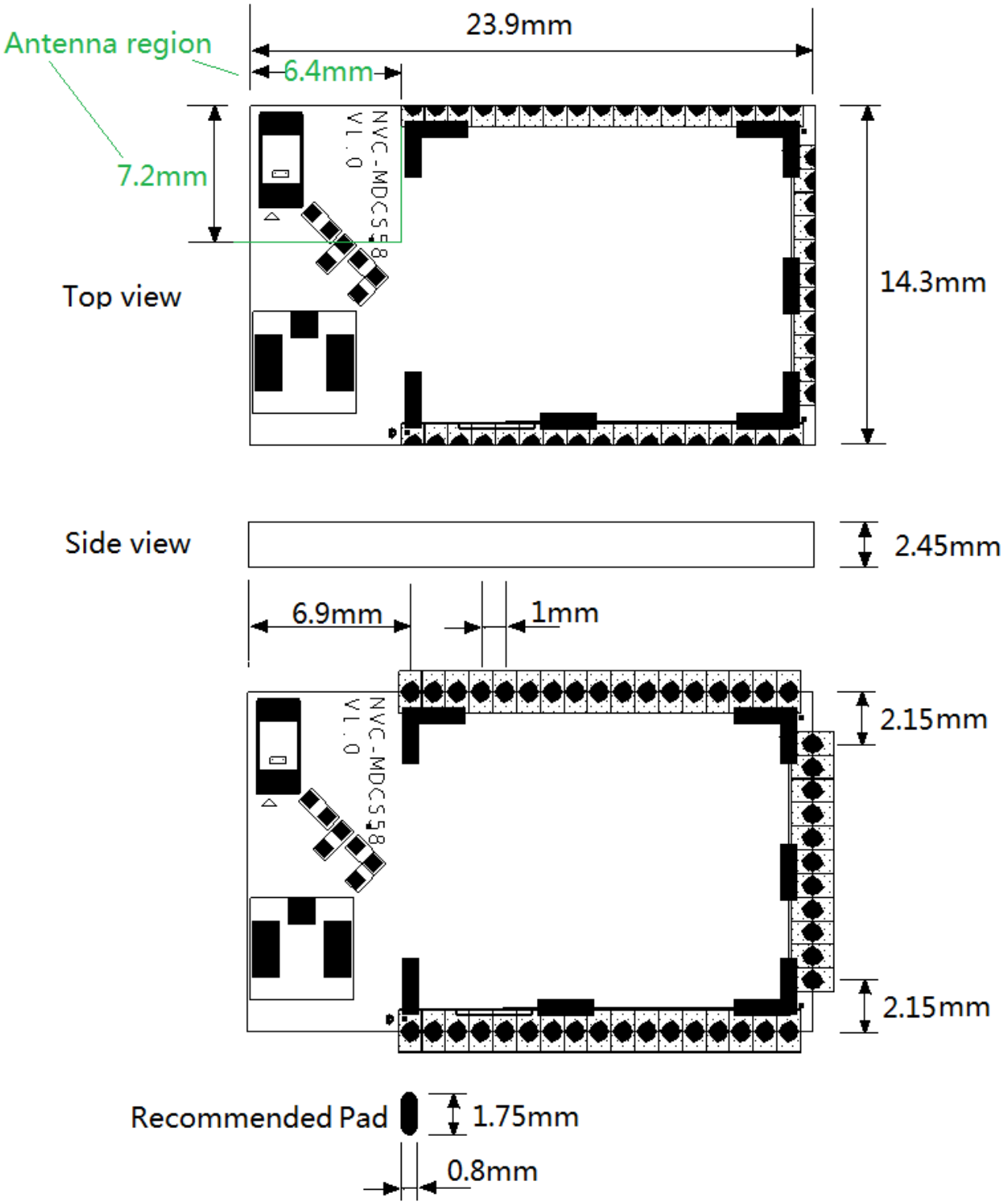


Figure 7: Mechanical Size and Recommended PCB Footprint

7 RF Layout Guidelines

NVC-MDCS58 integrates a chip antenna to radiate and receive the RF signals. The antenna has been well designed and tuned on the module but it still need to have good ground clearance around the antenna to get good RF performance.

1. No ground below antenna region (the rectangle with green line as the boarder in Figure 7) of the NVC-MDCS58.
2. There should also have a good ground panel on the main PCB board on which the module is mounted. As shown in Figure 8.

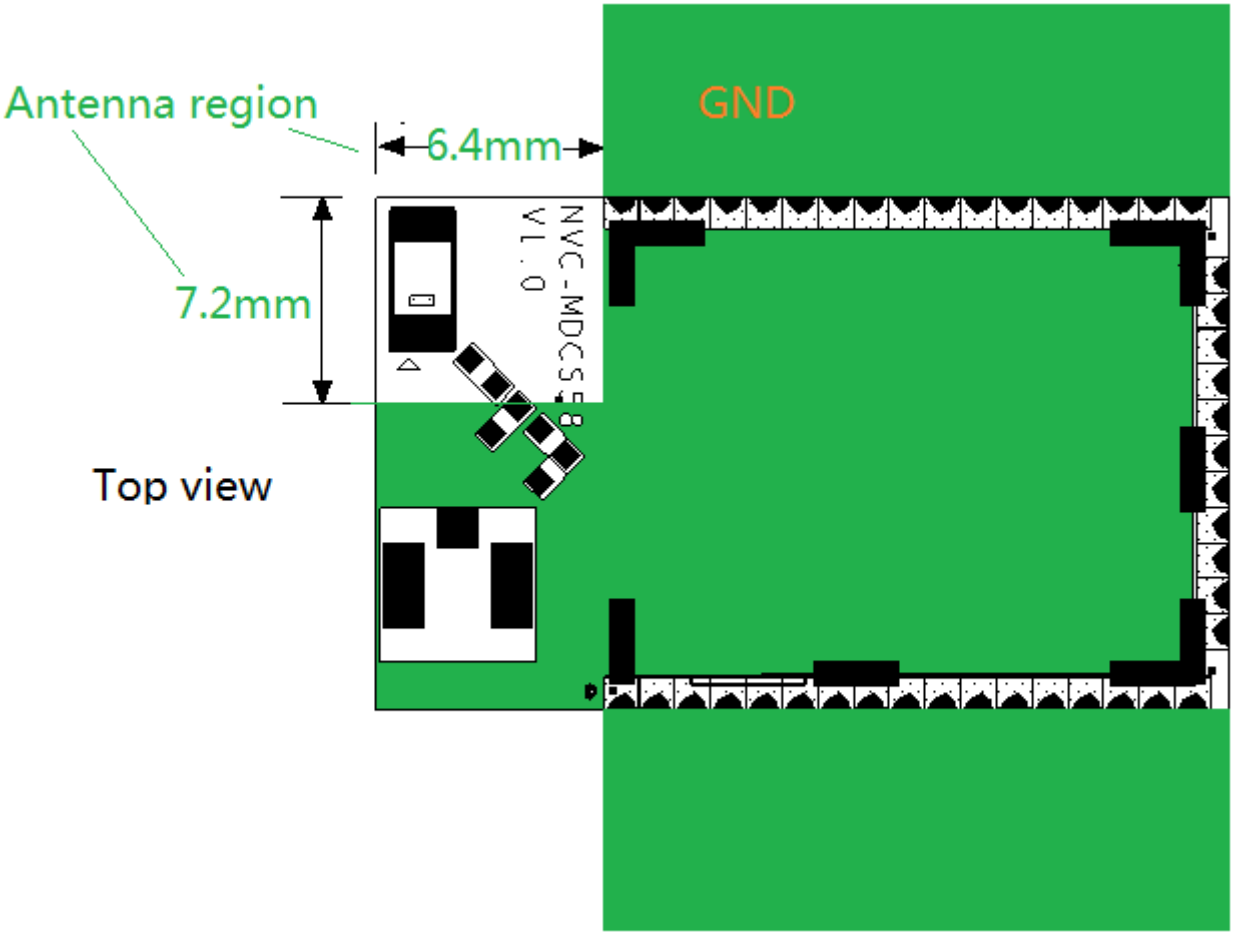


Figure 8 : Placement the module and the ground of main PCB Board

8 Reflow Profile

NVC-MDCS58 is compatible with industrial standard reflow profile for Pb-free solders. The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder re-flow.

There are four zones:

Preheat Zone - This zone raises the temperature at a controlled rate, typically 1-2.5°C/s.

Equilibrium Zone - This zone brings the board to a uniform temperature and also activates the flux. The

duration in this zone (typically 2-3 minutes) will need to be adjusted to optimise the out gassing of the flux.
Reflow Zone- The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint.
Cooling Zone - The cooling rate should be fast, to keep the solder grains small which will give a longer lasting joint. Typical rates will be 2-5°C/s.

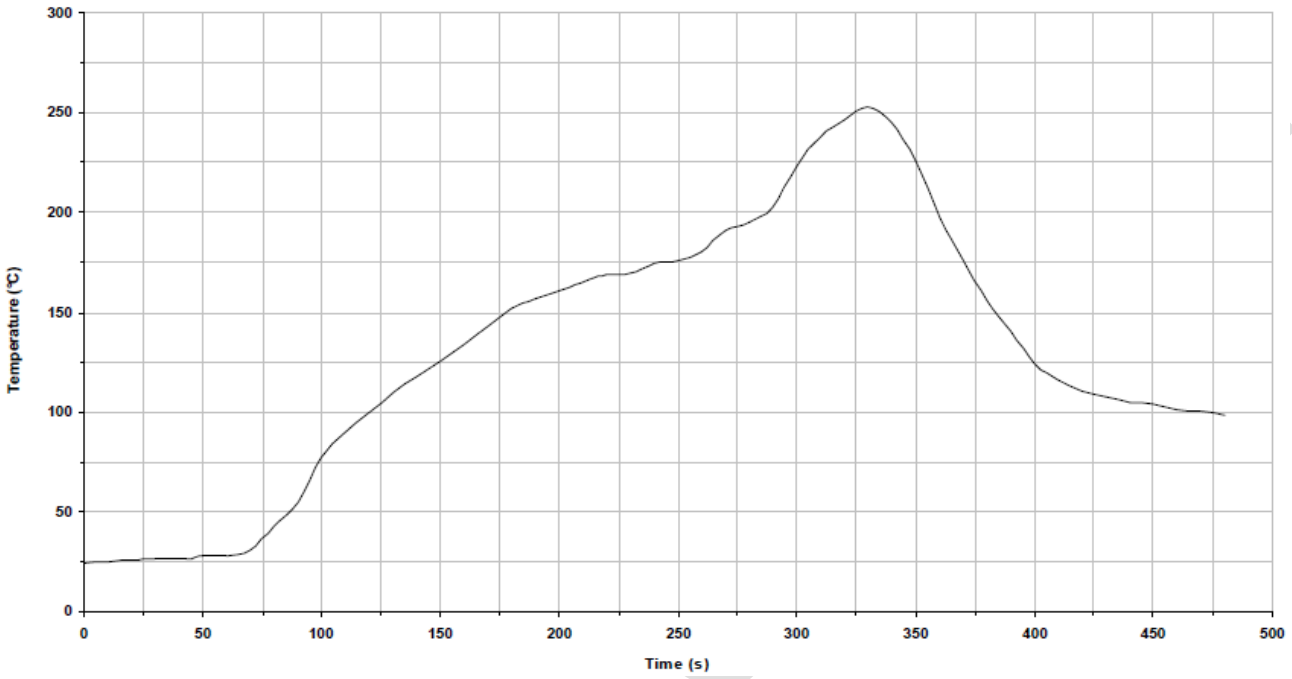


Figure 9: Typical Lead-Free Re-flow Solder Profile for NVC-MDCS58

Key features of the profile:

- Initial Ramp = 1-2.5°C/sec to 175°C ±25°C equilibrium
- Equilibrium time = 60 to 180 seconds
- Ramp to Maximum temperature (250°C) = 3°C/sec max.
- Time above liquidus temperature (217°C): 45-90 seconds
- Device absolute maximum reflow temperature: 255°C

Note: Customer might choose a local 0.2mm thickness solder cream for the module, or use 0.15mm to match other components in the same PCB.

9 Package

TBD

Figure 10: NVC-MDCS58 Package

Plastic tray, plus aluminum bags do vacuum packing. Items in One Package number of 100 PCS, external aluminum foil vacuum packaging.
The module's Moisture Sensitivity Level is level 3 in accordance with JEDEC J-STD-020.

FCC Statement

Any Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions:
(1) This device may not cause harmful interference, and
(2) This device must accept any interference received, including interference that may cause undesired operation.

FCC Radiation Exposure Statement:

This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment .This equipment should be installed and operated with minimum distance 20cm between the radiator& your body.

FCC Label Instructions

The outside of final products that contains this module device must display a label referring to the enclosed module. This exterior label can use wording such as: "Contains Transmitter Module FCC ID:OC3BM1858",or "Contains FCC ID:OC3BM1858", Any similar wording that expresses the same meaning may be used.

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