NovaComm
NVC-MDCS56 Datasheet

Ver.2.4

July 1, 2013

Release Record

Version	Release Date	Comments
2.0	Mar 03, 2012	Release
2.1	Sep 04,2012	Increase feature
2.2	Oct 01, 2012	Updates reference design. Fix several format and spell errors
2.3	Feb 22,2013	Updates reference design and Recommended PCB Mounting Pattern
2.4	July 1,2013	Updates mechanical and footprint information, fix print errors in IO descriptions.

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Description:

NVC-MDCS56 is a class 2 Bluetooth® 2.1+EDR (Enhanced Data Rate) module. It is based on CSR's BlueCore5-Multimedia. With internal DSP and audio codec, it is an ideal solution for integrating Bluetooth® audio functions into various products with minima efforts.

With NovaComm's iNova® stack, designers can easily customize their applications to support different Bluetooth profiles, such as HS/HF, A2DP, AVRCP, OPP, DUN, SPP, iAP over Bluetooth for Apple, HID and etc. The module support different flash size (8M/16M/32M bits) for different combination of profiles.

And the module can also interface with Apple's Authentication Coprocessor and build an iAP over Bluetooth application. Please contact NovaComm for special firmware.

Typical Bluetooth audio applications:

- Home entertainment
- Office and mobile accessories

Features:

- Bluetooth® v2.1+EDR（Class2）
- +4dBm TX power, -86.0dBm RX sensitivity
- Support Profiles: HS/HF, A2DP, AVRCP, OPP, DUN, SPP, iAP over Bluetooth for Apple, HID and etc.
- UART/I2C master
- 12 digital PIOs
- Support PCM interface (SPDIF ,I^2S)
- Software Support Apt-X ,AAC, Apt-XLL, SBC codec.
- Wakeup interrupt and watchdog timer
- 23.24mm x 11.93mm x 2.05mm
- SMT pads for easy and reliable PCB mounting,
- QDID:B019582
- RoHS compliant

Ordering Number	Package	Items in One Package	Comments
NVC-MDCS56	Plastic tray	100	16Mbits flash

Table 1: Ordering Information

Please also supply the customer firmware code issued by NovaComm Technologies when you place the order.

1 Pinout and Description

1.1 Pin Configuration

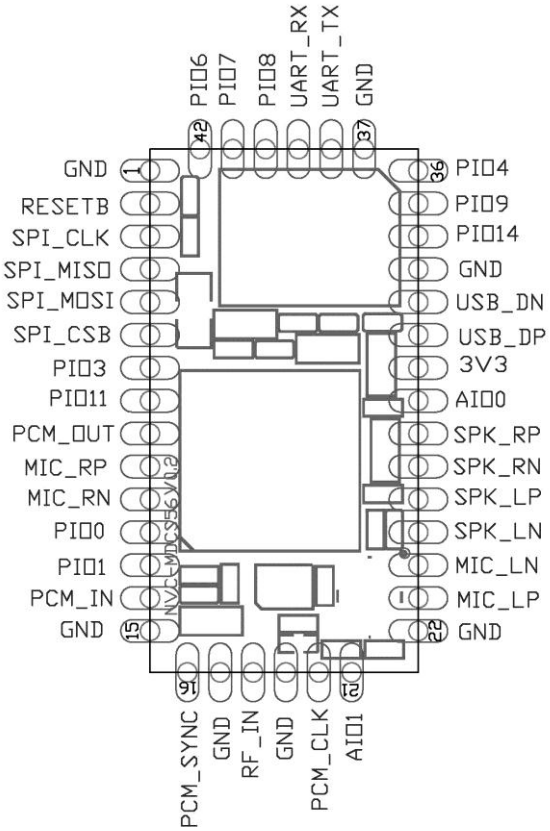

Figure 1: Pinout for NVC-MDCS56

1.2 Pin Configuration

Pin	Symbol	I/O Type	Description
1	GND	Ground	Ground
2	RESETB	CMOS input with weak internal pull-up	Active LOW reset, input debounced so must be low for >5ms to cause a reset
3	SPI_CLK	Input with weak internal pull-down	Serial Peripheral interface clock for programming only
4	SPI_MISO	CMOS output, tri-state, with weak internal pull-down	Serial Peripheral Interface output for programming only
5	SPI_MOSI	CMOS input, with weak internal pull-down	Serial Peripheral Interface input for programming only

6	SPI_CSB	Input with weak internal pull-up	Chip select for Synchronous Serial Interface for programming only, active low
7	PIO3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
8	PIO11	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
9	PCM_OUT	CMOS output, tri-state, with weak internal pull-down	Synchronous Data Output
10	MIC_RP	Analogue	Microphone input positive, right
11	MIC_RN	Analogue	Microphone input negative, right
12	PIO0	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
13	PIO1	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
14	PCM_IN	CMOS Input, with weak internal pull-down	Synchronous Data Input
15	GND	Ground	Ground
16	PCM_SYNC	Bi-directional with weak internal pull-down	Synchronous Data Sync
17	RF_GND	RF Ground	RF ground
18	RF_IN	RF	RF Transceiver input/output line
19	RF_GND	RF Ground	RF ground
20	PCM_CLK	Bi-directional with weak internal pull-down	Synchronous Data Clock
21	AIO1	Bi-directional	Analogue programmable input/output line
22	GND	Ground	Ground
23	MIC_LP	Analogue	Microphone input positive, left
24	MIC_LN	Analogue	Microphone input negative, right
25	SPK_LN	Analogue	Speaker output negative, left
26	SPK_LP	Analogue	Speaker output positive, left
27	SPK_RN	Analogue	Speaker output negative, right
28	SPK_RP	Analogue	Speaker output positive, right
29	AIO0	Bi-directional	Analogue programmable input/output line
30	VDD	3V3 power input	3V3 power input
31	USB_DP	Bi-directional	USB data plus with selectable internal 1.5K

			pull up resistor
32	USB_DN	Bi-directional	USB data minus
33	GND	Ground	Ground
34	PIO14	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
35	PIO9	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
36	PIO4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
37	GND	Ground	Ground
38	UART_TX	Bi-directional CMOS output, tri-state, with weak internal pull-up	UART data output
39	UART_RX	CMOS input with weak internal pull-down	UART data input
40	PIO8	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
41	PIO7	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
42	PIO6	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line

Table 2: Pin Definition

2 Electrical Characteristics

2.1 Absolute Maximum Rating

Rating	Min	Max	Unit
Storage Temperature	-40	+125	°C
Operating Temperature	-40	+85	°C
PIO Voltage	-0.4	+3.6	V
AIO Voltage	-0.4	+1.57	V

VDD Voltage	-0.4	+3.6	V
USB_DP/USB_DN Voltage	-0.4	+3.6	V
Other Terminal Voltages except RF	-0.4	VDD+0.4	V

Table 3: Absolute Maximum Rating

2.2 Recommended Operating Conditions

Operating Condition	Min	Typ	Max	Unit
Storage Temperature	-40	--	+105	°C
Operating Temperature Range	-40	--	+85	°C
PIO Voltage	+1.7	+3.3	+3.6	V
AIO Voltage	+1.42	+1.5	+1.57	V
VDD Voltage	+2.7	+3.3	+3.6	V

Table 4: Recommended Operating Conditions

2.3 Input/output Terminal Characteristics

2.3.1 Digital Terminals

Supply Voltage Levels	Min	Typ	Max	Unit
Input Voltage Levels				
V_{IL} input logic level low	-0.3	-	+0.25xVDD	V
V_{IH} input logic level high	0.625VDD	-	VDD+0.3	V
Output Voltage Levels				
V_{OL} output logic level low, I_{OL} = 4.0mA	-	-	0.125	V
V_{OH} output logic level high, I_{OH} = -4.0mA	0.75xVDD	-	VDD	V
Input and Tri-state Current				
I_i input leakage current at V_{in}=VDD or 0V	-100	0	100	nA
I_{oz} tri-state output leakage current at V_o=VDD or 0V	-100	0	100	nA
With strong pull-up	-100	-40	-10	uA
With strong pull-down	10	40	100	μA
With weak pull-up	-5	-1.0	-0.2	μA
With weak pull-down	-0.2	+1.0	5.0	μA

CI Input Capacitance	1.0	-	5.0	pF
Resistive Strength				
R_{puw} weak pull-up strength at VDD-0.2V	500k	-	2M	Ω
R_{pdw} weak pull-down strength at 0.2V	500k	-	2M	Ω
R_{pus} strong pull-up strength at VDD-0.2V	10k	-	50k	Ω
R_{pds} strong pull-down strength at 0.2V	10k	-	50k	Ω

Table 5: Digital Terminal

2.3.2 USB

USB Terminals	Min	Typ	Max	Unit
Input Threshold				
V_{IL} input logic level low	-	-	0.3xVDD	V
V_{IH} input logic level high	0.7xVDD	-	-	V
Input Leakage Current				
GND < VIN < VDD[(a)]	-1	1	5	µA
C_I Input capacitance	2.5	-	10.0	pF
Output Voltage Levels to Correctly Terminated USB Cable				
V_{OL} output logic level low	0.0	-	0.2	V
V_{OH} output logic level high	2.8	-	VDD	V

Table 6: USB Terminal

(a) Internal USB pull-up disabled

2.3.3 Internal CODEC - Analogue to Digital Converter

Parameter	Conditions		Min	Typ	Max	Unit
Resolution			-	-	16	Bits
Input Sample Rate, F_{sample}			8	-	44.1	kHz
Signal to Noise Ratio, SNR	f_{in}=1kHz B/W=20Hz->20kHz A-Weighted THD+N<1% 150mV Vpk-pk	F_{sample}				
		8kHz	-	82	-	dB
		11.025kHz	-	81	-	
		16kHz	-	80	-	
		22.050kHz	-	79	-	
		32kHz	-	79	-	
		44.1kHz	-	78	-	
Digital Gain	Digital Gain Resolution = 1/32 dB		-24	-	21.5	dB

Analogue Gain	Analogue Gain Resolution = 3dB	-3	-	42	dB
Input full scale at maximum gain (differential)		-	4	-	mV rms
Input full scale at minimum gain (differential)		-	800	-	mV rms
3dB Bandwidth		-	20	-	kHz
Microphone mode input impedance		-	6	-	kΩ
THD+N (microphone input) @ 30mv rms input			0.04		%

Table 7: Analogue to Digital Converter

2.3.4 Internal CODEC - Digital to Analogue Converter

Parameter	Conditions		Min	Typ	Max	Unit
Resolution			-	-	16	Bits
Output Sample Rate, F_{sample}			8	-	48	kHz
Signal to Noise Ratio, SNR	f_{in}=1kHz B/W=20Hz->20kHz A-Weighted THD+N<0.01% 0dBFS signal Load = 100kΩ	F_{sample}				
		8kHz	-	95	-	dB
		11.025kHz	-	95	-	
		16kHz	-	95	-	
		22.050kHz	-	95	-	
		32kHz	-	95	-	
		44.1kHz	-	95	-	
		48kHz	-	95		
Digital Gain	Digital Gain Resolution = 1/32 dB		-24	-	21.5	dB
Analogue Gain	Analogue Gain Resolution = 3dB		0	-	-21	dB
Output voltage full swing (differential)			-	750	-	mV rms
Allowed Load		Resistive	16(8)	-	OC	Ω
		Capacitive	-	-	500	pF
THD+N 100kΩ load			-	-	0.01	%
THD+N 16Ω load			-	-	0.1	%
SNR (Load=16Ω, 0dBFS input relative to digital silence)			-	95	-	dB

Table 8: Digital to Analogue Converter

2.4 Power consumptions

Operating Condition	Min	Average	Max	Unit
Connected Idle (Sniff(a)1.28 secs)		0.45		mA
Connected with audio streaming (A2DP)	30	35	40	mA

Deep Sleep Idle mode		50		uA
Radio On (Discovery)		23		mA
Radio On (Inquiry window time)		35		mA

Table 9: Power consumptions

Note :

Power consumption depends on the firmware used. Typical values are shown in the table.

(a)Sniff mode ----- In Sniff mode, the duty cycle of the slave's activity in the piconet may be reduced. If a slave is in active mode on an ACL logical transport, it shall listen in every ACL slot to the master traffic, unless that link is being treated as a scatternet link or is absent due to hold mode. With sniff mode, the time slots when a slave is listening are reduced, so the master shall only transmit to a slave in specified time slots. The sniff anchor points are spaced regularly with an interval of Tsniff.

3 Physical Interfaces

3.1 Power Supply

The module accepts a 3.3V DC power input. Power supply should guarantee good ripple suppression and enough current.

3.2 Reset

The module may be reset from several sources: RESETB pin, power-on reset, a UART break character or via software configured watchdog timer.

The RESETB pin is an active low reset and is internally filtered using the internal low frequency clock oscillator. A reset will be performed between 1.5 and 4.0ms following RESETB being active. It is recommended that RESETB be applied for a period greater than 5ms.

At reset the digital I/O pins are set to inputs for bi-directional pins and outputs are tri-state. The pull-down state is shown below.

Pin Name / Group	Pin Status on Reset
USB_DP	N/a
USB_DN	N/a
UART_RX	PD
UART_TX	PU
SPI_MOSI	PD
SPI_CLK	PD
SPI_CSB	PU
SPI_MISO	PD
RESETB	PU

PIOs	PD
PCM_IN	PD
PCM_CLK	PD
PCM_SYNC	PD
PCM_OUT	PD

Table 10: Pin Status on Reset

Note: Pull-up (PU) and pull-down (PD) default to weak values unless specified otherwise.

3.3 Digital Audio Interfaces

The audio interface circuit consists of:

- Stereo audio codec
- Dual audio inputs and outputs
- A configurable PCM, I²S or SPDIF interface

Figure 2 outlines the functional blocks of the interface. The codec supports stereo playback and recording of audio signals at multiple sample rates with a resolution of 16-bit. The ADC and the DAC of the codec each contain 2 independent channels. Any ADC or DAC channel can be run at its own independent sample rate.

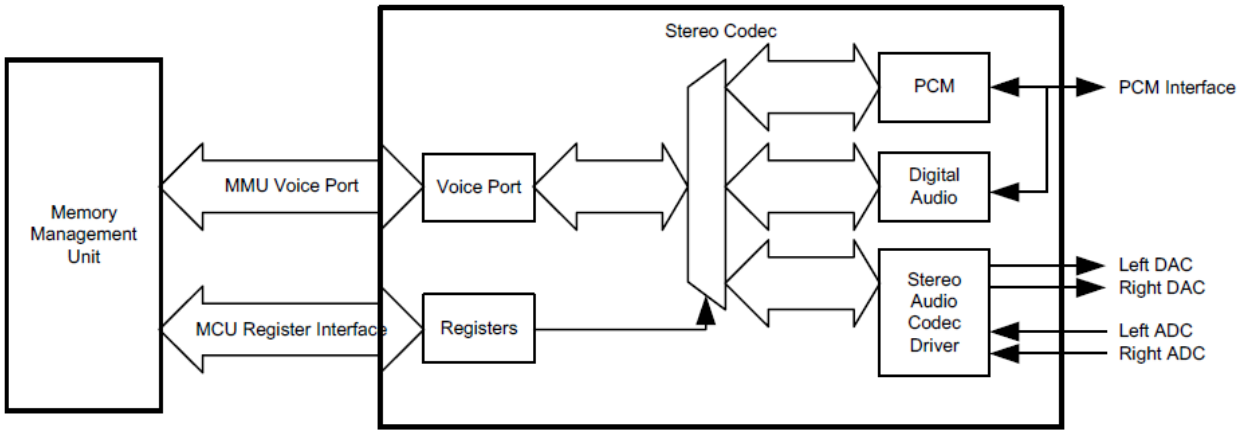

Figure 2 : Audio Interface

The interface for the digital audio bus shares the same pins as the PCM codec interface described in Table 11, which means each of the audio buses are mutually exclusive in their usage. Table 11 lists these alternative functions.

PCM Interface	SPDIF Interface	I²S Interface
PCM_OUT	SPDIF_OUT	SD_OUT
PCM_IN	SPDIF_IN	SD_IN
PCM_SYNC	-	WS
PCM_CLK	-	SCK

Table 11: Alternative Functions of the Digital Audio Bus Interface on the PCM Interface

The audio input circuitry consists of a dual audio input that can be configured to be either single-ended or

fully differential and programmed for either microphone or line input. It has an analogue and digital programmable gain stage for optimization of different microphones.
The audio output circuitry consists of a dual differential class A-B output stage.

3.3.1 PCM

The audio pulse code modulation (PCM) interface supports continuous transmission and reception of PCM encoded audio data over Bluetooth.
Hardware on NVC-MDCS56 allows the data to be sent to and received from a SCO connection. Up to three SCO connections can be supported by the PCM interface at any one time.
NVC-MDCS56 can operate as the PCM interface master generating PCM_SYNC and PCM_CLK or as a PCM interface slave accepting externally generated PCM_SYNC and PCM_CLK.
NVC-MDCS56 is compatible with a variety of clock formats, including Long Frame Sync, Short Frame Sync and GCI timing environments.
It supports 13-bit or 16-bit linear, 8-bit u-law or A-law companded sample formats and can receive and transmit on any selection of three of the first four slots following PCM_SYNC.
NVC-MDCS56 interfaces directly to PCM audio devices including the following:

- Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices
- OKI MSM7705 four channel A-law and μ-law CODEC
- Motorola MC145481 8-bit A-law and μ-law CODEC
- Motorola MC145483 13-bit linear CODEC
- STW 5093 and 5094 14-bit linear CODECs(8)
- NVC_MDCS56 is also compatible with the Motorola SSI interface

3.3.2 Digital Audio Interface (I^2S)

The digital audio interface supports the industry standard formats for I2S, left-justified or right-justified. The interface shares the same pins of the PCM interface as Table 11.
Special firmware is needed if I2S is used. Contact NovaComm for the special firmware when use I2S as the interface between the module and the host or the codec. The I2S support following formats:

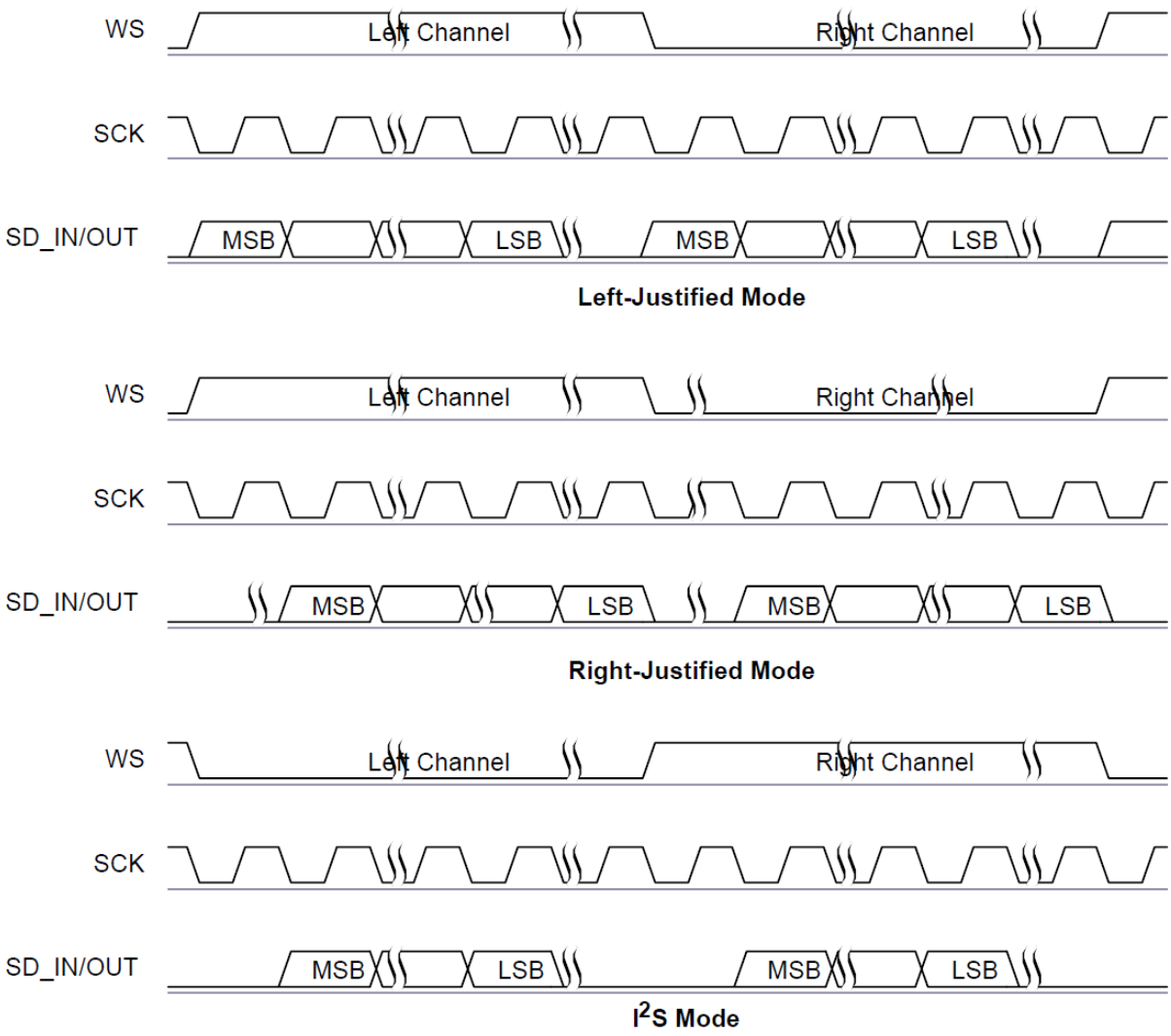

Figure 3 : Digital Audio Interface Modes

Symbol	Parameter	Min	Typical	Max	Unit
-	SCK Frequency	-	-	6.2	MHz
-	WS Frequency	-	-	96	kHz
t_{ch}	SCK high time	80	-	-	ns
t_{cl}	SCK low time	80	-	-	ns
t_{opd}	SCK to SD_OUT delay	-	-	20	ns
t_{ssu}	WS to SCK set up time	20	-	-	ns
t_{sh}	WS to SCK hold time	20	-	-	ns
t_{isu}	SD_IN to SCK set-up time	20	-	-	ns
t_{ih}	SD_IN to SCK hold time	20	-	-	ns

Table 12 : Digital Audio Interface Slave Timing

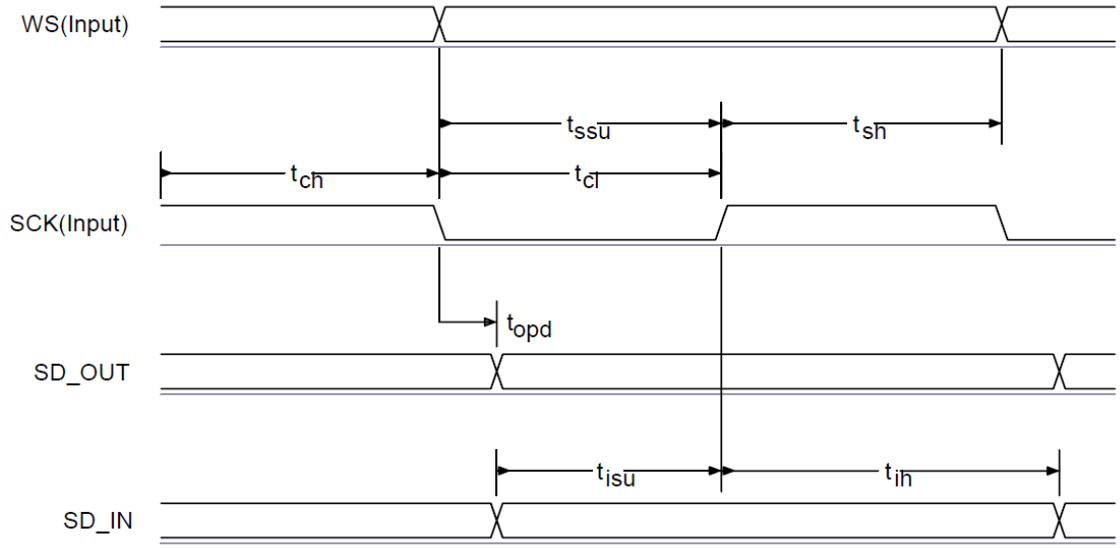

Figure 4 : Digital Audio Interface Slave Timing

Symbol	Parameter	Min	Typical	Max	Unit
-	SCK Frequency	-	-	6.2	MHz
-	WS Frequency	-	-	96	kHz
t_{opd}	SCK to SD_OUT delay	-	-	20	ns
t_{spd}	SCK to WS delay	-	-	20	ns
t_{isu}	SD_IN to SCK set-up time	20	-	-	ns
t_{ih}	SD_IN to SCK hold time	10	-	-	ns

Table 13 : Digital Audio Interface Master Timing

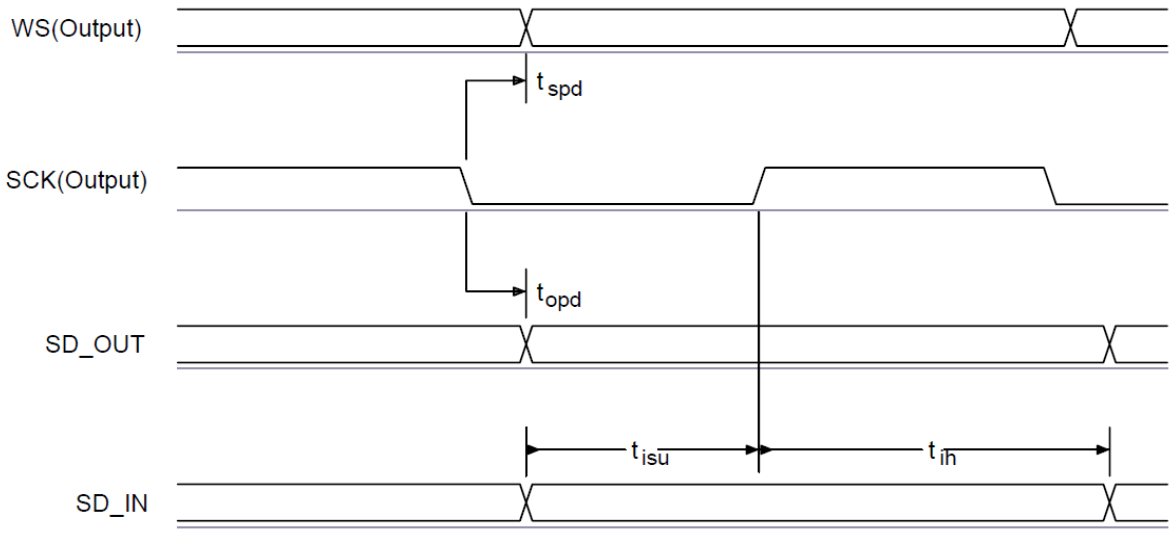

Figure 5 : Digital Audio Interface Master Timing

3.3.3 IEC 60958 Interface (SPDIF)

The IEC 60958 interface is a digital audio interface that uses bi-phase coding to minimise the DC content of the transmitted signal and allows the receiver to decode the clock information from the transmitted signal. The IEC 60958 specification is based on the 2 industry standards:

- AES/EBU
- Sony and Philips interface specification SPDIF

The interface is compatible with IEC 60958-1, IEC 60958-3 and IEC 60958-4.

The SPDIF interface signals are SPDIF_IN and SPDIF_OUT and are shared on the PCM interface pins.

The input and output stages of the SPDIF pins can interface to:

- A 75Ω coaxial cable with an RCA connector, see Figure 6.
- An optical link that uses Toslink optical components, see Figure 7.

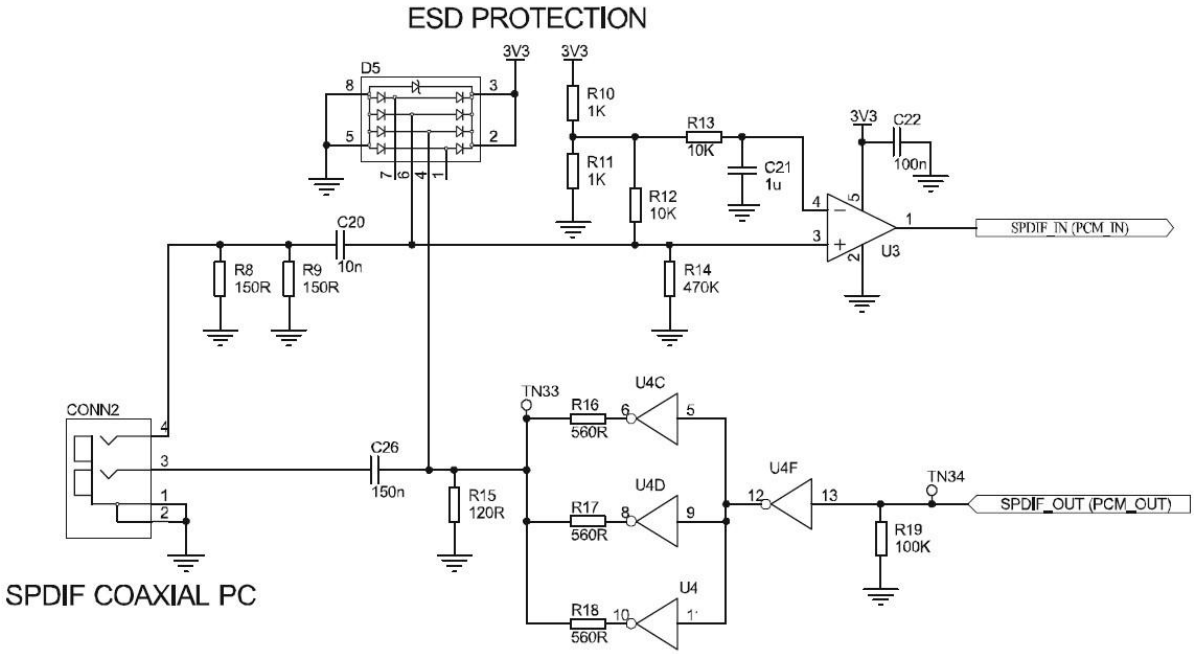

Figure 6: Example Circuit for SPDIF Interface (Co-Axial)

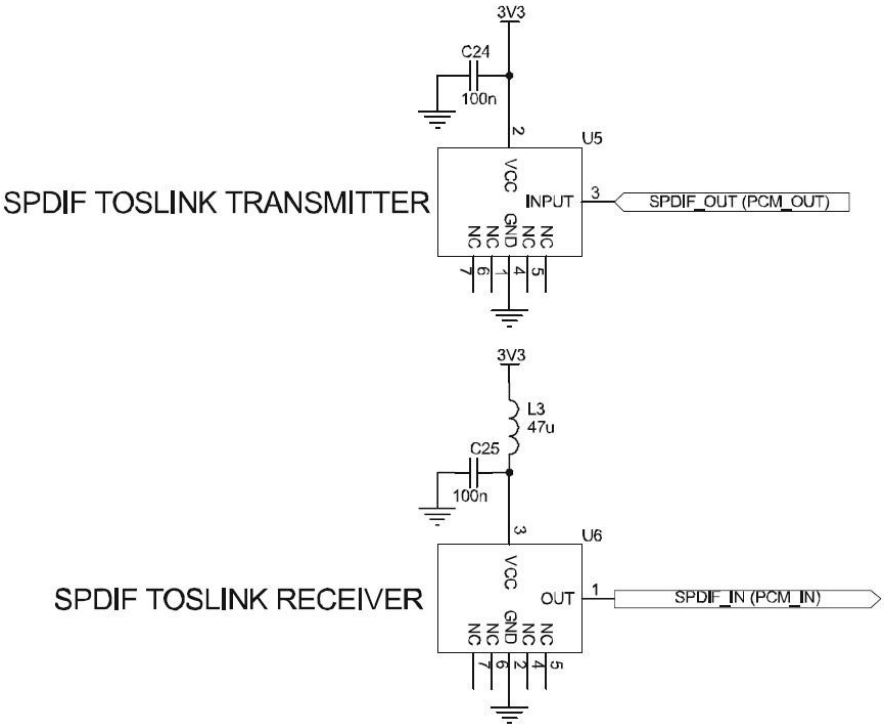

Figure 7: Example Circuit for SPDIF Interface (Optical)

3.4 Microphone input

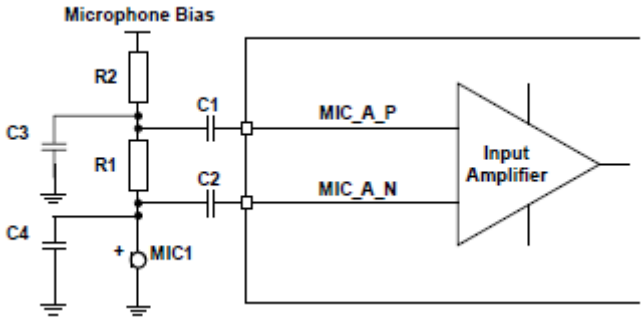

Figure 8: Microphone Biasing (Single Channel Shown)

The audio input is intended for use in the range from 1µA @ 94dB SPL to about 10µA @ 94dB SPL. With biasing resistors R1 and R2 equal to 1kΩ, this requires microphones with sensitivity between about –40dBV and –60dBV. The microphone for each channel should be biased as shown in Figure 8.

3.5 Analog Output stage

The output stage digital circuitry converts the signal from 16-bit per sample, linear PCM of variable sampling frequency to a 2Mbits/s 5-bit multi-bit bit stream, which is fed into the analogue output circuitry.

The output stage circuit is comprised a DAC with gain setting and class AB amplifier. The output is available as a differential signal between SPKR_A_N and SPKR_L_P for the right channel, as Figure 6 shows, and between SPKL_B_N and SPKL_B_P for the left channel.

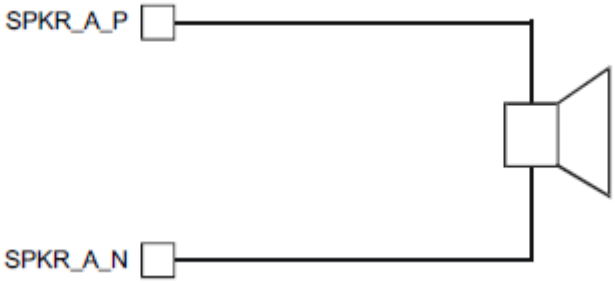

Figure 9: Speaker output

3.6 RF Interface

Input impedance of the RF port is 50Ω so the user can connect a 50Ω antenna directly to the RF port.

3.7 General Purpose Analog IO

The module has two general-purpose analogue interface pins, AIO0 and AIO1. These are used to access internal circuitry and control signals. Auxiliary functions available via these pins include a 10-bit ADC. Signals selectable at these pins include the band gap reference voltage and a variety of clock signals: 64, 48, 32, 24, 16, 12, 8, 6 and 2MHz (outputted from AIO0 only) and the XTAL and XTAL/2 clock frequency (outputted from AIO0 and AIO1).
Do not connect them if not use.

3.8 General Purpose Digital IO

The module has several general-purpose bi-directional input/outputs (I/O). Any of the PIO lines can be configured as interrupt request lines or wake-up lines from sleep modes.
There are nine general purpose digital IOs defined in the module. All these GPIOs can be configured by software to realize various functions, such as button controls, LED displays or interrupt signals to host controller, etc. Do not connect them if not use.

3.9 Serial Interfaces

3.9.1 Bluetooth UART

The module has a standard UART serial interface that provides a simple mechanism for communicating using RS232 protocol. When the module is connected to another digital device, UART_RX and UART_TX transfer data between the 2 devices.

Parameter		Possible Values
Baud Rate	Minimum	1200 baud (≤2%Error)

		9600 baud (≤1%Error)
	Maximum	4M baud (≤1%Error)
Parity		None, Odd or Even
Number of Stop Bits		1 or 2
Bits per Byte		8

Table 14 : Possible UART Settings

3.9.2 USB

This is a full speed (12M bits/s) USB interface for communicating with other compatible digital devices. The module acts as a USB peripheral, responding to request from a master host controller, such as a PC. The USB interface is capable of driving a USB cable directly. No external USB transceiver is required. The device operates as a USB peripheral, responding to requests from a master host controller such as a PC. Both the OHCI and the UHCI standards are supported. The set of USB endpoints implemented can behave as specified in the USB section of the Bluetooth specification v2.0+EDR or alternatively can appear as a set of endpoints appropriate to USB audio devices such as speakers.
The module has an internal USB pull-up resistor. This pulls the USB_DP pin weakly high when module is ready to enumerate. It signals to the USB master that it is a full speed (12Mbit/s) USB device.

3.9.3 I^2C

PIO8, PIO7 and PIO6 can be used to form a master I2C interface as shown in Figure 10. PIO lines need to be pulled up through 2.2Kohm resistors.

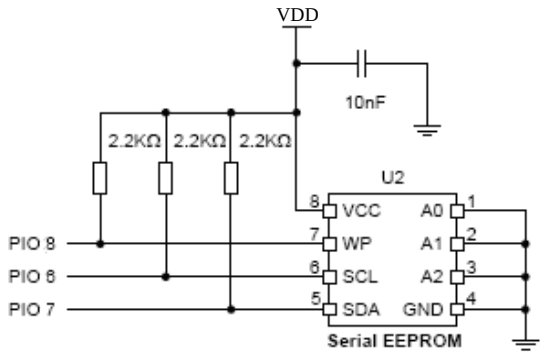

Figure 10: Example EEPROM Connection with I2C Interface

3.9.4 SPI Interface

The synchronous serial port interface (SPI) is used for flash/debug the module only. It cannot be used for any user functionality. Please always design test points for this interface on the PCB in case that the module is needed to re-flash or flash-in-field in manufacture.

4 iNova Stack

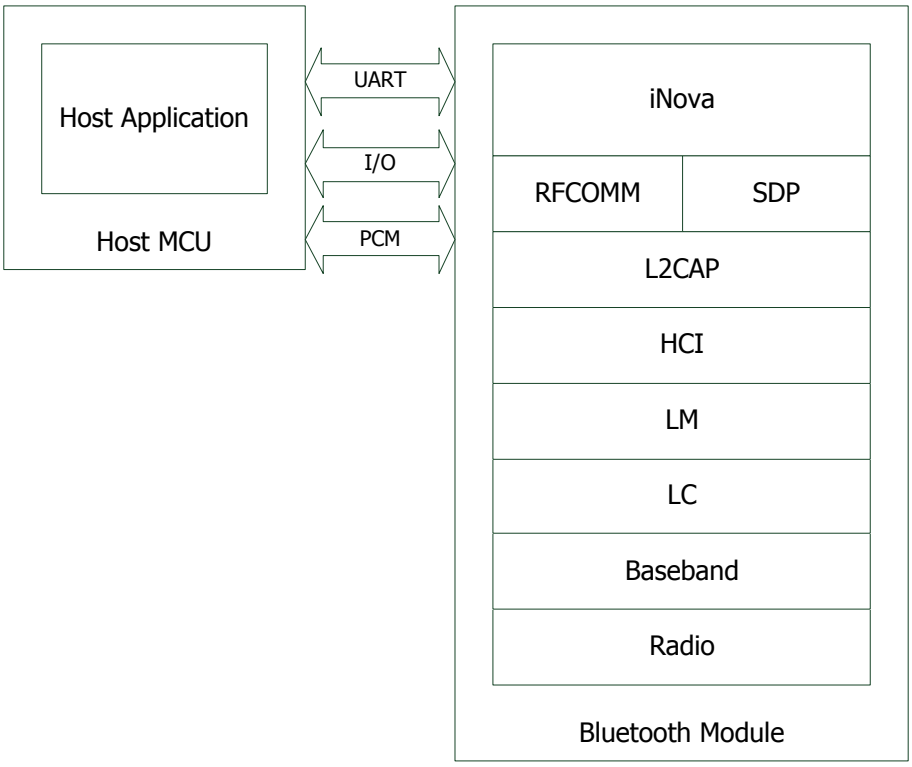

Figure 11: NVC-MDCS56 Stacks

NVC-MDCS56 is supplied with Bluetooth 2.1+EDR compliant stack firmware. With NovaComm's iNova profile stacks, the host MCU can easily integrate HFP, A2DP, AVRCP, SPP, HID profiles and iAP over Bluetooth functions.

5 Reference Design

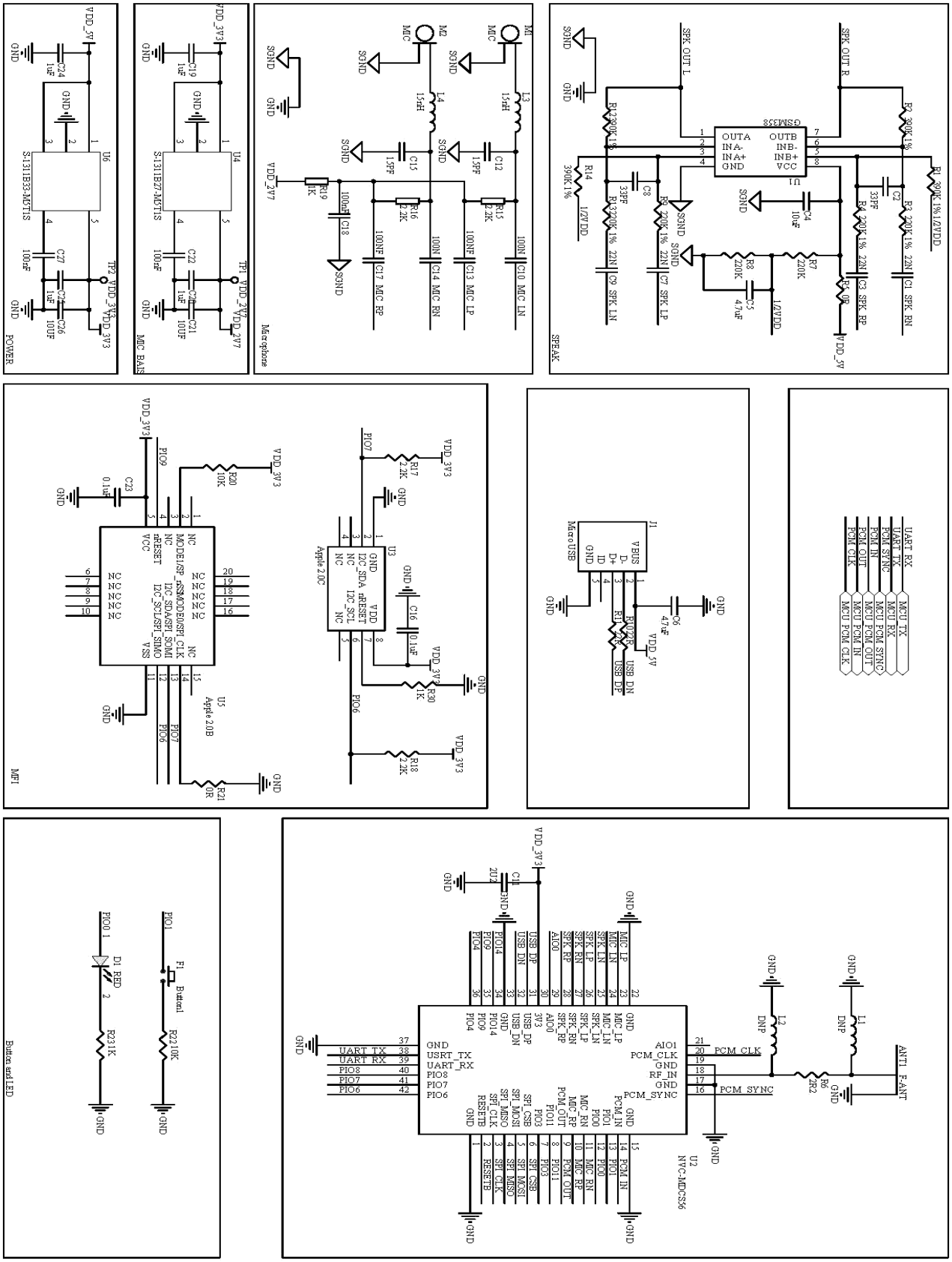

Figure 12: Schematics reference design

6 Mechanical and PCB Footprint Characteristics

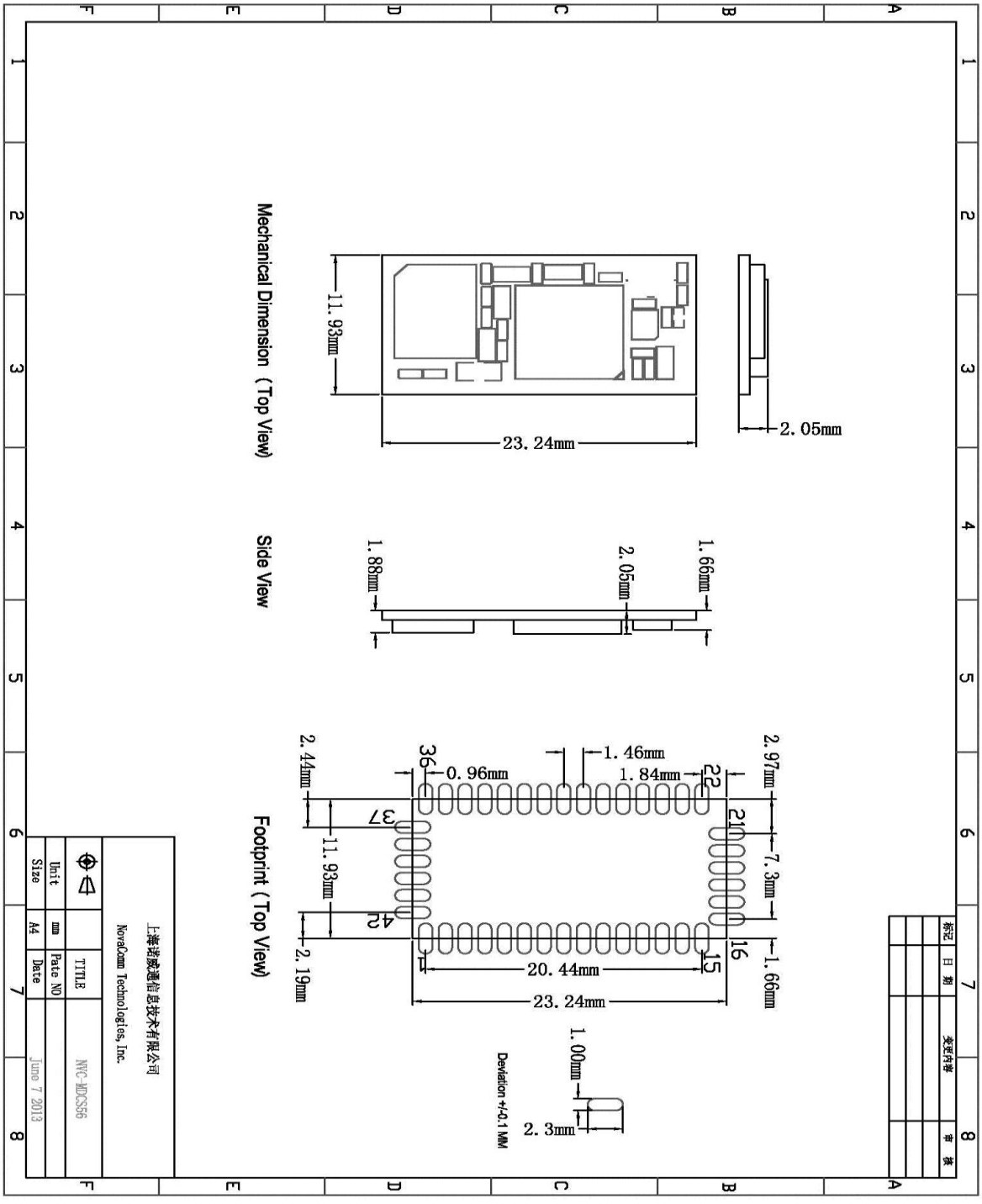

Figure 13: Recommended PCB Mounting Pattern

7 RF Layout Guidelines

NVC-MDCS56 needs a PCB or external antenna to radiate and receive the RF signals. Follow basic RF design guidelines will ensure the design a good RF performance.

7.1 Placement of the Module and Antenna

If PCB antenna is used, please consider the antenna placement according to Figure 14.

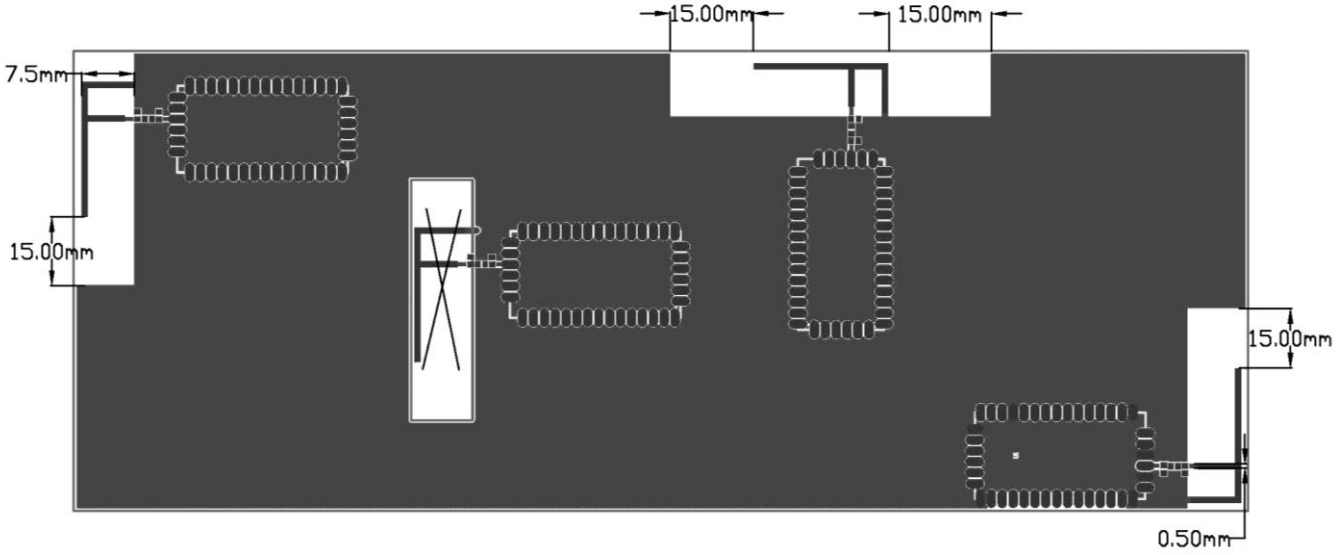

Figure 14 : Placement the module and antenna on a PCB Board

7.2 Feed Line and Antenna

The impedance of the feed line between the RF port and the antenna shall be 50Ω and 1dBi

- A good ground directly under the feed line is always needed for impedance control.
- Route the feed line as curve lines when needed, avoid 90 or even less degree angles style.
- The width of the feed line, the distance of the feed line to the ground plane are keys to the impedance. **Ask your PCB supplier to control the impedance of the feed line.**

For the antenna,

- When PCB antenna is used, matching networks shall be used to optimize the antenna's signal strength.
- Use as many vias as possible to connect the ground planes nearby the antenna.

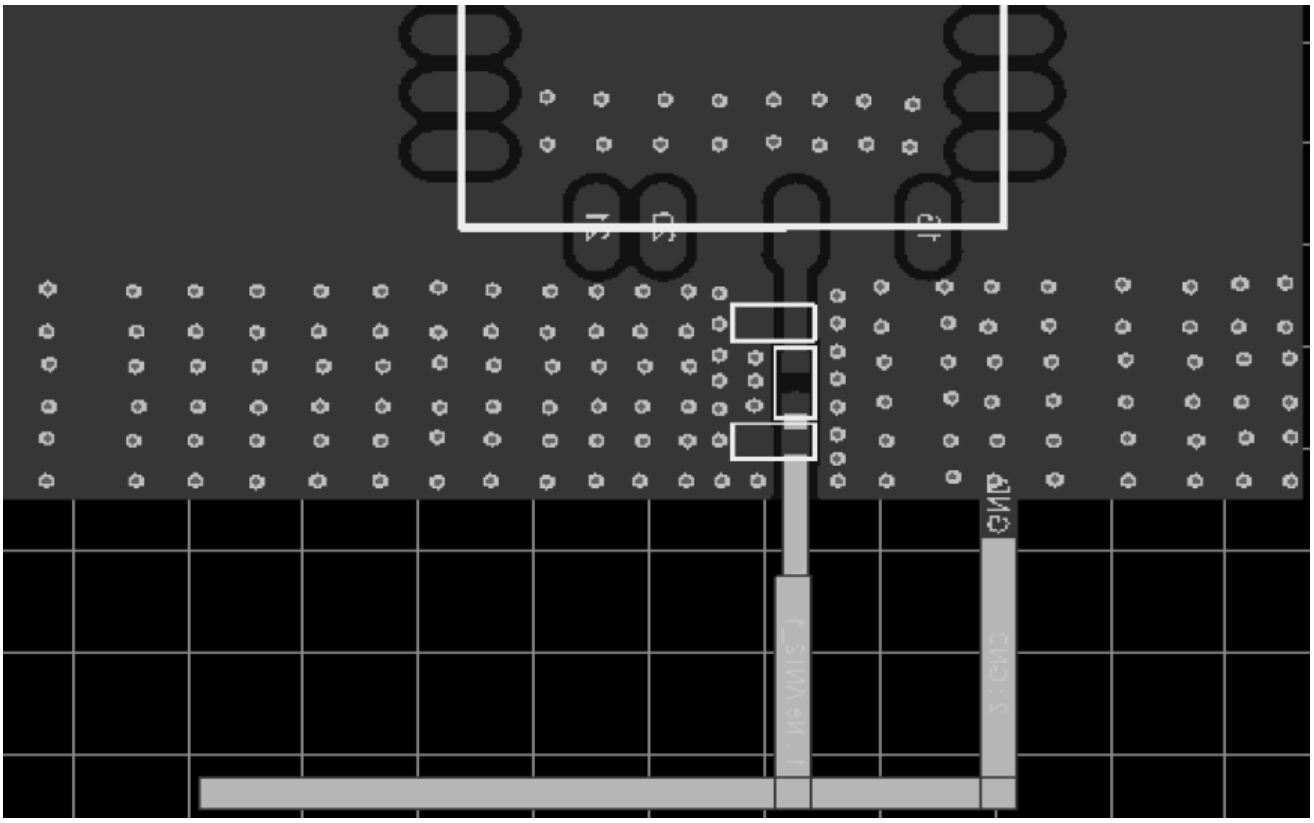

Figure 15: Antenna reference design

8 Reflow Profile

NVC-MDCS56 is compatible with industrial standard reflow profile for Pb-free solders. The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder re-flow.

There are four zones:

1. Preheat Zone - This zone raises the temperature at a controlled rate, typically 1-2.5°C/s.
2. Equilibrium Zone - This zone brings the board to a uniform temperature and also activates the flux. The duration in this zone (typically 2-3 minutes) will need to be adjusted to optimise the out gassing of the flux.
3. Reflow Zone- The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint.
4. Cooling Zone - The cooling rate should be fast, to keep the solder grains small which will give a longer lasting joint. Typical rates will be 2-5°C/s.

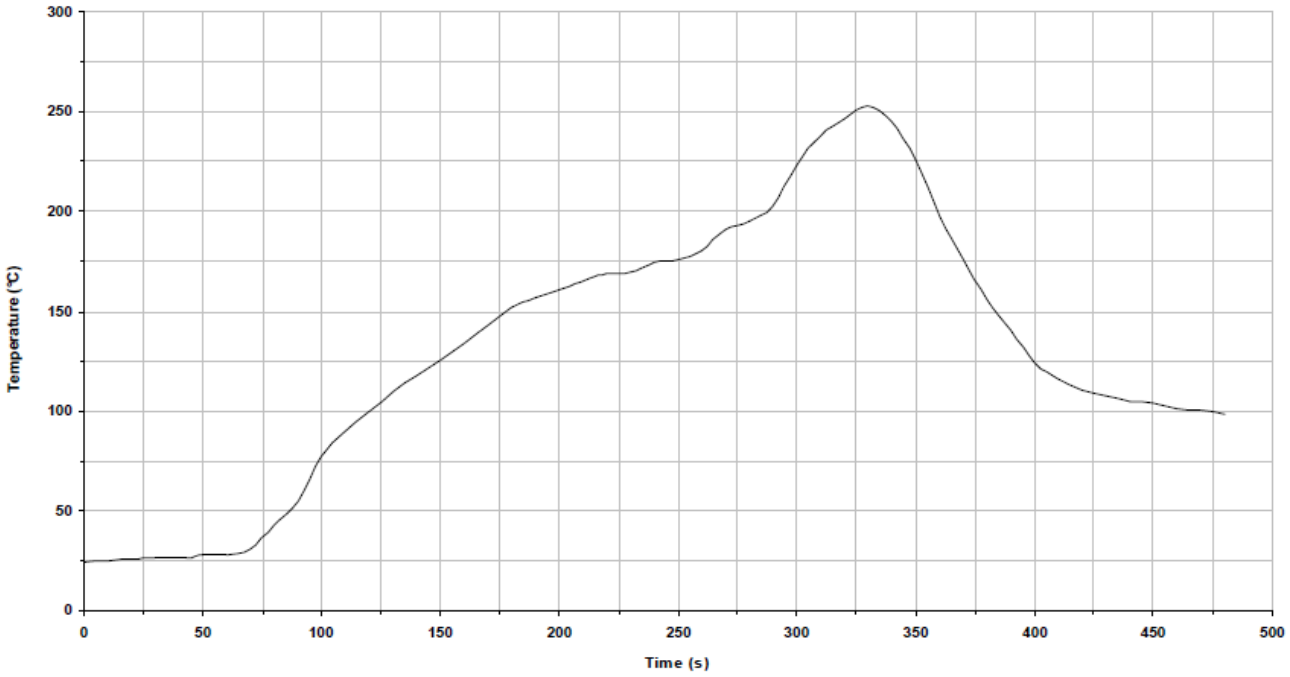

Figure 16: Typical Lead-Free Re-flow Solder Profile for NVC-MDCS56

Key features of the profile:

- Initial Ramp = 1-2.5°C/sec to 175°C ±25°C equilibrium
- Equilibrium time = 60 to 180 seconds
- Ramp to Maximum temperature (250°C) = 3°C/sec max.
- Time above liquidus temperature (217°C): 45-90 seconds
- Device absolute maximum reflow temperature: 255°C

Note: Customer might choose a local 0.2mm thickness solder cream for the module, or use 0.15mm to match other components in the same PCB.

9 Package

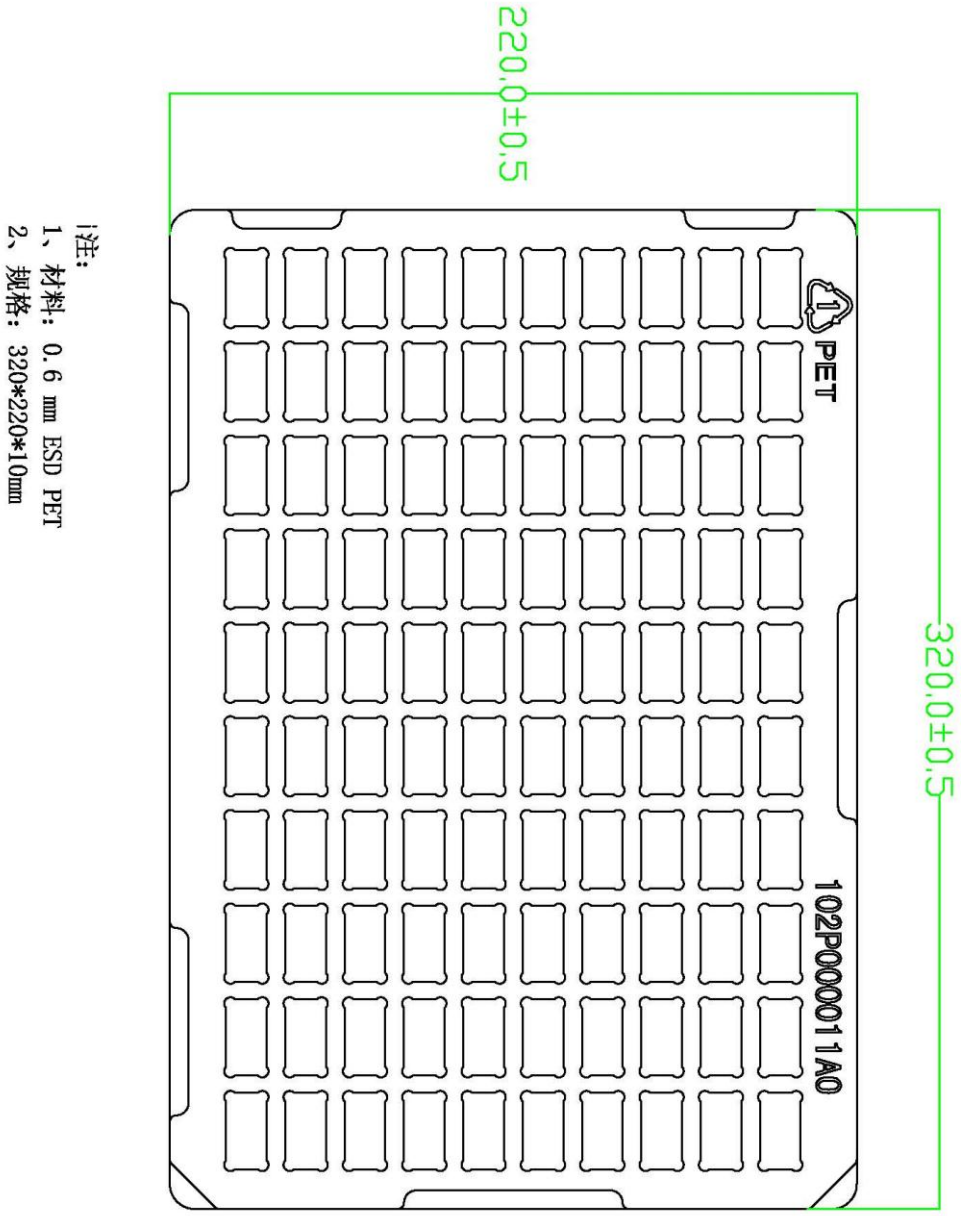

Figure 17: NVC-MDCS56 Package

Plastic tray, plus aluminum bags do vacuum packing. Items in One Package number of 100 PCS.

10 Statement and Contact Information

Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures: Reorient or relocate the receiving antenna; Increase the separation between the equipment and receiver; Connect the equipment into an outlet on a circuit different from that to which the receiver is connected; Consult the dealer or an experienced radio/TV technician for help.

In accordance with FCC Part 15C, this module is listed as a Limited Modular Transmitter device.

Therefore, the final host product must be submitted to [NovaComm Technologies Inc.] for confirmation that the installation of the module into the host is in compliance with the regulations of FCC and IC Canada. Specifically, if an antenna other than the model documented in the Filing is used, a Class 2 Permissive Change must be filed with the FCC.

Changes or modifications not expressly approved by the manufacturer could void the user's authority to operate the equipment.

FCC Label Instructions

The outside of final products that contains this module device must display a label referring to the enclosed module. This exterior label can use wording such as the following: "Contains Transmitter Module FCC ID: [OC3BM1856]" or "Contains FCC ID: [OC3BM1856]." Any similar wording that expresses the same meaning may be used.

To satisfy FCC RF Exposure requirements for mobile and base station transmission devices, a separation distance of 20 cm or more should be maintained between the antenna of this device and persons during operation. To ensure compliance, operation at closer than this distance is not recommended. The antenna(s) used for this transmitter must not be co-located or operating in conjunction with any other antenna or transmitter.

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