NVC-MDCS42 Datasheet

– Class2 Bluetooth V2.1

Innovative Communication in Wireless World

Version –V 2.1

Issue Date – Jan. 25, 2012

FCC and CE Caution NovaComm Technologies

FCC Caution:

§ 15.19 Labelling requirements.
This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

§ 15.21 Information to user.
Any Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

§ 15.105 Information to the user.
Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:
-Reorient or relocate the receiving antenna.
-Increase the separation between the equipment and receiver.
-Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
-Consult the dealer or an experienced radio/TV technician for help.

* RF warning for Portable device:
The device has been evaluated to meet general RF exposure requirement. The device can be used in portable exposure condition without restriction.

The module is designed to comply with the FCC statements.

The Host system using the module, should have label indicated "Contains FCC ID: OC3BM1842".

CE Caution:

The module is designed to comply the CE statements.

The host system using the module, should have label indicated “ CE2200 ”

Description:

NVC-MDCS42 is a class 2 Bluetooth® 2.1 module. It is a highly integrated and sophisticated module which contains all the necessary elements from radio to antenna and a fully implemented protocol stack. It is an idea solution for integrating Bluetooth® into various products with limited knowledge of Bluetooth® and RF technologies.

With NovaComm's iNova® bluetooth stack firmware, designers can easily customize their applications to support different Bluetooth profiles, such as SPP, OPP, HID and etc.

And the module can also interface with Apple's Authentication Coprocessor and build an iAP over Bluetooth application. Please contact NovaComm for special firmware.

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Typical Bluetooth applications:

- Cable replacement
- Bar code and RFID scanners
- Measurement and monitoring systems
- Industrial sensors and controls
- Medical devices
- Industrial PCs and laptops

Features:

- Bluetooth V2.1 (class2)
- Onboard Meander line PCB antenna support 10 meters
- Support sniff and deep sleep mode
- Supports master and slave
- Supports Bluetooth profiles SPP, OPP, HID)
- UART and USB programming and data interfaces
- I2C Master interface
- Support Apple iAP protocol (with special firmware)
- PCM digital audio interfaces
- 8MBit onboard flash
- 25.80x13.40x2.2mm
- BQB/FCC/CE Certified
- RoHS compliant

Table 1 Ordering Information

Ordering Number	Package	Items in One Package	Comments
NVC-MDCS42	Plastic tray	84 PCS	

Please also supply the customer firmware code issued by NovaComm Technologies when you place the order.

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Pinout and Description

1.1. Pin Configuration

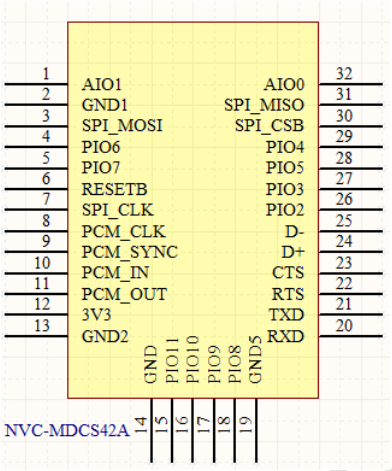

Figure 1: Pinout of NVC-MDCS42

Pin	Symbol	I/O Type	Description
1	AIO1	Bi-directional	Programmable input/output line
2	GND	Ground	Ground
3	SPI_MOSI	CMOS input, with weak internal pull-down	Serial Peripheral Interface input
4	PIO6	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
5	PIO7	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
6	RESETB	CMOS input with weak internal pull-down	Reset if low. Input denounced so must be low for >5ms to cause a reset
7	SPI_CLK	input with weak internal pull-down	Serial Peripheral Interface clock
8	PCM_CLK	Bi-directional	Synchronous Data Clock
9	PCM_SYNC	Bi-directional	Synchronous Data Sync
10	PCM_IN	CMOS Input	Synchronous Data Input
11	PCM_OUT	Bi-directional	Synchronous Data Output
12	3V3	3V3 power input	3V3 power input
13	GND	Ground	Ground
14	GND	Ground	Ground
15	PIO11	Bi-directional with programmable strength	Programmable input/output line

		internal pull-up/down	
16	PIO10	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
17	PIO9	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
18	PIO8	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
19	GND	Ground	Ground
20	UART_RX	CMOS input with weak internal pull-down	UART data input
21	UART_TX	CMOS input with weak internal pull-down	UART data output
22	UART_CTS	CMOS output, tri-state, with weak internal pull-up	UART request to send active low
23	UART_RTS	CMOS output, tri-state, with weak internal pull-up	UART request to send active low
24	USB_D+	Bi-directional	USB data plus with selectable internal 1.5Kohm pull-up resistor
25	USB_D-	Bi-directional	USB data minus
26	PIO2	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
27	PIO3	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
28	PIO5	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
29	PIO4	Bi-directional with programmable strength internal pull-up/down	Programmable input/output line
30	SPI_CSB	CMOS input with weak internal pull-up	Chip select for Synchronous Serial Interface active low
31	SPI_MISO	CMOS output, tri-state, with weak internal pull-down	Serial Peripheral Interface output
32	AIO0	Bi-directional	Programmable input/output line

Table 2 : Pin Definition

2. Electrical Characteristic

2.1. Absolute Maximum Rating

Rating	Min	Max	Unit
Storage Temperature	-40	+120	°C
Operating Temperature	-40	+85	°C
PIO/AIO Voltage	-0.4	+3.6	V
VDD Voltage	-0.4	+3.7	V
USB_DP/USB_DN Voltage	-0.4	+3.6	V
Other Terminal Voltages except RF	-0.4	VDD+0.4	V

Table 3 : Absolute Maximum Rating Recommended Operating Conditions

2.2. Recommend operation conditions

Operating Condition	Min	Typical	Max	Unit
Storage Temperature	-40	--	+85	°C
Operating Temperature Range	-20	--	+70	°C
VDD Voltage	+3	+3.3	+3.6	V

Table 4 : Recommended Operating Conditions

2.3. Power consumptions

Operating Condition	Min	Typical	Max	Unit
Radio On*(Discovery)		23		mA
Radio On*(Inquiry window time)		35		mA
Connected (Deep sleep disable, sniff enable)	1.4	3	11	mA
Connected (Deep sleep enable, sniff enable)	0.04	2.4	11	mA
Connected with data transfer	3	10	15	mA

Table 5: Power consumptions

Note :

Sniff mode ----- In Sniff mode, the duty cycle of the slave's activity in the piconet may be reduced. If a slave is in active mode on an ACL logical transport, it shall listen in every ACL slot to the master traffic, unless that link is being treated as a scatternet link or is absent due to hold mode. With sniff mode, the time slots when a slave is listening are reduced, so the master shall only transmit to a slave in specified time slots. The sniff anchor points are spaced regularly with an interval of Tsniff.

2.4. Input/output Terminal Characteristics

2.4.1. Digital Terminals

Supply Voltage Levels	Min	Typical	Max	Unit
Input Voltage Levels				
V_{IL} input logic level low	-0.4	-	+0.8	V
V_{IH} input logic level high	0.7VDD	-	VDD+0.4	V
Output Voltage Levels				
V_{OL} output logic level low, I_{OL} = 4.0mA	-	-	0.4	V
V_{OH} output logic level high, I_{OH} = -4.0mA	VDD-0.2	-	-	V
Input and Tri-state Current				
With strong pull-up	-100	-40	-10	µA
With strong pull-down	10	40	100	µA
With weak pull-up	-5	-1.0	-0.2	µA
With weak pull-down	-0.2	+1.0	5.0	µA
I/O pad leakage current	-1	0	+1	µA
C_I Input Capacitance	1.0	-	5.0	pF

Table 6 : Digital Terminal

2.4.2. USB

USB Terminals	Min	Typical	Max	Unit
Input Threshold				
V_{IL} input logic level low	-	-	0.3VDD	V
V_{IH} input logic level high	0.7VDD	-	-	V
Input Leakage Current				
GND < VIN < VDD[(a)]	-1	1	5	µA
C_I Input capacitance	2.5	-	10.0	pF
Output Voltage Levels to Correctly Terminated USB Cable				
V_{IL} output logic level low	0.0	-	0.2	V
V_{IH} output logic level high	2.8	-	VDD	V

Table 7: USB Terminal

Internal USB pull-up disable

3. Physical Interfaces

3.1. Power Supply

The module is power supply voltage 3.0V to 3.6V. The transient response of the regulator is also important. At the start of a packet, power consumption will jump to

high levels. See the average current consumption section. The regulator should have a response time of 20s or less; it is essential that the power rail recovers quickly.

3.2. Internal Antenna

The module integrates a Meander line PCB chip antenna so there's no need to use antenna on customer's PCB. Simply pay attention to leave enough clearance for the antenna.

3.3. PIO

10 PIOs are provided. They are powered from VDD_3.3V.PIO lines are software-configurable as weak pull-up, weak pull-down, strong pull-up or strong pull-down.

Note:

At reset all PIO lines are inputs with weak pull-downs.

Any of the PIO lines can be configured as interrupt request lines or as wake-up lines from sleep modes.

3.4. AIO

2 AIOs are provided. Their functions depend on software. They can be used to read or output a voltage between 0V to 1.8V. They can also be used as a digital PIO.

3.5. UART

This is a standard UART interface for communicating with other serial devices. The UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol.

The UART CTS and RTS signals can be assigned to any PIO pin by the on-chip firmware.

Table 8 Possible UART Settings

Parameter		Possible Values
Baud Rate	Minimum	1200 baud (≤2%Error)
		9600 baud (≤1%Error)
	Maximum	2M baud (≤1%Error)
Flow Control		RTS/CTS or None
Parity		None, Odd or Even
Number of Stop Bits		1 or 2
Bits per Byte		8

3.6. I2C Master

PIO5, PIO7 and PIO6 can be used to form a master I^2C interface. The interface is formed using software to drive these lines. It is suited only to relatively slow functions such as driving a LCD, Keyboard, scanner or EEPROM. In the case, PIO lines need to be pulled up through 2.2Kohm resistors.

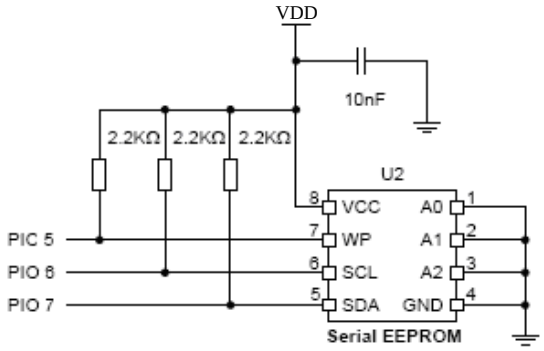

Figure 2 : Example EEPROM Connection with I^2C Interface

3.7. SPI interface

The synchronous serial port interface (SPI) is for interfacing with other digital devices. The SPI port can be used for system debugging. It can also be used for programming the Flash memory. SPI interface is connected using the MOSI, MISO, CSB and CLK pins.

3.8. PCM interface

The module has offered PCM digital audio interface.

PCM is a standard method used to digitize audio (particularly voice) for transmission over digital communication channels. Through its PCM interface, the module has hardware support for continual transmission and reception of PCM data, thus reducing processor overhead for applications. The module offers a bi-directional digital audio interface that routes directly into the baseband layer of the on-chip firmware. It does not pass through the HCI protocol layer.

Hardware on the module allows the data to be sent to and received from a SCO connection. Up to three SCO connections can be supported by the PCM interface at any one time.

The module can operate as the PCM interface master generating an output clock of 128, 256 or 512kHz. When configured as PCM interface slave, it can operate with an input clock up to 2048kHz. The module is compatible with a variety of clock formats, including Long Frame Sync, Short Frame Sync and GCI timing environments.

It supports 13-bit or 16-bit linear, 8-bit µ-law or A-law companied sample formats at 8k samples/s and can receive and transmit on any selection of three of the first four slots following PCM_SYNC.

The module interfaces directly to PCM audio devices including the following:

- Qualcomm MSM 3000 series and MSM 5000 series CDMA baseband devices
- OKI MSM7705 four channels A-law and µ-law CODEC
- Motorola MC145481 8-bit A-law and µ-law CODEC
- Motorola MC145483 13-bit linear CODEC
- STW 5093 and 5094 14-bit linear CODECs

The module is also compatible with the Motorola SSI™ interface.

3.8.1. PCM Interface Master/Slave

When PCM is configured as a master, the module generates PCM_CLK and PCM_SYNC.

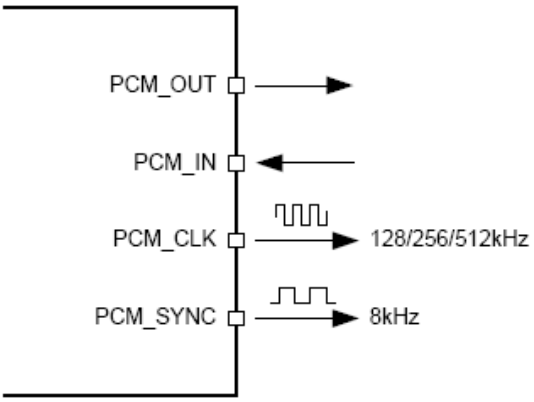

Figure 3: Configured PCM as a Master

When PCM is configured as the slave, the module accepts PCM_CLK rates up to 2048kHz.

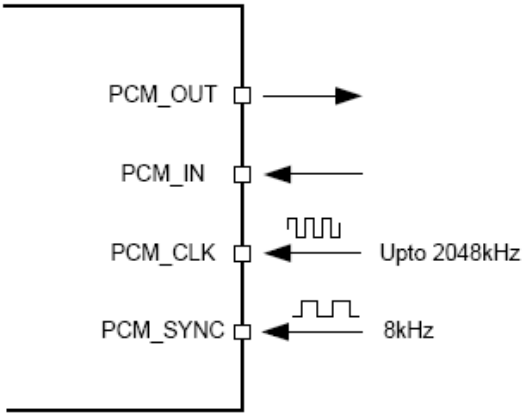

Figure 4: Configured PCM as a Slave

3.8.2. Long Frame Sync

Long Frame Sync is the name given to a clocking format that controls the transfer of PCM data words or samples. In Long Frame Sync, the rising edge of PCM_SYNC indicates the start of the PCM word. When the module is configured as PCM master, generating PCM_SYNC and PCM_CLK, then PCM_SYNC is 8-bits long. When the module is configured as PCM Slave, PCM_SYNC may be from two consecutive falling edges of PCM_CLK to half the PCM_SYNC rate, i.e., 62.5µs long.

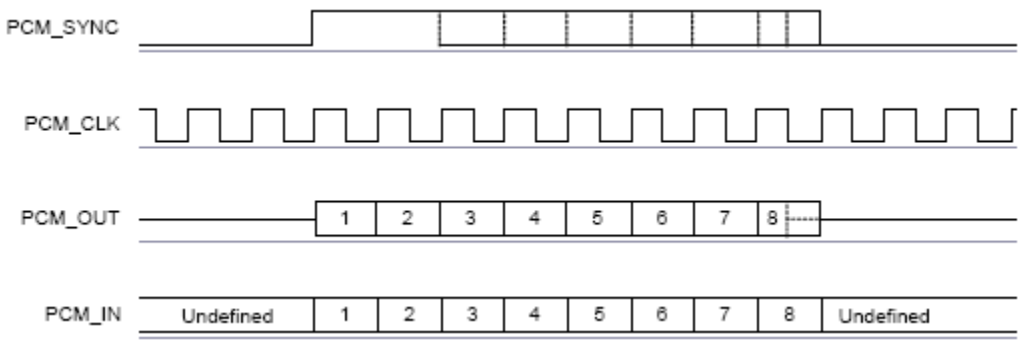

Figure 5: Long Frame Sync (Shown with 8-bit Companded Sample)

3.8.3. Short Frame Sync

In Short Frame Sync, the falling edge of PCM_SYNC indicates the start of the PCM word. PCM_SYNC is always one clock cycle long.

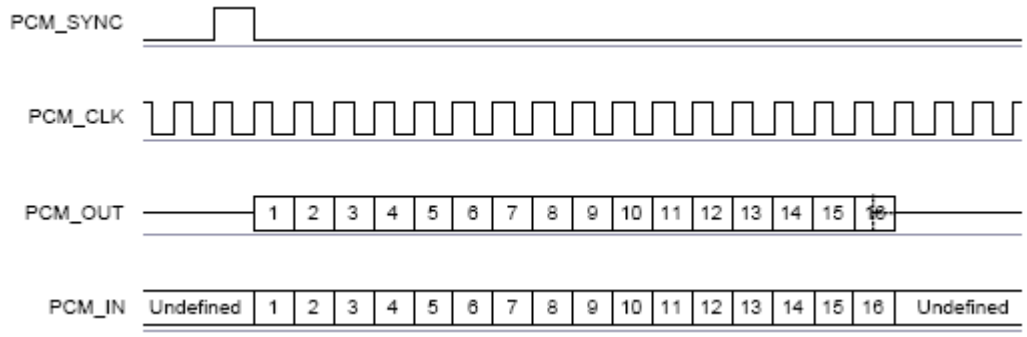

Figure 6: Short Frame Sync (Shown with 16-bit Sample)

As with Long Frame Sync, the module samples PCM_IN on the falling edge of PCM_CLK and transmits PCM_OUT on the rising edge. PCM_OUT may be configured to be high impedance on the falling edge of PCM_CLK in the LSB position or on the rising edge.

3.8.4. Multi-slot Operation

More than one SCO connection over the PCM interface is supported using multiple slots. Up to three SCO connections can be carried over any of the first four slots.

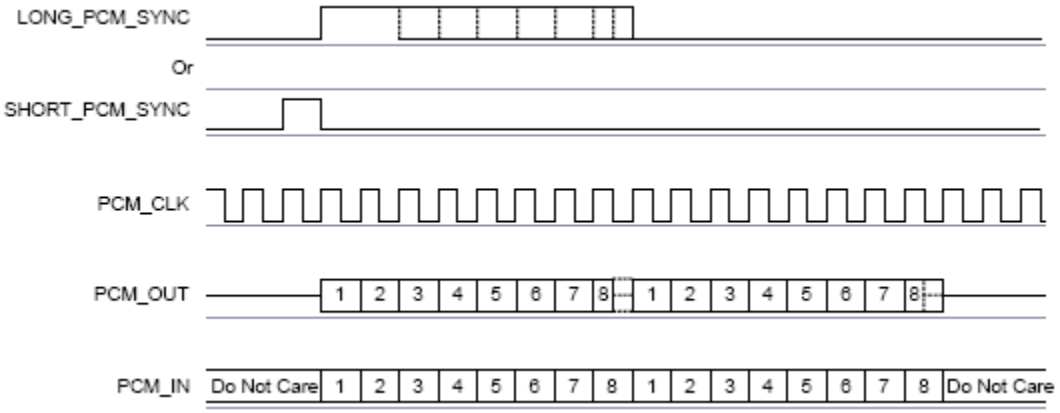

Figure 7: Multi-Slot Operation with Two Slots and 8-bit Companded Samples

3.8.5. GCI Interface

The module is compatible with the General Circuit Interface (GCI), a standard synchronous 2B+D ISDN timing interface. The two 64Kbps B channels can be accessed when this mode is configured.

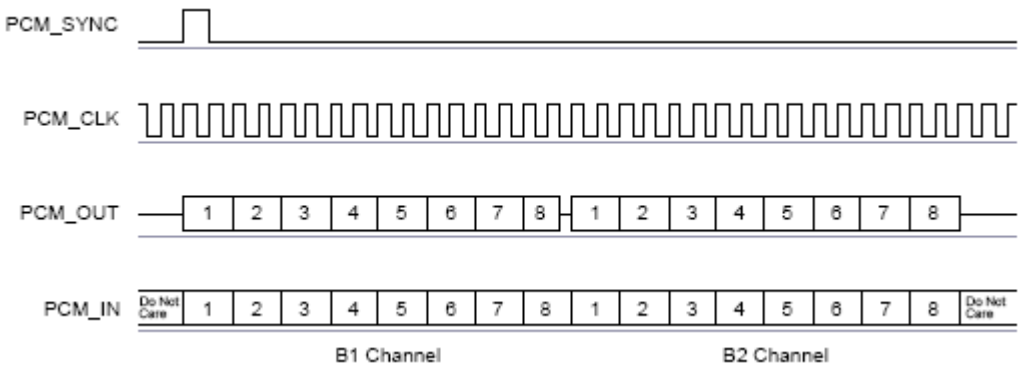

Figure 8: GCI Interface

The start of a frame is indicated by the rising edge of PCM_SYNC and runs at 8kHz. With the module in slave mode, the frequency of PCM_CLK can be up to 4.096MHz.

3.8.6. Slots and Sample Formats

The module can receive and transmit on any selection of the first four slots following each sync pulse. Slot durations can be either 8 or 16 clock cycles. Durations of 8 clock cycles may only be used with 8-bit sample formats. Durations of 16 clocks may be used with 8-bit, 13-bit or 16-bit sample formats. The module supports 13-bit linear, 16-bit linear and 8-bit μ-law or A-law sample formats. The sample rate is 8k samples/s. The bit order may be little or big endian. When 16-bit slots are used, the 3 or 8 unused bits in each slot may be filled with sign extension, padded with zeros or a programmable 3-bit audio attenuation compatible with some Motorola CODECs.

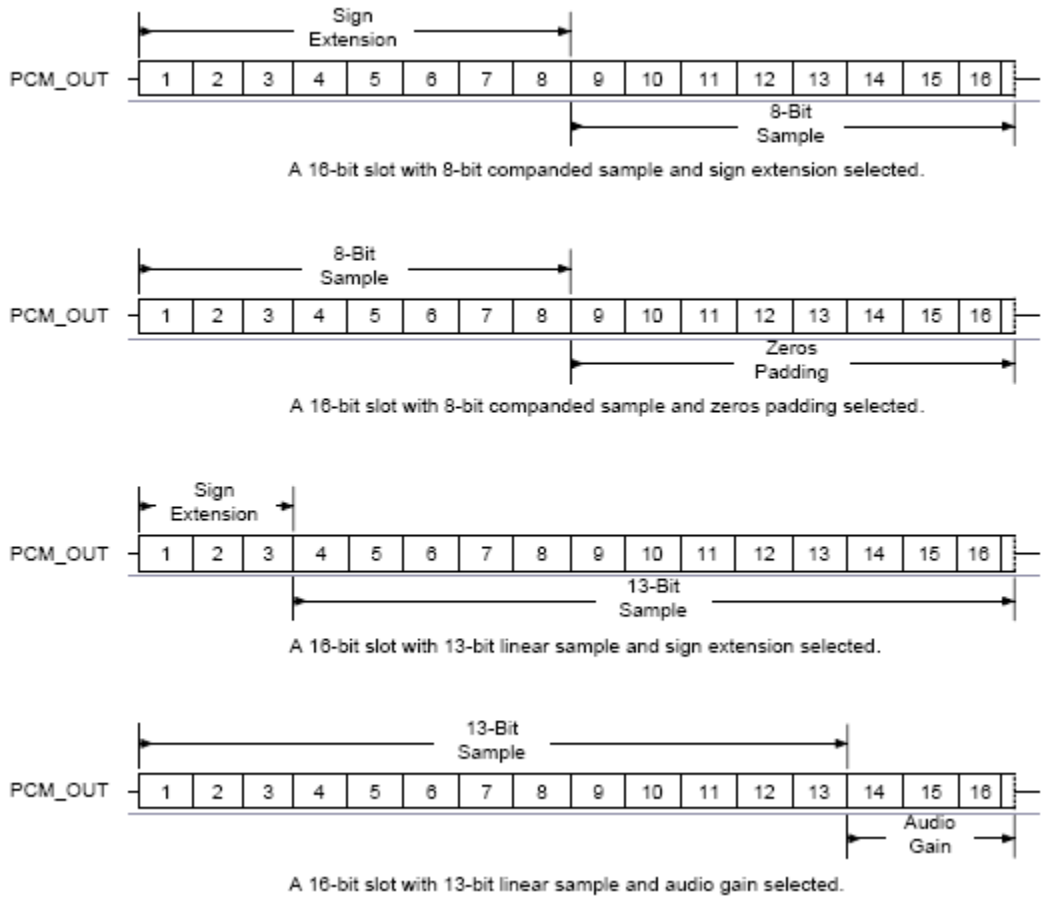

Figure 9: 16-Bit Slot Length and Sample Formats

3.8.7. Additional Features

The module has a mute facility that forces PCM_OUT to be 0. In master mode, PCM_SYNC may also be forced to 0 while keeping PCM_CLK running which some CODECS use to control power down.

3.8.8. PCM Timing Information

Symbol	Parameter		Min	Typical	Max	Unit
fmclk	PCL_CLK Frequency	4MHz DDS generation. Selection of frequency is programmable.	-	128	-	kHz
				256		
				512		

		48MHz DDS generation. Selection of frequency is programmable.	2.9		-	kHz
-	PCM_SYNC frequency		-	8		kHz
tmclkh[(a)]	PCM_CLK high	4MHz DDS generation	980	-	-	ns
tmclkl[(a)]	PCM_CLK low	4MHz DDS generation	730	-		ns
-	PCM_CLK jitter	48MHz DDS generation			21	ns pk-pk
tdmclksynch	Delay time from PCM_CLK high to PCM_SYNC high		-	-	20	ns
tdmclkpout	Delay time from PCM_CLK high to valid PCM_OUT		-	-	20	ns
tdmclklsyncl	Delay time from PCM_CLK low to PCM_SYNC low (Long Frame Sync only)		-	-	20	ns
tdmclkhsyncl	Delay time from PCM_CLK high to PCM_SYNC low		-	-	20	ns
tdmclklpoutz	Delay time from PCM_CLK low to PCM_OUT high impedance		-	-	20	ns
tdmclkhpoutz	Delay time from PCM_CLK high to PCM_OUT high impedance		-	-	20	ns
tsupinclkl	Set-up time for PCM_IN valid to PCM_CLK low		30	-	-	ns
thpinclkl	Hold time for PCM_CLK low to PCM_IN invalid		10	-	-	ns

Table 9: PCM Master Timing

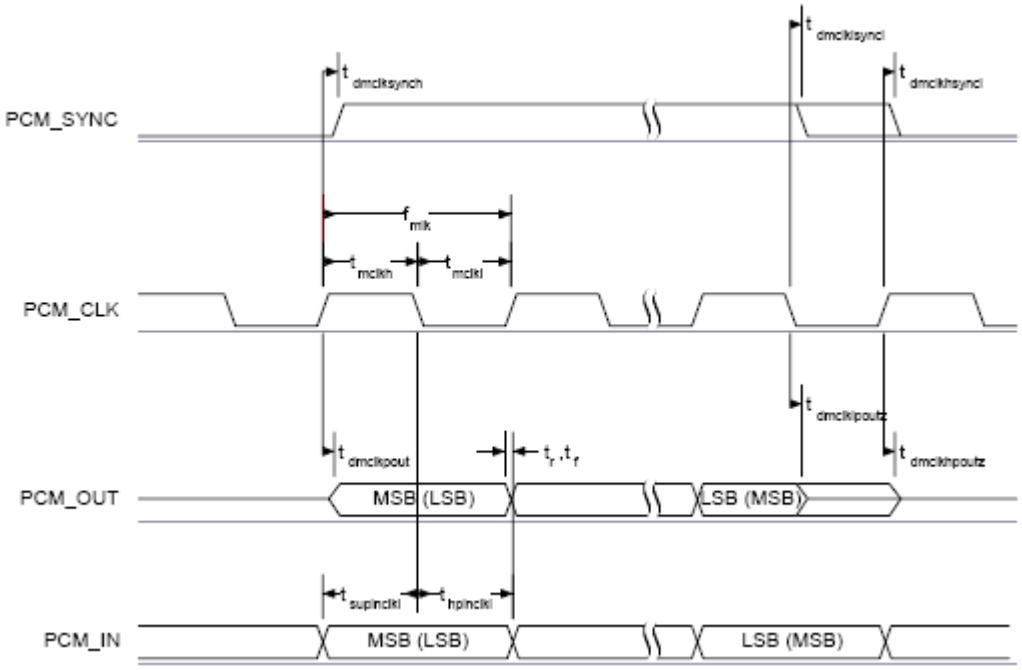

Figure 10: PCM Master Timing Long Frame Sync

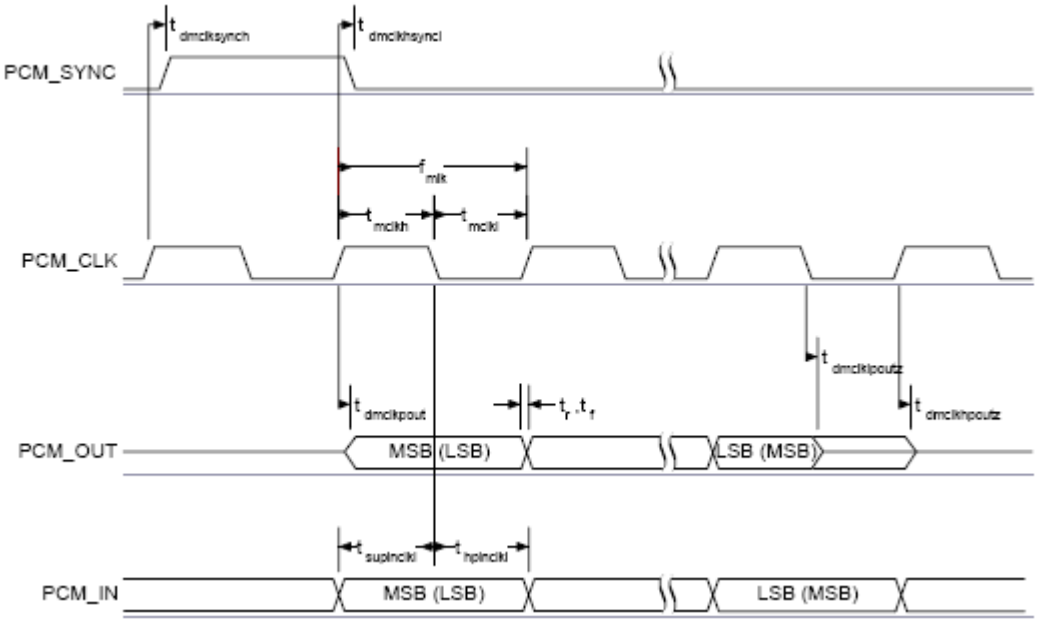

Figure 11: PCM Master Timing Short Frame Sync

Symbol	Parameter	Min	Typical	Max	Unit
fsclk	PCM clock frequency (Slave mode: input)	64	-	2048	kHz

fsclk	PCM clock frequency (GCI mode)	128	-	4096	kHz
tsclkl	PCM_CLK low time	200	-	-	ns
tsclkh	PCM_CLK high time	200	-	-	ns
thsclksynch	Hold time from PCM_CLK low to PCM_SYNC high	30	-	-	ns
tsusclksynch	Set-up time for PCM_SYNC high to PCM_CLK low	30	-	-	ns
tdpout	Delay time from PCM_SYNC or PCM_CLK whichever is later, to valid PCM_OUT data (Long Frame Sync only)	-	-	20	ns
tdsclkhpout	Delay time from CLK high to PCM_OUT valid data	-	-	20	ns
tdpoutz	Delay time from PCM_SYNC or PCM_CLK low, whichever is later, to PCM_OUT data line high impedance	-	-	20	ns
tsupinsclkl	Set-up time for PCM_IN valid to CLK low	30	-	-	ns
thpinsclkl	Hold time for PCM_CLK low to PCM_IN invalid	30	-	-	ns

Table 10: PCM Slave Timing

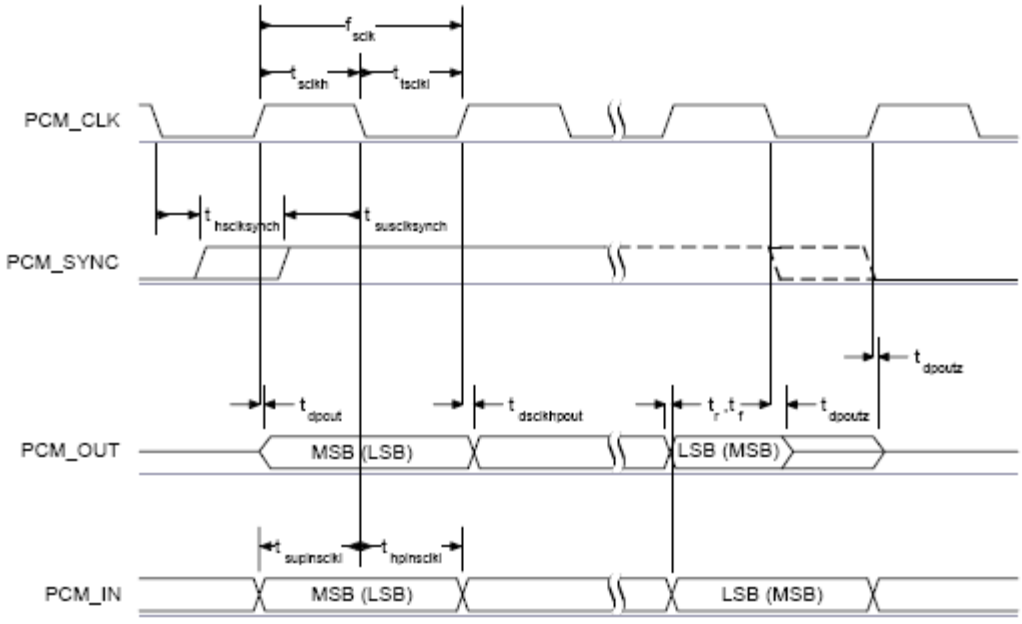

Figure 12: PCM Slave Timing Long Frame Sync

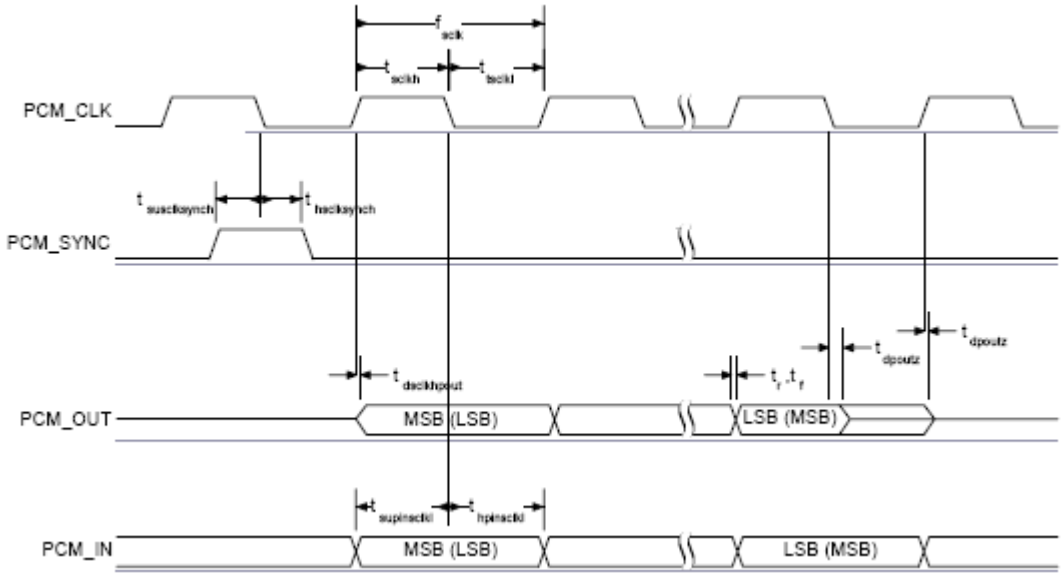

Figure 13: PCM Master Timing Short Frame Sync

3.9. USB

There is a full speed (12M bits/s) USB interface for communicating with other compatible digital devices. The module acts as a USB peripheral, responding to request from a master host controller, such as a PC.

The module features an internal USB pull-up resistor. This pulls the USB_DP pin weakly high when module is ready to enumerate. It signals to the USB master that it is a full speed (12Mbit/s) USB device. The USB internal pull-up is implemented as a current source, and is compliant with section 7.1.5 of the USB specification v1.2. The internal pull-up pulls USB_DP high to at least 2.8V when loaded with a 15kΩ ±5% pull-down resistor (in the hub/host) when VDD =3.1V. This presents a Thevenin resistance to the host of at least 900Ω. Alternatively, an external 1.5kΩ pull-up resistor can be placed between a PIO line and DP on the USB cable.

3.9.1Self-Powered Mode

In self-powered mode, the module is powered from its own power supply and not from the VBUS (5V) line of the USB cable. It draws only a small leakage current (below 0.5mA) from VBUS on the USB cable. This is the easier mode for which to design, as the design is not limited by the power that can be drawn from the USB hub or root port. However, it requires that VBUS be connected to module via a resistor network (Rvb1 and Rvb2), so the module can detect when VBUS is powered up. The module will not pull USB_DP high when VBUS is off.

Self-powered USB designs (powered from a battery or LDO) must ensure that a PIO line is allocated for USB pull-up purposes. A 1.5KΩ 5% pull-up resistor between USB_DP and the selected PIO line should be fitted to the design. Failure to fit this resistor may result in the design failing to be USB compliant in self-powered mode. The

internal pull-up in the module is only suitable for bus-powered USB devices, e.g., dongles.

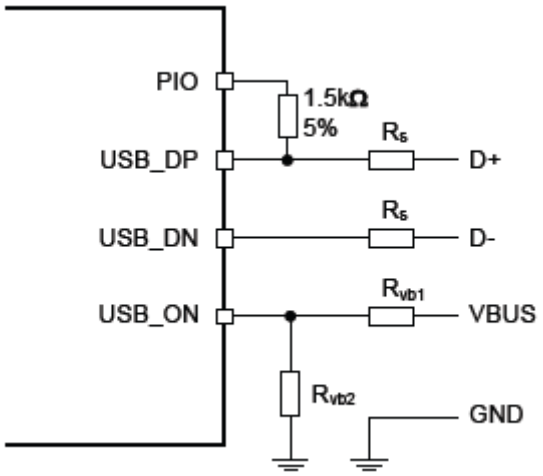

Figure 14: USB Connections for Self-Powered Mode

Note:

USB_ON is shared with the module PIO terminals.

Identifier	Value	Function
R_s	27Ω Nominal	Impedance matching to USB cable
Rvb1	22kΩ 5%	VBUS ON sense divider
Rvb2	47kΩ 5%	VBUS ON sense divider

Table 11: USB Interface Component Values

3.9.2 Bus-Powered Mode

In bus-powered mode, the application circuit draws its current from the 5V VBUS supply on the USB cable. The module negotiates with the PC during the USB enumeration stage about how much current it is allowed to consume. For Class 2 Bluetooth applications, NVC recommends that the regulator used to derive 3.3V from VBUS is rated at 100mA average current and should be able to handle peaks of 120mA without foldback or limiting. In bus-powered mode, the module requests 100mA during enumeration. For Class 1 Bluetooth applications, the USB power descriptor should be altered to reflect the amount of power required. This is higher than for a Class 2 application due to the extra current drawn by the Transmit RF PA. When selecting a regulator, be aware that VBUS may go as low as 4.4V. The inrush current (when charging reservoir and supply decoupling capacitors) is limited by the USB specification. See USB Specification v1.1, section 7.2.4.1. Some applications may require soft start circuitry to limit inrush current if more than 10µF is present between VBUS and GND.

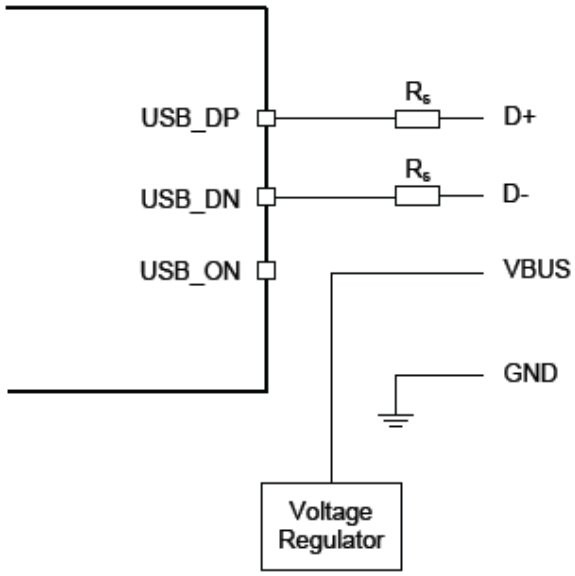

Figure 15: USB Connections for Bus-Powered Mode

4. Software Stacks

NVC-MDCS42 is Bluetooth 2.1 module, the embedded iNova Bluetooth Stack firmware supports the SPP, SDP, OPP, FAX, HID Profile, and supports up to seven devices simultaneously connected.

Furthermore, the Apple iAP (iPod Accessory Protocol) which is used to connect with iOS devices has also been implemented and included in iNova Bluetooth Stack firmware.

Contact with the sales agent for support for more profiles and applications with iNova Bluetooth stack firmware.

4.1. iNova Stack

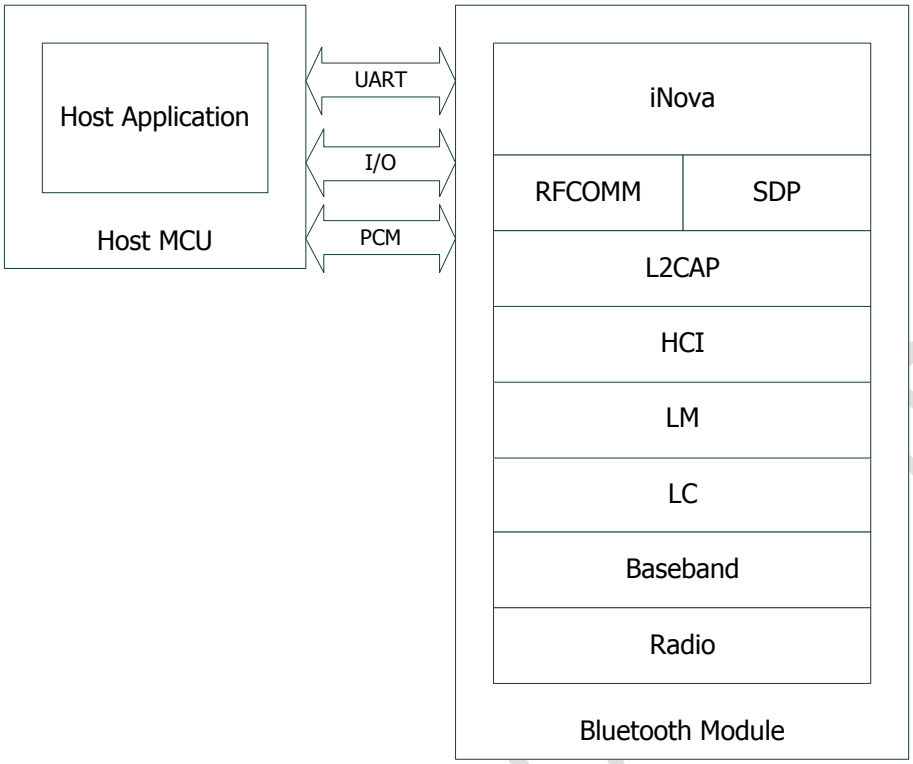

Figure 16 iNova Stack

The iNova Bluetooth Stack is illustrated as Figure 16 above. The host microcontroller interfaces to iNova Bluetooth Stack firmware through one or more of the physical interfaces, which are also shown in the Figure 16. The most common interfacing is done through the UART interface using the NCCI (NovaComm Control Interface) supported by the iNova firmware. With the NCCI, the user can access Bluetooth functionality without paying any attention to complexity, which lies in the Bluetooth protocol stack.

The user may write application code to run on the host microcontroller to control iNova firmware by using NCCI and to develop their own Bluetooth applications.

Notes:

For detailed information about NCCI, please refer to the document named *NovaComm Control Interface User Guide.*

4.2. iNova Bluetooth Stack with iAP

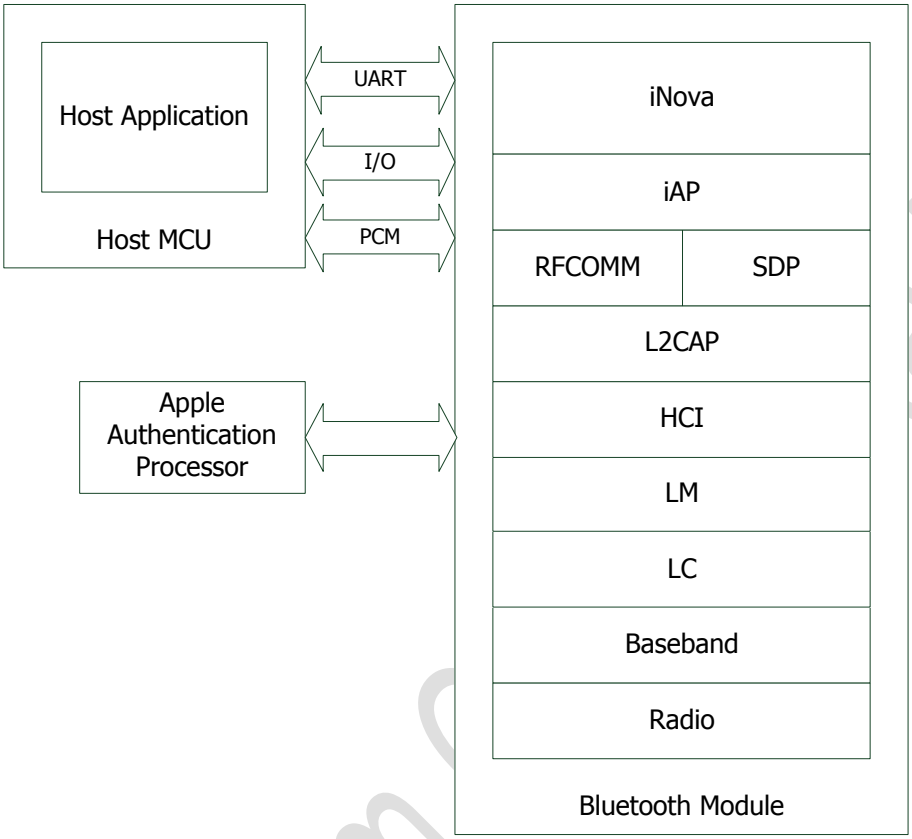

Figure 17 iNova Bluetooth Stack with iAP

The iNova Bluetooth Stack with iAP is illustrated as

Figure 17 above. For the host microcontroller and its application, there is almost no difference with common requirement. No need to develop iAP in the host application since the authentication process and iAP have been implemented in iNova Bluetooth firmware stack completely. What the developer needs to do is just connecting the Apple authentication processor with NovaComm's Bluetooth Module simply following reference design provided by NovaComm.Notes:

To develop accessories for iOS devices or products to connect to iOS devices, the developers must register and be approved by Apple's Made for iPod (MFi) program. Licensed developers gain access to technical documentation, hardware components, technical support and certification logos.

To get more detailed information, you can visit Apple's developer portal at:

http://developer.apple.com/ipod/

5. Reference Design

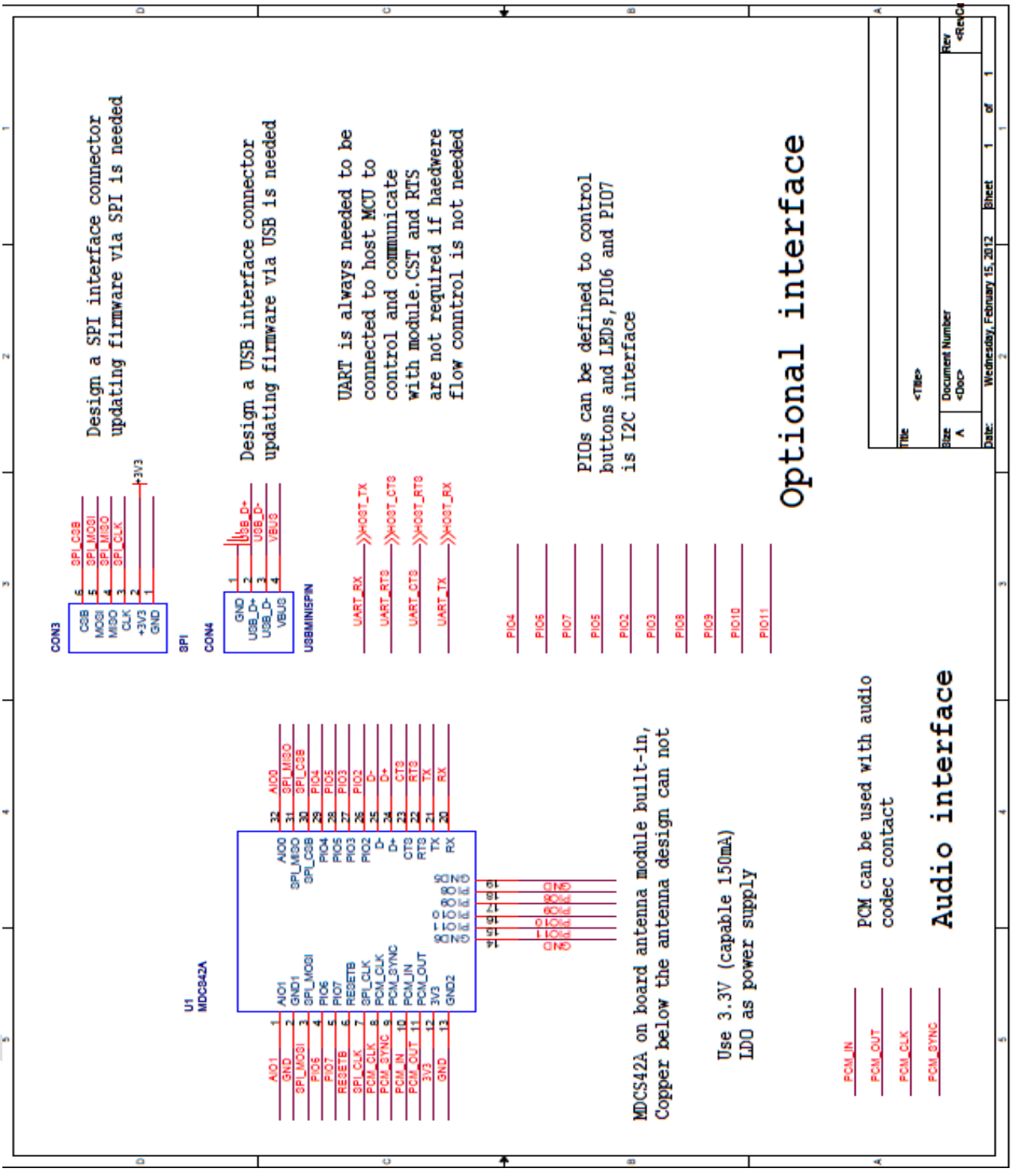

Figure 18 : Reference Design

6. Layout and Soldering Considerations

6.1. Soldering Recommendations

NVC-MDCS42 is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Novacomm Technologies will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

- Refer to technical documentations of particular solder paste for profile configurations
- Avoid using more than one flow.
- Reliability of the solder joint and self-alignment of the component are dependent on the solder volume. Minimum of 150 m stencil thickness is recommended.
- Aperture size of the stencil should be 1:1 with the pad size.
- A low residue, “no clean” solder paste should be used due to low mounted height of the component.

6.2. Layout Guidelines

Strongly recommended that the display module designed in accordance with the antenna copper in the following figure 1.2.4 , the preferred antenna design 1， does not recommend the use of antenna design 3 . For the protection module RF distance in the copper when the size of the design in accordance with the following figure , Place the GND vias as close to the GND pins as possible. Use good layout practices in order to avoid any excessive noise coupled to the signal line or power supply voltage line .

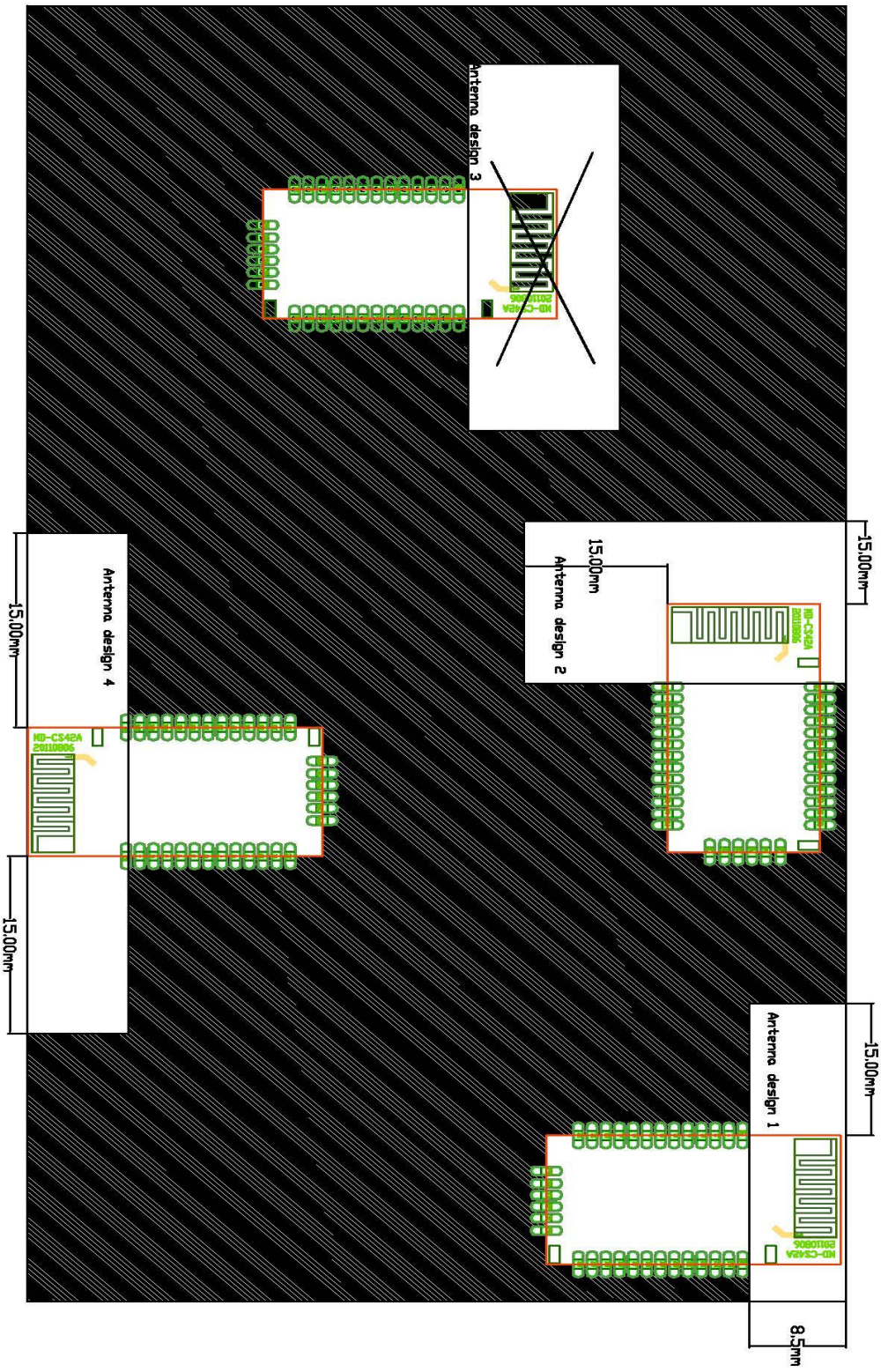

Figure 19 : Placement of the Module on a Main Board

7. Physical Dimensions

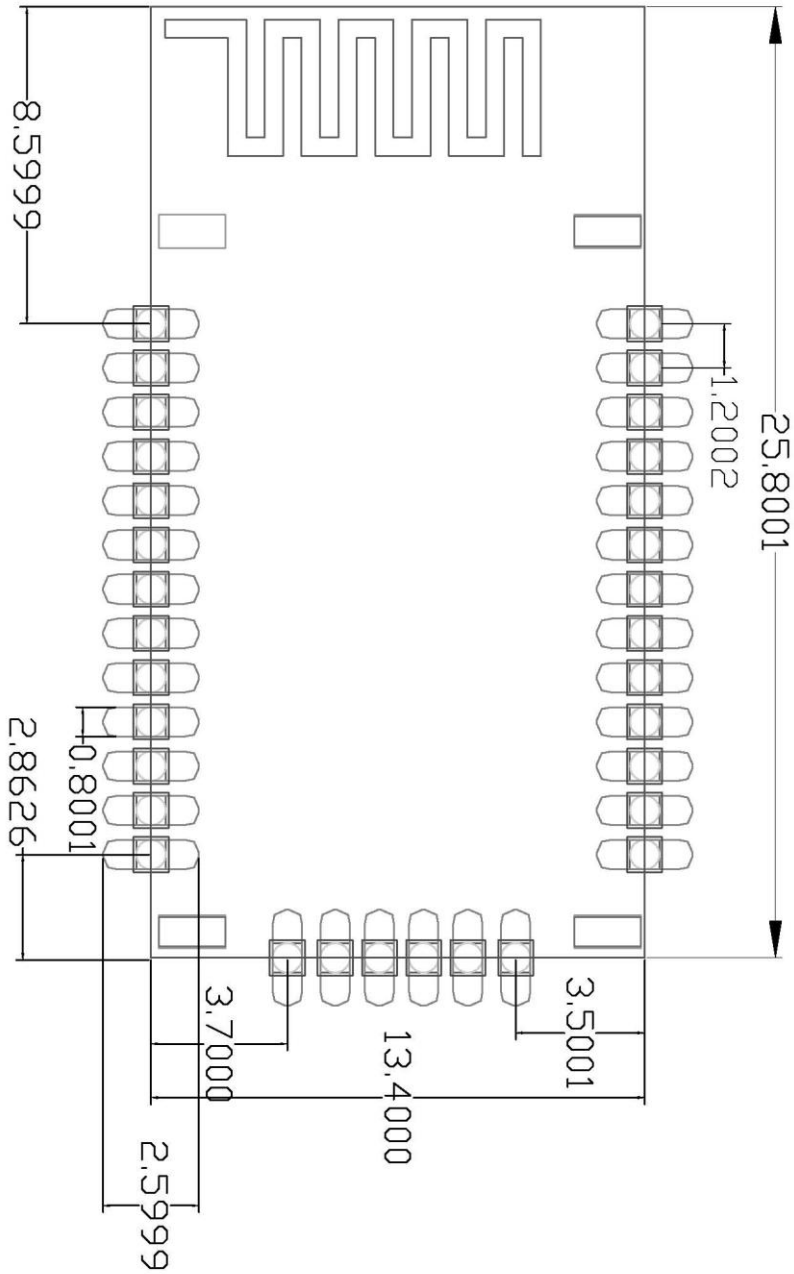

Figure 20 :Physical Dimensions and Recommended Footprint (Unit: mm, Deviation:0.02mm)

8. Package

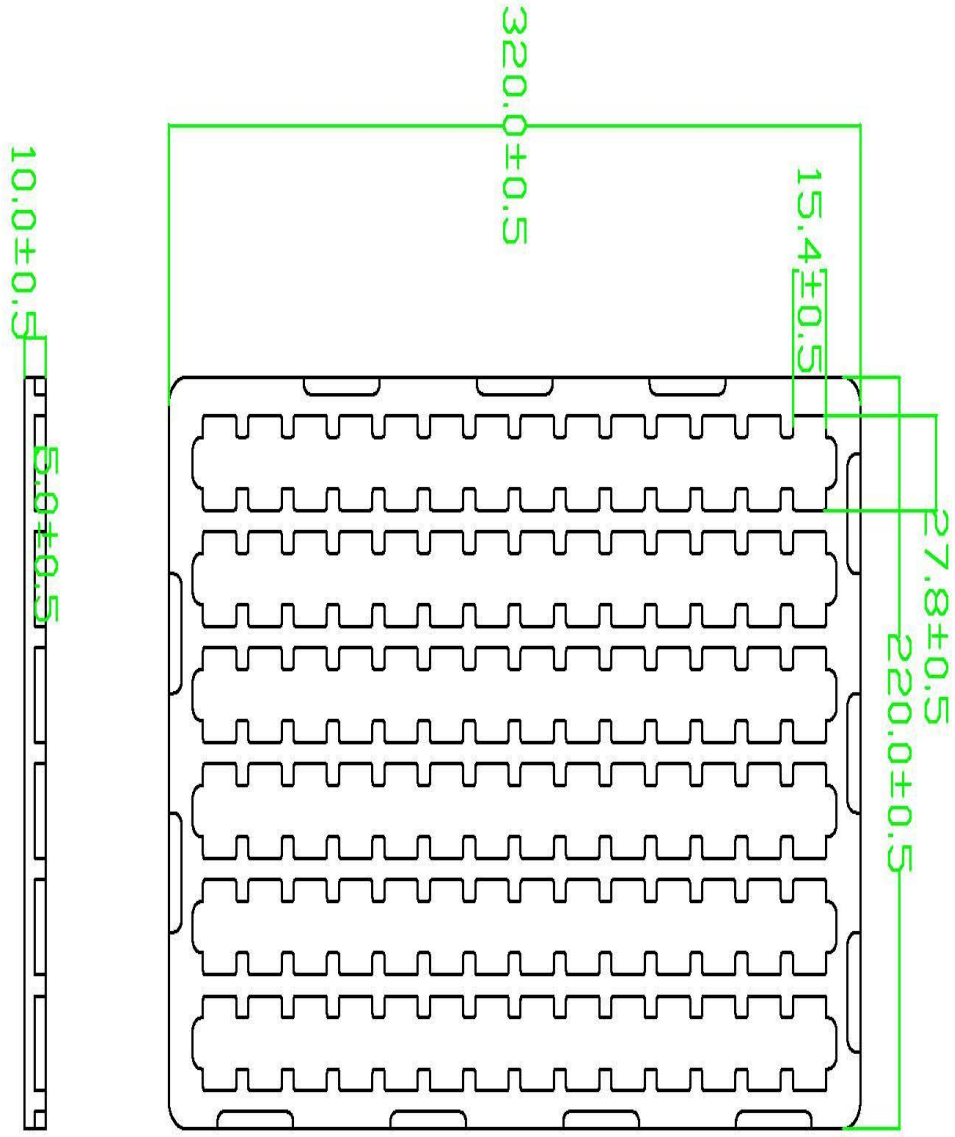

Figure 21: NVC-MDCS42 Package

Plastic tray, plus aluminum bags do vacuum packing. Items in One Package number of 84PCS

9. Contact Information

Sales: sales@novacomm.cn

Technical support: support@novacomm.cn

Orders: orders@novacomm.cn

Phone: +86 21 60453799

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Street address: 902A, #560 Shengxia Rd., ZJ Inno Park, Shanghai 201203, China