

Active Seal Circuit description:

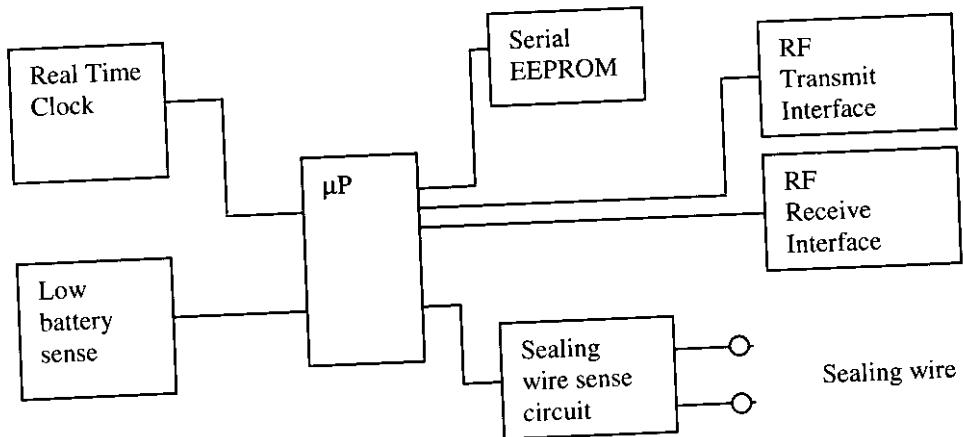
1. Reference documents: Circuit Diagram #31U10010 REV-B

2. Functional description:

The seal is generally in sleep mode and wakes up periodically (~2S period) to test the sealing wire. If the sealing wire is OK, the seal goes back to sleep. If the sealing wire is tampered (Resistance changed or open) an event is logged in the seal memory. When interrogation cycle begins the seal wakes up and communicate with reader. The data transmitted, has a 250KHz carrier which is modulated with 2KHz data, the modulation is pulsed RF.

3. Circuit description:

Block diagram:



The  $\mu$ P (U1) is RISC PIC16C622 and it controls the seal system. Its clock frequency is 2MHz. Real Time Clock (U2) has 32768Hz clock and communicate with the  $\mu$ P via a serial 2 wire communication with ~50KHz clock.

Serial EEPROM: (U5) 8Kbit EEPROM which contains the seal data and all sealing events. It communicates the  $\mu$ P via an I<sup>2</sup>C protocol with ~50KHz clock.

**Transmit RF Interface:** Q2,Q3 are drivers to the antenna (ferrite rod type), the modulated data goes out from the  $\mu$ P to the drivers. R18 is for transmission current limit. C12&C13 together with L1 are the resonance circuit for transmit and receive.

**Receive circuit:** The received data on the antenna L1, goes to the detection diodes D1,D2 and to the comparator (U4) which compares the received data to a reference produced by R13,R14. The comparator output is the received digital data which goes to the  $\mu$ P.

**Sealing wire measurement circuit:** The sealing wire resistance is measured by a one slope A/D. The measuring circuitry contains R9, R10, R11, R12, C8, and a comparator, which is in the  $\mu$ P.

The sealing wire is connected to the sockets S1,S2.

The seal power is a lithium 3.6V battery (BT1).

Q1 is not populated.

JS1 is used to enter the  $\mu$ P to a special programming mode in the production line.

JS1 is used to enter the  $\mu$ P to a special programming mode in the production line.

**Figure 1**  
**Hi-G-Seal schematic diagram**

