DataSeal circuit description

1. General

1.1. Reference documents
  1.1.1. CPU module schematics (Digital board circuit diagram), document 47S10010
  1.1.2. RF module schematics (RF board circuit diagram), document 47S10030
1.2. Pages number referenced in the following description, are referred to the schematics.

2. General Description

2.1. The DataSeal is used to seal assets during storage or shipment. If the seal wire is opened or tampered, the seal records an event and reports to the interrogator (DataReader).

2.2. The DataSeal is a stand-alone unit. It is battery operated, it has RF receiver and transmitter and microprocessor (P), which controls the DataSeal operation.

2.3. The DataSeal has two RF channels, high frequency (HF) and low frequency (LF). The HF is 916.5MHz carrier with FSK modulated data by 40KHz deviation. The LF is 125KHz carrier with OOK modulated data.

3. Functional Description

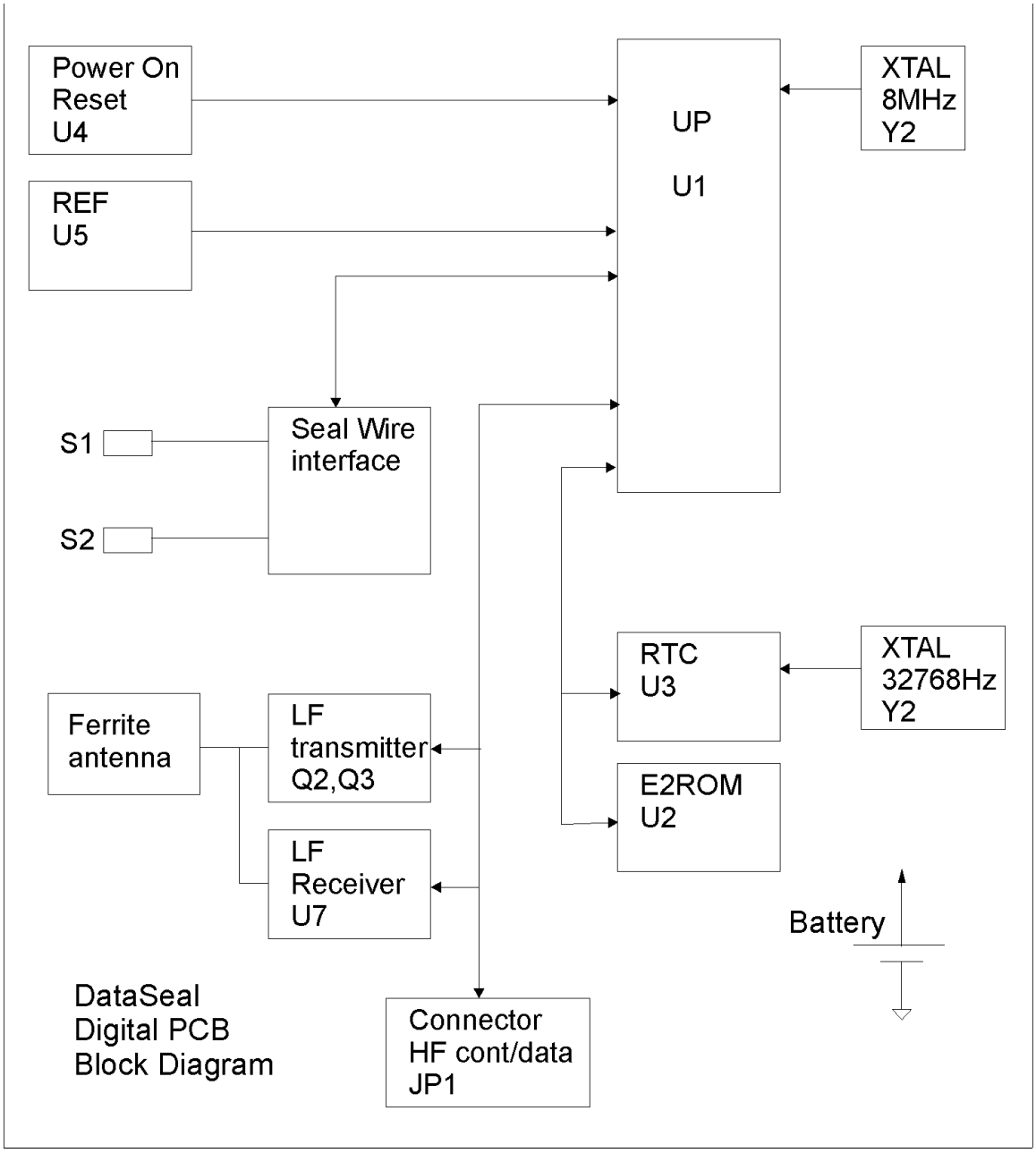
3.1. The DataSeal opens its HF receiver once every 3 seconds to look for an interrogator. If an interrogator is not found, the DataSeal goes to sleep for another 3 s. If an interrogator is found, the DataSeal receives the command and transmits a message according to the command received. During the DataSeal wake up, it performs seal wire test and integrity test of its stored data. The LF receiver is always opened for data.

4. Hardware Description

4.1. There are 3 PCBs in the DataSeal unit. Digital PCB, RF PCB and antenna PCB. The digital PCB includes the battery, P, real time clock (RTC), E2ROM and LF transceiver. The RF PCB includes the HF transceiver. The antenna PCB is located on RF PCB.

5. Digital PCB circuit description.

5.1. Block Diagram



5.2. **P** (U1 Pg.2): PIC16F876 P timed by an 8MHz ceramic resonator.

5.3. **POR** (U4 Pg.2): Power on and low voltage reset.

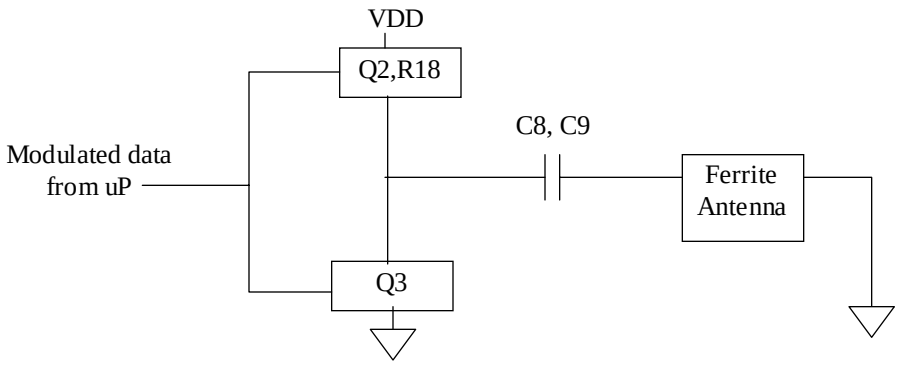
5.4. **REF** (U5 Pg.2): P A/D reference.

5.5. **Seal wire Interface** (Q1 Pg.2): A small current flows to the seal wire via R12, R13. If the seal wire opens, an interrupt is generated in U1(26). The P measures seal wire resistance by opening Q1 and measuring voltage in U1(5). D1 is surge protector.

5.6. **RTC** (U3 Pg.2): Real time clock IC with 32768Hz crystal used as calendar IC. It is serially connected to the P.

5.7. **E2ROM** (U2 Pg.2): Serial E2ROM stores unit parameters and data.

5.8. **LF Transmitter** (Q2, Q3 Pg.3): OOK modulated data comes from the P to the driver transistors Q2,Q3 which drives a ferrite antenna, connected between pads ANT1 and GND1.



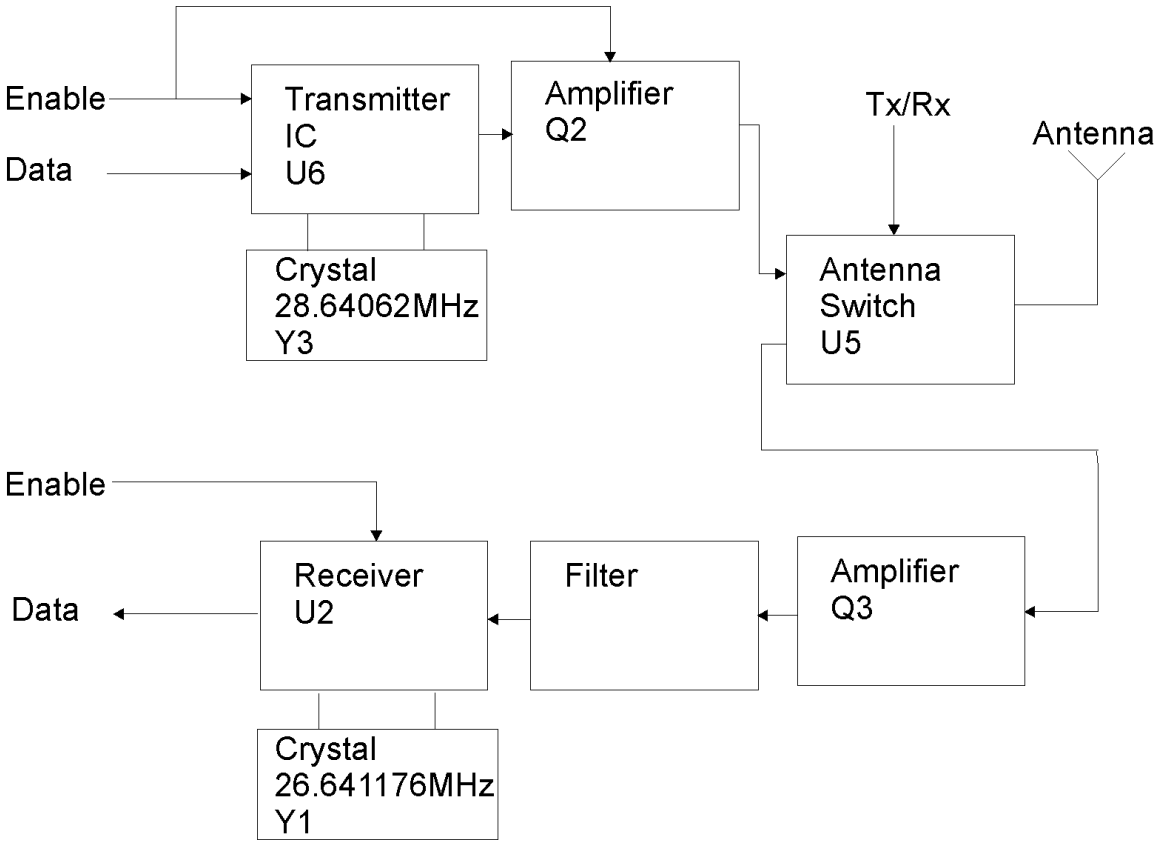
5.9. **LF Receiver** (R19 to U7 Pg.3): Data received in the ferrite antenna, is chopped by D5, then clamped by D2, D4 and Q4. Data then rectified by D3 and demodulated by U7.

5.10. **HF Board connector** (JP1 Pg.1): Power, data and control signals go to the HF board through JP1.

5.11. **Battery** (BT1 Pg.2): 3.6V Lithium battery, TL4935 by TADIRAN.

6. RF PCB circuit description

6.1. Block Diagram



6.2. **Transmitter** (U6 Pg.2): U6 is integrated transmitter; it has a 26.64062MHz with PLL to generate 916.5MHz. Data is FSK modulated with 40KHz deviation. Data rate is 15625bps. A modulated carrier goes out at U6(12).

6.3. **Amplifier** (Q2 Pg.2): The transmitted RF is filtered by C49, L14, amplified by Q2, and filtered again by C43, L2, C44.

6.4. **Antenna Switch** (U5 Pg.2): U5 switches the antenna between transmitter and receiver. It is controlled by the P.

6.5. **Amplifier** (Q3 Pg.2): Q3 functions as LNA for the receiving channel; it is optional and not populated in this circuit.

6.6. **Filter** (U1 Pg.2): HF SAW filter.

6.7. **Receiver** (U2 Pg. 2): U2 is integrated receiver; it has 26.641176MHz crystal. IF is filtered by U3, a ceramic 10.7MHz filter. Data is demodulated by Y2, goes out at U2(23,24) and shaped by comparator U4. The receiver is controlled by the P.

6.8. **Antenna** (Pads A1, A2 Pg.2): Antenna is internal and is connected to pads A1, A2 of PCB.