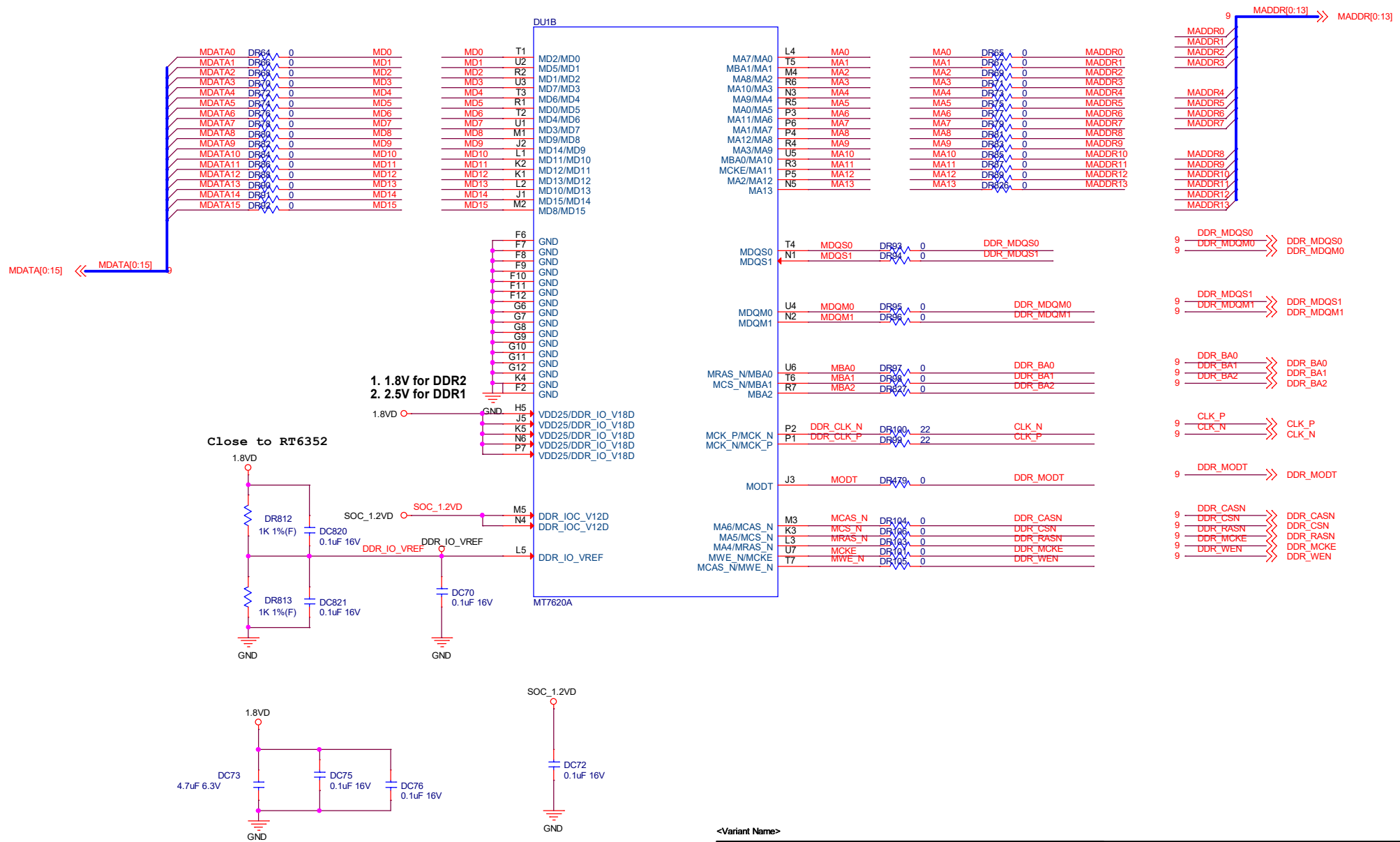
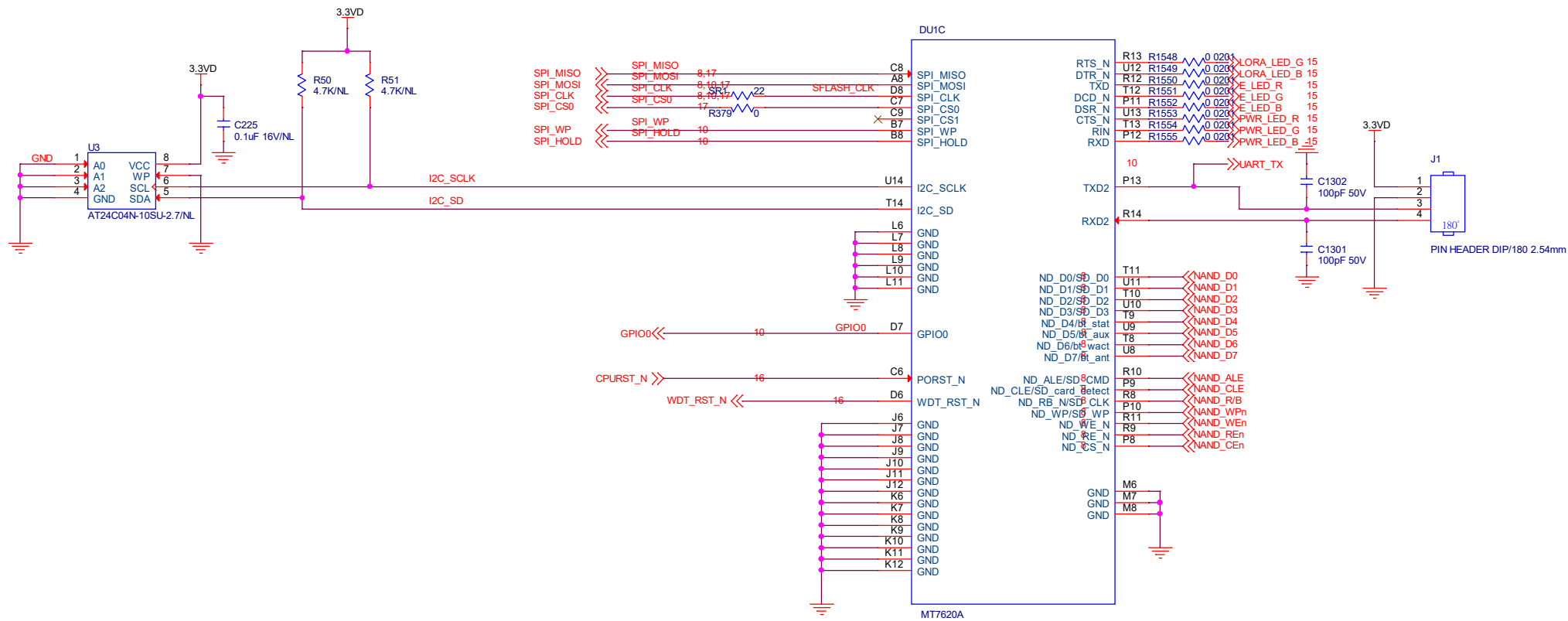


$Z = 50 \text{ ohm}$

<b>&lt;Variant Name&gt;</b>		<b>&lt;OrgName&gt;</b>		<b>Title</b>	
		<b>&lt;OrgAddr1&gt;</b>		<b>02.MT7620A RF Front End-A</b>	
<b>&lt;OrgAddr2&gt;</b>					
Date	Tuesday, February 26, 2019	Size	B	Rev	V03
Sheet	2	of	18	DWG NO	
					<b>&lt;Doc&gt;</b>

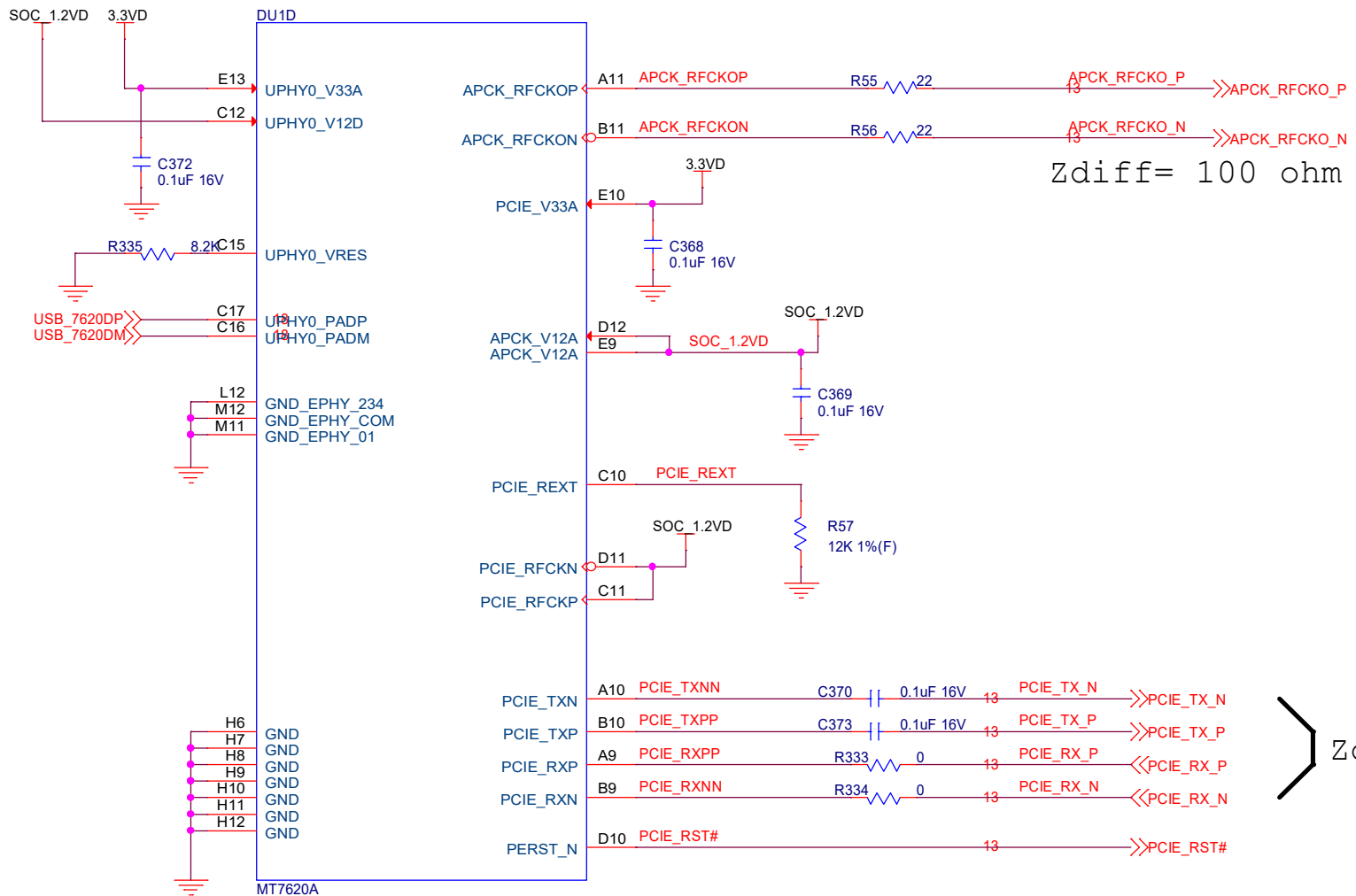


<Variant Name>		<OrgName>		Title	
		<OrgAddr1> <OrgAddr2>		<b>03.MT7620A DDR I/F-C</b>	
Date	Tuesday, February 26, 2019	Size	B	Rev	V03
Sheet	3	of	18	DWG NO	
					<Doc>



<Variant Name>

<b>&lt;OrgName&gt;</b> <OrgAddr1> <OrgAddr2>		Title <b>04.MT7620A Peripheral-C</b>	
Date	Tuesday, February 26, 2019	Size	Custom
Rev	V03	Sheet	4 of 18
			DWG NO <Doc>



Zdiff= 100 ohm +/-10%

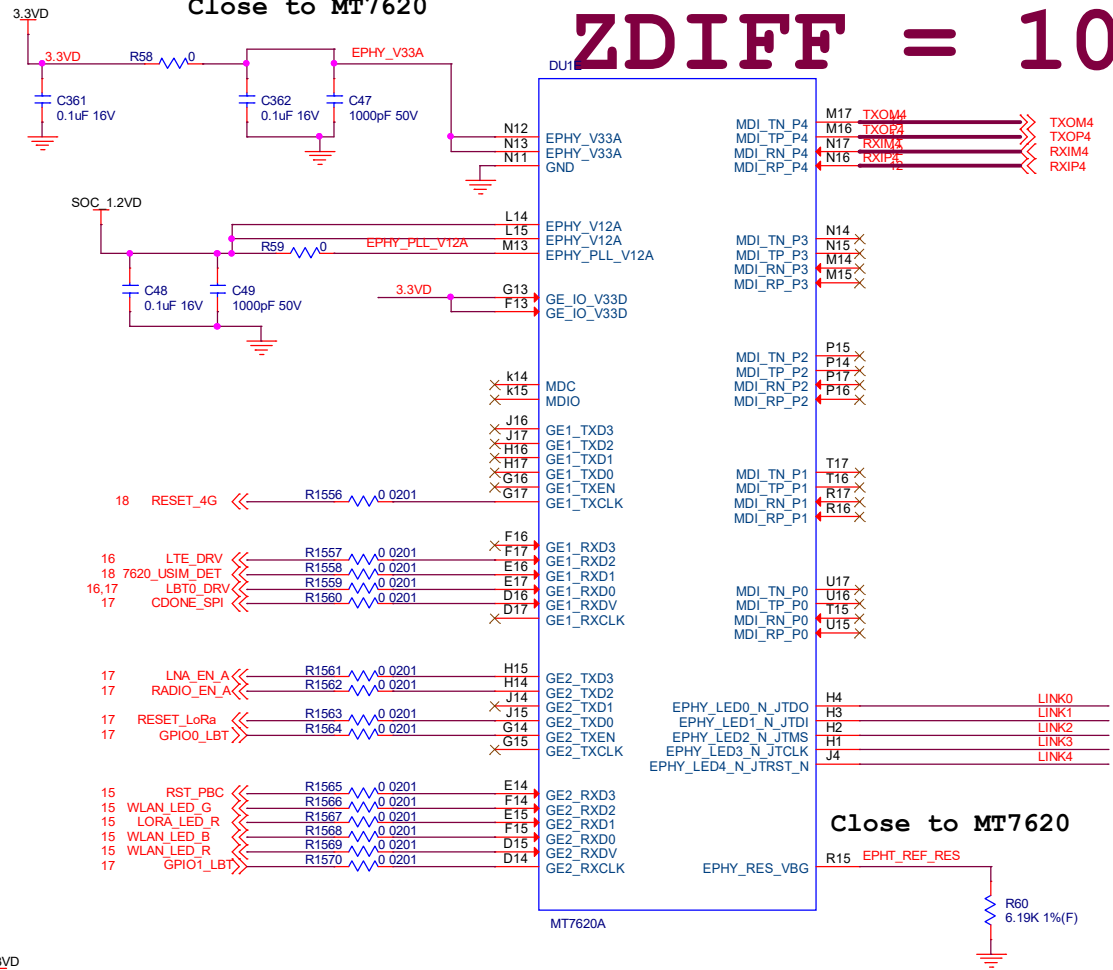
Zdiff= 100 ohm +/-10%

<Variant Name>

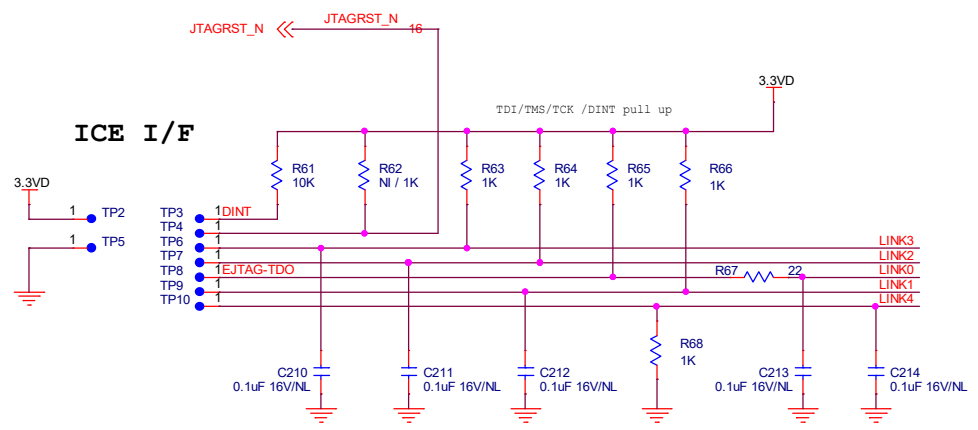
<OrgName> <OrgAddr1> <OrgAddr2>				Title <b>05.MT7620A USB-D</b>					
Date	Tuesday, February 26, 2019	Size	Custom	Rev	V03	Sheet	5 of 18	DWG NO	<Doc>

# ZDIFF = 100 ohm

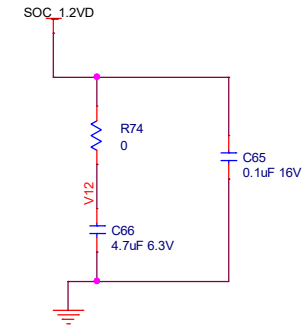
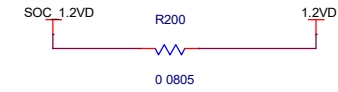
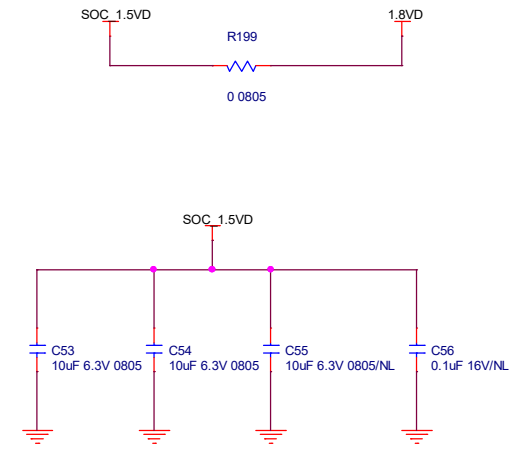
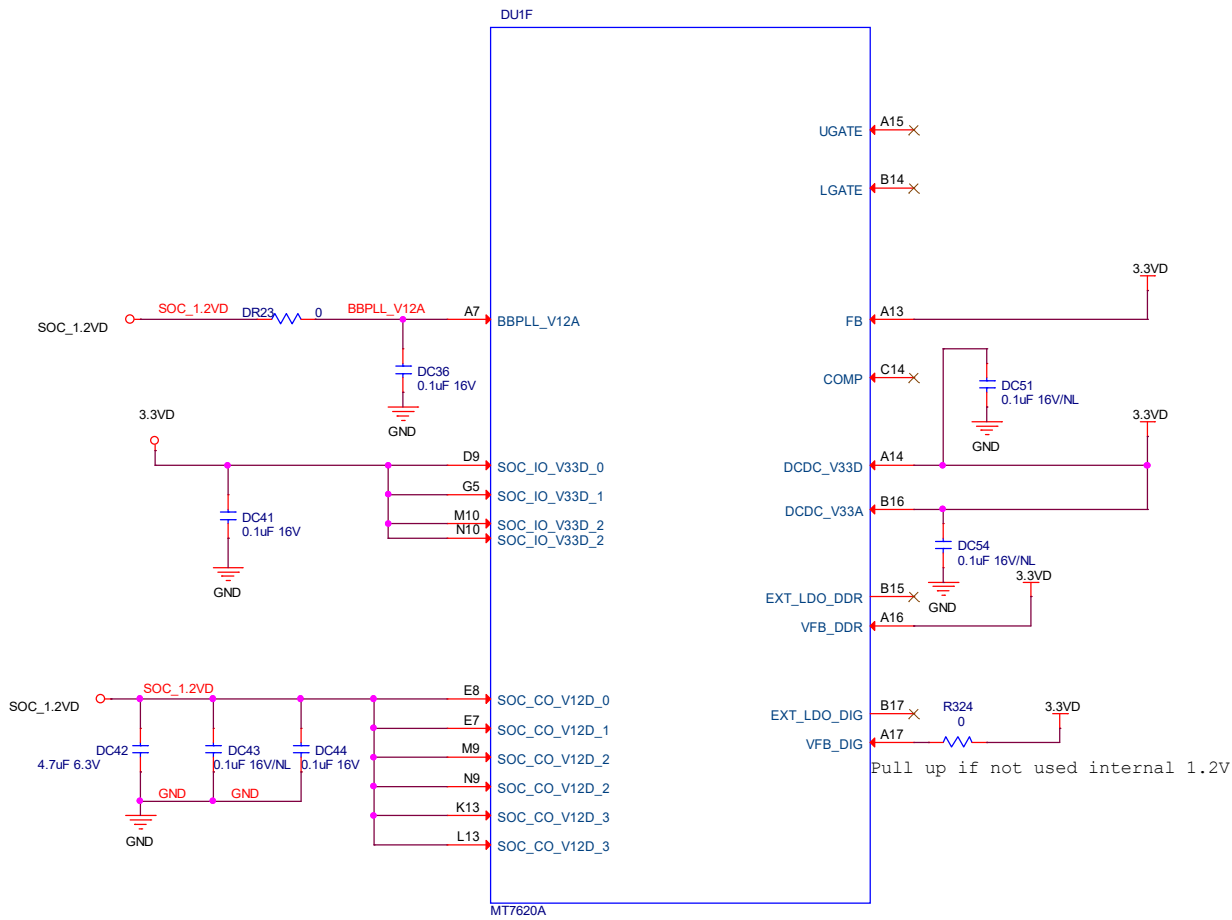
## Close to MT7620



## ICE I/F



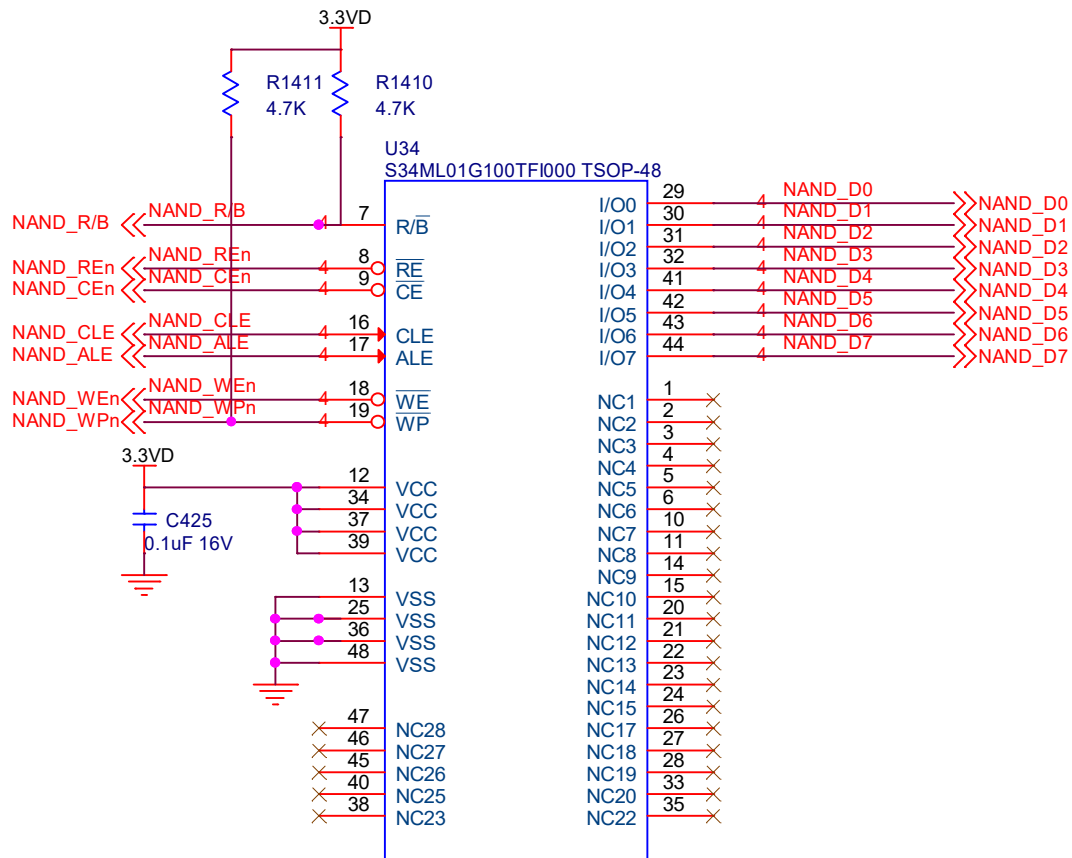
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		<b>&lt;OrgAddr1&gt;</b>		<b>06.MT7620A Ethernet-E</b>	
<b>Date</b>		<b>Size</b>		<b>Rev</b>	
Tuesday, February 26, 2019		B		V03	
<b>Sheet</b>		<b>of</b>		<b>DWG NO</b>	
6		18		DWG NO	
<b>&lt;Doc&gt;</b>					



Pull up if not used internal 1.2V

<Variant Name>

<OrgName> <OrgAddr1> <OrgAddr2>			Title <b>07.MT7620A Power-F</b>		
Date	Tuesday, February 26, 2019	Size	B	Rev	V03
Sheet	7	of	18	DWG NO	
					<Doc>

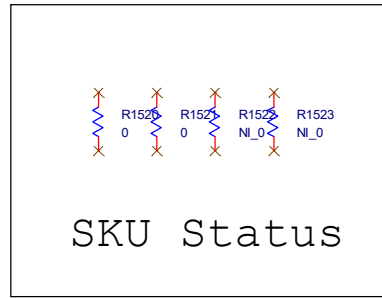
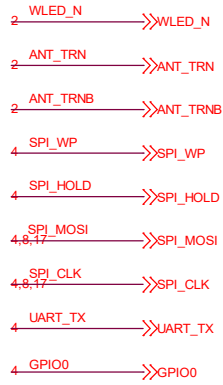


<Variant Name>

<b>&lt;OrgName&gt;</b> <OrgAddr1> <OrgAddr2>				Title <b>08.NAND-Flash</b>					
Date	Tuesday, February 26, 2019	Size	A	Rev	V03	Sheet	8 of 18	DWG NO	<Doc>

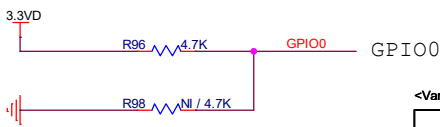
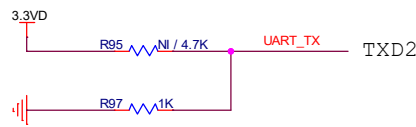
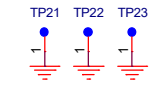
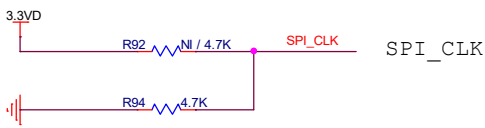
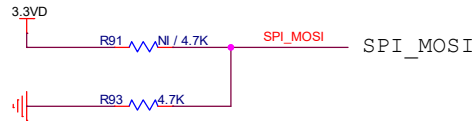
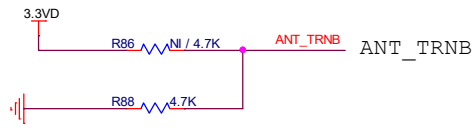
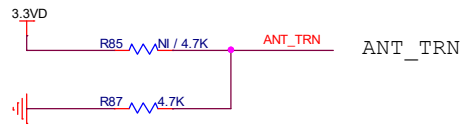
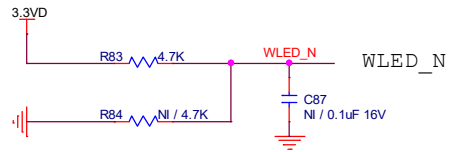






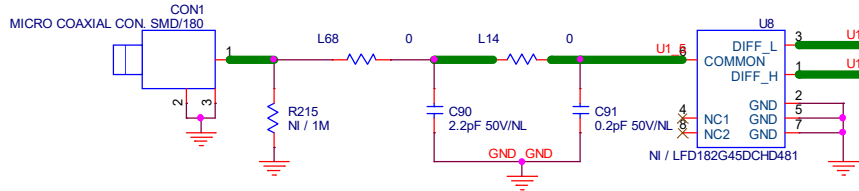
### MT7620 Boot Up Strapping

Pin Name	Description	Value
WLED_N	DRAM_FROM_EE For non scan mode:	0: DRAM configuration from EEPROM 1: DRAM configuration from Auto Detect
ANT_TRN	DBG_JTAG_MODE	0: EPHY_LED 1: JTAG MODE
ANT_TRNB	XTAL_FREQ_SEL	0: 20MHz
{SPI_WP, SPI_HOLD}	DRAM_TYPE	01: DDR1 (CPU/3) TSOP 10: DDR2 (CPU/3) FBGA 11: DDR1 (CPU/3) FBGA
{SPI_MOSI, SPI_CLK, TXD2, GPIO0 }	CHIP_MODE[3:0]	A vector to set chip function/test/debug modes. In non-test/debug operation,  0001: Normal mode (boot from ROM+NAND flash 4 cycle address) 0010: Normal mode (boot from SPI 3Byte Addr) 0011: Normal mode (boot from SPI 4Byte Addr) 0100 :iNIC RGMII mode(boot from ROM) 0101: iNIC MII mode(boot from ROM) 0110: iNIC RVMII mode(boot from ROM) 0111: iNIC PHY mode(boot from ROM) 1000: iNIC USB mode(boot from ROM) 1001: iNIC PCIe mode(boot from ROM)



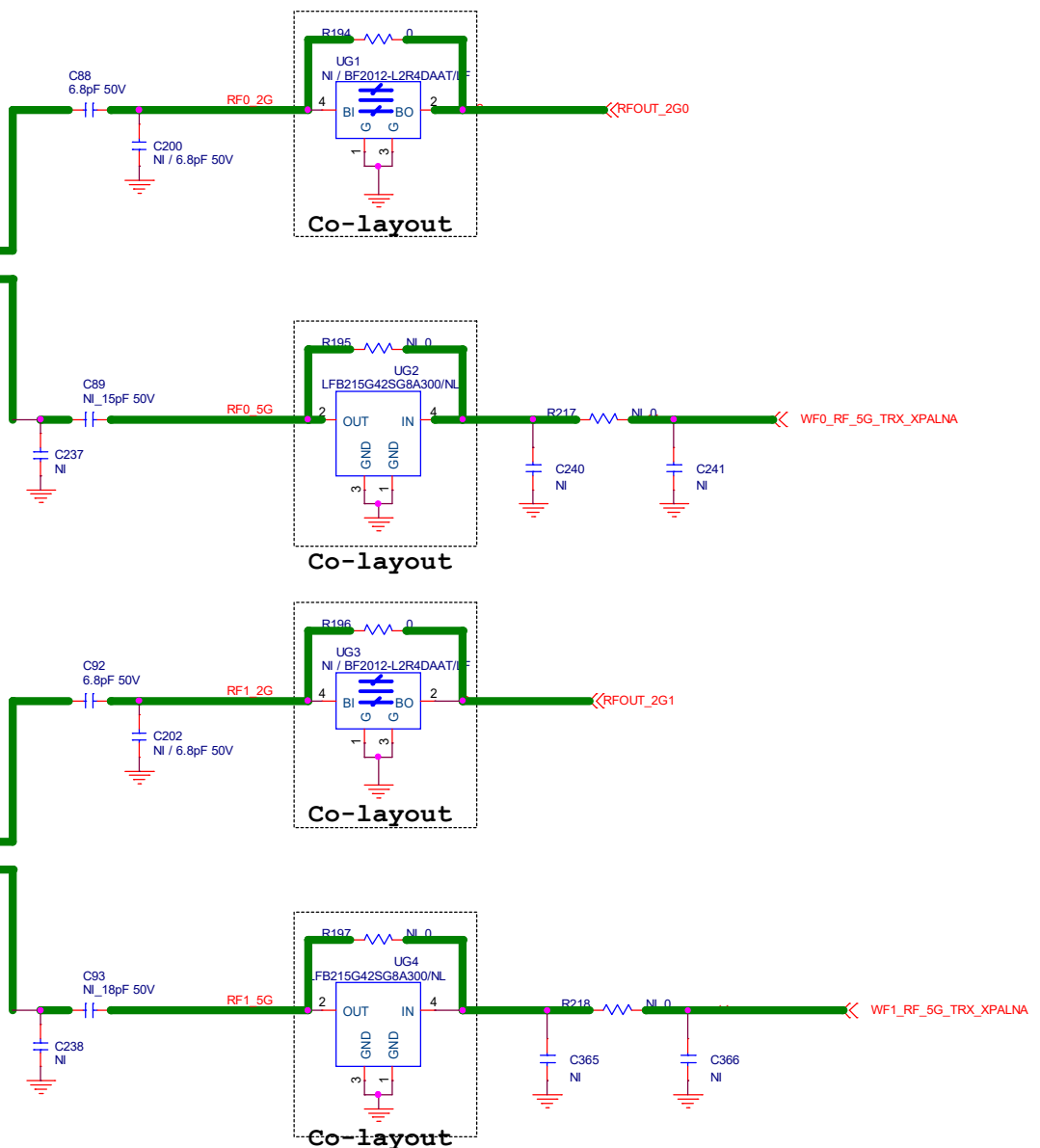
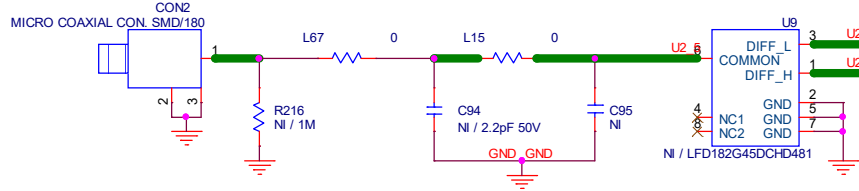
<Variant Name>		<b>&lt;OrgName&gt;</b>		Title	
		<OrgAddr1> <OrgAddr2>		<b>10.Config</b>	
Date	Tuesday, February 26, 2019	Size	B	Rev	V03
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					<b>&lt;Doc&gt;</b>

ANTENNA 0



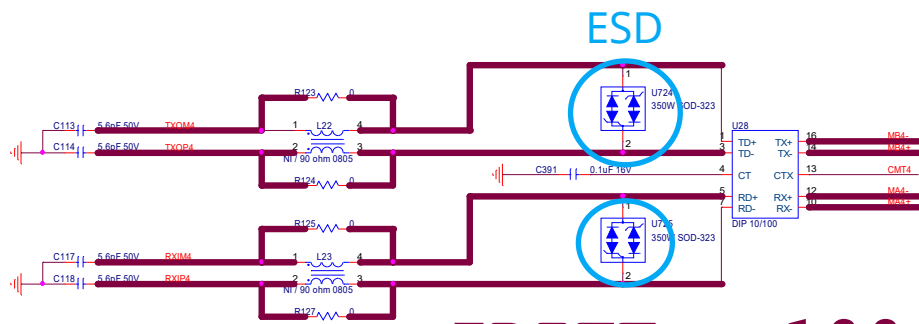
$Z = 50 \text{ ohm}$

ANTENNA 1



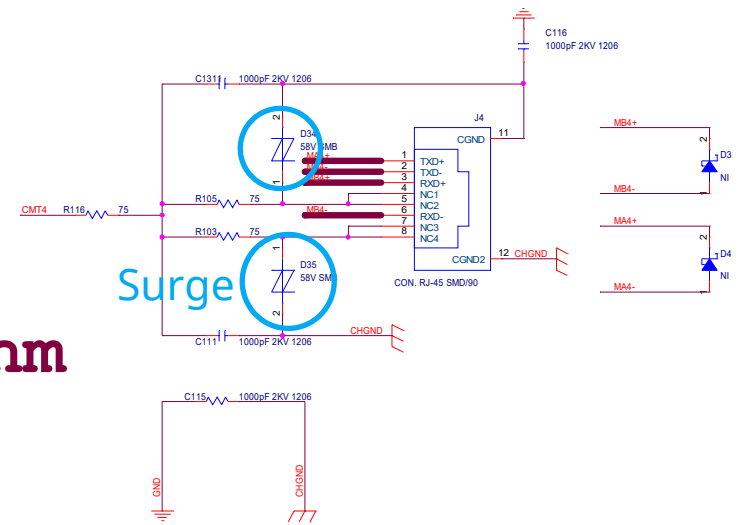
<Variant Name>		<OrgName>		Title	
		<OrgAddr1> <OrgAddr2>		<b>11.RF trace</b>	
Date	Tuesday, February 26, 2019	Size	B	Rev	V03
Sheet	11 of 18	Rev	V03	Sheet	11 of 18
					DWG NO
					<Doc>

Zdiff= 100 ohm +/-10%



**ZDIFF = 100 ohm**

Ethernet WAN

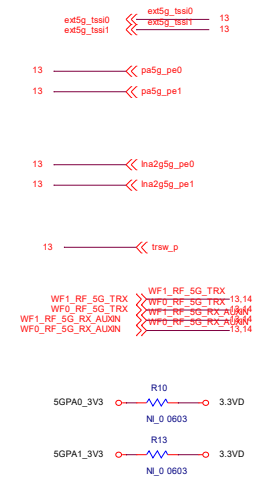
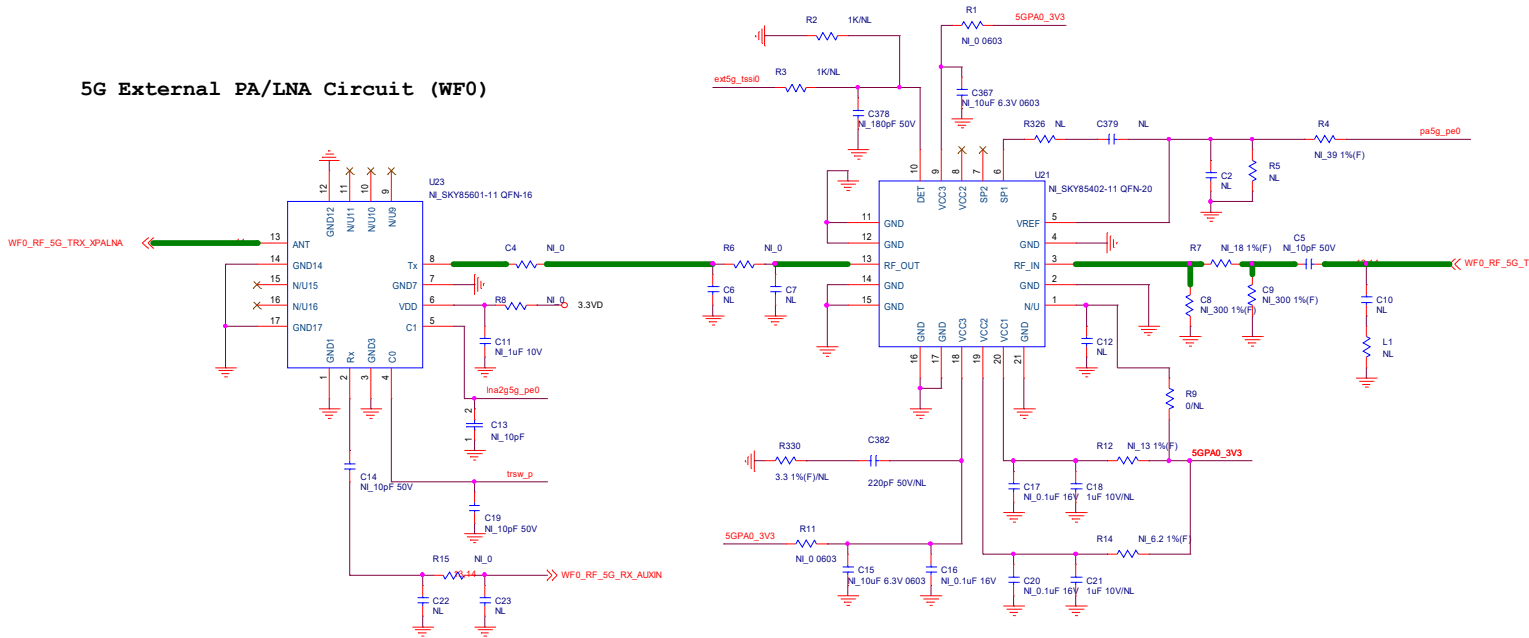


<Variant Name>

<OrgName> <OrgAddr1> <OrgAddr2>				Title <b>12.RJ45</b>			
Date	Tuesday, February 26, 2019	Size	Custom	Rev	V03	Sheet	12 of 18
DWG NO							<Doc>

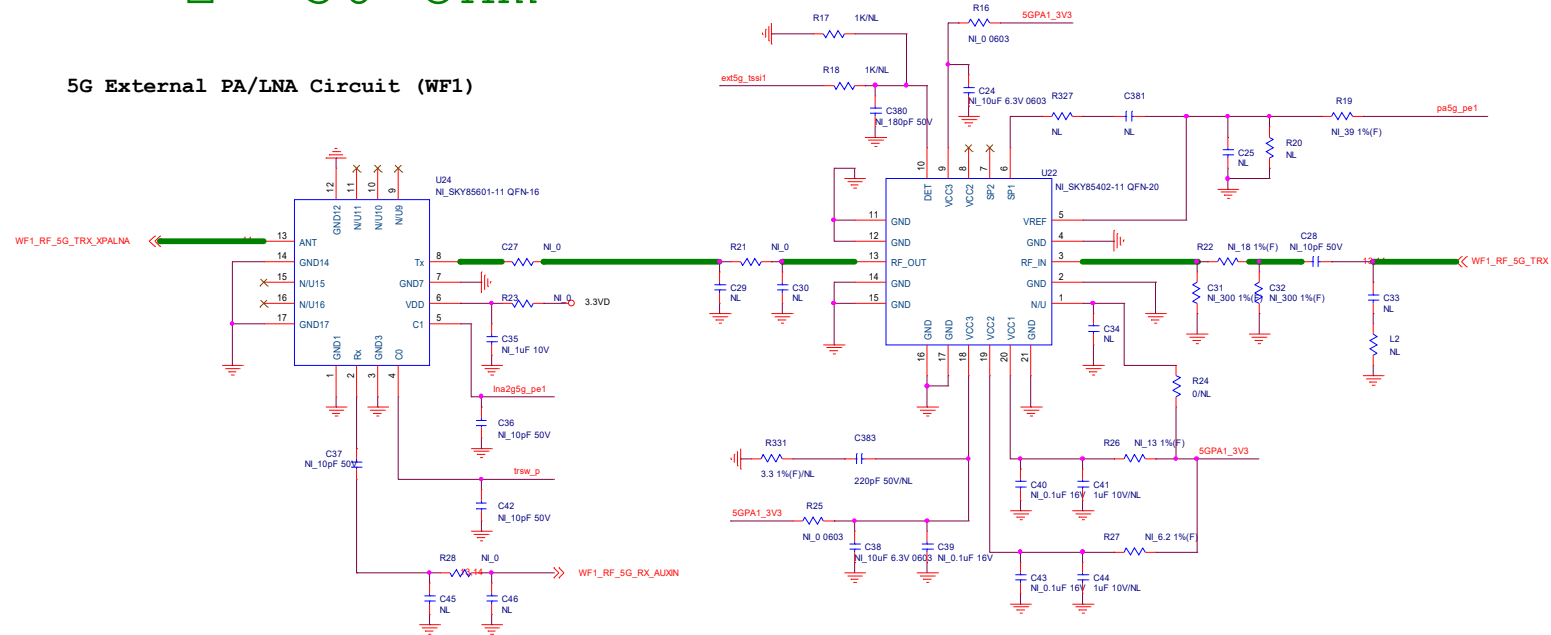


### 5G External PA/LNA Circuit (WF0)

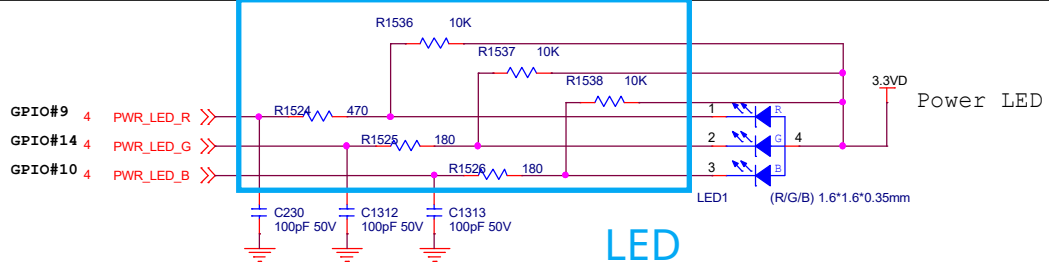


Z= 50 ohm

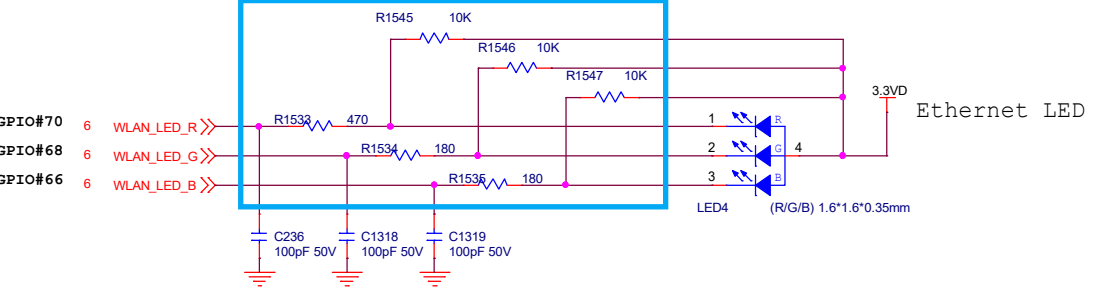
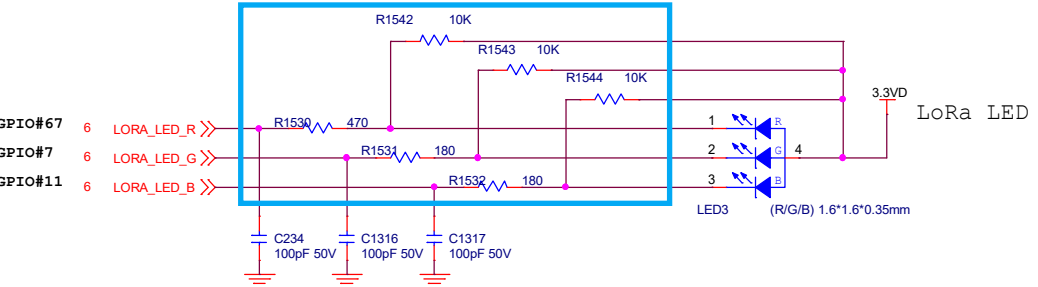
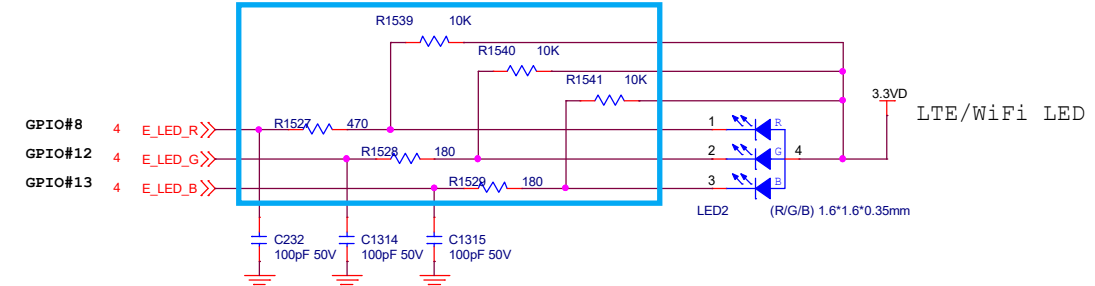
### 5G External PA/LNA Circuit (WF1)



Variant Name		OrgName		Title	
		<OrgAddr1> <OrgAddr2>		14. 5G RF	
Date	Tuesday, February 26, 2019	Size	C	Rev	V03
Sheet	14	of	18	DWG NO	<Doc>

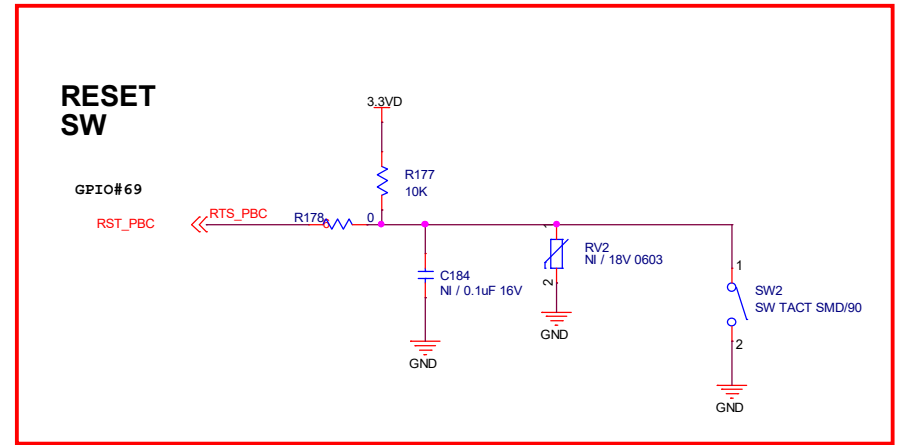


LED



mark (+) on PCB

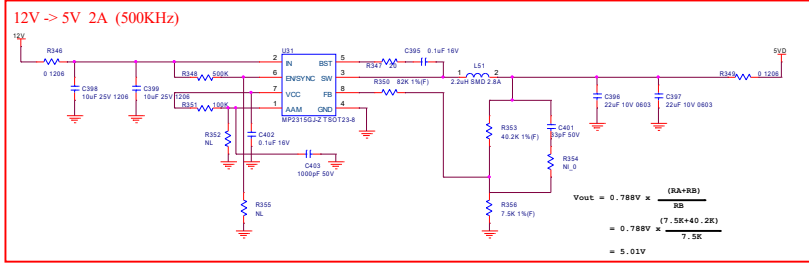
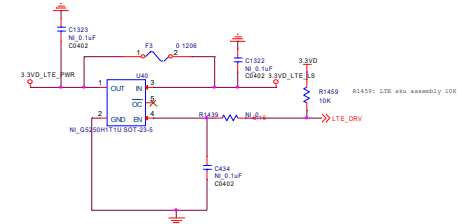
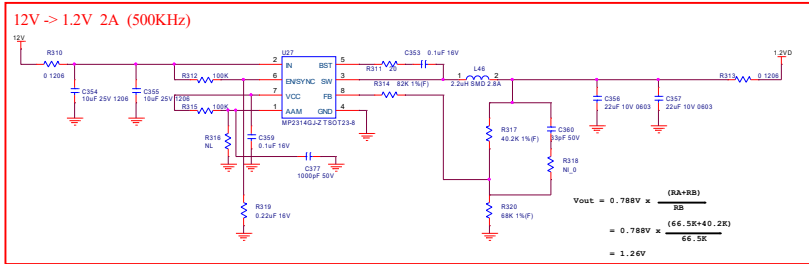
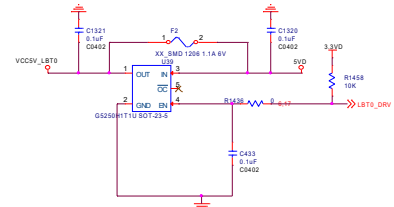
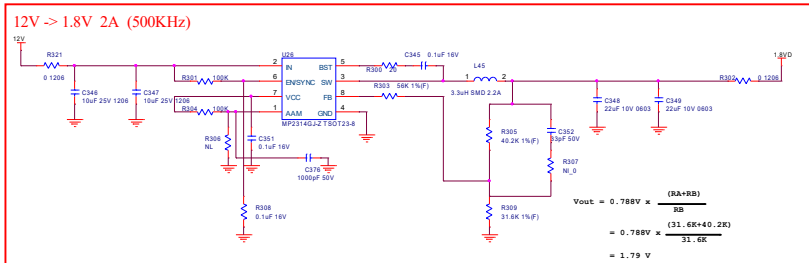
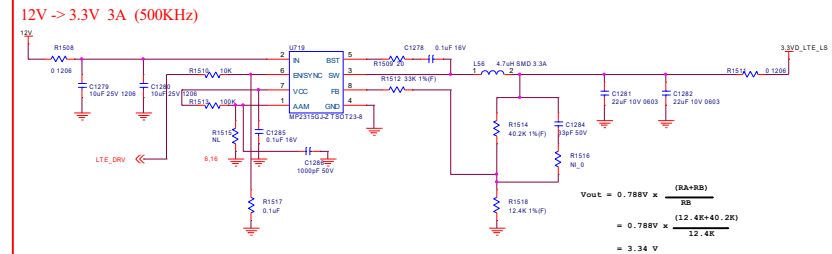
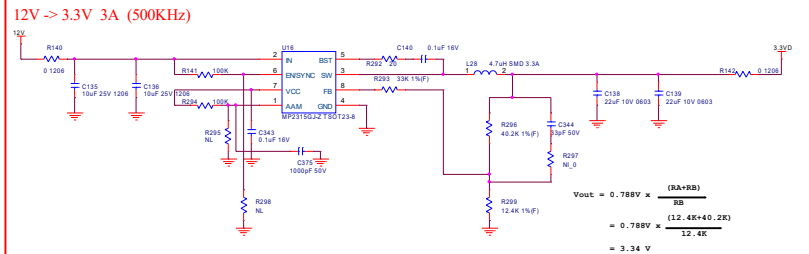
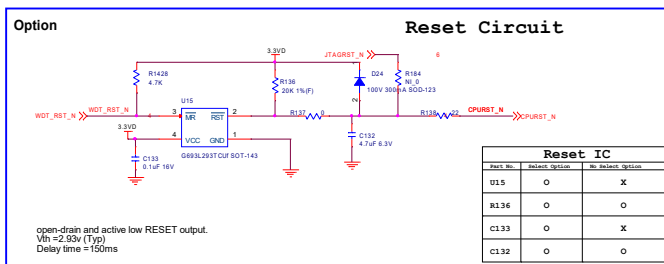
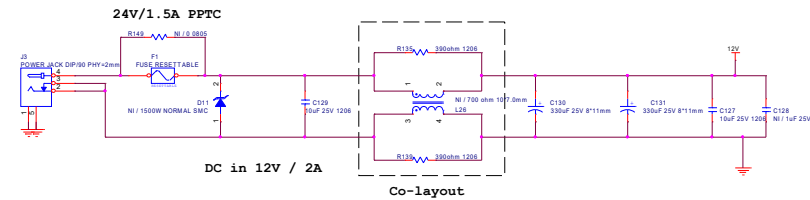
PUSH BUTTON SWITCHES



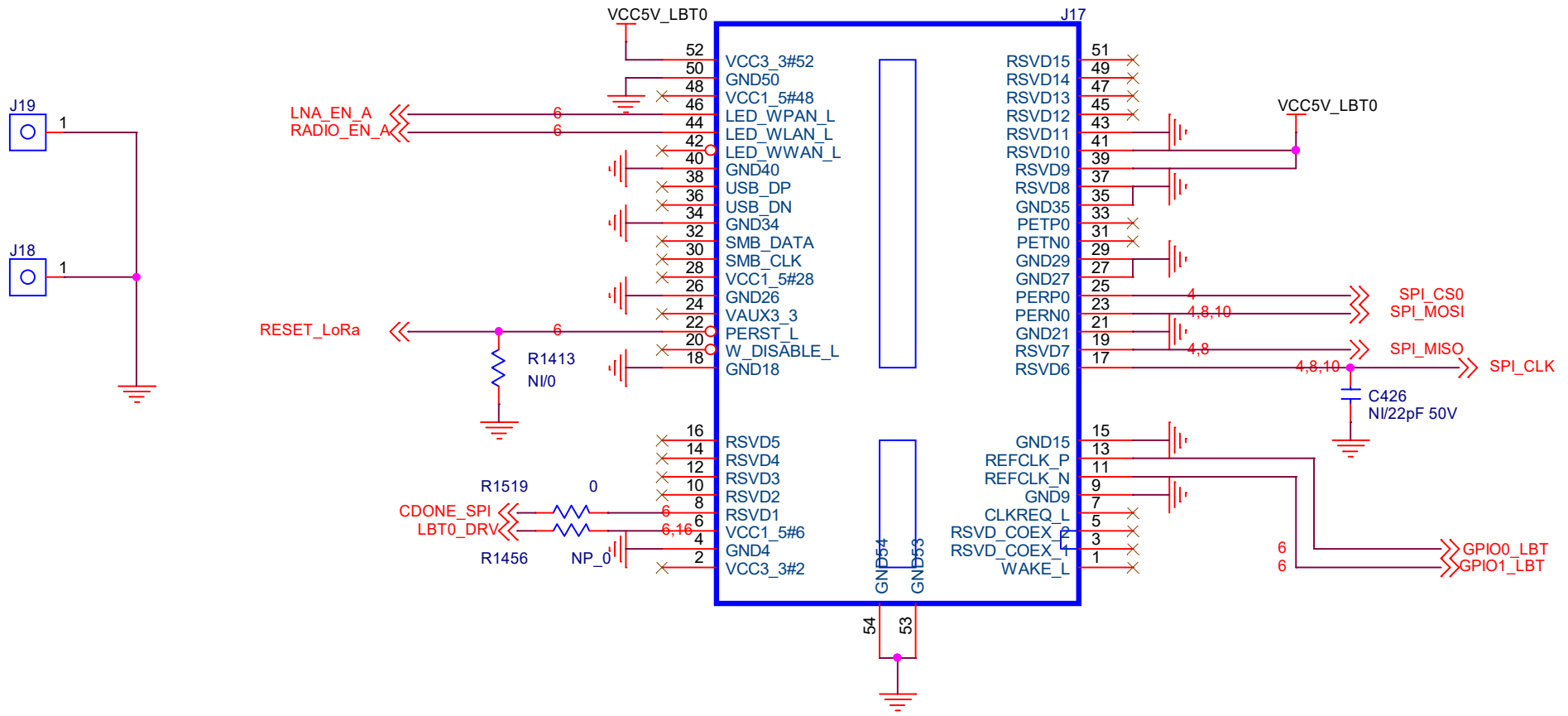
<Variant Name>

<OrgName> <OrgAddr1> <OrgAddr2>				Title <b>15. LED</b>			
Date	Tuesday, February 26, 2019	Size	B	Rev	V03	Sheet	15 of 18
							DWG NO <Doc>

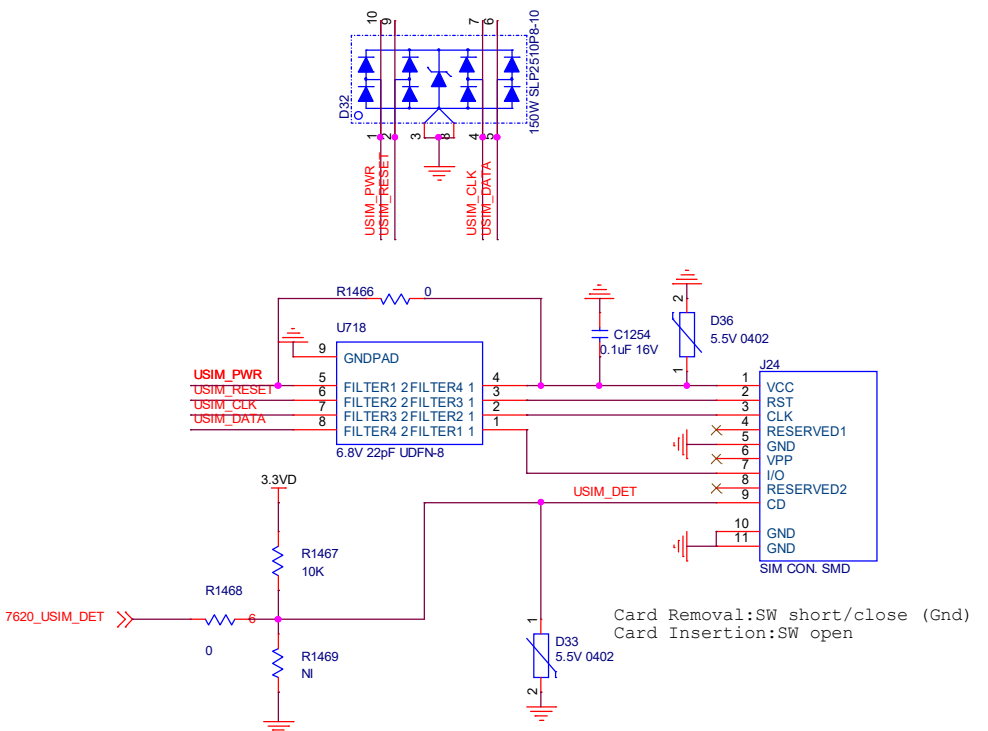
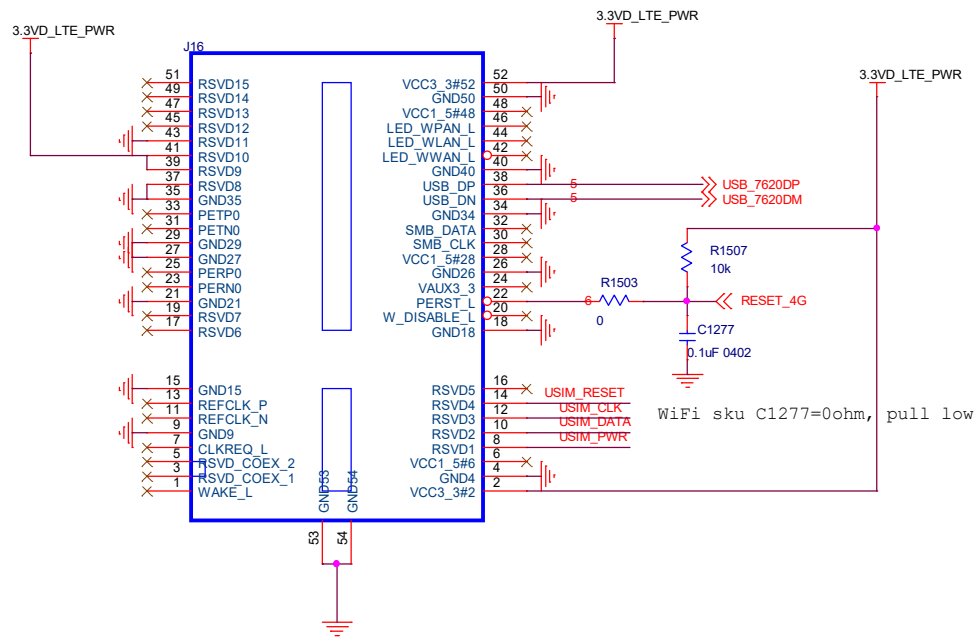
Vin = 12V / 1.5A



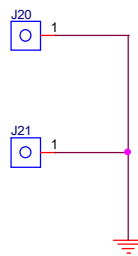




<b>&lt;OrgName&gt;</b> <OrgAddr1> <OrgAddr2>				Title <b>17. LoRa module</b>					
Date	Tuesday, February 26, 2019	Size	A	Rev	V03	Sheet	17 of 18	DWG NO	<Doc>



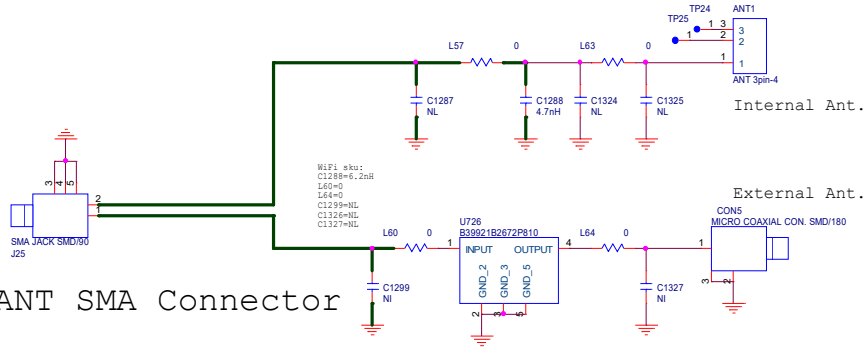
### mPCIE stud



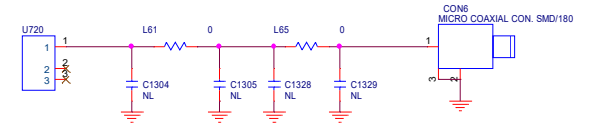
Card Removal:SW short/close (Gnd)  
Card Insertion:SW open

<OrgName>				Title <b>18. LTE module</b>			
<OrgAddr1>				<OrgAddr2>			
Date	Tuesday, February 26, 2019	Size	B	Rev	V03	Sheet	18 of 18
							DWG NO <Doc>

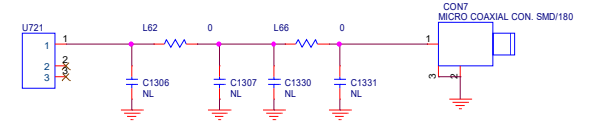
LoRa ANT SMA Connector



LTE ANT Div.

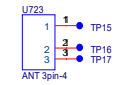


LTE ANT Main

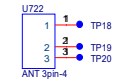


$$Z = 50 \text{ ohm}$$

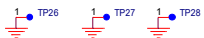
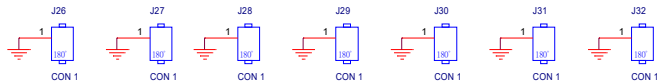
WiFi ANT Main



WiFi ANT Div.



RF cable clip



<b>&lt;OrgName&gt;</b>				<b>Title 19. Antenna</b>			
<b>&lt;OrgAddr1&gt;</b>				<b>&lt;OrgAddr2&gt;</b>			
Date	Tuesday, February 26, 2019	Size	Custom	Rev	V03	Sheet	18 of 18
						DWG NO	<Doc>