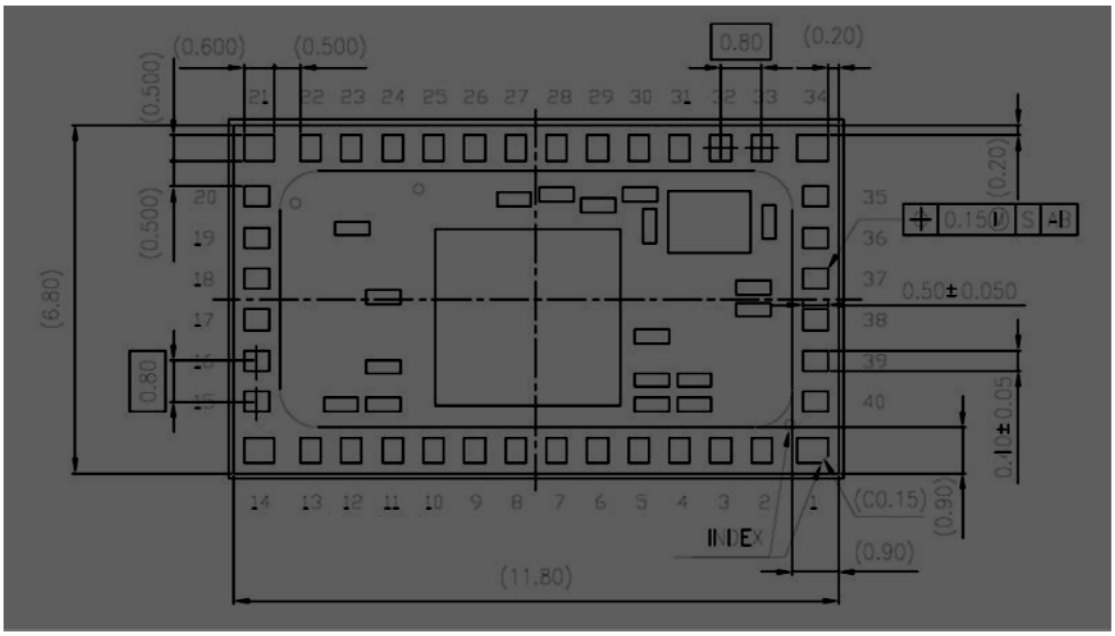
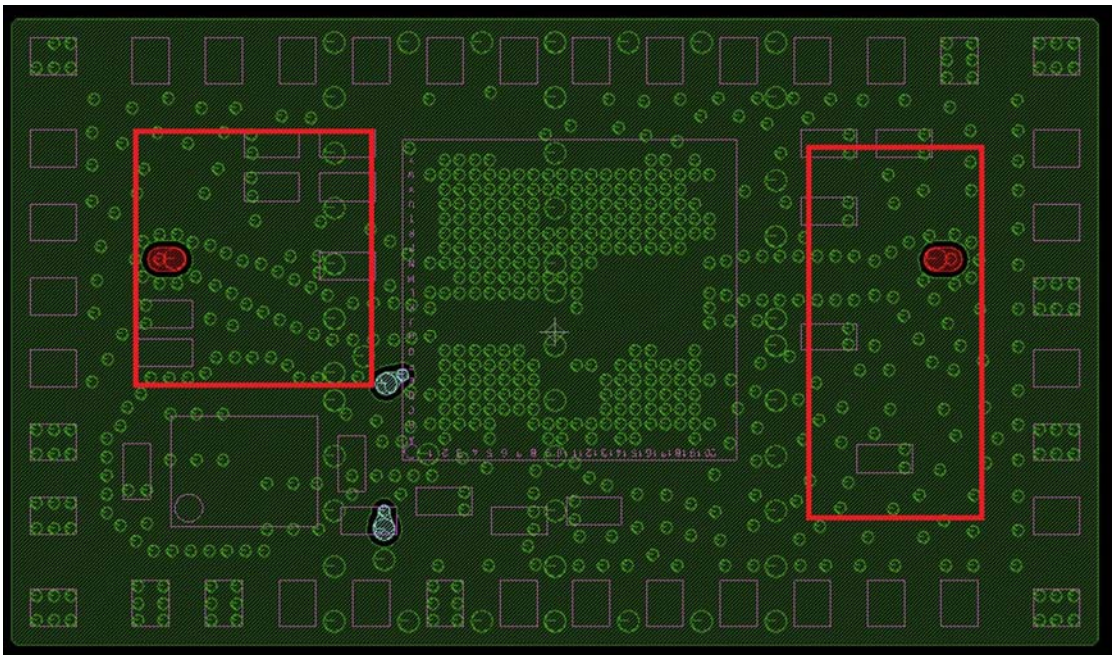
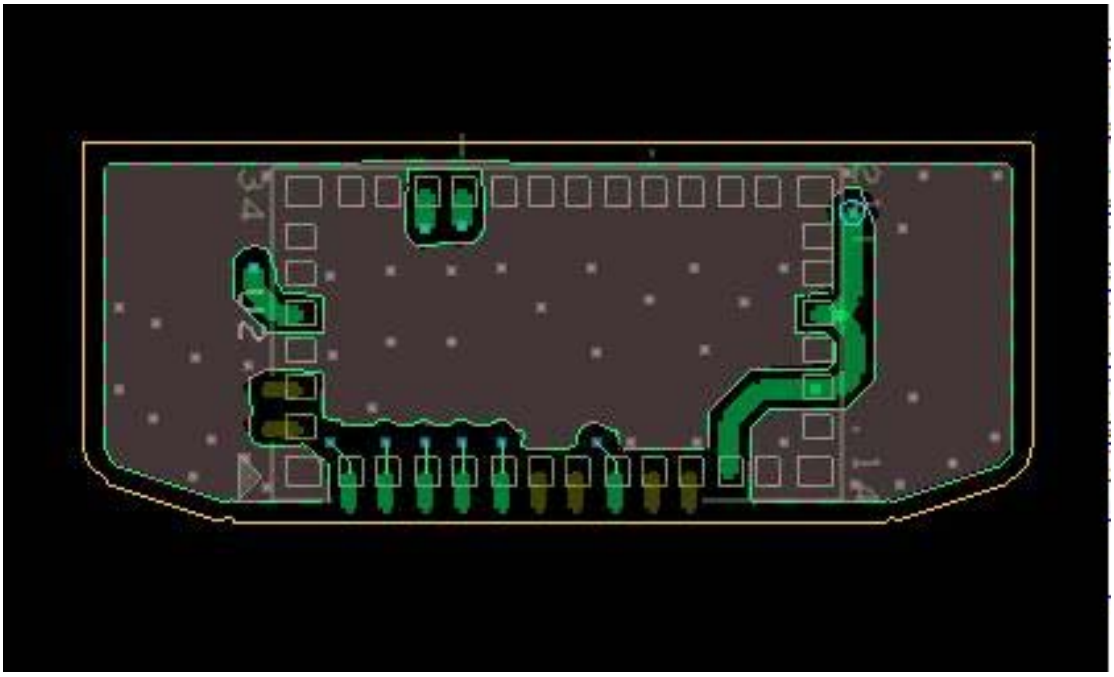
Layout for top side





No	Terminal Name	I/O	Type	Voltage	Description
1	VSS	-	G	0	Ground
2	NRST	input	D	2.5	Logic master reset (default) Pull-up
3	SENB1	input	D	2.5	SPI1 enable (default) Pull-up
4	SDAT1	input	D	2.5	SPI1 data write in (default) Pull-down.
5	SDAT1R	output	D	2.5	SPI1 data read out (default) Hi-Z. w/o Pull-down
6	SCLK1	input	D	2.5	SPI1 clock (default) Pull-up
7	SENB2	output	D	2.5	SPI2 enable (default) High output w/o Pull-up
8	SDAT2	output	D	2.5	SPI2 data (default) Low output w/o Pull-down
9	SCLK2	output	D	2.5	SPI2 clock (default) Low output w/o Pull-down
10	CLKOUT	output	D	2.5	Clock output for a microcomputer. (default) Low output w/o Pull-down
11	PLL_LOCK	output	D	2.5	PLL lock detect signal. When PLL lock is detected, this terminal is high output. (default) Low output w/o Pull-down
12	VDD_DIGIO	-	S	2.5	Digital I/O 2.5V Power supply
13	VSS	-	G	0	Ground
14	VSS	-	G	0	Ground
15	VSS	-	G	0	Ground
16	VDD_TXBB	-	S	2.5	TX Base Band 2.5V Power supply
17	VSS	-	G	0	Ground
18	VDD_TXRF	-	S	2.5	TX RF 2.5V Power supply
19	VSS	-	G	0	Ground

No	Terminal Name	I/O	Type	Voltage	Description
20	VSS	-	G	0	Ground
21	VSS	-	G	0	Ground
22	VSS	-	G	0	Ground
23	VSS	-	G	0	Ground
24	VSS	-	G	0	Ground
25	VSS	-	G	0	Ground
26	VSS	-	G	0	Ground
27	VSS	-	G	0	Ground
28	VSS	-	G	0	Ground
29	VSS	-	G	0	Ground
30	VDD_PLL	-	S	2.5	PLL Synthesizer 2.5V Power supply
31	VDD_PLL	-	S	2.5	PLL Synthesizer 2.5V Power supply
32	VSS	-	G	0	Ground
33	VSS	-	G	0	Ground
34	VSS	-	G	0	Ground
35	VSS	-	G	0	Ground
36	VSS	-	G	0	Ground
37	VDD_RX	-	S	2.5	RX 2.5V Power supply
38	VSS	-	G	0	Ground
39	RX_I_FIL	output	A	2.5	Baseband RX Analog I output. (default) Hi-Z
40	RX_Q_FIL	output	A	2.5	Baseband RX Analog Q output. (default) Hi-Z



Antenna layout.

Two red areas are antenna.