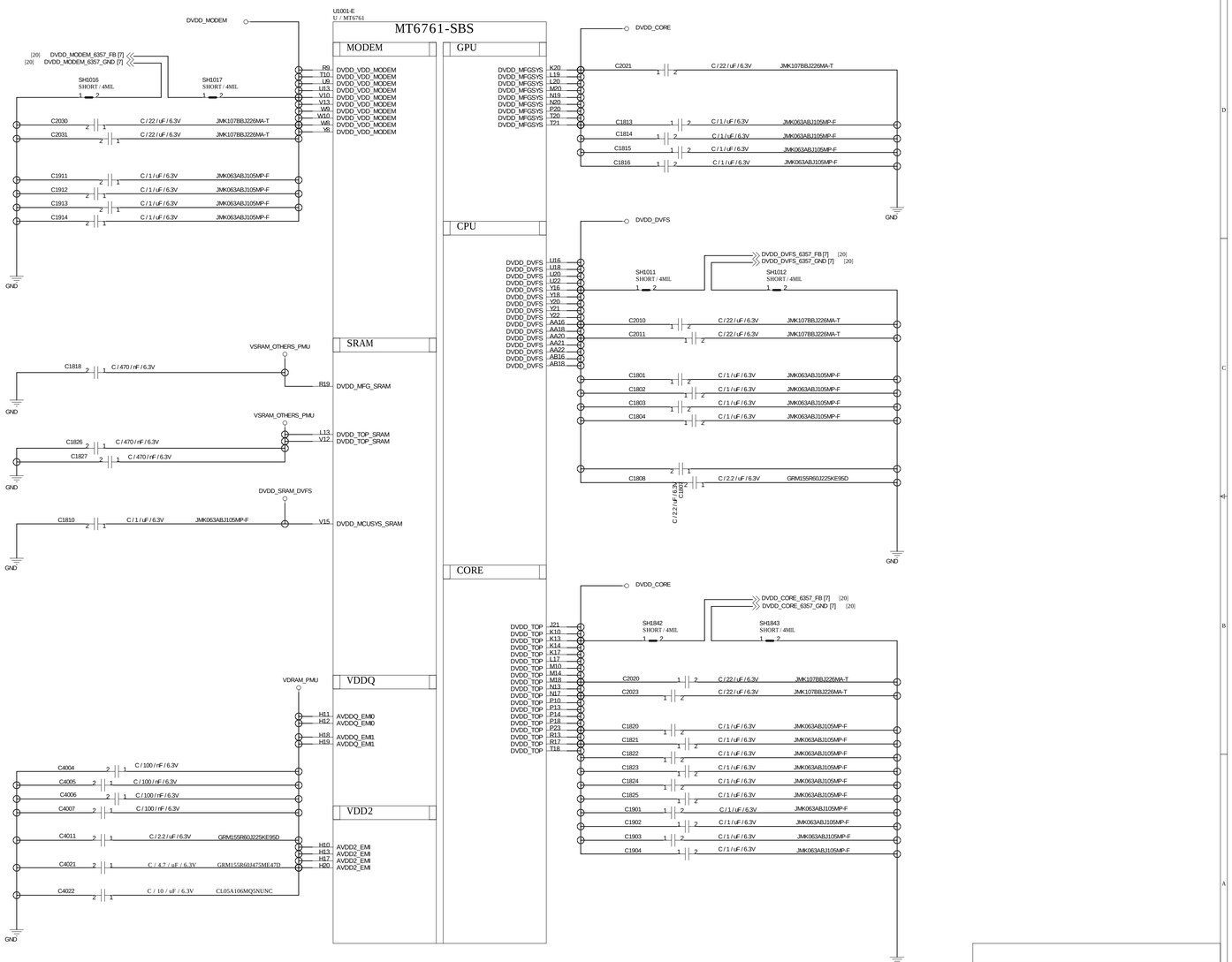
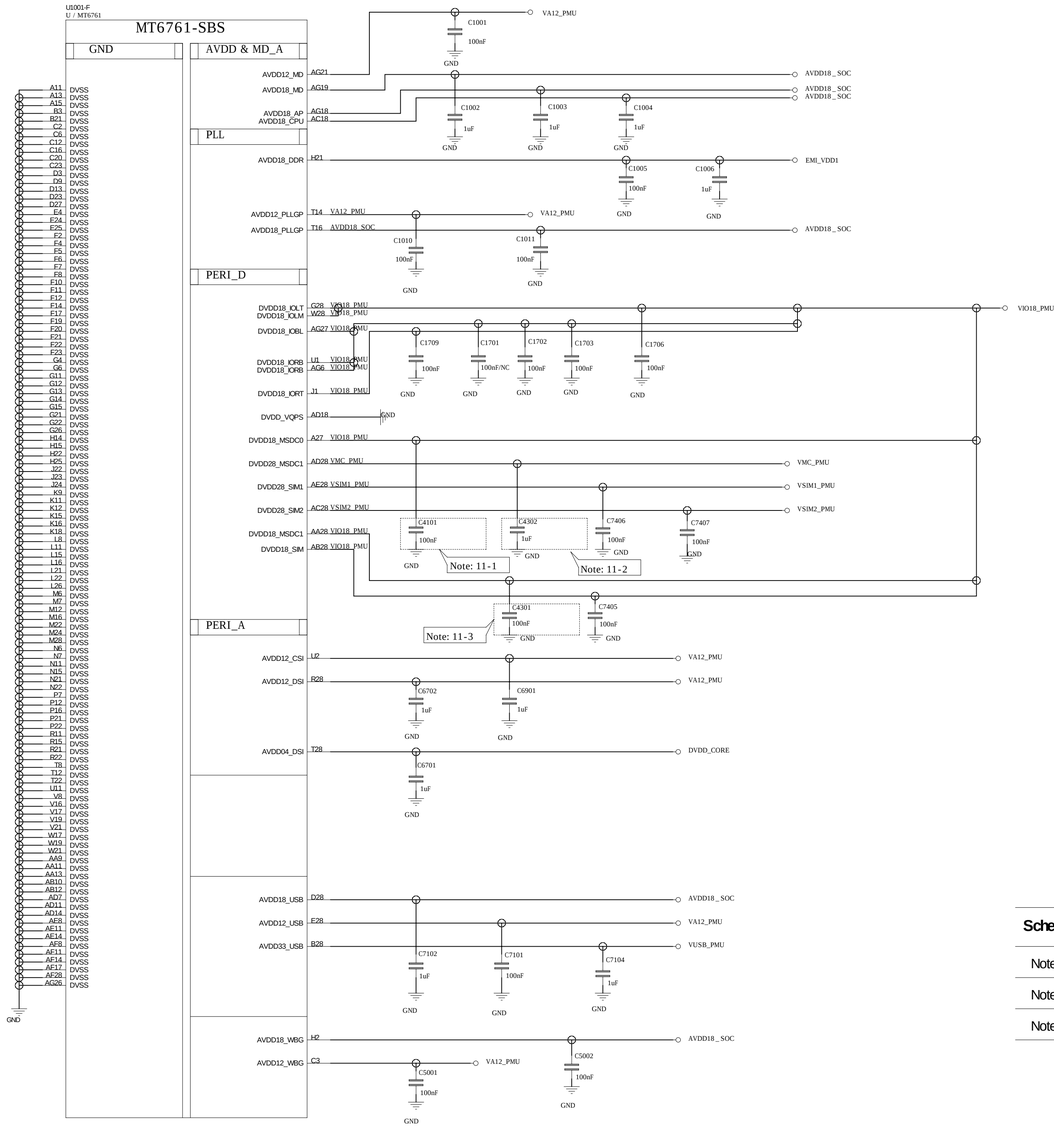

U1001:E
U / MT6761
MT6761-SBS
MODEM
SRAM
VDDQ
VDD2
GPU
CPU
CORE
DVDD_MODEM
[20] DVDD_MODEM_6357_FB [7]
[20] DVDD_MODEM_6357_GND [7]
SH1016
SHORT / 4MIL
SH1017
SHORT / 4MIL
R9 DVDD_VDD_MODEM
T10 DVDD_VDD_MODEM
U9 DVDD_VDD_MODEM
U11 DVDD_VDD_MODEM
V10 DVDD_VDD_MODEM
V13 DVDD_VDD_MODEM
W9 DVDD_VDD_MODEM
W10 DVDD_VDD_MODEM
W8 DVDD_VDD_MODEM
V8 DVDD_VDD_MODEM
C2030 C / 22 / uF / 6.3V JMK107BBJ226MA-T
C2031 C / 22 / uF / 6.3V JMK107BBJ226MA-T
C1911 C / 1 / uF / 6.3V JMK063ABJ105MP-F
C1912 C / 1 / uF / 6.3V JMK063ABJ105MP-F
C1913 C / 1 / uF / 6.3V JMK063ABJ105MP-F
C1914 C / 1 / uF / 6.3V JMK063ABJ105MP-F
GND
VSRAM_OTHERS_PMU
C1818 C / 470 / nF / 6.3V
R19 DVDD_MFG_SRAM
VSRAM_OTHERS_PMU
C1826 C / 470 / nF / 6.3V
C1827 C / 470 / nF / 6.3V
L13 DVDD_TOP_SRAM
V12 DVDD_TOP_SRAM
DVDD_SRAM_DVFS
C1810 C / 1 / uF / 6.3V JMK063ABJ105MP-F
V15 DVDD_MCUSYS_SRAM
VDRAM_PMU
H11 AVDDQ_EMI0
H12 AVDDQ_EMI0
H18 AVDDQ_EMI1
H19 AVDDQ_EMI1
C4004 C / 100 / nF / 6.3V
C4005 C / 100 / nF / 6.3V
C4006 C / 100 / nF / 6.3V
C4007 C / 100 / nF / 6.3V
C4011 C / 2.2 / uF / 6.3V GRM155R60J225KE95D
C4021 C / 4.7 / uF / 6.3V GRM155R60J475ME47D
C4022 C / 10 / uF / 6.3V CL05A106MQ5NUNC
H10 AVDDZ_EMI
H13 AVDDZ_EMI
H17 AVDDZ_EMI
H20 AVDDZ_EMI
DVDD_CORE
DVDD_MFGSYS K20
DVDD_MFGSYS L19
DVDD_MFGSYS L20
DVDD_MFGSYS M20
DVDD_MFGSYS N19
DVDD_MFGSYS N20
DVDD_MFGSYS P20
DVDD_MFGSYS T20
DVDD_MFGSYS T21
C2021 C / 22 / uF / 6.3V JMK107BBJ226MA-T
C1813 C / 1 / uF / 6.3V JMK063ABJ105MP-F
C1814 C / 1 / uF / 6.3V JMK063ABJ105MP-F
C1815 C / 1 / uF / 6.3V JMK063ABJ105MP-F
C1816 C / 1 / uF / 6.3V JMK063ABJ105MP-F
GND
DVDD_DVFS
DVDD_DVFS U16
DVDD_DVFS U18
DVDD_DVFS U20
DVDD_DVFS U22
DVDD_DVFS Y16
DVDD_DVFS Y18
DVDD_DVFS Y20
DVDD_DVFS Y21
DVDD_DVFS Y22
DVDD_DVFS AA16
DVDD_DVFS AA18
DVDD_DVFS AA20
DVDD_DVFS AA21
DVDD_DVFS AA22
DVDD_DVFS AB16
DVDD_DVFS AB18
DVDD_DVFS_6357_FB [7] [20]
DVDD_DVFS_6357_GND [7] [20]
SH1011
SHORT / 4MIL
SH1012
SHORT / 4MIL
C2010 C / 22 / uF / 6.3V JMK107BBJ226MA-T
C2011 C / 22 / uF / 6.3V JMK107BBJ226MA-T
C1801 C / 1 / uF / 6.3V JMK063ABJ105MP-F
C1802 C / 1 / uF / 6.3V JMK063ABJ105MP-F
C1803 C / 1 / uF / 6.3V JMK063ABJ105MP-F
C1804 C / 1 / uF / 6.3V JMK063ABJ105MP-F
C1808 C / 2.2 / uF / 6.3V GRM155R60J225KE95D
C1805 C / 22 / uF / 6.3V
GND
DVDD_CORE
DVDD_TOP J21
DVDD_TOP K10
DVDD_TOP K13
DVDD_TOP K14
DVDD_TOP K17
DVDD_TOP L17
DVDD_TOP M10
DVDD_TOP M14
DVDD_TOP M18
DVDD_TOP N13
DVDD_TOP N17
DVDD_TOP P10
DVDD_TOP P13
DVDD_TOP P14
DVDD_TOP P18
DVDD_TOP P23
DVDD_TOP R13
DVDD_TOP R17
DVDD_TOP T18
DVDD_CORE_6357_FB [7] [20]
DVDD_CORE_6357_GND [7] [20]
SH1842
SHORT / 4MIL
SH1843
SHORT / 4MIL
C2020 C / 22 / uF / 6.3V JMK107BBJ226MA-T
C2023 C / 22 / uF / 6.3V JMK107BBJ226MA-T
C1820 C / 1 / uF / 6.3V JMK063ABJ105MP-F
C1821 C / 1 / uF / 6.3V JMK063ABJ105MP-F
C1822 C / 1 / uF / 6.3V JMK063ABJ105MP-F
C1823 C / 1 / uF / 6.3V JMK063ABJ105MP-F
C1824 C / 1 / uF / 6.3V JMK063ABJ105MP-F
C1825 C / 1 / uF / 6.3V JMK063ABJ105MP-F
C1901 C / 1 / uF / 6.3V JMK063ABJ105MP-F
C1902 C / 1 / uF / 6.3V JMK063ABJ105MP-F
C1903 C / 1 / uF / 6.3V JMK063ABJ105MP-F
C1904 C / 1 / uF / 6.3V JMK063ABJ105MP-F
GND
Title
10_BB_POWER_PDN
Size
A1
MTK Confidential
Date: Wednesday, November 07, 2018
Sheet 2 of 25



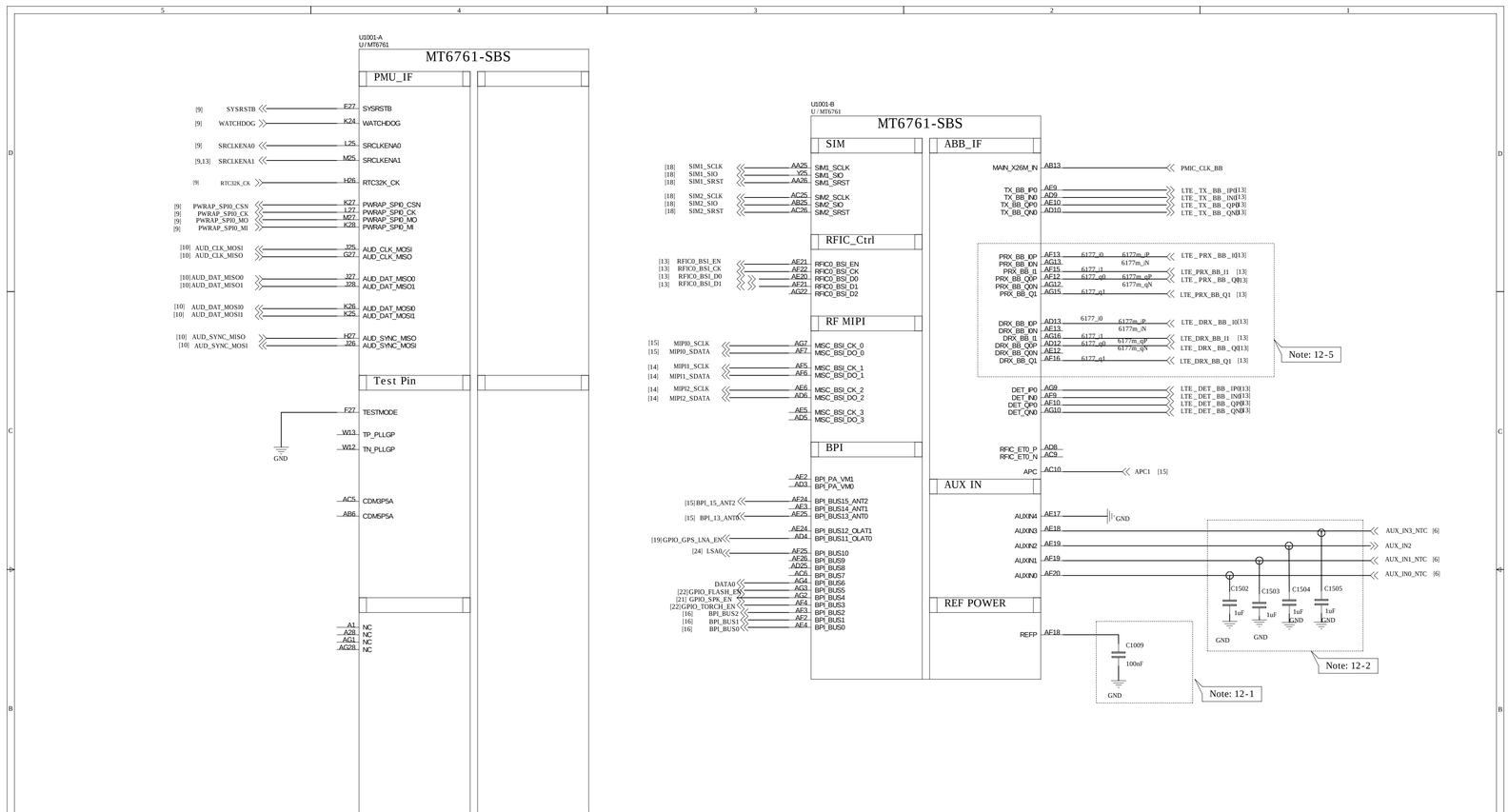
Schematic design notice of "11_BB_POWER_IO" page.

Note 11-1: C4101 closed DVDD18_MSDC0 150mil

Note 11-2: C4302 closed DVDD28_MSDC1 150mil

Note 11-3: C4301 closed DVDD18_MSDC1 150mil

Title	11_BB_POWER_PDN
Size: A1	MTK Confidential
Date: Wednesday, November 07, 2018	Sheet 3 of 25



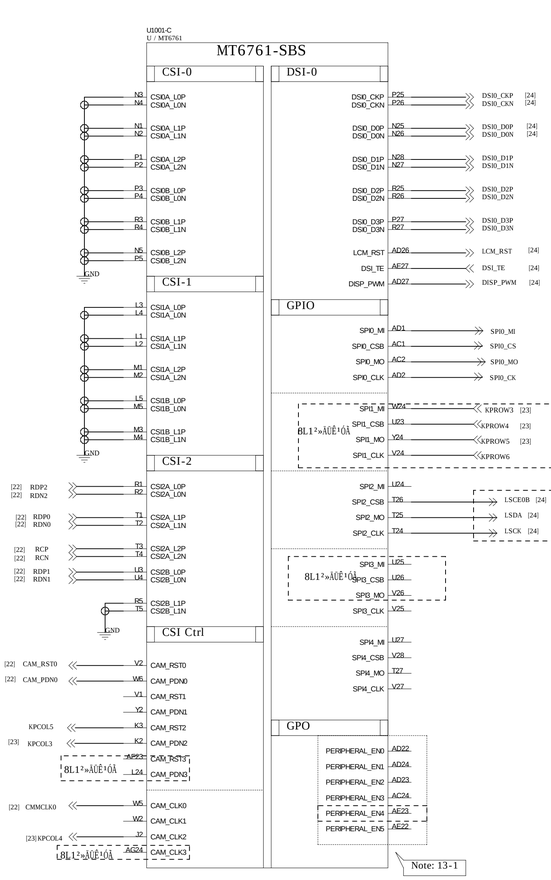
Schematic design notice of "12_BB_1" page.

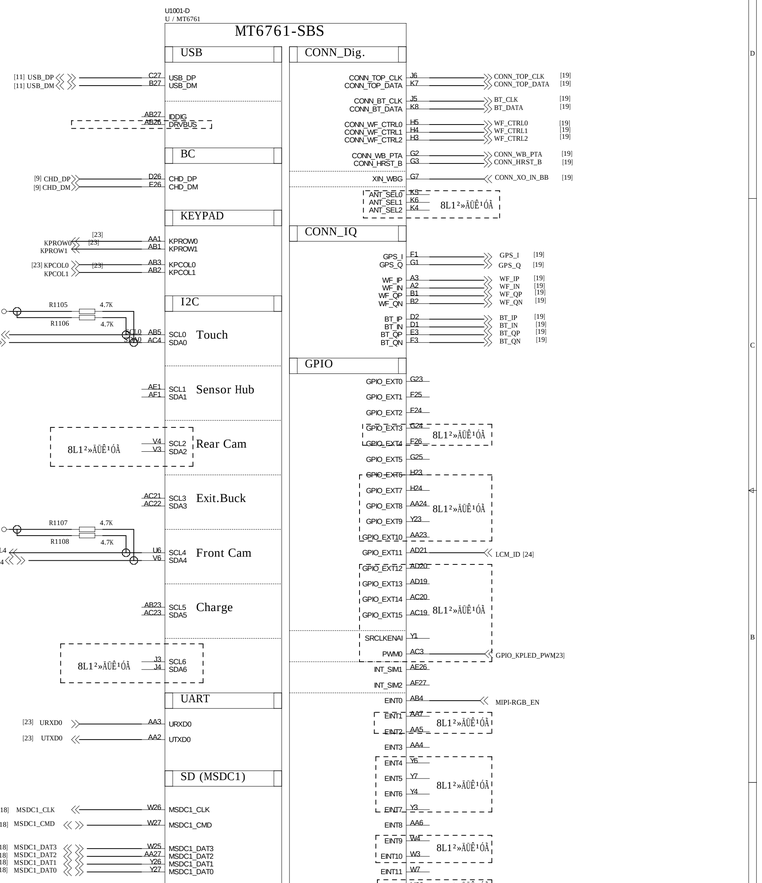
Note 12-1: The de-coupling cap. for REFP (AF18 ball) have to be placed as close to BB as possible.

Note 12-2: To shunt a 1uF capacitor in the AUXIN ADC input to prevent noise coupling. It should be placed as close to BB as possible. Connect the unused AUX ADC input to GND.

Note 12-5: Please set unused IQ pins in NC

Title	12_BB_1
Size	A1
	MTK Confidential
Date:	Friday, November 09, 2018
Sheet	4 of 25





Schematic design notice of "13_BB_2" page.

Note 13-1: The enable pin of acoustic or optoelectronic devices (e.g. SPK AMP/Backlight/Charger OCP/OVP) suggest to use Peripheral_EN[0:5]
If use other GPIOs as enable pin, suggest to reserve 0201 NC to GND

Title	4_BB_2
Size: A1	MTK Confidential
Date:	Friday, December 08, 2017 Sheet 5 of 25

U1001-G
U / MT6761

MT6761-SBS

EMI_DDR

EM0_DQ0 [17]	D5	EM0_DQ0	EM0_CS0	E8	EM0_CS0 [17]
EM0_DQ1 [17]	E5	EM0_DQ1	EM0_CS1	A9	EM0_CS1 [17]
EM0_DQ2 [17]	D6	EM0_DQ2	EM1_CS0	D18	EM0_CKE0 [17]
EM0_DQ3 [17]	E6	EM0_DQ3	EM1_CS1	C17	EM0_CKE1 [17]
EM0_DQ4 [17]	A5	EM0_DQ4			
EM0_DQ5 [17]	C7	EM0_DQ5	EM0_CKE0	D8	EM0_DM0 [17]
EM0_DQ6 [17]	C5	EM0_DQ6	EM0_CKE1	E7	EM0_DM1 [17]
EM0_DQ7 [17]	B5	EM0_DQ7	EM1_CKE0	E18	EM0_DM2 [17]
EM0_DQ8 [17]	B12	EM0_DQ8	EM1_CKE1	D19	EM0_DM3 [17]
EM0_DQ9 [17]	E11	EM0_DQ9			
EM0_DQ10 [17]	B11	EM0_DQ10	EM0_DM0	A7	EM0_CK_T [17]
EM0_DQ11 [17]	C11	EM0_DQ11	EM0_DM1	E10	EM0_CK_C [17]
EM0_DQ12 [17]	B13	EM0_DQ12	EM1_DM0	B19	EM0_DQS0_C [17]
EM0_DQ13 [17]	D10	EM0_DQ13	EM1_DM1	B16	EM0_DQS0_T [17]
EM0_DQ14 [17]	C10	EM0_DQ14			
EM0_DQ15 [17]	D12	EM0_DQ15	EM0_DQS0_C	C4	EM0_DQS1_C [17]
			EM0_DQS0_T	D4	EM0_DQS1_T [17]
EM0_DQ16 [17]	E21	EM1_DQ0	EM1_DQS0_C	E22	EM0_DQS2_C [17]
EM0_DQ17 [17]	D21	EM1_DQ1	EM1_DQS0_T	D22	EM0_DQS2_T [17]
EM0_DQ18 [17]	E20	EM1_DQ2	EM0_DQS1_C	E13	EM0_DQS3_C [17]
EM0_DQ19 [17]	D20	EM1_DQ3	EM0_DQS1_T	F13	EM0_DQS3_T [17]
EM0_DQ20 [17]	C21	EM1_DQ4	EM1_DQS1_C	E14	
EM0_DQ21 [17]	B20	EM1_DQ5	EM1_DQS1_T	D14	
EM0_DQ22 [17]	A21	EM1_DQ6			
EM0_DQ23 [17]	C22	EM1_DQ7	EM0_CK_T	F9	
EM0_DQ24 [17]	C14	EM1_DQ8	EM0_CK_C	F9	
EM0_DQ25 [17]	D15	EM1_DQ9	EM1_CK_T	E17	
EM0_DQ26 [17]	C15	EM1_DQ10	EM1_CK_C	D17	
EM0_DQ27 [17]	E16	EM1_DQ11			
EM0_DQ28 [17]	C13	EM1_DQ12	EM0_CA0	D11	EM0_CA0 [17]
EM0_DQ29 [17]	B17	EM1_DQ13	EM0_CA1	C9	EM0_CA1 [17]
EM0_DQ30 [17]	B15	EM1_DQ14	EM0_CA2	B7	EM0_CA2 [17]
EM0_DQ31 [17]	E15	EM1_DQ15	EM0_CA3	B8	EM0_CA3 [17]
			EM0_CA4	B9	EM0_CA4 [17]
EVREF [17]	F16	EM_TP	EM0_CA5	D7	EM0_CA5 [17]
	G16	EM_TN			
			EM1_CA0	F18	EM0_CA6 [17]
			EM1_CA1	A17 EM0_CA7	EM0_CA7 [17]
	E23	EM_RESET_N	EM1_CA2	A19 EM0_CA8	EM0_CA8 [17]
			EM1_CA3	C19 EM0_CA9	EM0_CA9 [17]
	B4	EM_EXTR	EM1_CA4	C18	
			EM1_CA5	E19	

Note: 14-1

EM_EXTR

R4001
R / 34.8 / ohm
1%

GND

Note: 14-2

eMMC (MSDC0)

MSDE0_DAT7	A26	MSDC0_DAT7	MSDC0_RSTB	C25	MSDC0_RSTB [17]
MSDE0_DAT6	D24	MSDC0_DAT6	MSDC0_CMD	B25	MSDC0_CMD [17]
MSDE0_DAT5	C26	MSDC0_DAT5	MSDC0_CLK	D25	MSDC0_CLK [17]
MSDE0_DAT4	A25	MSDC0_DAT4	MSDC0_DSL	B26	MSDC0_DSL [17]
MSDE0_DAT3	C24	MSDC0_DAT3			
MSDE0_DAT2	B23	MSDC0_DAT2			
MSDE0_DAT1	B24	MSDC0_DAT1			
MSDE0_DAT0	A24	MSDC0_DAT0			

Thermistor to sense Board Edges

VIO18_PMU

R1504
390K

R1505
10K/NTC

GND

[4] AUX_IN3_NTC

VIO18_PMU

R1502
390K

R1602
10K/NTC

GND

VIO18_PMU

R1501
390K

R1601
10K/NTC

GND

[4] AUX_IN1_NTC

[4] AUX_IN0_NTC

Thermistor to sense RF PA temperature

1. NTC1502 must close to LTE Band 7 PA or the hottest PA <2mm.
2. The distance is the shortest distance from package edge to edge.

Thermistor to sense AP temperature

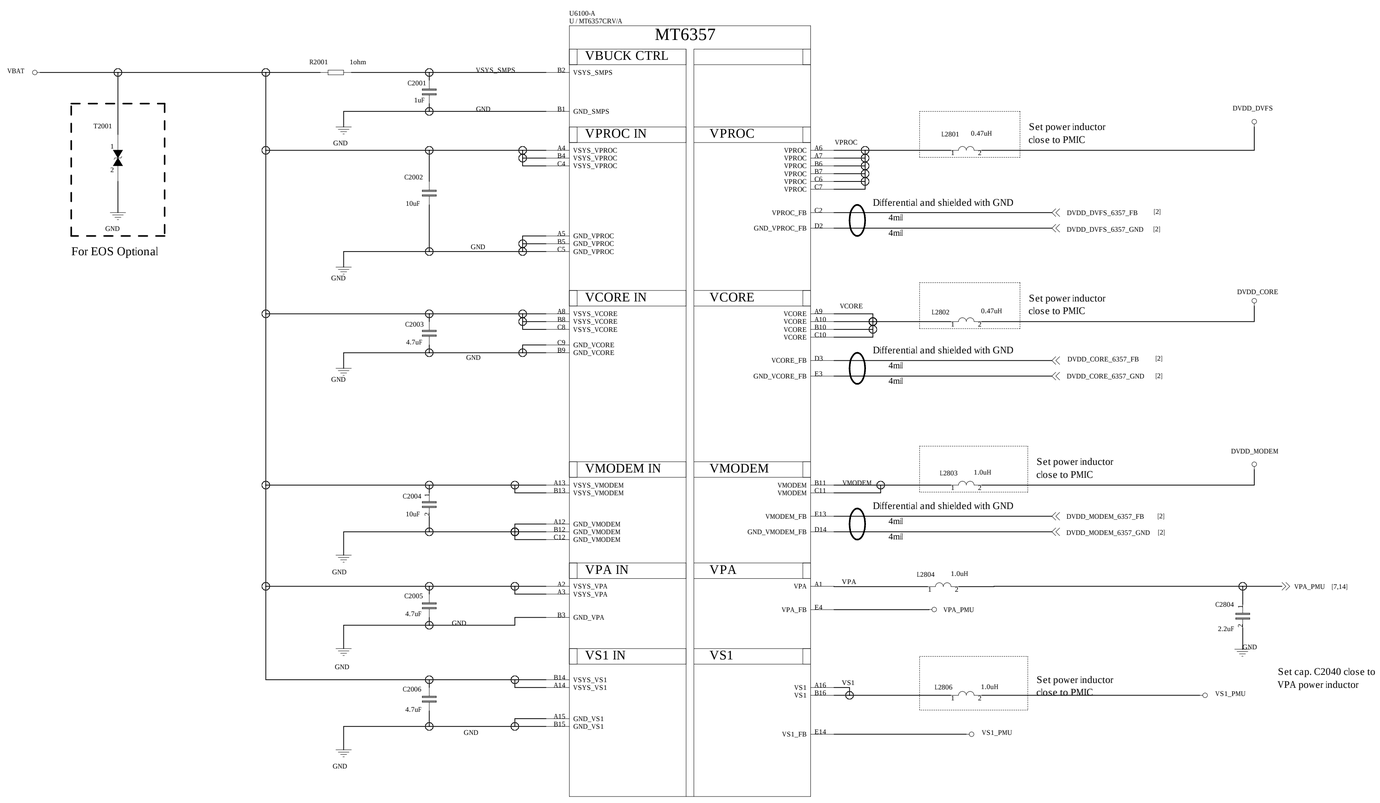
1. NTC1501must keep a distance about 6~8 mm away from AP and far from other heat sources 10 mm at least.
2. The distance is the shortest distance from package edge to edge.

Schematic design notice of "14_BB_3" page.

Note 14-1: R4001 please select 60.4 ohm (1%) resistor

Note 14-2: Please check eMCP LP3 and eMCP LP4X/LP4 pin mux

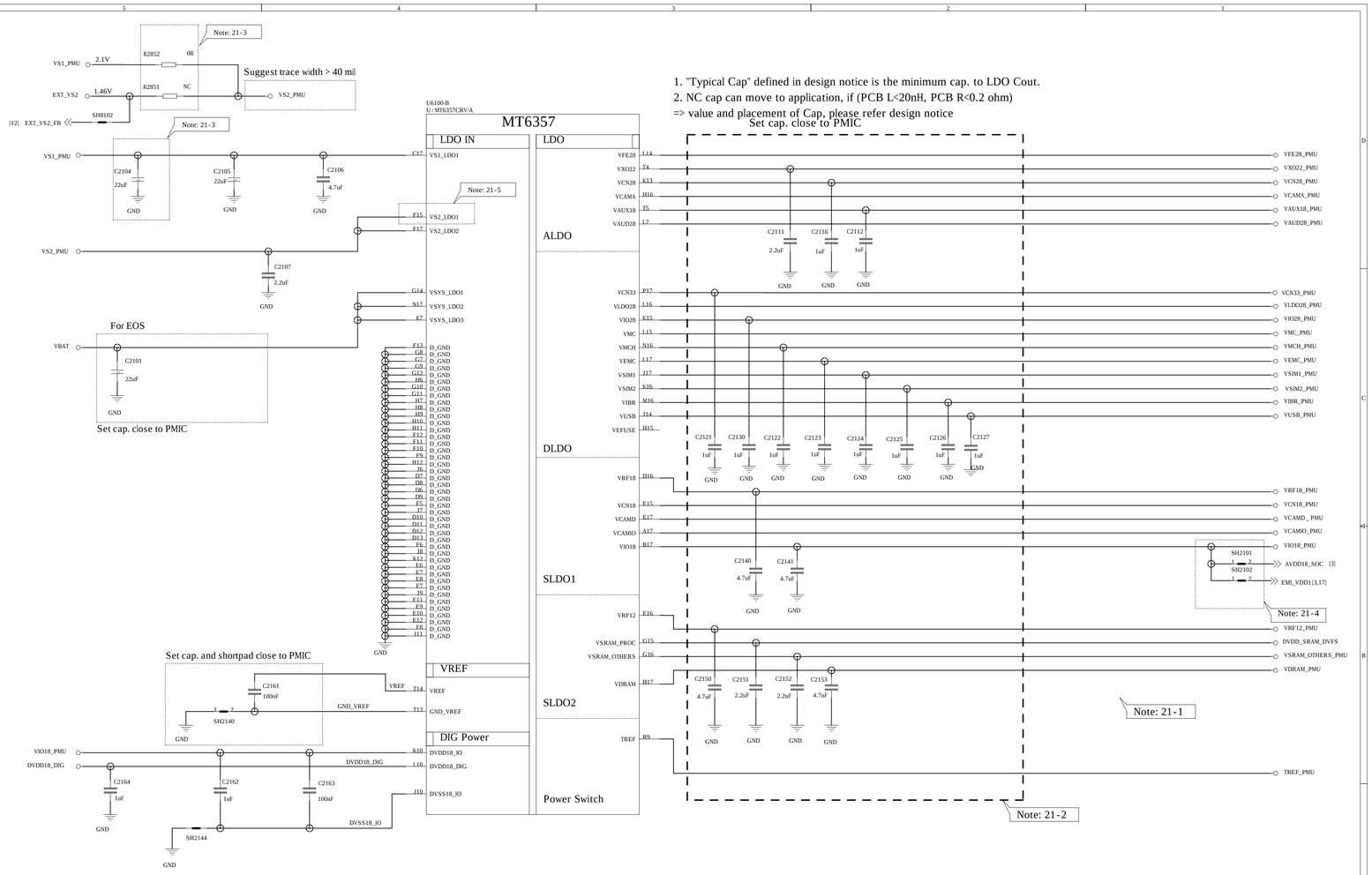
Title	14_BB_3
Size A1	MTK Confidential
Date: Friday, November 09, 2018	Sheet 6 of 25



Schematic design notice of "20_POWER_MT6357_Buck"

Note 20-1: C2040, please choose 0603 size

Title	6_POWER_MT6357-Buck
Size: A1	MTK Confidential
Date: Friday, December 08, 2017	Sheet 7 of 25



1. "Typical Cap" defined in design notice is the minimum cap. to LDO Cout.
2. NC cap can move to application, if (PCB L<20nH, PCB R<0.2 ohm)
   => value and placement of Cap, please refer design notice

Schematic design notice of "21_POWER_MT6357_LDO"

Note 21-1: If these power trace can meet LDO layout constraint, these CAP can be NC or removed. Please refer to MT6357 design notice.

Note 21-2: Output cap range please follow MT6357CRV LDO design notice

Note 21-3: Ext Buck BOM option

	Ext. buck option	
	w/ EXT VS2 Buck	w/o EXT VS2 Buck
C2104	10uF	22uF
R2851	0-ohm , 0603	NC
R2852	NC	0-ohm , 0603

Note 21-4: Please set SH2101 and SH2102 close to C2141, making star connection among VIO18_PMU, AVDD18_SOC, and EMI_VDD1 near to LDO cap. C2141

Please also refer to MT6357 design notice for further detail design information

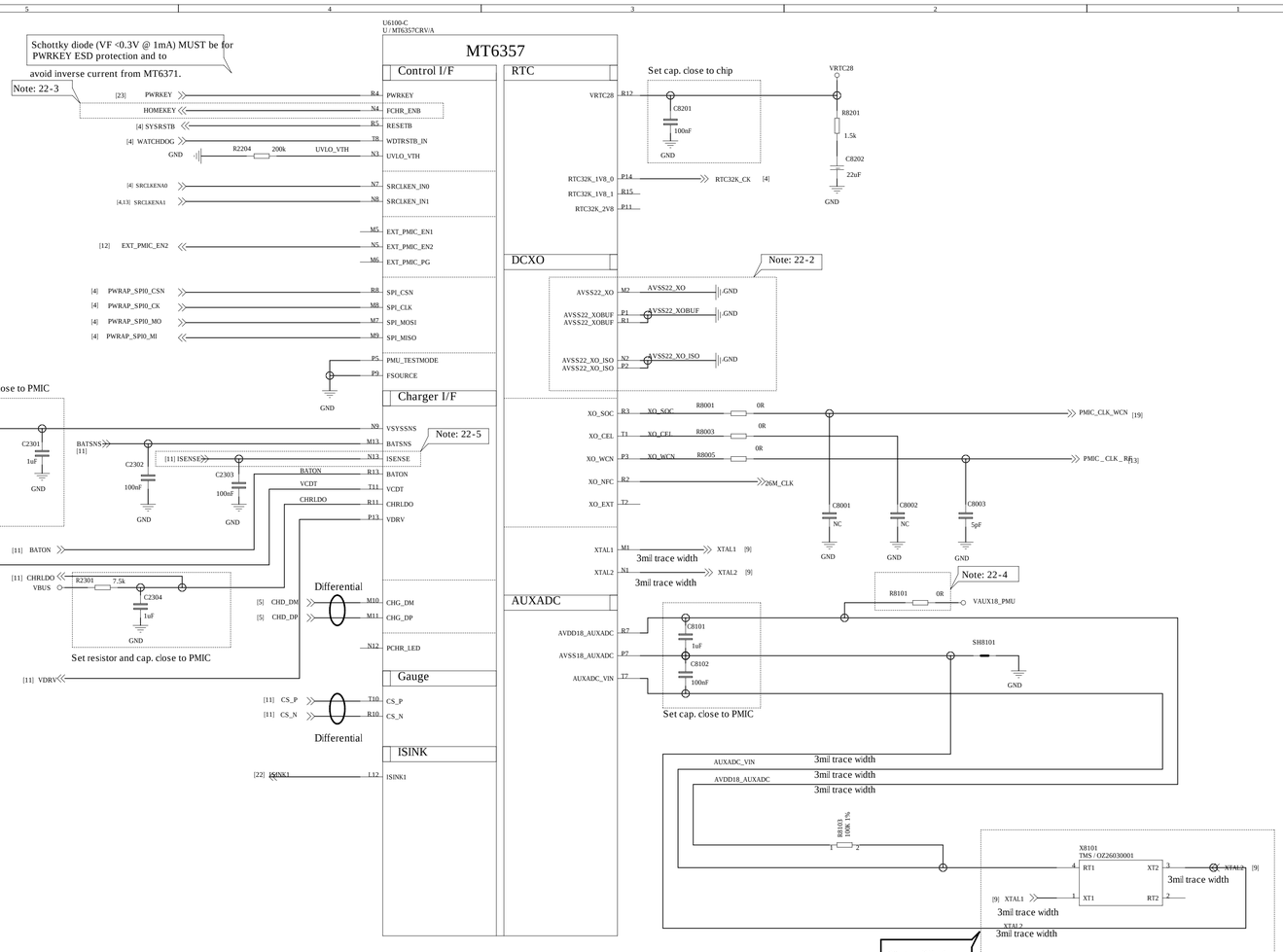
Note 21-5: Please connect VS2_LDO1(F15) to VS1_PMU if voltage applied to VCAMD(E17) >= 1.3 V

Title: 7 _ POWER _ MT6357-LDO

Size: A1

MTK Confidential

Date: Friday, December 08, 2017 Sheet 8 of 25



Schematic design notice of "22_POWER_MT6357-IF"	
Note 22-1:	Please implement 2520 & 2016 Size TMS PCB co-layout.
Note 22-2:	Please refer to MT6765_MT6357 Co-Clock Design Notice for co-layout guide 1. Please Connect P1 and R1 ball first and then to GND 2. Please Connect P2 and N2 ball first and then to GND 3. Please connect DCXO GND to main GND by independent L1-2 GND via.; DO NOT connect it through L1 GND
Note 22-3:	Let floating if disable HOMEKEY function
Note 22-4:	Please follow MT6765_MT6357 Co-Clock Design Notice for Layout guide of VAUX18, then R8101 can use 0 ohm to replace BEAD.
Note 22-5:	Please connect to battery connector

Title	8 _ POWER _ MT6357-IF
Size: A1	MTK Confidential
Date: Friday, December 08, 2017	Sheet 9 of 25

U6100-D
U / MT6357CRV/A

MT6357

AUDIO IF

[4]	AUD_CLK_MISO	R16	AUD_CLK_MISO
[4]	AUD_DAT_MISO0	T17	AUD_DAT_MISO0
[4]	AUD_DAT_MISO1	R17	AUD_DAT_MISO1
[4]	AUD_SYNC_MISO	T16	AUD_SYNC_MISO
[4]	AUD_CLK_MOSI	P16	AUD_CLK_MOSI
[4]	AUD_DAT_MOSI0	P15	AUD_DAT_MOSI0
[4]	AUD_DAT_MOSI1	N14	AUD_DAT_MOSI1
[4]	AUD_SYNC_MOSI	M14	AUD_SYNC_MOSI

AUDIO INPUT

P-N pair should be differential pair & shielded with GND

[21]	AU_VIN0_P	K3	AU_VIN0_P
[21]	AU_VIN0_N	K4	AU_VIN0_N
[20]	AU_VIN1_P	K5	AU_VIN1_P
[20]	AU_VIN1_N	L5	AU_VIN1_N

P-N pair should be differential pair & shielded with GND

		J4	AU_VIN2_P
		J5	AU_VIN2_N

P-N pair should be differential pair & shielded with GND

ACCDET

[20]	ACCDET	M4	ACCDET
[20]	HP_EINT	J1	HP_EINT

- AU_HPL and AU_HPR should be routed as single end signal, and be guarded by GND, up and down, left and right respectively
- The suggested layout pattern of AU_HPL/ AU_HPR/ AU_REFN is " GND AU_HPL AU_REFN AU_HPR GND"

AUDIO OUTPUT

[20]	AU_HPL	J2	AU_HPL
[20]	AU_REFN	H3	AU_REFN
[20]	AU_HPR	G3	AU_HPR
[21]	AU_LOLP	E4	AU_LOLP
[21]	AU_LOLN	F3	AU_LOLN
[21]	AU_HSP	G6	AU_HSP
[21]	AU_HSN	G5	AU_HSN

C6107 1N8 GND

Set cap. close to PMIC

P-N pair should be differential pair & shielded with GND

P-N pair should be differential pair & shielded with GND

UL POWER

AVDD28_AUD	K1		VAUD28_PMU
AVSS28_AUD	H5	[20] AVSS28_AUD	
AU_MICBIAS0	L3		AU_MICBIAS0 [21]
AU_MICBIAS1	M3		AU_MICBIAS1 [20]

C6101 1uF
C6102 1uF
C6103 1uF
SH6100
GND

Set cap. and shortpad close to PMIC

CHARGE PUMP

AVDD18_AUD	G2		VIO18_PMU
AVSS18_AUD	F2	GND	
AU_V18N	D1	AU_V18N	
FLYP	F1	FLYP	
FLYN	E2	FLYN	

C6104 2.2uF
C6105 4.7uF
C6106 4.7uF
GND

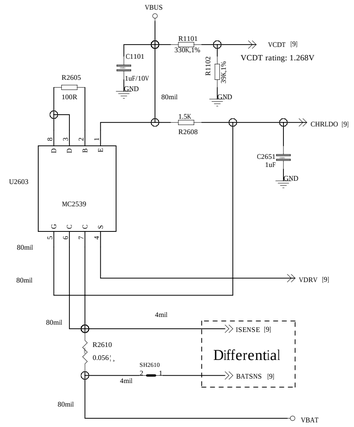
Set cap. close to PMIC

1. AVSS18_AUD is connected to GND in very short trace

2. AVSS18_AUD is connected to de-couple cap of AVDD18_AUD and AU_V18N with 6mil trace respectively

Title	9 _ POWER _ MT6357-Audio
Size	A1
	MTK Confidential
Date:	Friday, December 08, 2017 Sheet 10 of 25

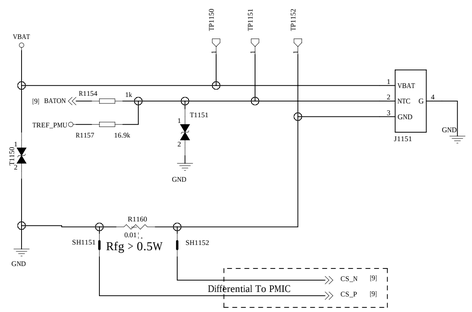
Charger

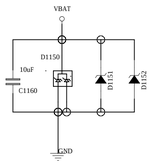


Close To Bat Connector
Care about thermal

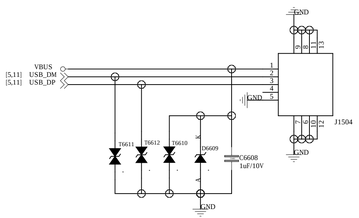
BATTERY

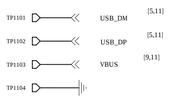
CONNECTOR



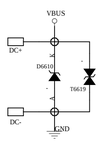


USB





Pedestal

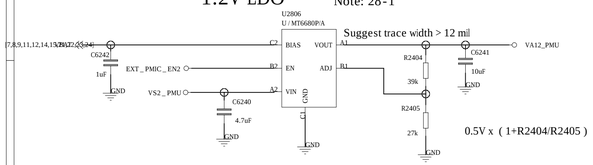


Title	11 _ POWER _ SubPMIC-Charger
Size A1	MTK Confidential
Date: Friday, December 08, 2017	Sheet 11 of 25

LDO for VA12

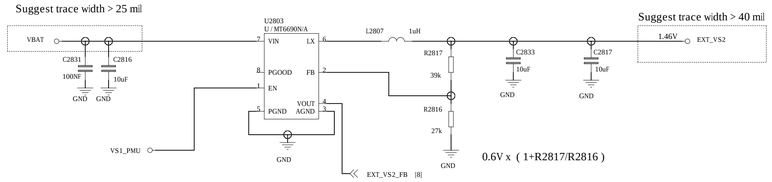
1.2V LDO

Note: 28-1



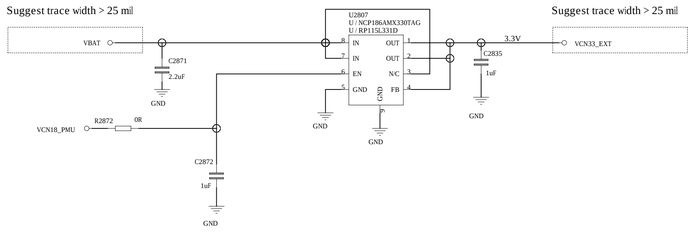
Ext. Bulk for VS2

Note: 28-2



LDO for VCN33

Note: 28-3



Schematic design notice of "28_POWER_ThirdParty-Power"

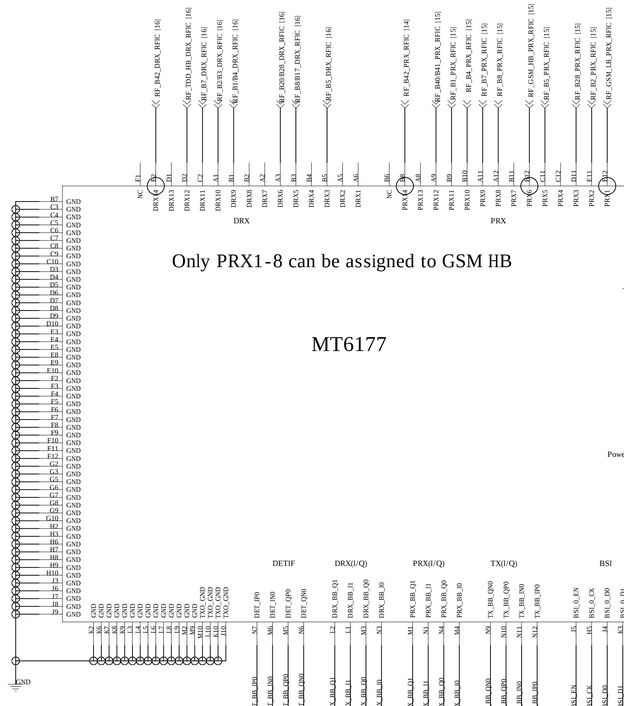
Note 28-1:	VA12 Layout placement please close to AP
Note 28-2:	VS2 Buck Layout placement please close to PMIC MT6357
Note 28-3:	VCN33 LDO Layout placement please close to MT6631
Note 28-4:	1.MT6691OOP/A Buck Layout Placement please close to LP4X/LP4 2.MT6691ZXP/A Buck Layout Placement please close to LP4X 3.If DRAM Application is LPDDR4 , MT6691ZXP/A NC
Note 28-5:	U2810 LDO Layout Placement Please close to LPDDR4X/LPDDR4 VDD1 power ball
Note 28-6:	For EMI_VDD2_FB and EMI_VDDQ_FB, please follow MMD rule

Title: 13 _ POWER _ ThirdParty _ Powers

Size: A1 — MTK Confidential

Date: Friday, December 08, 2017 Sheet 12 of 25

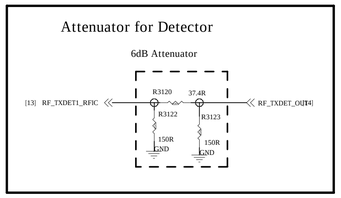
PRX/DRX1~8:LMB:600M~2.025G
PRX/DRX9~12:MHB:1.805M~2.69G



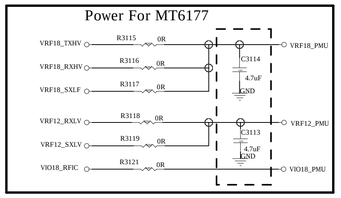
Only PRX1-8 can be assigned to GSM HB

MT6177

Attenuator for Detector

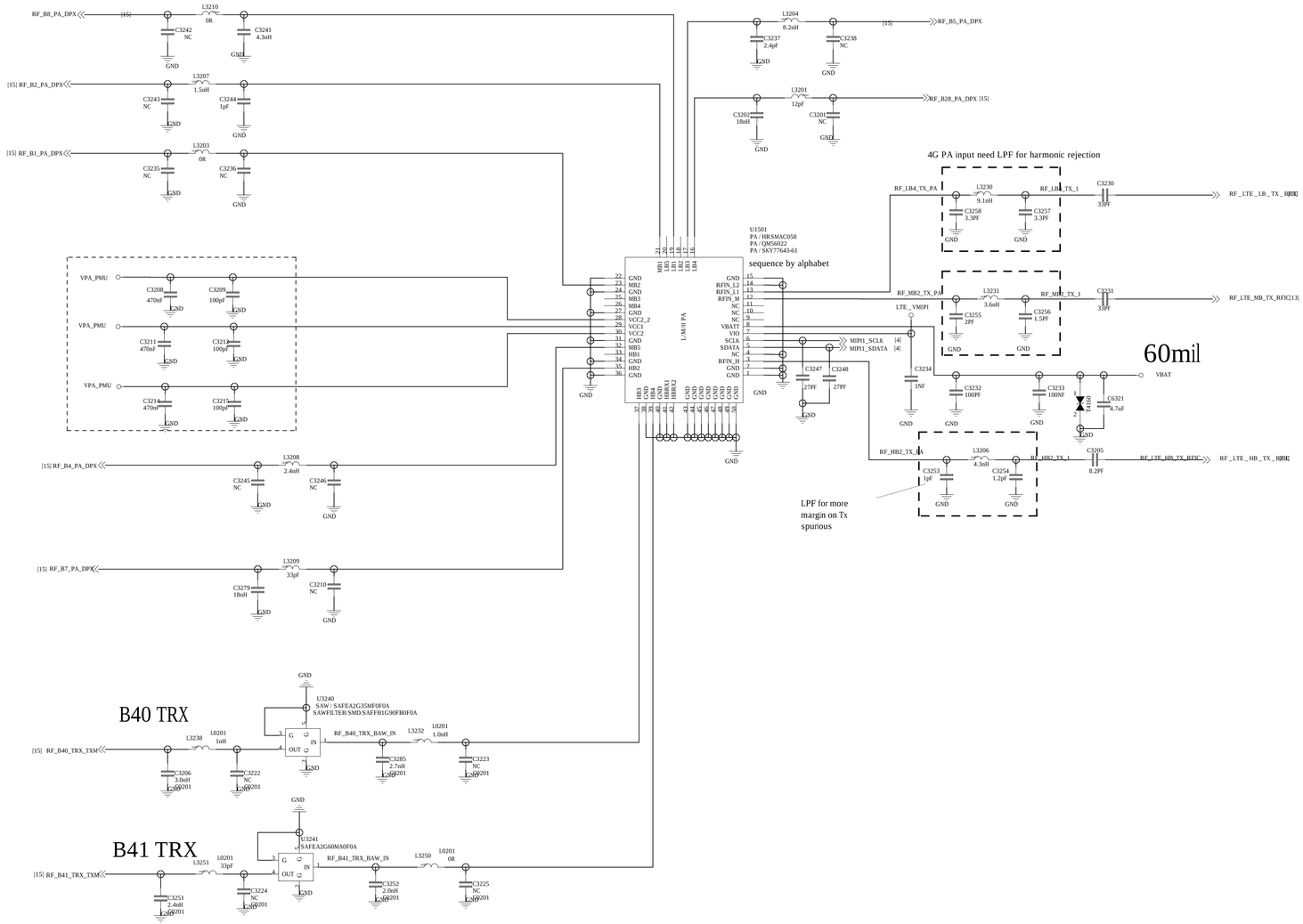


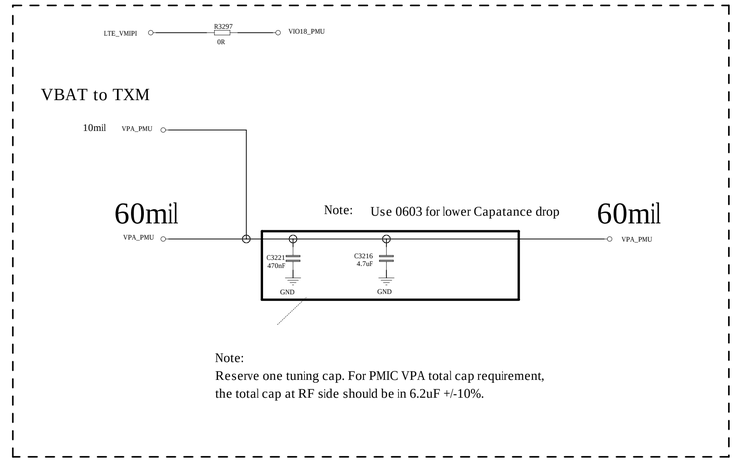
Power For MT6177

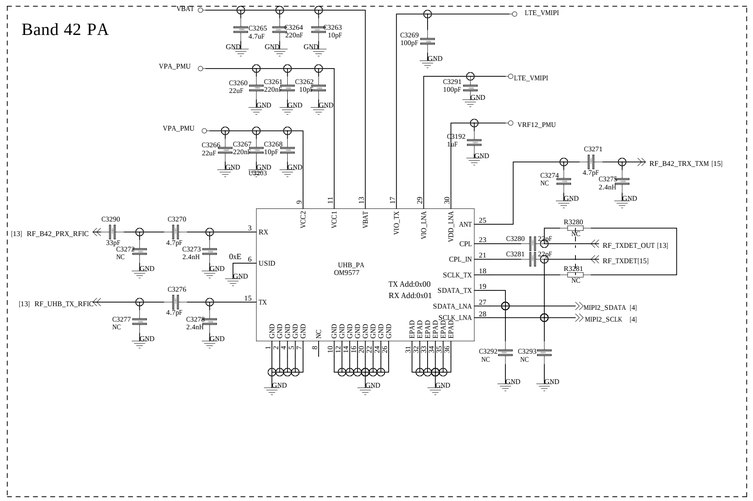


4.7uF close to RFIC

Title	31_RF_MT6177_Pin_Out
Size A1	MTK Confidential
Date: Friday, November 09, 2018	Sheet 13 of 25

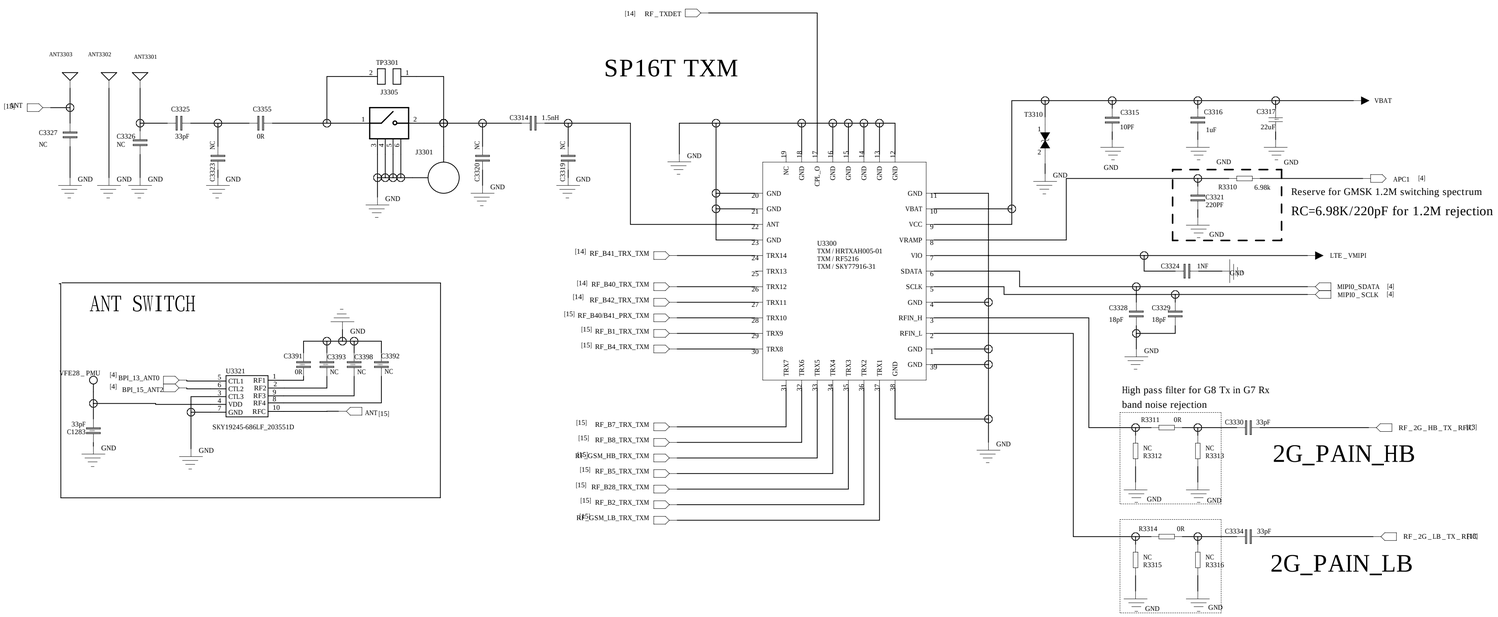






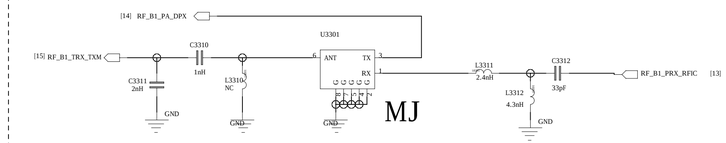
Title	15 _ RF _ MT6177M _ RF _ TX		
Size A1	MTK Confidential		
Date:	Monday, August 14, 2017	Sheet 14 of 25	

Main ANT



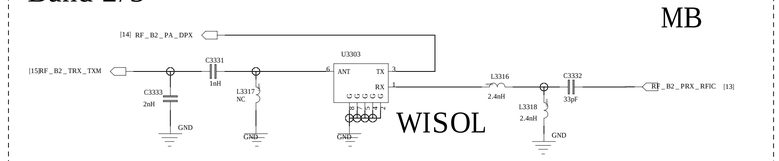
Band 1

MB



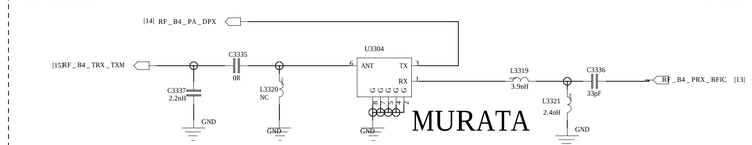
Band 2/3

MB



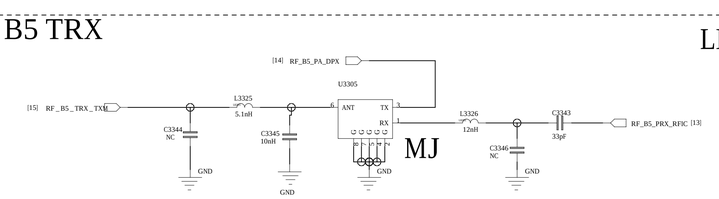
Band 4

MB



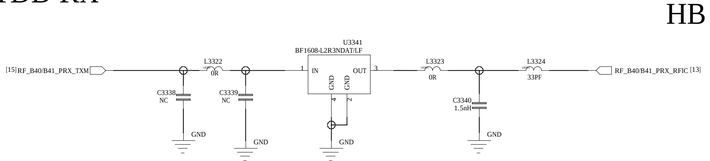
B5 TRX

LB

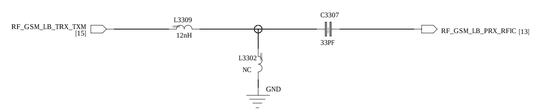


TDD RX

HB

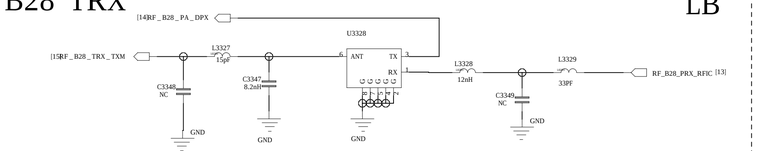


GSM LB RX



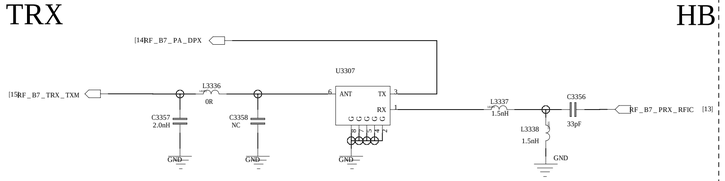
B28 TRX

LB

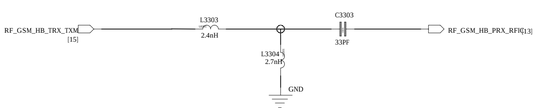


B7 TRX

HB

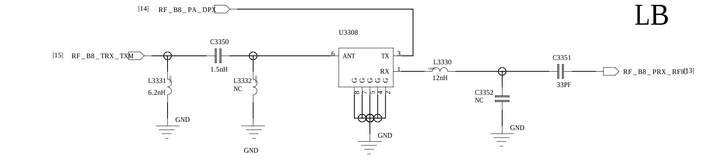


GSM HB RX

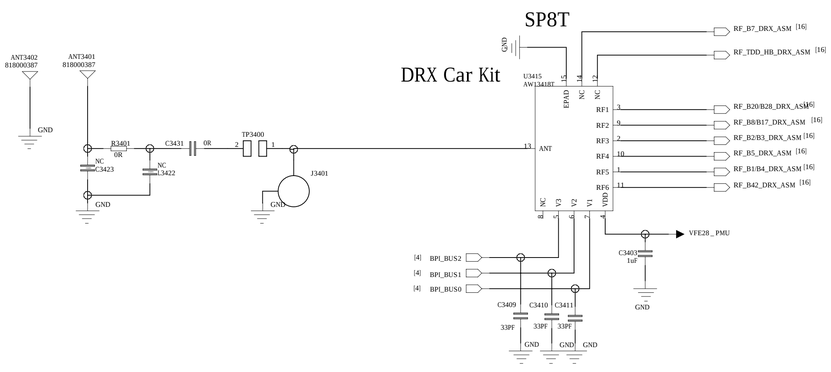


B8 TRX

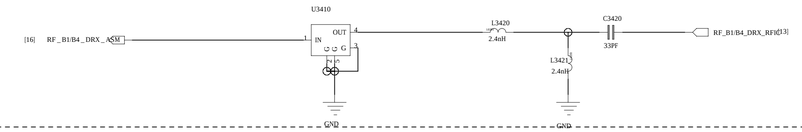
LB



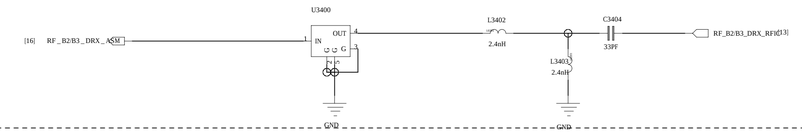
DRX Antenna



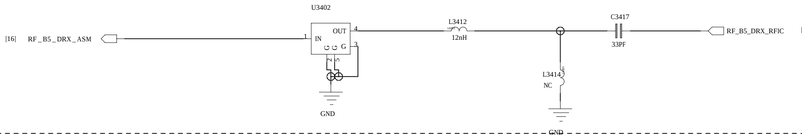
Band 1/4



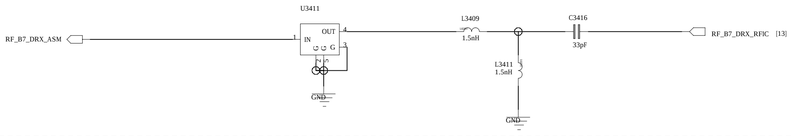
Band 2/3



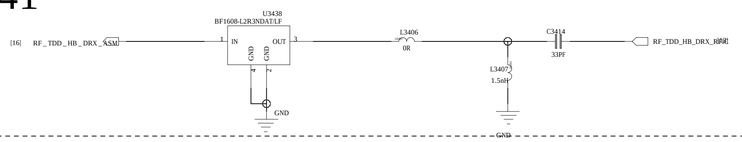
Band 5



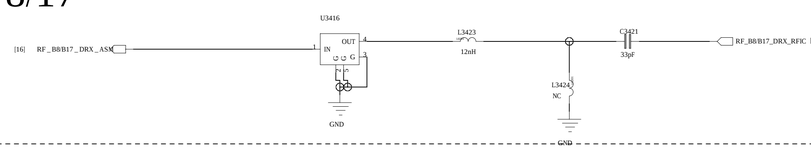
Band 7



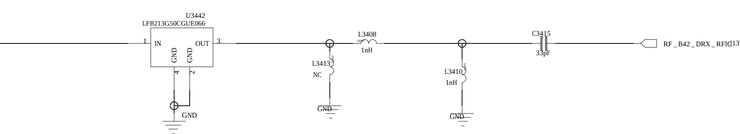
Band 40/41



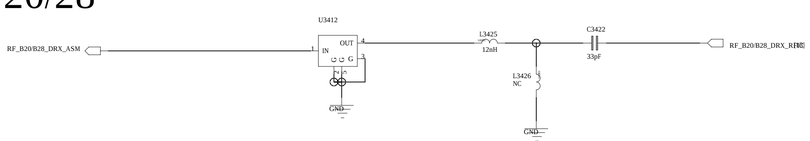
Band 8/17



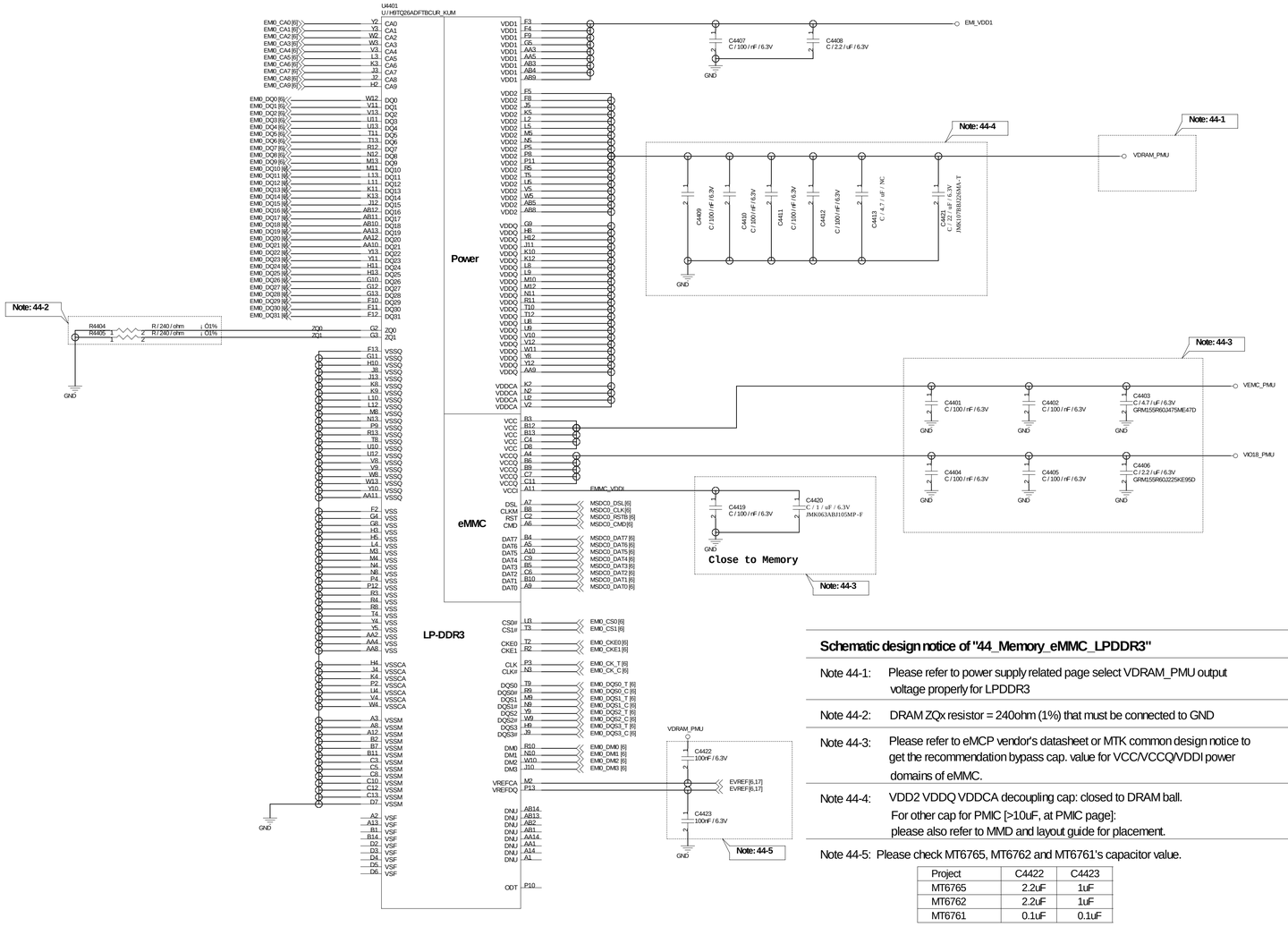
Band 42



Band 20/28



Title	17 _ RF _ MT6177M _ RF _ DRX
Size A1	MTK Confidential
Date: Monday, August 14, 2017	Sheet 16 of 25



Schematic design notice of "44_Memory_eMMC_LPDDR3"

Note 44-1: Please refer to power supply related page select VDRAM_PMU output voltage properly for LPDDR3

Note 44-2: DRAM ZQx resistor = 240ohm (1%) that must be connected to GND

Note 44-3: Please refer to eMCP vendor's datasheet or MTK common design notice to get the recommendation bypass cap. value for VCC/VCCQ/VDDI power domains of eMMC.

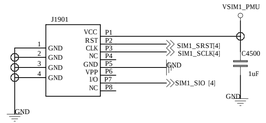
Note 44-4: VDD2 VDDQ VDDCA decoupling cap: closed to DRAM ball.
For other cap for PMIC [>10uF, at PMIC page]:
please also refer to MMD and layout guide for placement.

Note 44-5: Please check MT6765, MT6762 and MT6761's capacitor value.

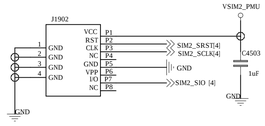
Project	C4422	C4423
MT6765	2.2uF	1uF
MT6762	2.2uF	1uF
MT6761	0.1uF	0.1uF

Title	44_Memory_eMMC_LPDDR3
Size A1	MTK Confidential
Date: Wednesday, November 07, 2018	Sheet 17 of 25

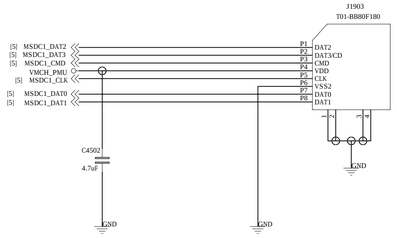
NANO _ SIM1



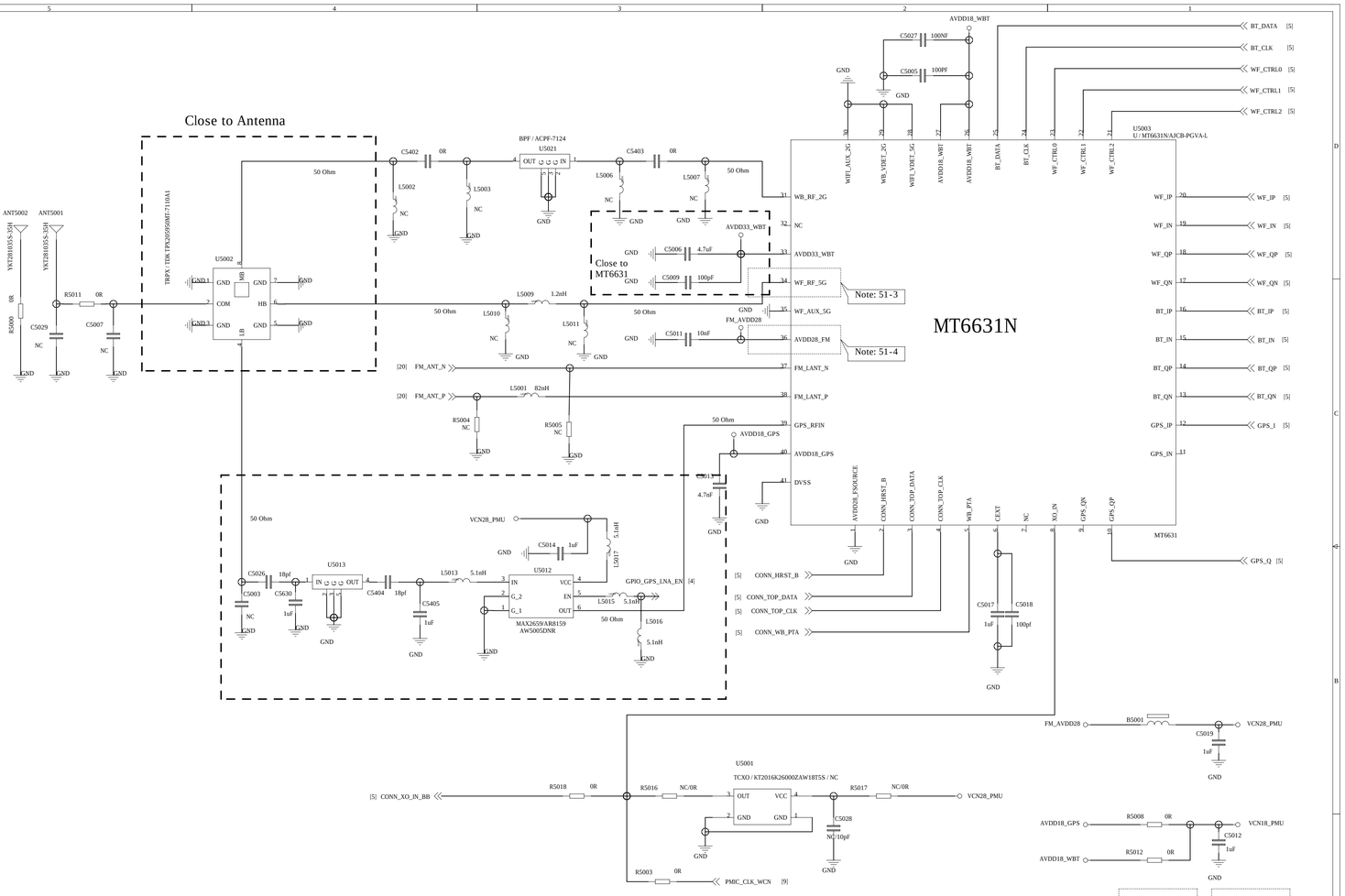
NANO _ SIM2



T _ Card



Title	19 _ SIM _ SD Card _ LED
Size: A1	MTK Confidential
Date: Friday, December 08, 2017	Sheet 18 of 25



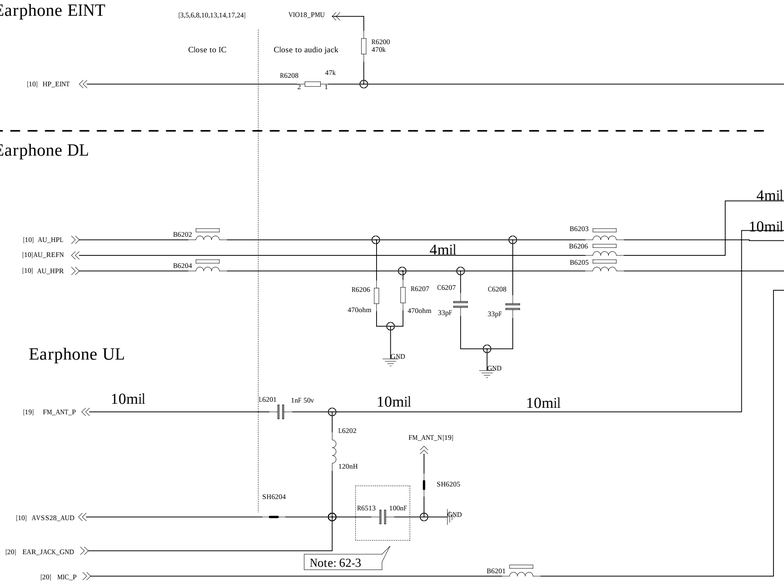
PMIC R5016/R5017 NC, R5003/R8005 0ohm
TCXO R5016/R5017 0ohm, R5003/R8005 NC

Schematic design notice of "51_CONNECTIVITY_CONSYS_MT6631"	
Note 51-1:	For R5015 size, please select 0402 size or larger one
Note 51-2:	Please refer to MT6765 Baseband design notice for VCN33 LDO selection guide
Note 51-3:	If WiFi 5G not support, connect pin 34(WF_RF_5G) to GND
Note 51-4:	Pin 36 (AVDD28_FM) must be connected to VCN28 even if FM not support

Title	20 _ CONNECTIVITY _ CONSYS _ MT6631
Size: A1	MTK Confidential
Date:	Friday, December 08, 2017 Sheet 19 of 25

Earphone Audio

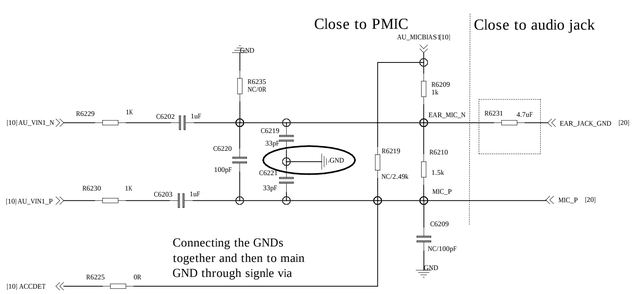
Earphone EINT



Earphone DL

Earphone UL

Earphone Microphone

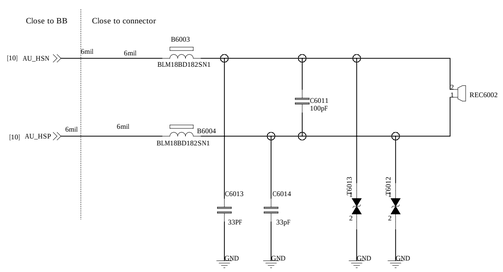


Note 62-3:

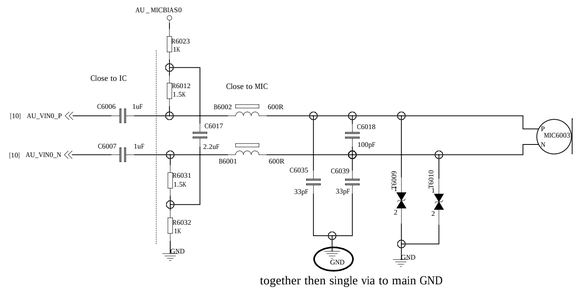
	Earphone Jack @ Main board	Earphone Jack @ Sub board
R6513	0 ohm	100nF

Title	21 _ EARPHONE
Size: A1	MTK Confidential
Date:	Friday, December 08, 2017 Sheet 20 of 25

Receiver

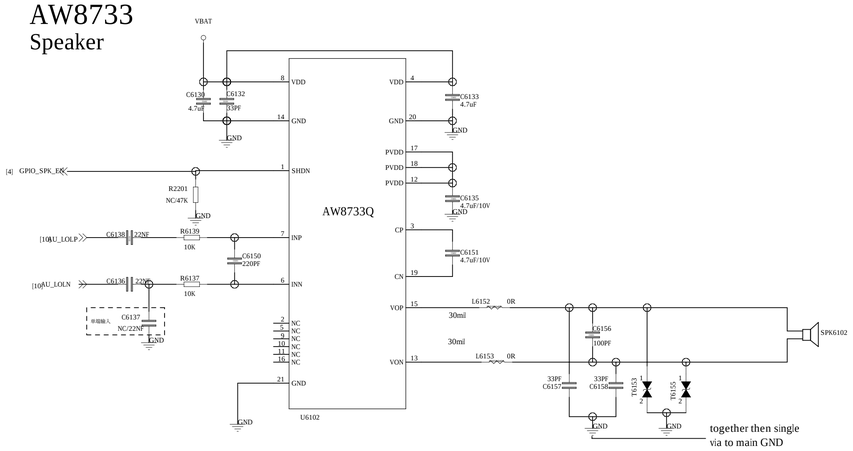


Microphone



together then single via to main GND

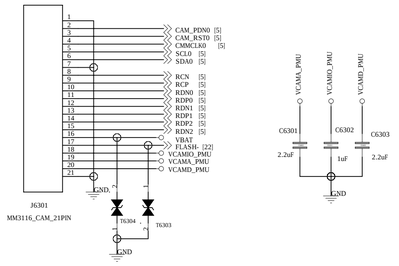
AW8733
Speaker



together then single via to main GND

Title	22 _ MIC _ AUDIO _ VIBR
Size: A1	MTK Confidential
Date: Friday, December 08, 2017	Sheet 21 of 25

Rear and Front Camera



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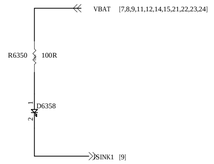
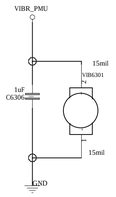
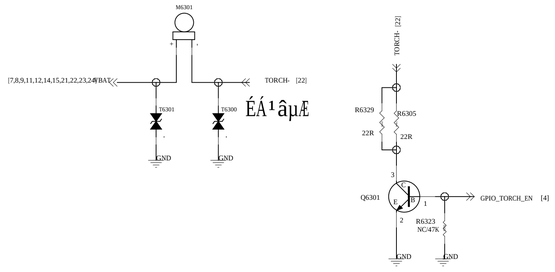
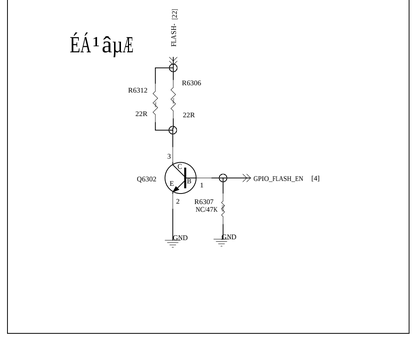


VIBRATOR



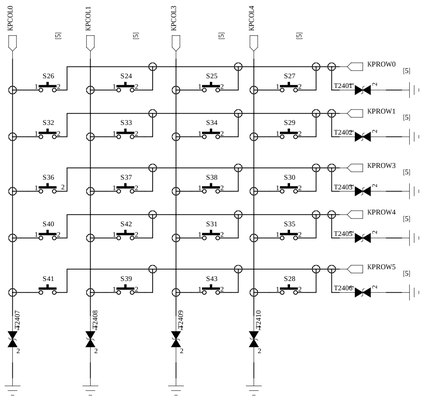




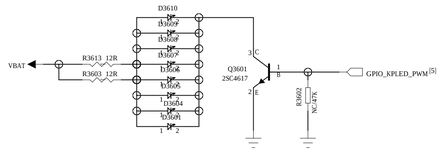
Title	63_PERI_CAMERA
Size: A1	MTK Confidential
Date: Wednesday, November 28, 2018	Sheet 22 of 25

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

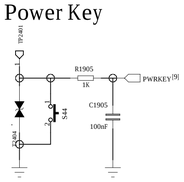
KEYPAD



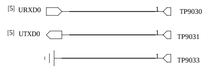
KEYPAD LED



Power Key



Debug

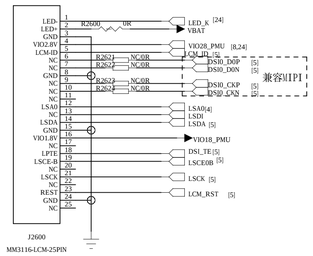


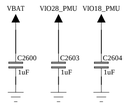
Hole

DRAWN: <Drawn By>	DATED: <Drawn Date>	COMPANY: <Company Name>			
CHECKED: <Checked By>	DATED: <Checked Date>	TITLE: <Title>			
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE: <Code>	SIZE: A1	DRAWING NO: <Drawing Number>	REV: <Revision>
RELEASED: <Released By>	DATED: <Release Date>	SCALE: <Scale>		SHEET: 23 25	

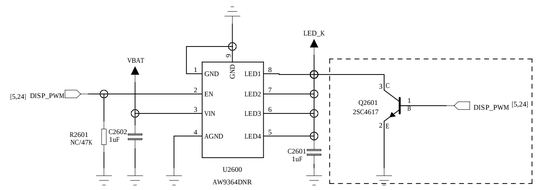
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

SPI Display





BackLight



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