FCC ID: O3U-98231

Technical Description :

The brief circuit description is listed as follows :
- Antenna acts as Loop Antenna.
- U201 HL5233 acts as RFID Reader.
- X201 and associated circuit act as 13.56 MHz Oscillator.
- U101 RSC-4128 acts as MCU and Speech Recognition Processor.
- U102 S29AL016D acts as Flash Memory.
- PB104 acts as Reset Button.
- U4 GPY0030A and associated circuit act as Audio Amplifier.
- U1 74HC374 acts as 3-State Octal D-Type Flip Flop.
- Q302 – Q307 and associated circuit act as Motor 1 Driver.
- Q302-2 – Q307-2 and associated circuit act as Motor 2 Driver.
- Q302-3 – Q307-3 and associated circuit act as Motor 3 Driver.
- U103 74HC08 acts as Logic Gate.
- Disc 0, 1 and 2 act as Eyes, mouth, neck, tail and legs location detect key.
- U105 AT24C04N acts as EEPROM.
- RP1 and associated circuit act as Resistor Port.
- PB1, SW2, SW3 and SW4 act as Control Keys.
- D4, Q2, Q3 and associated circuit act as Low Voltage Detector.
- U2 and associated circuit act as Voltage Regulator.

Antenna Used :

An integral loop antenna has been used.

Features

- Low standby current.
- Low power consumption.
- Simple application circuit.
- Stable performance.
- The system and oscillator can be enable separately.
- 3 kinds of decoder outputs.
- Level hold mode and one-shot trigger mode.
- High active and low active output selectable.

<Patent : US6731177B2>

Applications

- Toy RFID.
- Asset control.
- Contactless entry control.
- Education.

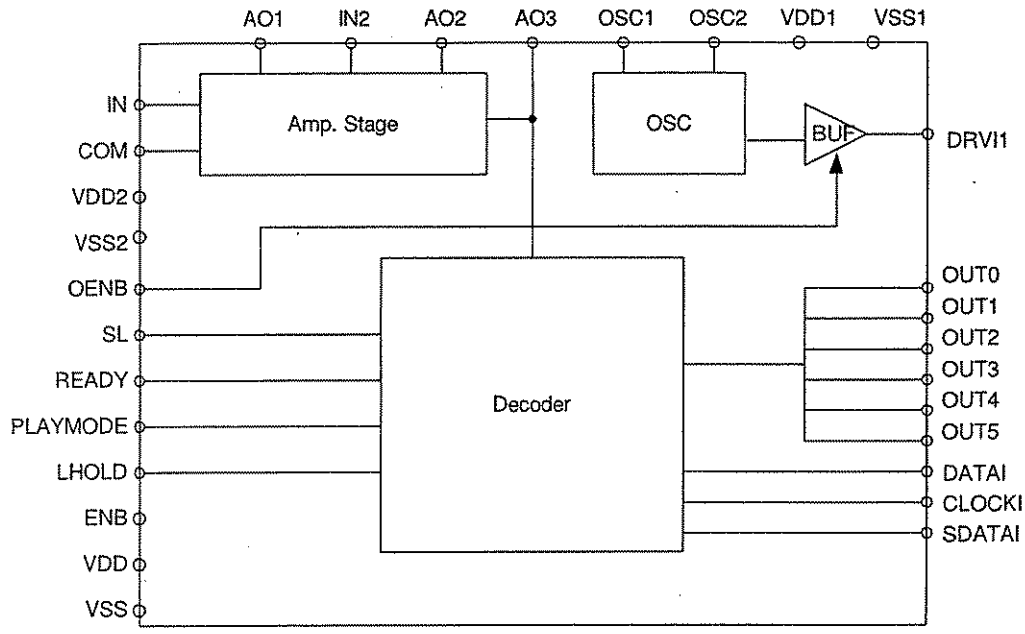
General Description

HL5233 is a CMOS IC used to perform the function of a RFID Reader. A RFID contains two parts: RFID TAG (HL5230) and RFID Reader (HL5233). HL5233 contains of a 13.56MHz crystal oscillator, a 13.56MHz output buffer, a preamplifier and data decoder. The output buffer drives an antenna which can transmits RF signal to the RFID TAG.

If TAG is close enough to the Reader, the encoder of TAG will send out a data train. The data train is used to modulate the RF signal in the TAG, and the amplitude of RF signal in the Reader will be modulated also. Preamplifier is used to amplify the modulating signal. The decoder is used to decoder the encoded data transmitted from TAG.

There are three kinds of output data: Synchronous, Asynchronous and Direct drive outputs. In order to interface to most of power Speech IC, the data rate of the outputs is slower than the data rate of the RFID TAG.

Block Diagram



Absolute Maximum Ratings

Power Supply 5V
Input Voltage ..... VSS-0.3V to VDD+0.3V
Operating Temperature ..... 0 °C to 60 °C
Storage Temperature ..... -65 °C to 125°C

Electrical Characteristics

SYSTEM	DESCRIPTION	TEST CONDITION	LIMIT			UNIT
			MIN.	TYP.	MAX.	
VDD	Supply Voltage		3	4.5	5	V
VIL	Input Voltage Low	VDD=4.5V			0.3*VDD	V
VIH	Input Voltage High	VDD=4.5V	0.7*VDD			V
VOSC	Oscillator Starting Voltage			2.2		V
IOP1	Operating Current 1	VDD=4.5V		19*		mA
IOP2	Operating Current 2 (Driver Off)	VDD=4.5V		0.4		mA
IST	Stand-by Current	VDD=4.5V		0.5		uA

* IOP depends on external coil.

Functional Description

There are three major function provided by HL5233: support a 13.56MHz driver, to transform DATA Bit rate for easy interface with MCU or power Speech IC and to provide direct decoder output.

After received the modulating signal from the RFID TAG, the modulating signal is amplified and filtered by preamplifier. There is decoder and error detector built in the HL5233. The decoded output can be sent to output pin directly, or encoded again at a slower bit rate. When PLAYMODE = 1, there are 8 direct output provided. Besides the 3 bits which is used as decoder inputs, there is 1 bit, which is used as parity check bit. The output will be activated only when parity is correct. In HL5233 even parity is used, Bit0~Bit2 is used as decoder input and Bit7 is parity Bit.

OENB is coil driver enable pin. When OENB=0, coil driver is off, while others circuit still work.

SENSORY®

RSC-4128
Speech Recognition Processor

Data Sheet

General Description

The RSC-4128 represents Sensory's next generation speech and analog I/O mixed signal processor. The RSC-4128 is designed to bring advanced speech I/O features to cost sensitive embedded and consumer products. Based on an 8-bit microcontroller, the RSC-4128 integrates speech-optimized digital and analog processing blocks into a single chip solution capable of accurate speech recognition; high quality, low data-rate compressed speech; and advanced music. Products can use one or all features in a single application.

The RSC-4128 supports Sensory Speech™ 7 technology, which includes advanced speech algorithms that add features and improve performance. Capable of running both new HMM and enhanced neural network technologies, accuracy in all kinds of noise is dramatically improved. New Speaker Verification technology is perfect for voice password security applications that must work in noisy environments. New high quality compressed speech technology reduces data rates by 5 times. New 8 voice MIDI-compatible music includes drum tracks, effectively increasing instruments beyond 8. Simultaneous music and speech rounds out the Sensory Speech™ 7 technology.

The RSC-4128 also supports the revolutionary capability of creating speaker independent recognition sets by simply typing in the desired recognition vocabulary! A few keystrokes creates a recognition set in seconds without the wait or cost of recording sessions to train the recognizer, speeding time to sales.

A new and unique Audio Wakeup feature listens while the RSC-4128 is in power down mode. When an audio event such as a clap or whistle occurs, Audio Wakeup will wakeup the RSC-4128 for speech or application tasks. Audio Wakeup is perfect for battery applications that require continuous listening and long battery life.

In addition to improved recognition performance, the RSC-4128 provides further on-chip integration of features. A complete speech I/O application can be built with as few additional parts as a clock crystal, speaker, microphone, and few resistors and capacitors.

Moreover, the RSC-4128 provides an unprecedented level of cost effective system-on-chip (SOC) integration, enabling many applications that require DSP and/or audio processing. The RSC-4128 may be used as a general-purpose mixed signal processor platform for custom algorithms, technologies and applications.

Features

Full Range of Sensory Speech™ 7 Capabilities

- Enhanced Word Spotting capability (10 SI or 4 SD words) in parallel
- Noise robust Speaker Independent, Dependent & Continuous Listening recognition
- Speaker Verification (SVWS) – Noise robust voice biometric security
- High quality, 3.7-7.8 kbps speech synthesis & sound effects with Sensory "SX" synthesis technology
- 8 voice MIDI-compatible music synthesis coincident with speech; drum track feature enables additional voices
- Voice record & playback
- Audio Wakeup from sleep

Integrated Single-Chip Solution

- 8-bit microcontroller
- ROMless, 128KByte and 256KByte ROM options
- 16 bit ADC, 10 bit DAC and microphone pre-amplifier
- Independent, programmable Digital Filter engine
- 4.8 KBytes total RAM (256Bytes "user" application RAM)
- Five timers (3 GP, 1 Watchdog, 1 Multi Tasking)
- Twin-DMA, Vector Math accelerator, and Multiplier
- Built-in Analog Comparator Unit (4 inputs)
- External memory bus: 20-bit Address(1Mbyte), 8-bit Data
- On chip storage for SD, SV, templates (10 templates)
- Code security through no ROM dump capability
- Uses low cost 3.58MHz crystal (internal PLL)
- Low EMI design for FCC and CE requirements
- 24 configurable I/O lines with 10 mA (typical) outputs
- Fully nested interrupt structure with up to 8 sources
- Optional Real Time Clock

Long Battery Life

- 2.4 – 3.6V operation
- 12mA (typical) operating current at 3V
- 2 low power modes; 1 µA typical sleep current

Full Suite of Quick & Powerful Tools

- Quick Text-to-SI (T2SI) text entry to build noise robust SI recognition sets – low cost & push-button – no recording!
- Quick Synthesis for push-button speech compression
- Integrated Development Environment, C Compiler, Debugger & In Circuit Emulator from Phyton, Inc.

RSC-4128 Overview

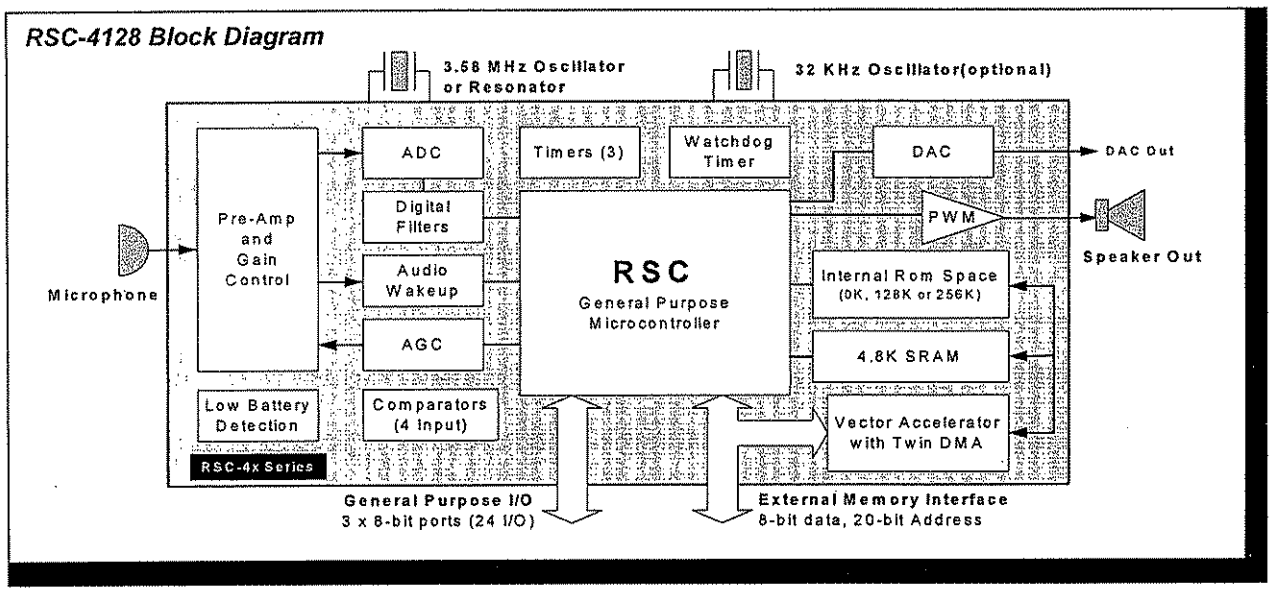
The RSC-4128 is a member of the Interactive Speech™ line of products from Sensory. It features a high-performance 8-bit microcontroller with on-chip ADC, DAC, preamplifier, RAM, ROM (except on ROM-less version), and optimized audio processing blocks. The RSC-4128 is designed to bring a high degree of integration and versatility into low-cost, power-sensitive applications. Various functional units have been integrated onto the CPU core in order to reduce total system cost and increase system reliability.

The RSC-4128 operates in tandem with Sensory Speech™ 7 firmware, an ultra compact suite of recognition and synthesis technologies. This reduced software footprint enables, for example, products with over 150 seconds of compressed speech, multiple speaker dependent and independent vocabularies, speaker verification, and all application code built into the RSC-4128 as a single chip solution. Revolutionary Text-to-Speaker-Independent (T2SI) technology allows the creation of SI recognition sets by simply entering text.

The CPU core embedded in the RSC-4128 is an 8-bit, variable-length-instruction microcontroller. The instruction set is similar to the 8051 microcontroller, and has a variety of addressing mode, *MOV* and 16 bit instructions. The RSC-4128 processor avoids the limitations of dedicated A, B, and DPTR registers by having completely symmetrical sources and destinations for all instructions.

The RSC-4128 provides a high level of on-chip features and special DSP engines, providing a very cost effective mixed signal platform for general-purpose applications and development of custom algorithms. The full suite of industry standard tools for easy product development makes the RSC-4128 an ideal platform for consumer electronics.

RSC-4128 Block Diagram



Speech Technologies

Speech Recognition

The RSC-4128 is designed to support HMM (Hidden Markov Modeling) as well as Neural Network technologies provided in Sensory Speech™ 7 firmware, to perform speaker independent (SI) speech recognition. Speaker independent recognition requires on-chip or off-chip ROM to store the words to be recognized.

Speaker dependent (SD) recognition requires programmable memory to store personalized speech templates. This programmable memory may be on-chip SRAM or off-chip Serial EEPROM, Flash Memory, or SRAM.

The RSC-4128 has several additional speech recognition features as described below:

- *Speaker Independent* recognition requires no user training. The RSC-4128 can recognize up to 20 words in an active set (number of sets is limited only by internal ROM or external memory size). Text-to-SI (T2SI) recognition, based on HMM technology, allows creation of SI recognition sets in seconds by simply typing in the vocabulary desired, with no costs or delays associated with recording and training the recognizer.
- *Speaker Dependent* recognition allows the user to create names for products or customize vocabularies. Up to 100 words can be recognized in an active set (number of sets is limited only by internal ROM or external memory size). The RSC-4128 can store up to 10 SD words in on-chip SRAM.
- *Continuous Listening* allows the chip to continuously listen for a specific trigger word. With this feature, a product "activates" when a specific word is spoken, framed by quiet before and after. Continuous listening provides the lowest false fire rate for trigger words.
- *Word Spotting* allows the chip to continuously recognize for up to 10 SI or 5 SD words at a time. In word spotting mode, the word(s) to be recognized may be spoken in the middle of speech.

Speaker Verification

The RSC-4128 also supports Sensory's speaker verification (SV) technology – the most successful biometric security on the market. After a speaker trains the chip on a specific word or words, the chip is able to identify whether a particular word is spoken by the original speaker. The RSC-4128 can store up to 10 SV templates on-chip, or more with external programmable memory.

Speech and Music Synthesis

The RSC-4128 provides high-quality speech synthesis using state-of-the-art frequency domain techniques in Sensory's new "SX" synthesis technology. Typical data rates for SX are approximately 6000 bits per second. One may select various data rates from approximately 3.7 to 7.8Kbps to manage speech quality versus allotted memory.

Speech, music and sound effects may also be produced using the RSC-4128 8 bit, 58Kbps or 4 bit, 30Kbps compression technologies.

The RSC-4128 provides high-quality, eight-voice, wave table music synthesis which allows multiple, simultaneous instruments for harmonizing. The RSC-4128 uses a MIDI-like system to generate music. One or more of the eight voices may be speech playback instead of music. One or more of the eight voices may be a drum track comprising multiple drums. In effect, this allows the number of simultaneous instruments to exceed 8.

Speech and music synthesis requires on-chip or off-chip ROM to store data for synthesis playback. Easy to use tools allow the developer to record and compress their own voice talents and create with the push of a button, or to create their own MIDI scores and instruments.

Record and Playback

The RSC-4128 can perform speech record and playback (sometimes called "voice memo") at various compression levels depending on the quantity and quality of playback desired. Data rates less than 14,000 bits per second are achievable while maintaining very high quality reproduction. The record and playback technology also performs silence removal to improve sound quality and reduce memory requirements.

RSC-4128 Architecture

The RSC-4128 is a highly integrated speech and analog I/O mixed signal processor that combines:

- 8-bit microcontroller with enhanced instructions and interrupt control, superior register architecture, independent Digital Filter engine and "L1" Vector Math Accelerator
- On-chip ROM and RAM (4.8 Kbytes), and the ability to address off-chip RAM, ROM, EPROM or Flash.
- Input microphone preamp and 16 bit Analog-to-Digital Converter (ADC) for speech and audio/analog input
- 10 bit Digital-to-Analog Converter (DAC), and 10 bit Pulse Width Modulator (PWM) to directly drive a speaker or other analog device
- Low power Audio Wakeup from power down mode, when a selected audio event, such as clap or whistle, occurs

The RSC-4128 has 20-bit address and 8-bit data busses for interfacing with external memory. It includes an -XM input pin capable of enabling or disabling the internal ROM.

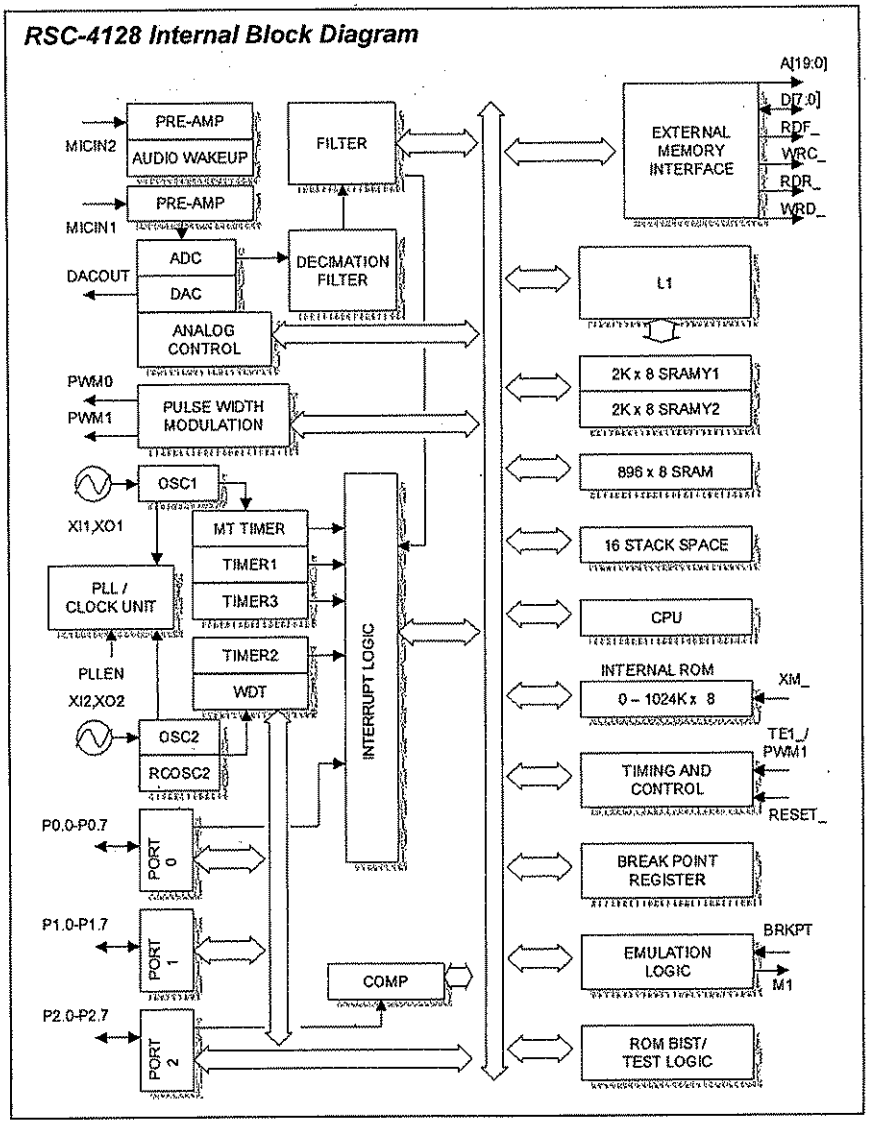
NOTE: Neither the -XM input pin nor the extended memory busses are available on 64-lead LQFP packaged versions of the RSC-4128 with internal ROM. These are available on the die and 100 LQFP versions.

Three bi-directional ports provide 24 configurable, general-purpose I/O pins to communicate with or control external devices with a variety of source and sink currents. Up to 4 of these I/O may be used as programmable Analog Comparator inputs. 16 may be used as I/O wakeup.

The RSC-4128 has a high frequency (14.32 MHz) clock as well as a low frequency (32,768 Hz) clock. The processor clock can be selected from either source, with a selectable divider value. The device performs speech recognition when running at 14.32 MHz. The RSC-4128 also supports programmable wait states to allow the use of slower memory.

OSC1 is a very low-cost 3.58 MHz crystal oscillator which is used by a 4X PLL to generate the 14.32MHz clock. The OSC2 oscillator provides the options of using an external crystal or its own internal RC devices (no external components required for the internal RC mode).

RSC-4128 Internal Block Diagram



There are three programmable, general-purpose 8-bit counters / timers – Timers 1 and 3 are derived from OSC1, and Timer2 from OSC2. There is also a Watchdog timer that may be used to exit an undesired condition in program flow, and Multi-tasking timer to allow chip operations to share resources in parallel.

A single chip speech I/O solution may be created with the RSC-4128. An external microphone passes an audio signal to the preamplifier and ADC to convert the incoming speech signal into digital data. Speech features are extracted using the Digital Filter engine. The microcontroller CPU processes these speech features using speech recognition algorithms in firmware, with the help of the "L1" Vector Accelerator and enhanced instruction set. The resulting speech recognition results may be used to control the consumer product application code, or to output speech or audio in the form of a dialog with the user of the consumer product. If desired, the output speech or audio signal from the RSC-4128 is generated by a DAC for external amplification into a speaker, or a PWM capable of directly driving a speaker at typical consumer product volumes. A typical product will require about $0.30 - $1.00 (in high volume) of additional components, in addition to the RSC-4128.

The RSC-4128 also provides a very cost effective mixed signal platform for general-purpose applications and development of custom algorithms. A typical general purpose application will require about $0.30 - $0.50 (in high volume) of additional components, in addition to the RSC-4128.

S29AL016D

16 Megabit (2 M x 8-Bit/1 M x 16-Bit) CMOS 3.0 Volt-only Boot Sector Flash Memory

Data Sheet

Distinctive Characteristics

Architectural Advantages

- **Single Power Supply Operation**
  - Full voltage range: 2.7 to 3.6 volt read and write operations for battery-powered applications
- **Manufactured on 200 nm Process Technology**
  - Fully compatible with 200 nm Am29LV160D and MBM29LV160E devices
- **Flexible Sector Architecture**
  - One 16 Kbyte, two 8 Kbyte, one 32 Kbyte, and thirty-one 64 Kbyte sectors (byte mode)
  - One 8 Kword, two 4 Kword, one 16 Kword, and thirty-one 32 Kword sectors (word mode)
- **Sector Protection Features**
  - A hardware method of locking a sector to prevent any program or erase operations within that sector
  - Sectors can be locked in-system or via programming equipment
  - Temporary Sector Unprotect feature allows code changes in previously locked sectors
- **Unlock Bypass Program Command**
  - Reduces overall programming time when issuing multiple program command sequences
- **Top or Bottom Boot Block Configurations Available**
- **Compatibility with JEDEC standards**
  - Pinout and software compatible with single-power supply Flash
  - Superior inadvertent write protection

Performance Characteristics

- **High Performance**
  - Access times as fast as 70 ns
  - Extended temperature range (-40°C to +125°C)
- **Ultra Low Power Consumption (typical values at 5 MHz)**
  - 200 nA Automatic Sleep mode current
  - 200 nA standby mode current
  - 9 mA read current
  - 20 mA program/erase current
- **Cycling Endurance: 1,000,000 cycles per sector typical**
- **Data Retention: 20 years typical**

Package Options

- **48-ball FBGA**
- **48-pin TSOP**
- **44-pin SOP**

Software Features

- **CFI (Common Flash Interface) Compliant**
  - Provides device-specific information to the system, allowing host software to easily reconfigure for different Flash devices
- **Erase Suspend/Erase Resume**
  - Suspends an erase operation to read data from, or program data to, a sector that is not being erased, then resumes the erase operation
- **Data# Polling and Toggle Bits**
  - Provides a software method of detecting program or erase operation completion

Hardware Features

- **Ready/Busy# Pin (RY/BY#)**
  - Provides a hardware method of detecting program or erase cycle completion
- **Hardware Reset Pin (RESET#)**
  - Hardware method to reset the device to reading array data

Publication Number S29AL016D_00 **Revision** A **Amendment** 5 **Issue Date** May 22, 2006

General Description

The S29AL016D is a 16 Mbit, 3.0 Volt-only Flash memory organized as 2,097,152 bytes or 1,048,576 words. The device is offered in 48-ball FBGA, and 48-pin TSOP packages. The word-wide data (x16) appears on DQ15–DQ0; the byte-wide (x8) data appears on DQ7–DQ0. This device is designed to be programmed in-system with the standard system 3.0 volt V_{CC} supply. A 12.0 V V_{PP} or 5.0 V_{CC} are not required for write or erase operations. The device can also be programmed in standard EPROM programmers.

The device offers access times of 70 ns and 90 ns allowing high speed microprocessors to operate without wait states. To eliminate bus contention the device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

The device requires only a **single 3.0 volt power supply** for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The S29AL016D is entirely command set compatible with the **JEDEC single-power-supply Flash standard**. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-machine that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other Flash or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the **Embedded Program** algorithm—an internal algorithm that automatically times the program pulse widths and verifies proper cell margin. The **Unlock Bypass** mode facilitates faster programming times by requiring only two write cycles to program data instead of four.

Device erasure occurs by executing the erase command sequence. This initiates the **Embedded Erase** algorithm—an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by observing the RY/BY# pin, or by reading the DQ7 (Data# Polling) and DQ6 (toggle) **status bits**. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The **hardware sector protection** feature disables both program and erase operations in any combination of the sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend/Erase Resume** feature enables the user to put erase on hold for any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The **hardware RESET# pin** terminates any operation in progress and resets the internal state machine to reading array data. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read the boot-up firmware from the Flash memory.

The device offers two power-saving features. When addresses have been stable for a specified amount of time, the device enters the **automatic sleep mode**. The system can also place the device into the **standby mode**. Power consumption is greatly reduced in both these modes.

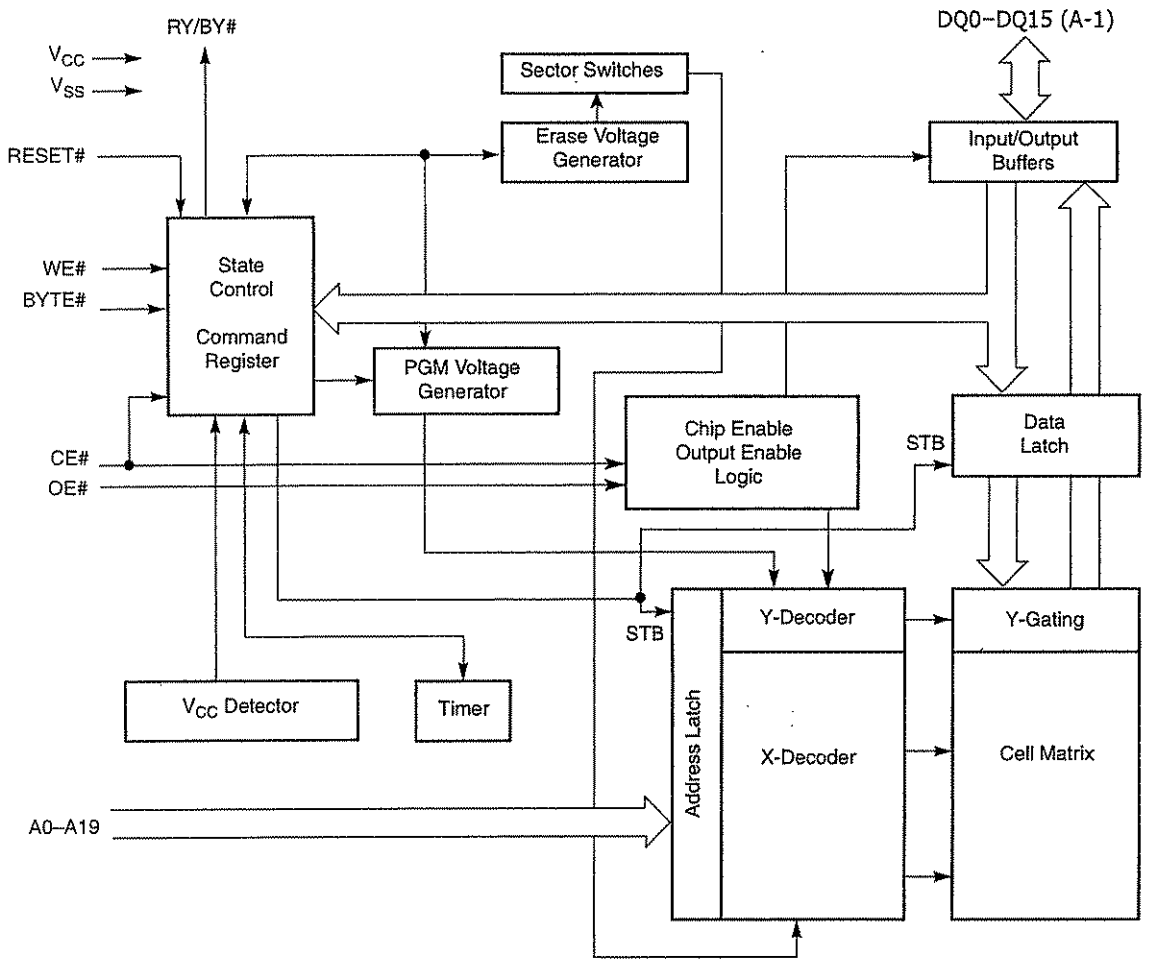
Spansion's Flash technology combines years of Flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via Fowler-Nordheim tunneling. The data is programmed using hot electron injection.

1. Product Selector Guide

Family Part Number		S29AL016D	
Speed Option	Voltage Range: V_{CC} = 2.7–3.6 V	70	90
Max access time, ns (t_{ACC})		70	90
Max CE# access time, ns (t_{CE})		70	90
Max OE# access time, ns (t_{OE})		30	35

Note
See AC Characteristics on page 37 for full specifications.

2. Block Diagram



Features

- Low Voltage and Standard Voltage Operation
  - 5.0 (V_{CC} = 4.5V to 5.5V)
  - 2.7 (V_{CC} = 2.7V to 5.5V)
  - 2.5 (V_{CC} = 2.5V to 5.5V)
  - 1.8 (V_{CC} = 1.8V to 5.5V)
- Internally Organized 128 x 8 (1K), 256 x 8 (2K), 512 x 8 (4K), 1024 x 8 (8K) or 2048 x 8 (16K)
- 2-Wire Serial Interface
- Bidirectional Data Transfer Protocol
- 100 kHz (1.8V, 2.5V, 2.7V) and 400 kHz (5V) Compatibility
- Write Protect Pin for Hardware Data Protection
- 8-Byte Page (1K, 2K), 16-Byte Page (4K, 8K, 16K) Write Modes
- Partial Page Writes Are Allowed
- Self-Timed Write Cycle (10 ms max)
- High Reliability
  - Endurance: 1 Million Cycles
  - Data Retention: 100 Years
- Automotive Grade and Extended Temperature Devices Available
- 8-Pin and 14-Pin JEDEC SOIC and 8-Pin PDIP Packages

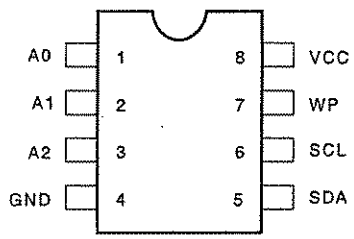
Description

The AT24C01A/02/04/08/16 provides 1024/2048/4096/8192/16384 bits of serial electrically erasable and programmable read only memory (EEPROM) organized as 128/256/512/1024/2048 words of 8 bits each. The device is optimized for use in many industrial and commercial applications where low power and low voltage operation are essential. The AT24C01A/02/04/08/16 is available in space saving 8-pin PDIP, 8-pin and 14-pin SOIC packages and is accessed via a 2-wire serial interface. In addition, the entire family is available in 5.0V (4.5V to 5.5V), 2.7V (2.7V to 5.5V), 2.5V (2.5V to 5.5V) and 1.8V (1.8V to 5.5V) versions.

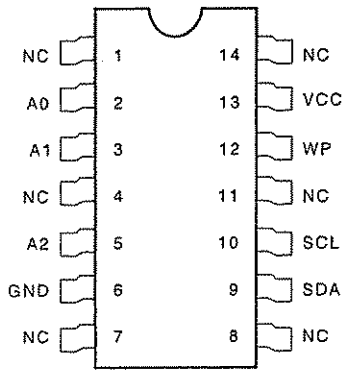
Pin Configurations

Pin Name	Function
A_0 to A_2	Address Inputs
SDA	Serial Data
SCL	Serial Clock Input
WP	Write Protect
NC	No Connect

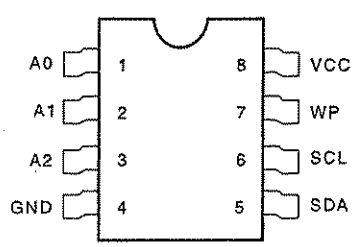
8-Pin PDIP



14-Pin SOIC



8-Pin SOIC



2-Wire Serial CMOS E²PROM

1K (128 x 8)

2K (256 x 8)

4K (512 x 8)

8K (1024 x 8)

16K (2048 x 8)

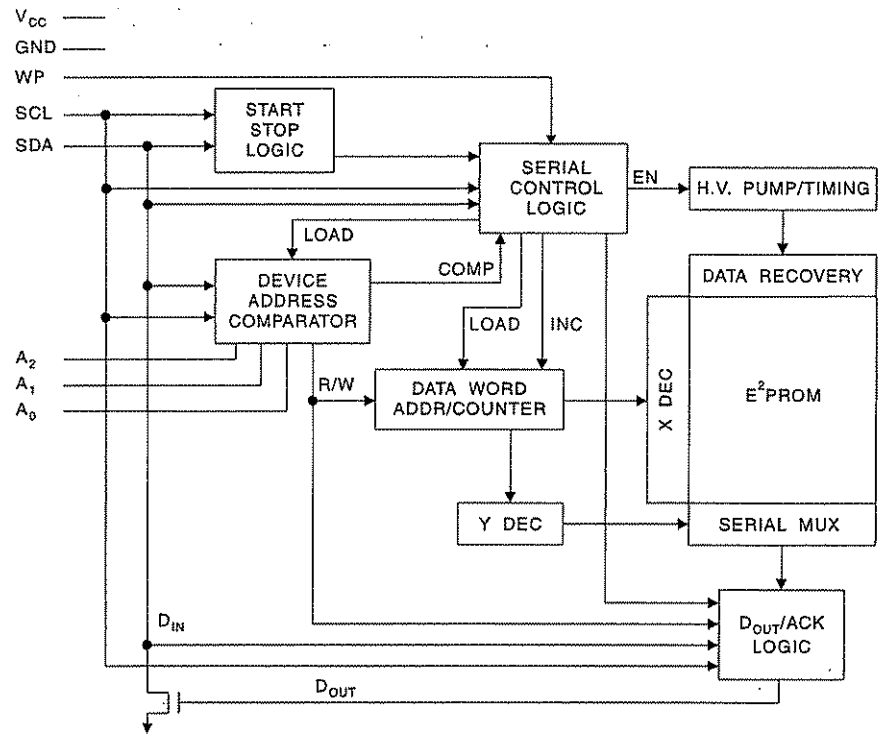
0180C

Absolute Maximum Ratings*

Operating Temperature	-55°C to +125°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin with Respect to Ground	-0.1V to +7.0V
Maximum Operating Voltage	6.25V
DC Output Current	5.0 mA

*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Block Diagram



Pin Description

SERIAL CLOCK (SCL): The SCL input is used to positive edge clock data into each E^2PROM device and negative edge clock data out of each device.

SERIAL DATA (SDA): The SDA pin is bidirectional for serial data transfer. This pin is open-drain driven and may be wire-ORed with any number of other open-drain or open collector devices.

DEVICE/PAGE ADDRESSES (A2, A1, A0): The A2, A1 and A0 pins are device address inputs that are hard wired for the AT24C01A and the AT24C02. As many as eight 1K/2K devices may be addressed on a single bus system (device addressing is discussed in detail under the Device Addressing section).

The AT24C04 uses the A2 and A1 inputs for hard wire addressing and a total of four 4K devices may be addressed on a single bus system. The A0 pin is a no connect.

The AT24C08 only uses the A2 input for hardwire addressing and a total of two 8K devices may be addressed on a single bus system. The A0 and A1 pins are no connects.

The AT24C16 does not use the device address pins which limits the number of devices on a single bus to one. The A0, A1 and A2 pins are no connects.

(continued)