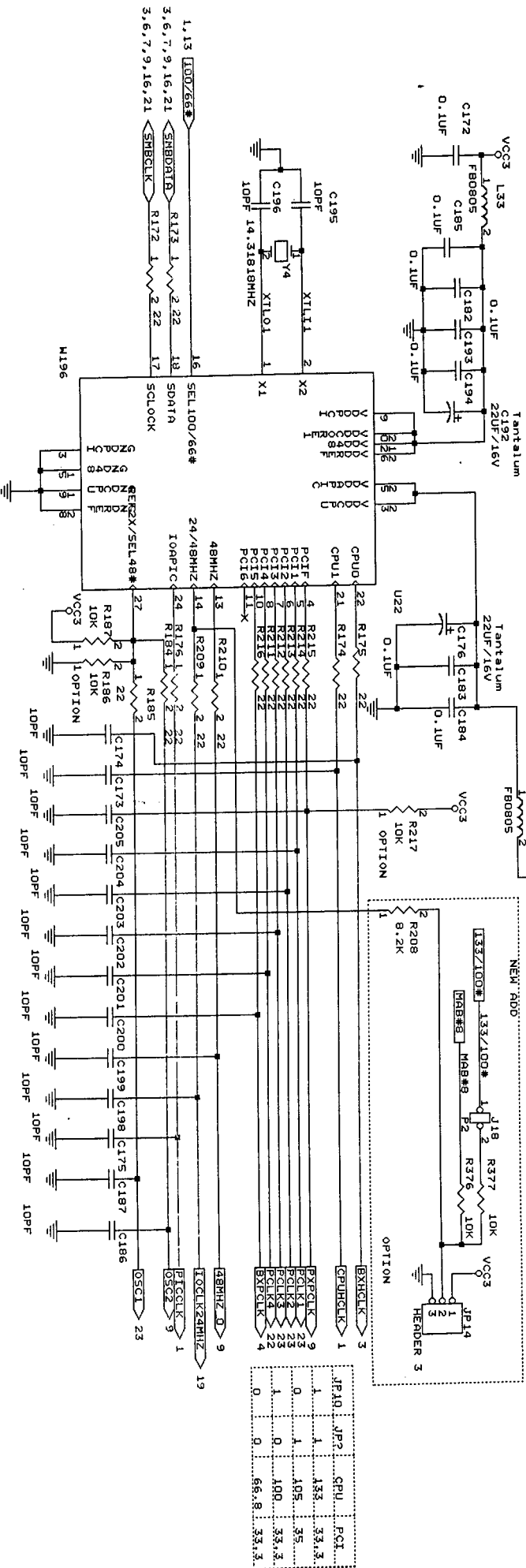


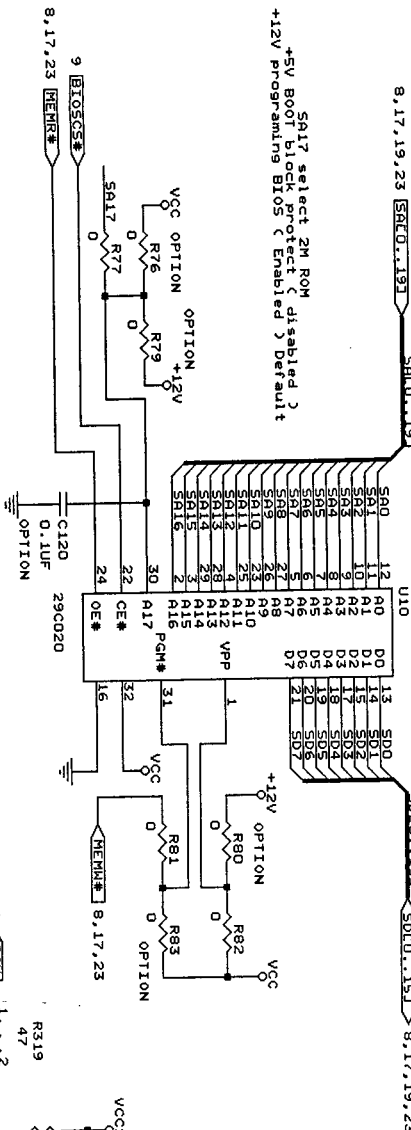
CLOCK SYNTHESIZER

J2 = OFF HOST CLOCK BY 4 TEST 100 CPU RUN 133MHZ
 JP2 = 1-2 & JP ON BY CPU SET

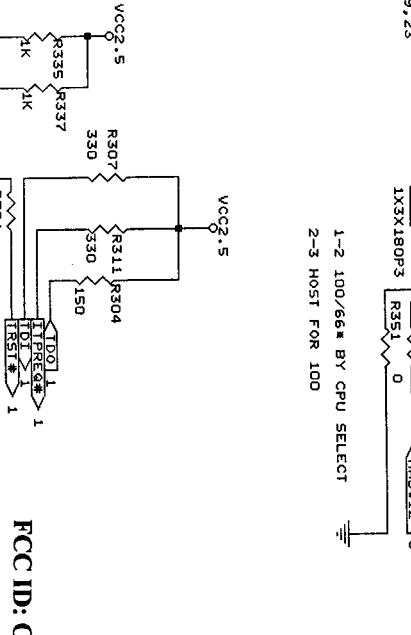


SYSTEM ROM

FLASH SOCKET

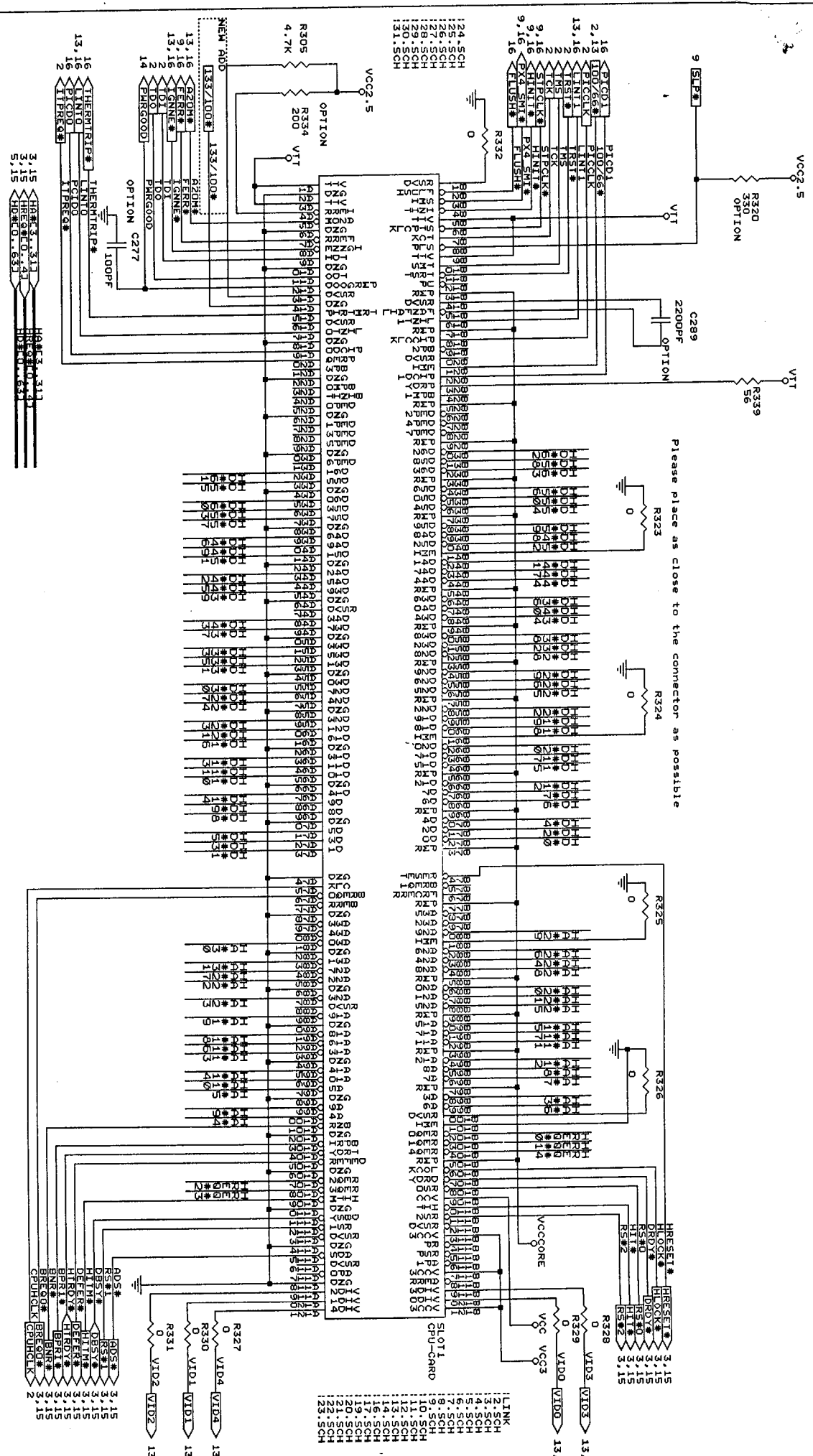


+5V BOOT select 2M ROM
 +12V Programming BIOS (Enabled) Default



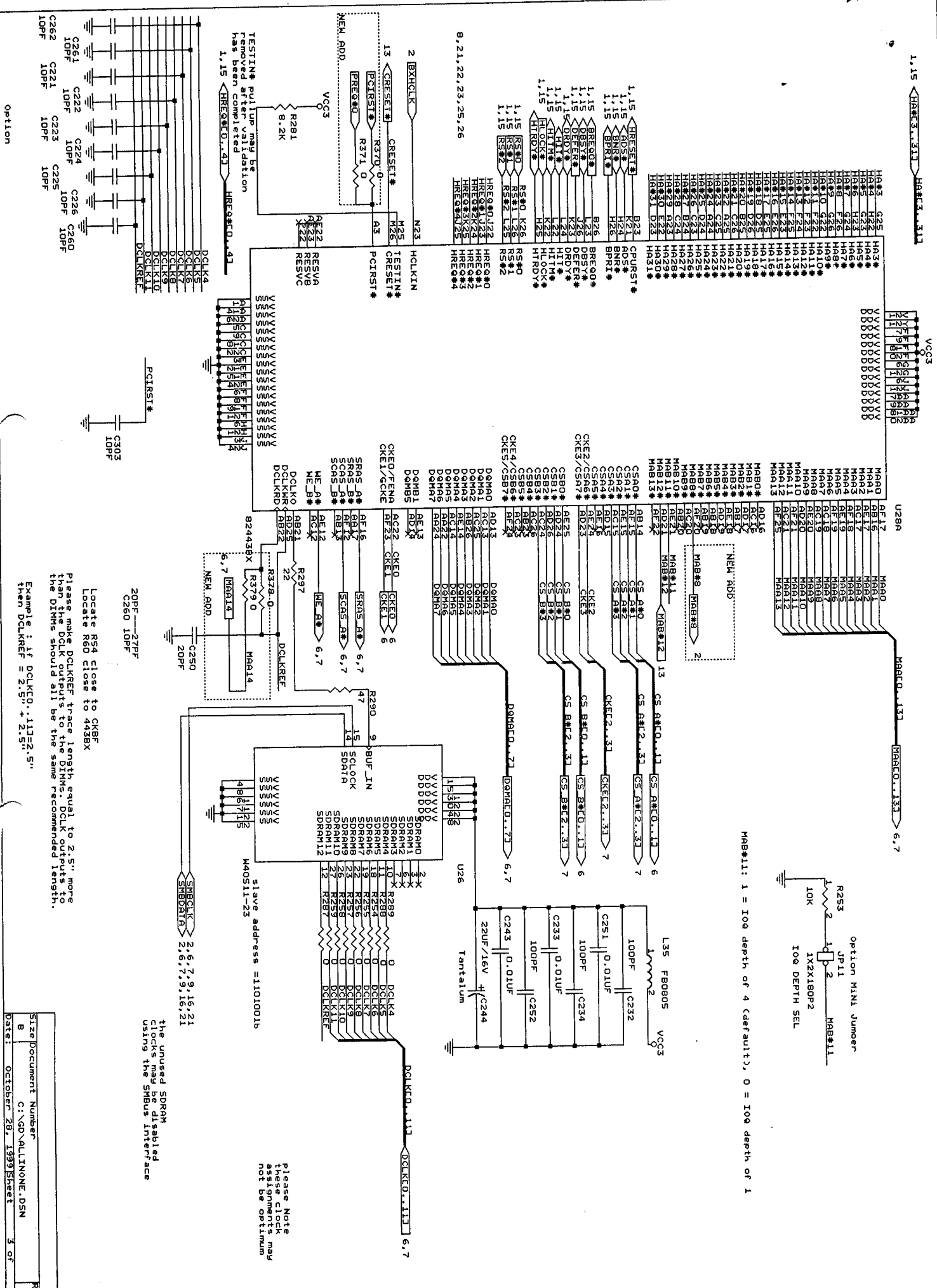
FCC ID: 02PMILLENNIUM-X

Note : This strong pullup resistor on SLIP is Necessary when using an LAI



Please place as close to the connector as possible

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8.21,22,23,25,26

MAB#11: 1 = 10q depth of 4 (default), 0 = 10q depth of 1

TESTIN# pullup may be removed after validation has been completed

slave address = 1101001b

the unused SDRAM clocks may be disabled using the SDBus interface

Please Note
These components may not be optimum

Example : if DCLKREF = 2.5" + 2.5"

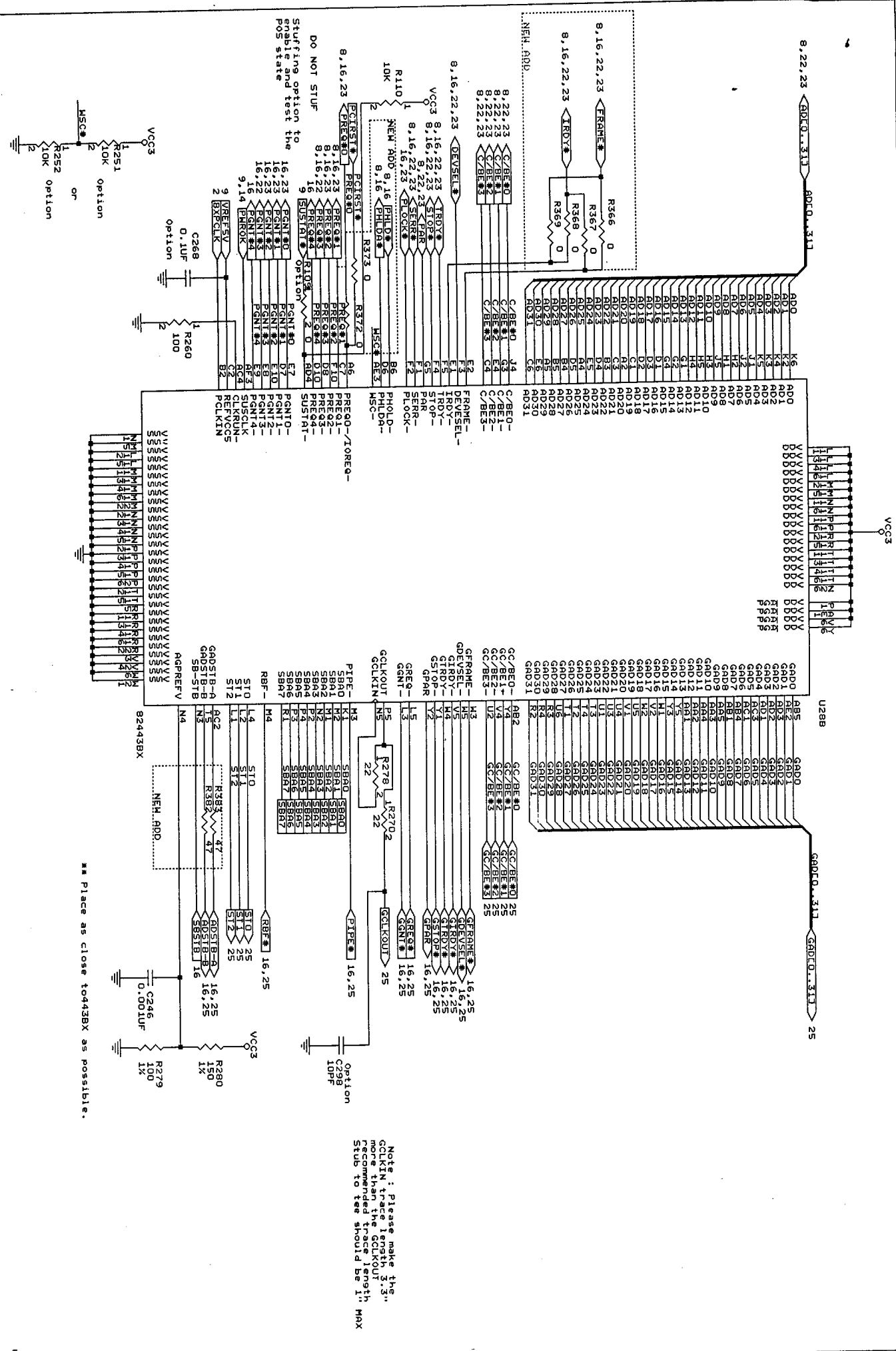
Locate R54 close to CKBF

Locate R60 close to 4458X

Please make DCLKREF trace length equal to 2.5" more than the DCLK outputs to the DIMMs. DCLK outputs to the DIMMs should all be the same recommended length.

Option

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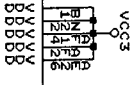


Place as close to443BX as possible.

Note: Please make the GCLKIN trace 10 mils Recommended trace length Stud to tee should be 1" MAX

6,7 HD#D.O..633 HD#D.O..633

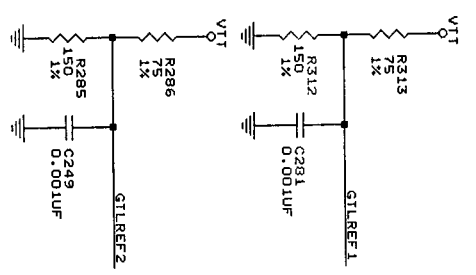
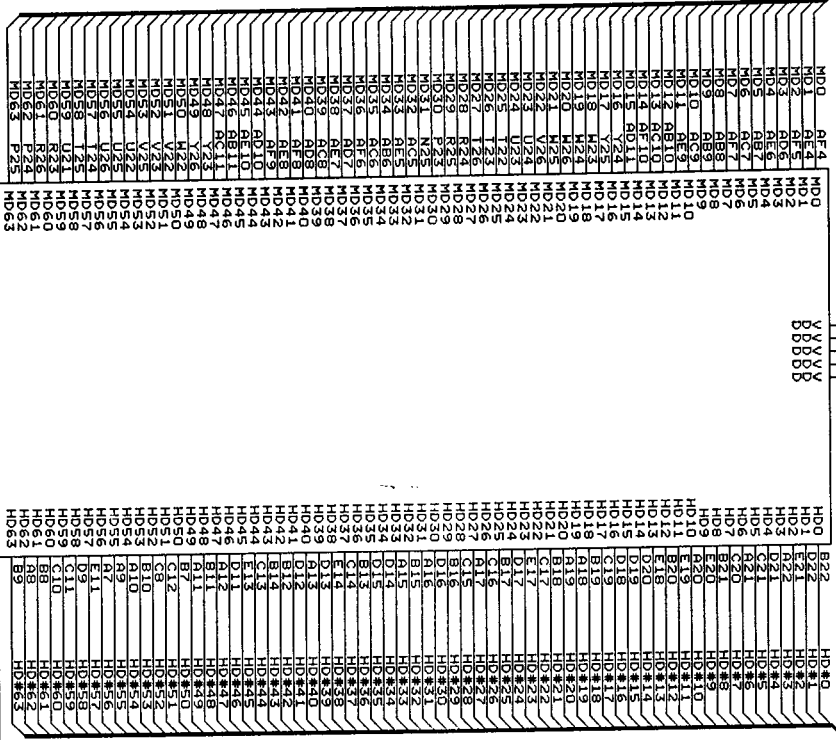
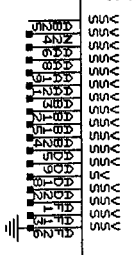
1,15



U28C

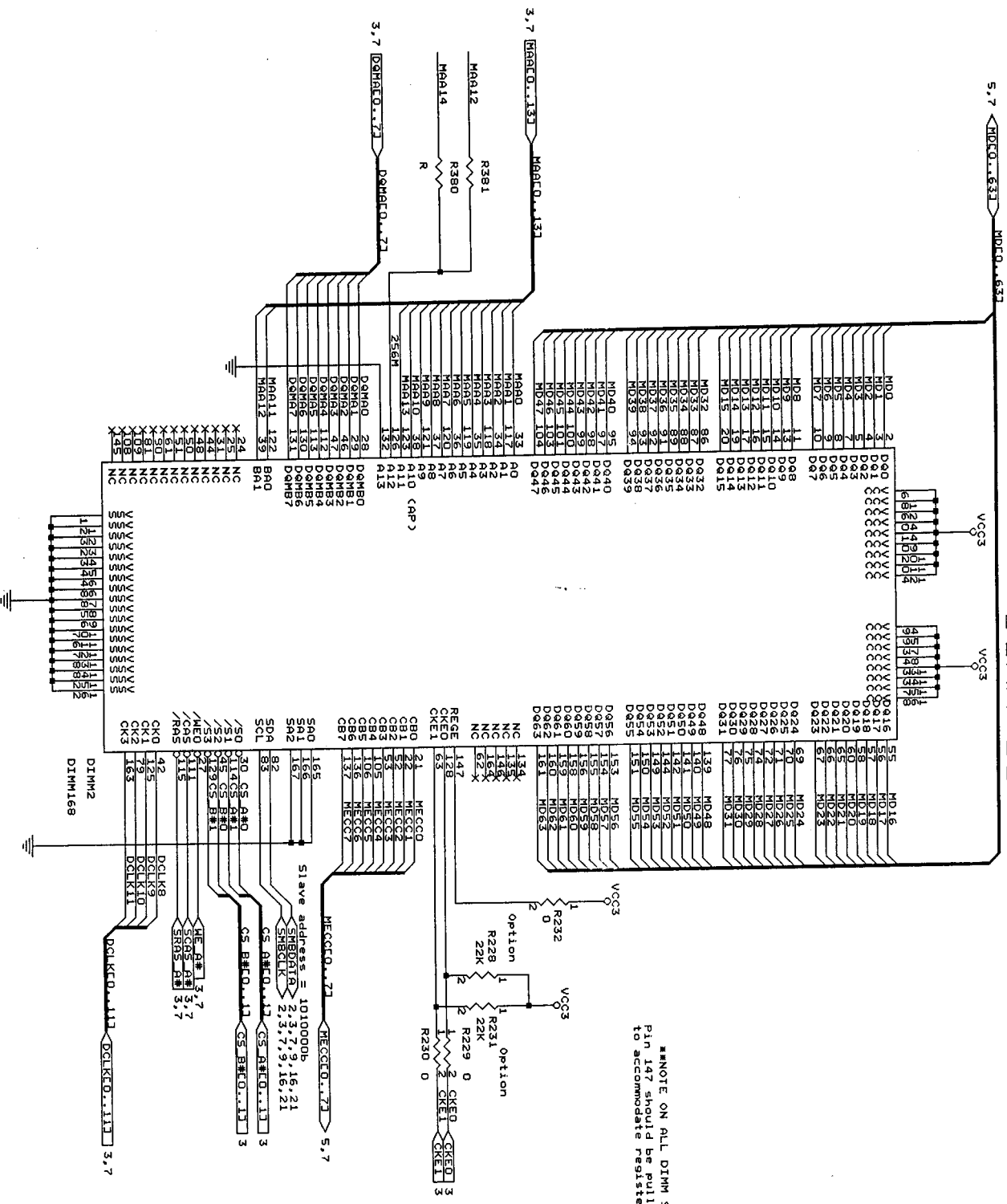
6,7 MECCD.O..73 MECCD.O..73

824438X



5,7 MDIO..633 MDIO..633

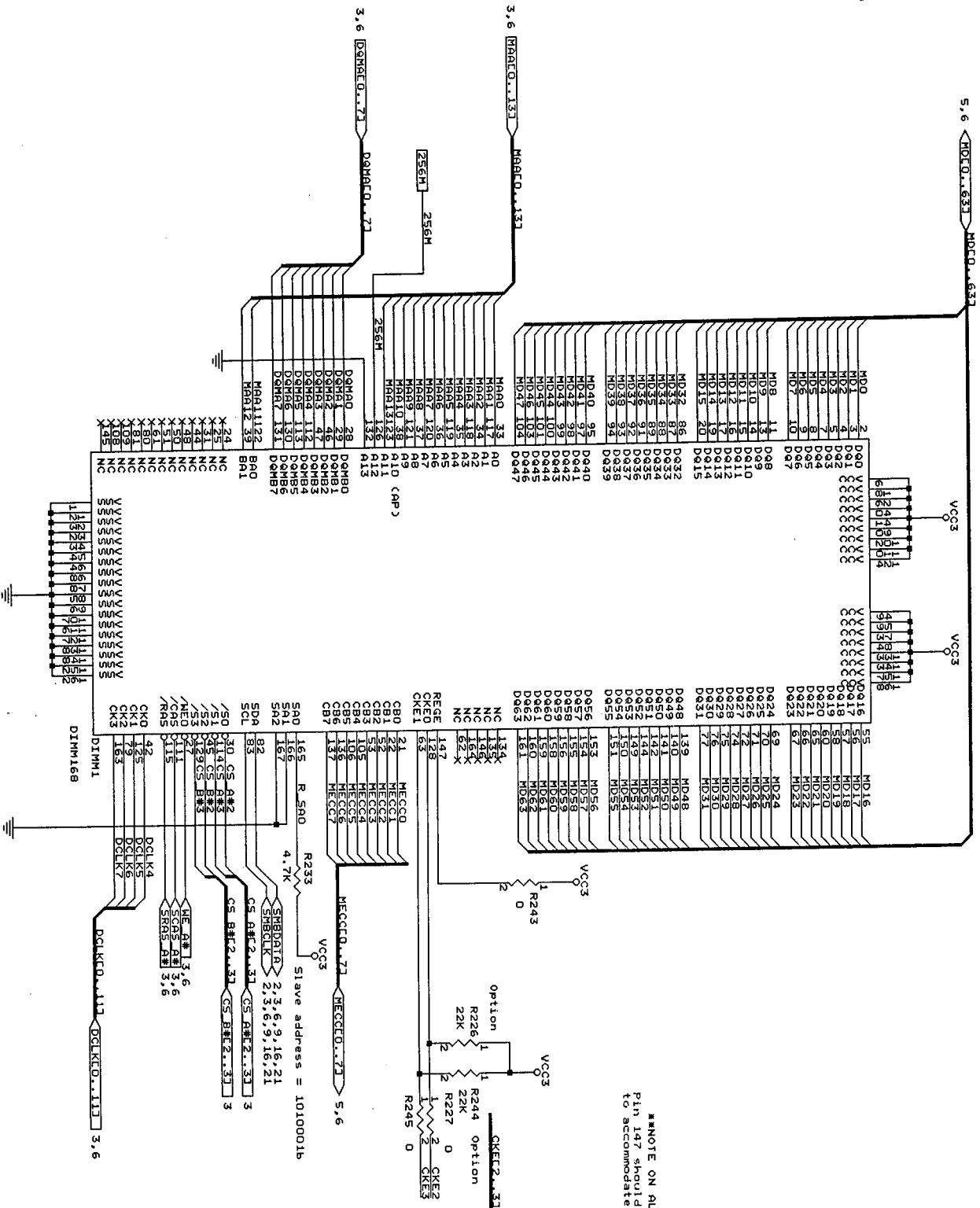
DIMM SOCKET Ø



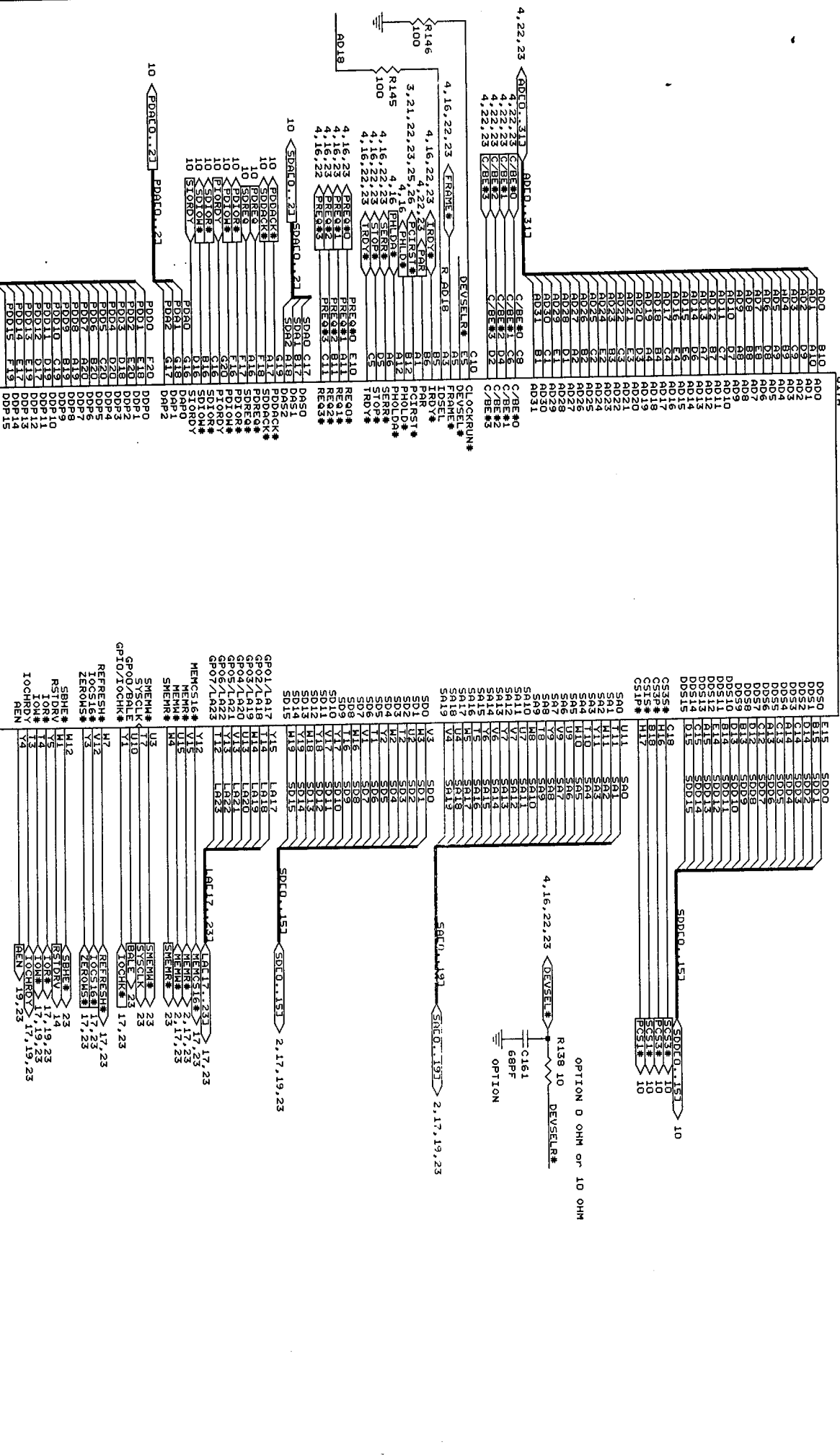
NOTE ON ALL DIMM SOCKETS: Pin 147 should be registered to a high state to accommodate registered DIMMs.

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DIMM SOCKET 1

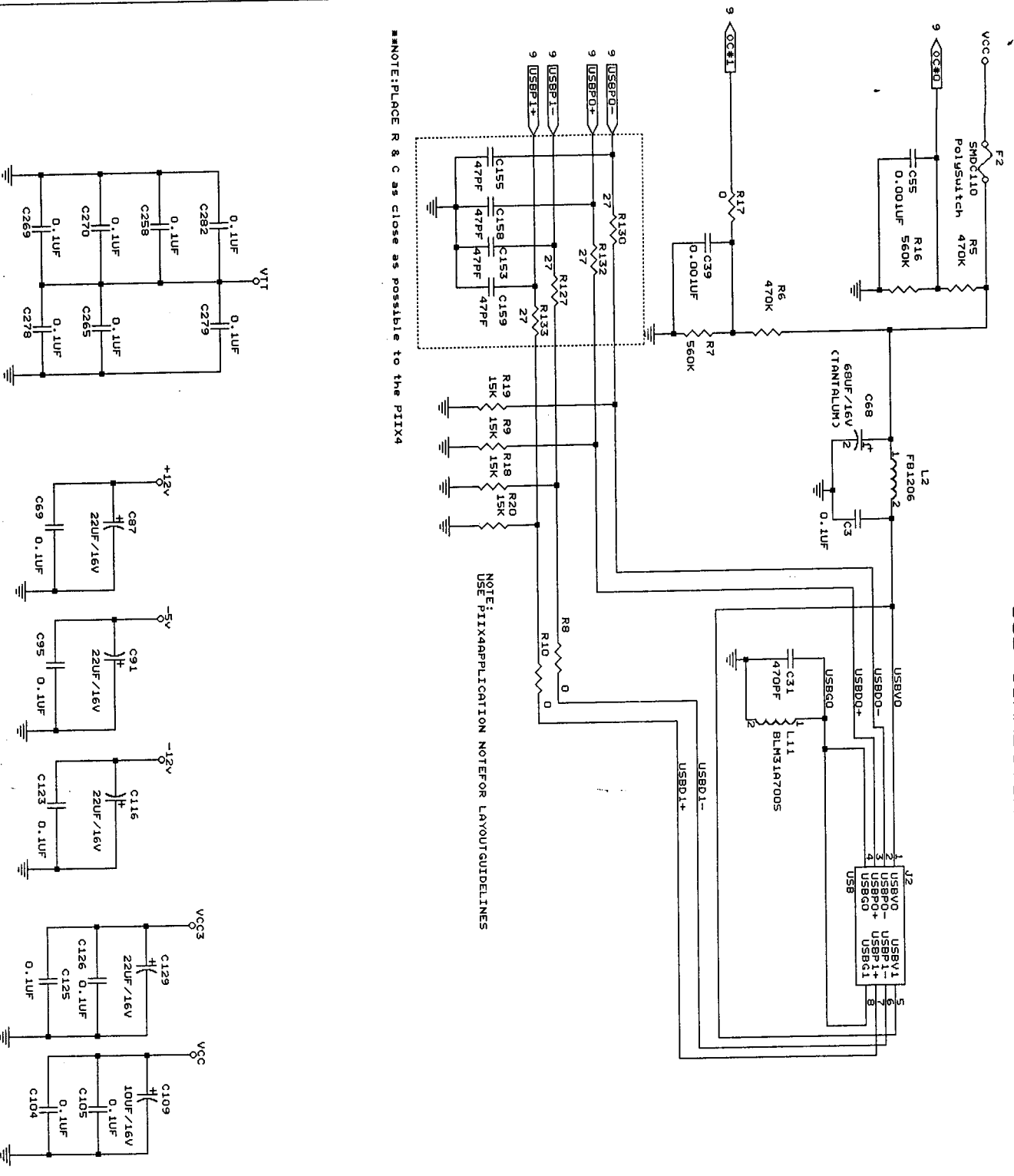


NOTE ON ALL DIMM SOCKETS:
Pin 147 should be pulled to a high state to accommodate registered DIMMs.



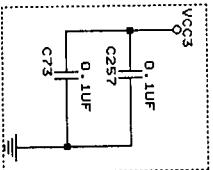
Size Document Number
 B C:\VD\ALLINONE.OSN
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USB CONNECTORS

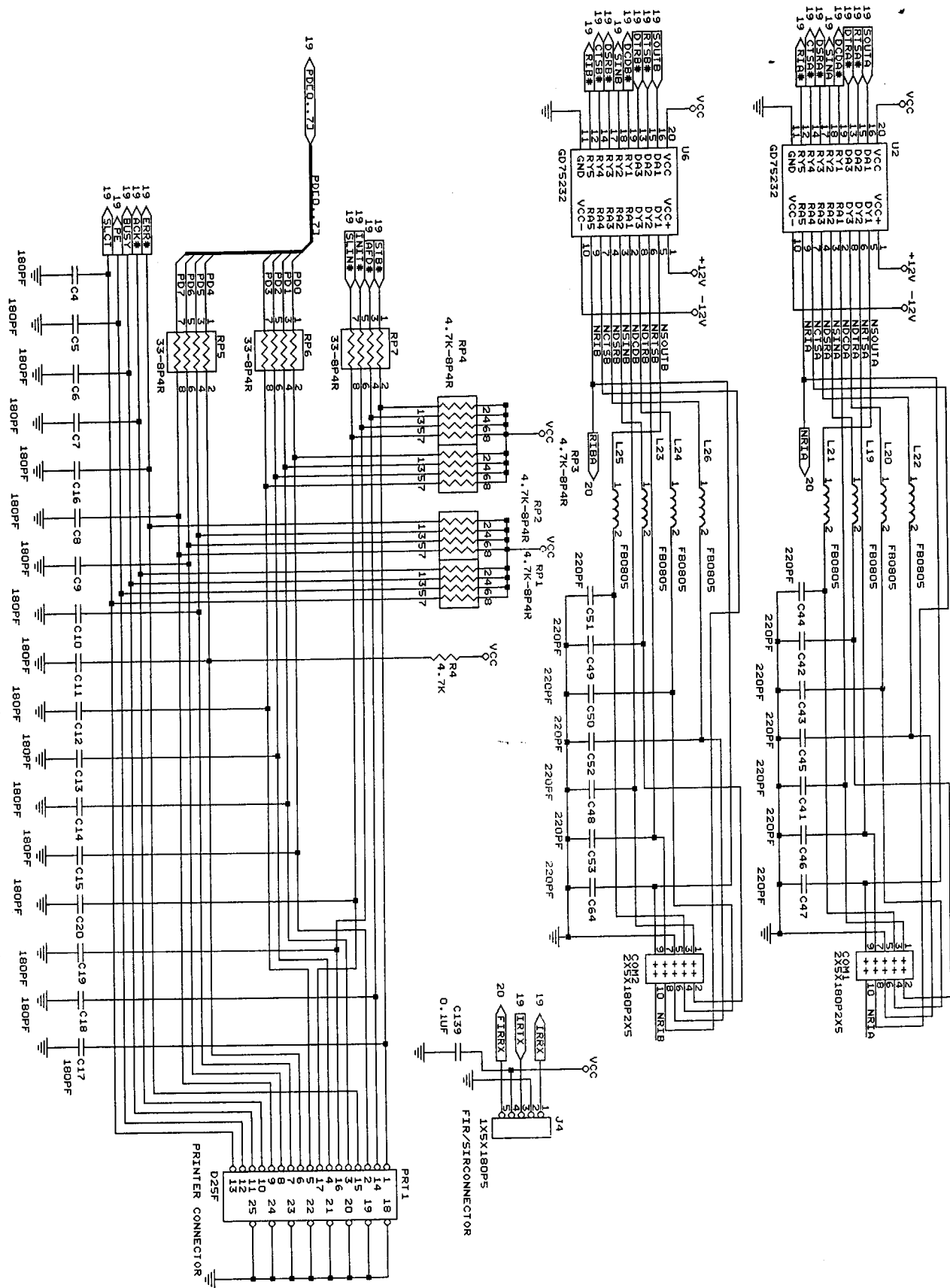


NOTE: PLACE R & C as close as possible to the PIIX4

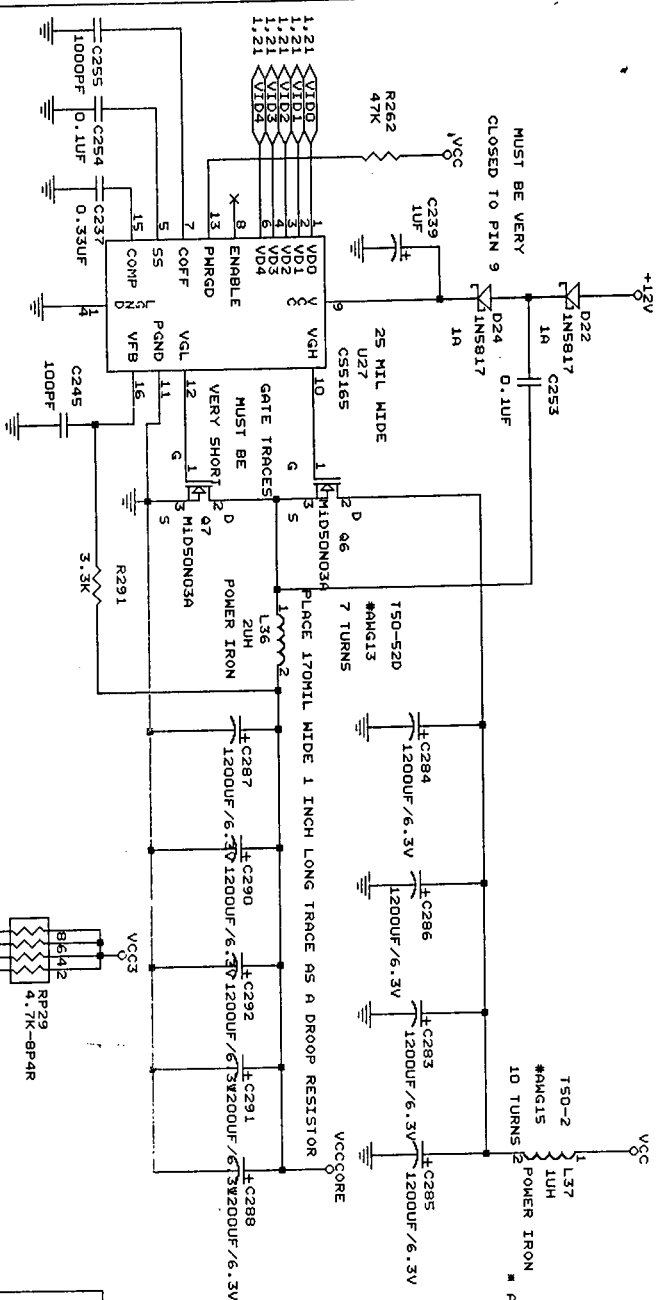
NOTE: PIIX4 APPLICATION NOTE FOR LAYOUT GUIDELINES



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REV	

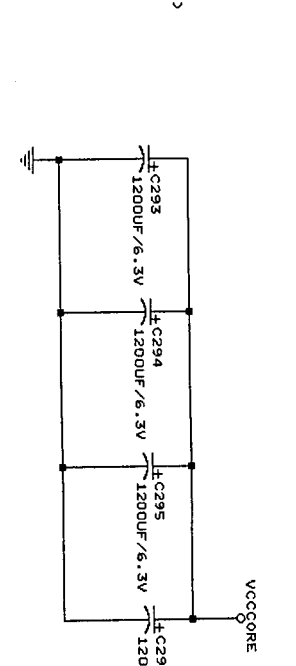
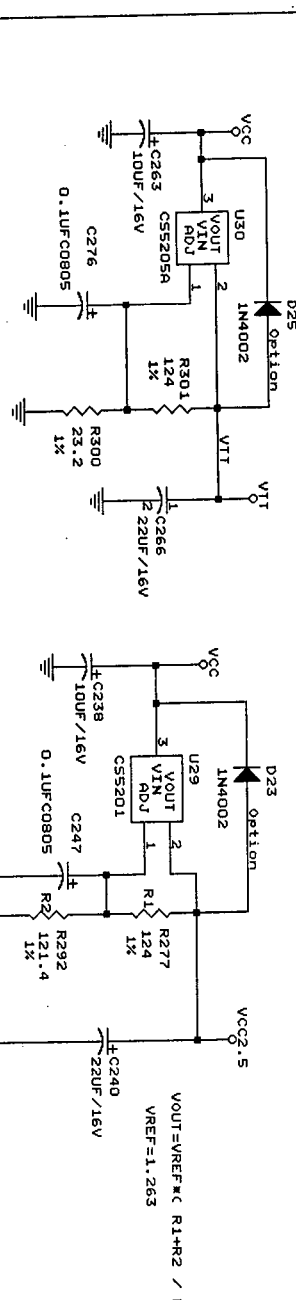
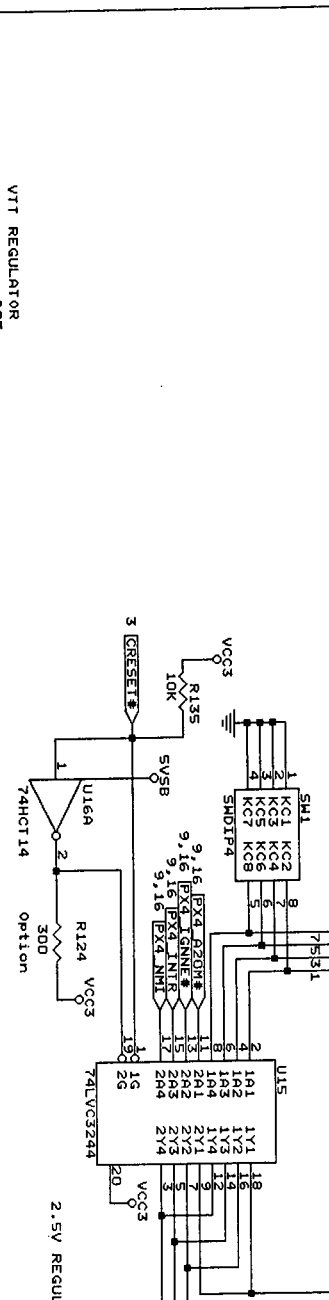


INPUT CHOKE IS OPTIONAL DEPENDED ON THE LAYOUT AND HOW FAR AWAY FROM THE POWERCONNECTOR

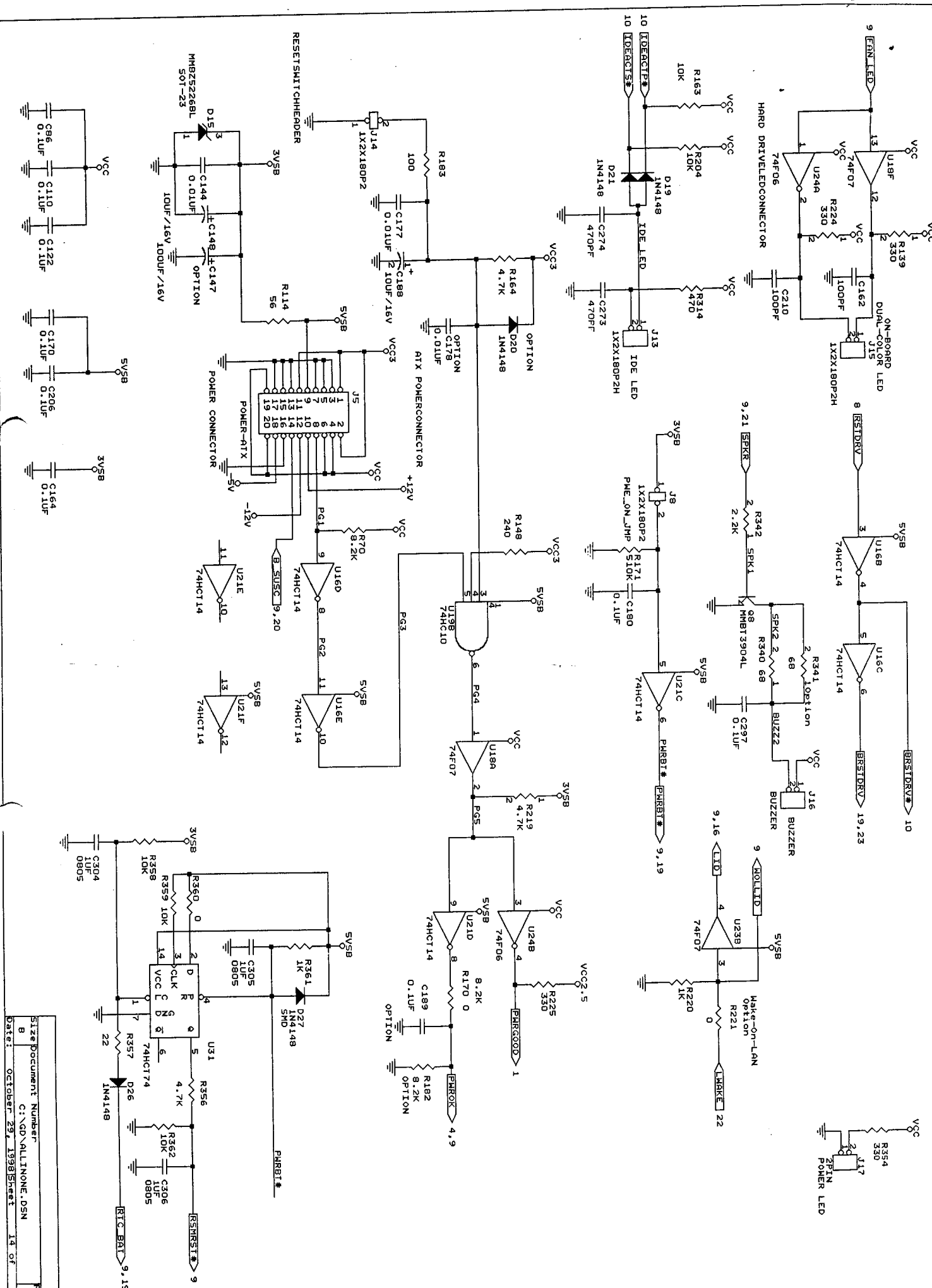


ADDITIONAL STRAP CONFIGURATIONS MAY BE NECESSARY TO SUPPORT THE DS1P.

Frequency Multiplier:	LINT1	LINT0	IGNNE#	R20M#
C System Bus to Process. Core. }	KC7	KC5	KC3	KC1
3	L	L	H	L
4	L	L	H	H
5	L	L	H	H
5/2	L	H	L	L
7/2	L	H	H	L
9/2	L	H	L	H

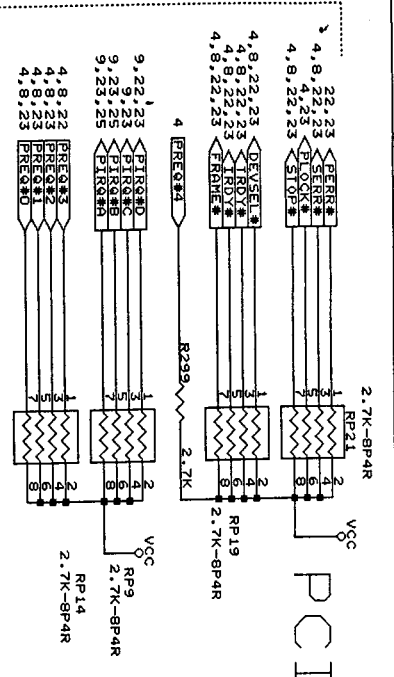


NOTE: VOLTAGE REGULATOR SHOULD BE LOCATED NEAR THE 440BX

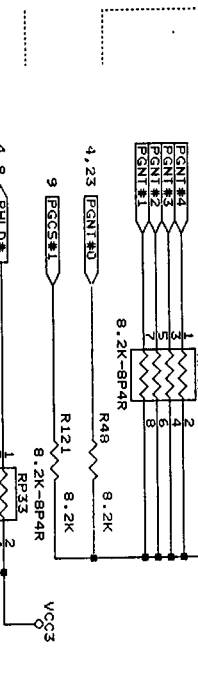


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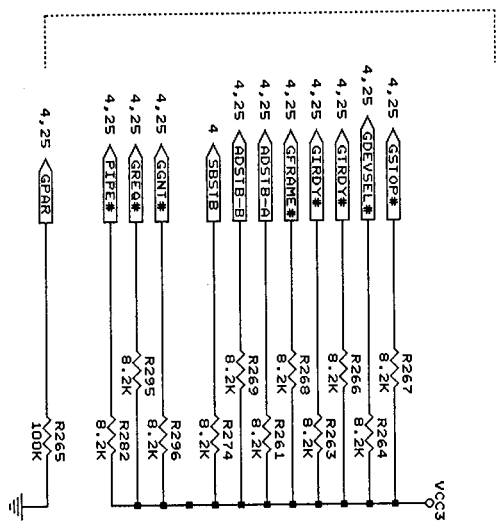
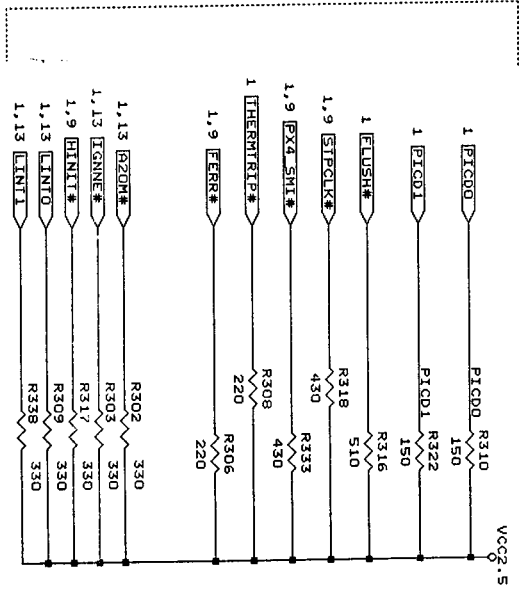
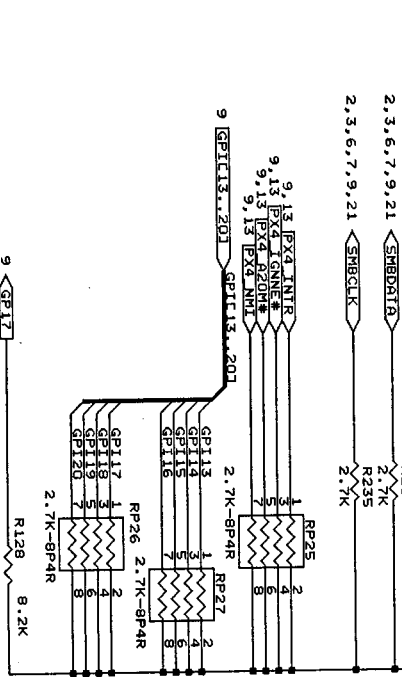
PCI BUS

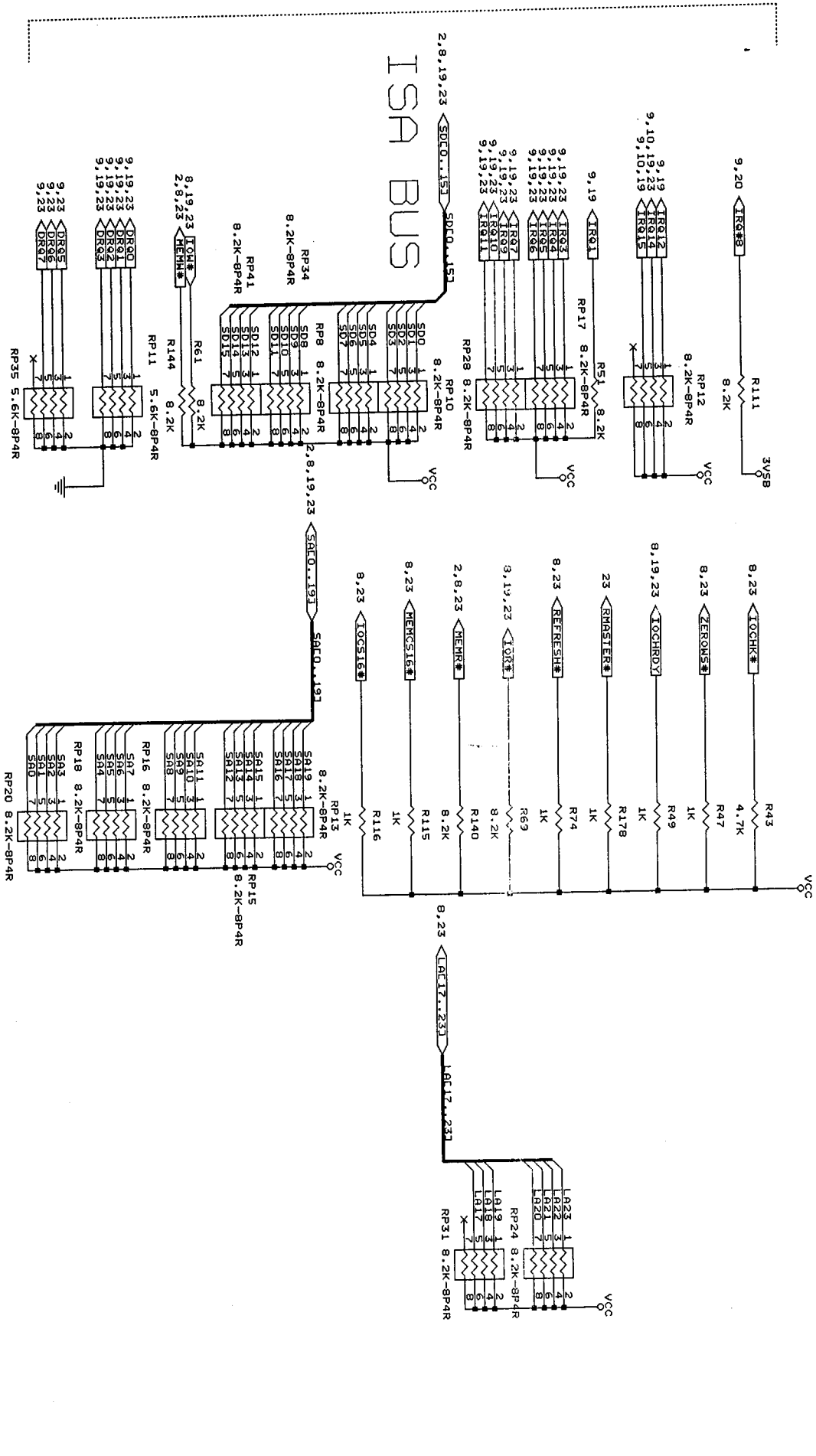


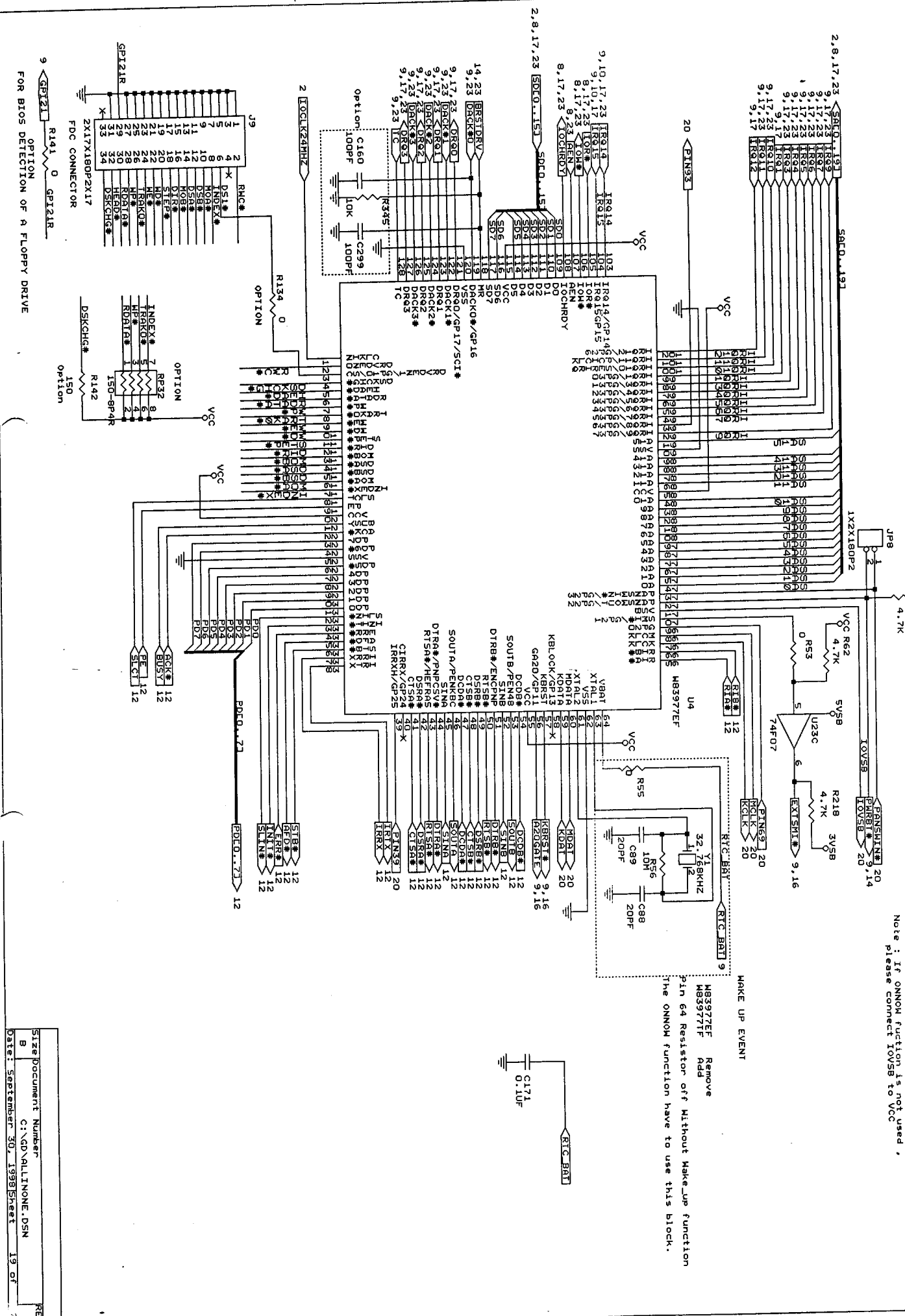
SLOT 1



AGP

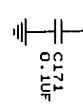


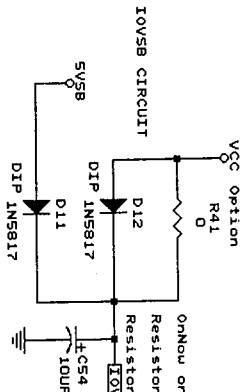
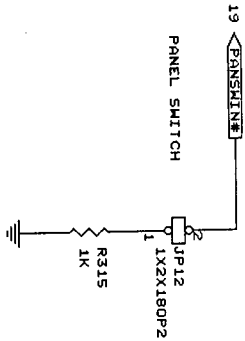
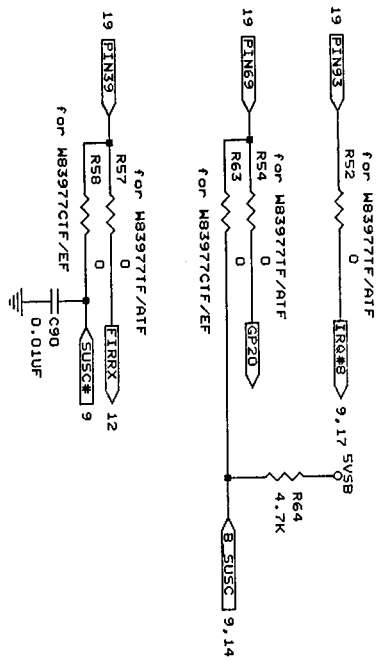




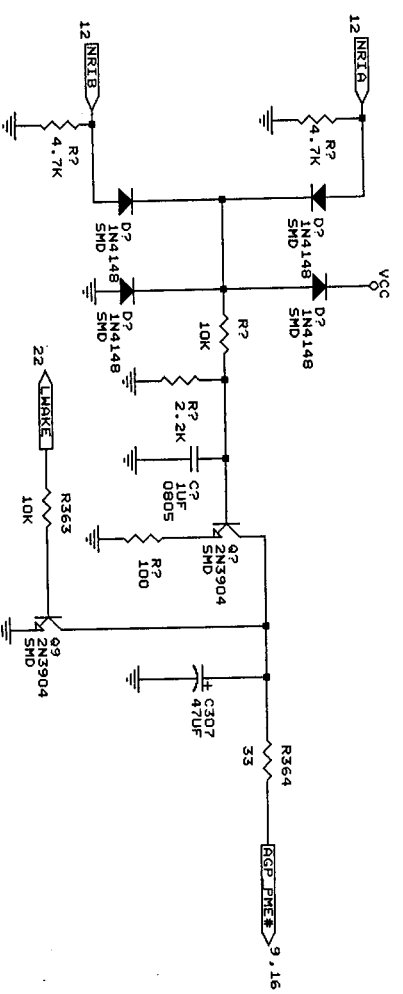
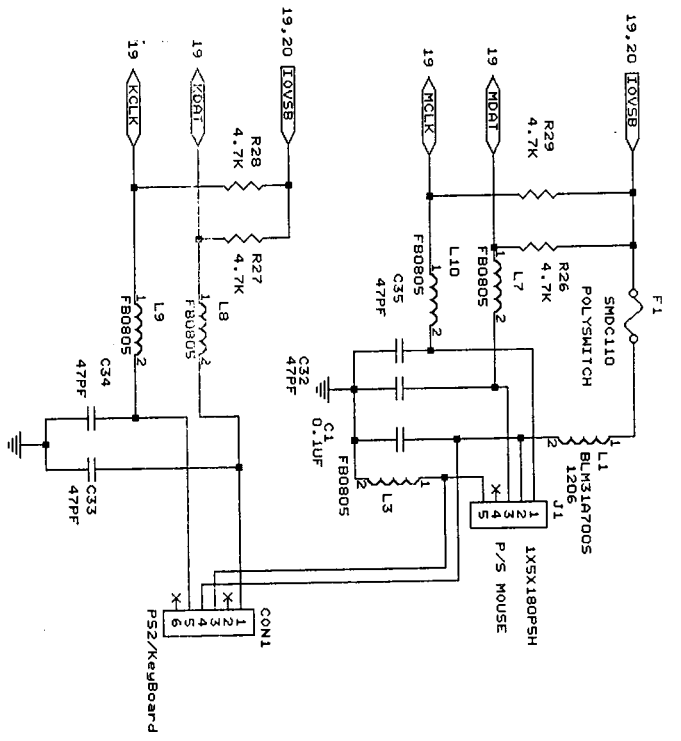
ONNOM Function
 FROM PANEL SWITCH ANSMV function.
 1-2 on CAN CONTROL function always enabled.
 2-3 on PRISM function always enabled.
 Note : If ONNOM function is not used ,
 please connect I0V5B to VCC

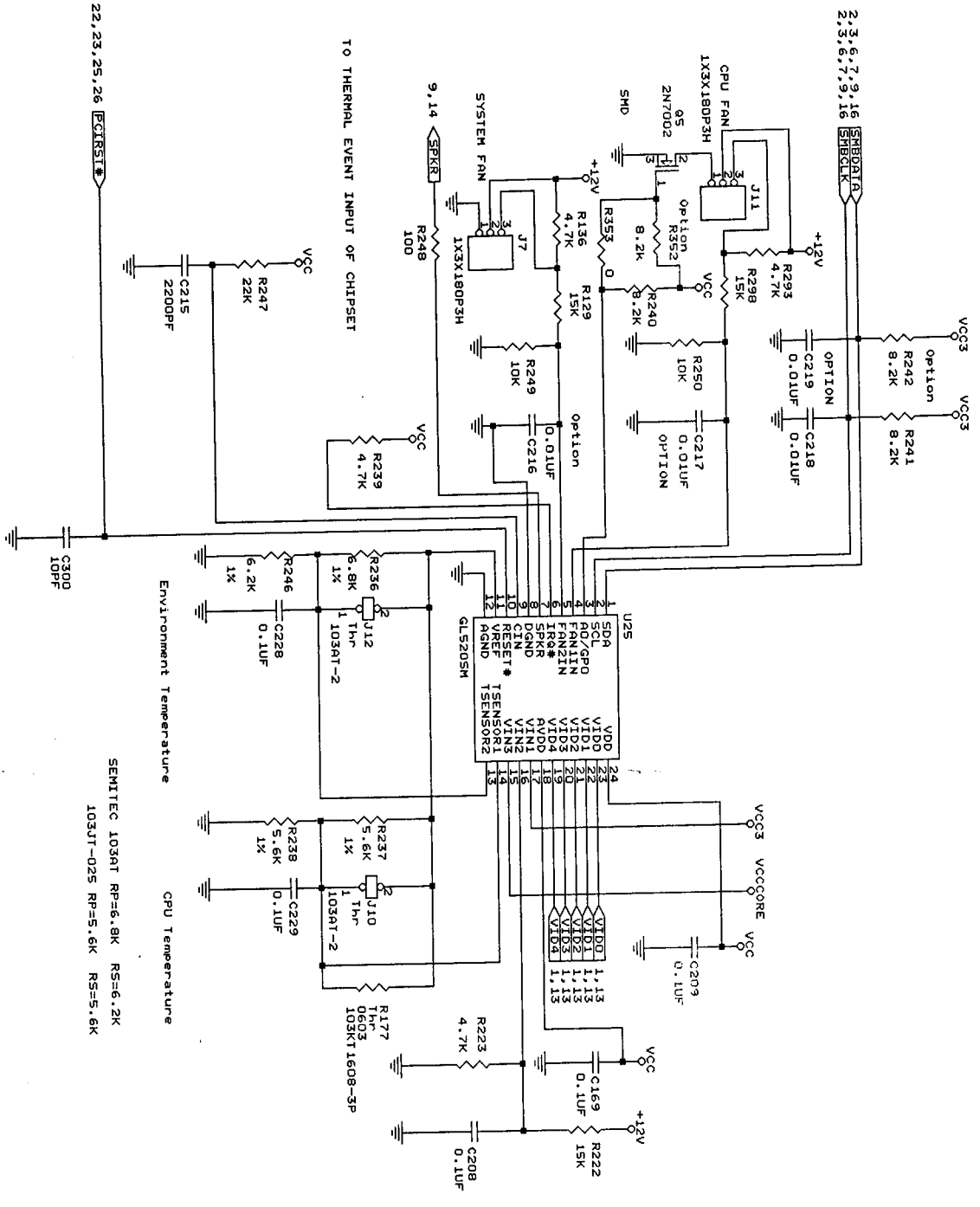
MAKE UP EVENT
 M83977EF Remove
 M83977TF Add
 pin 64 Resistor off Without Make-up function
 The ONNOM function have to use this block.





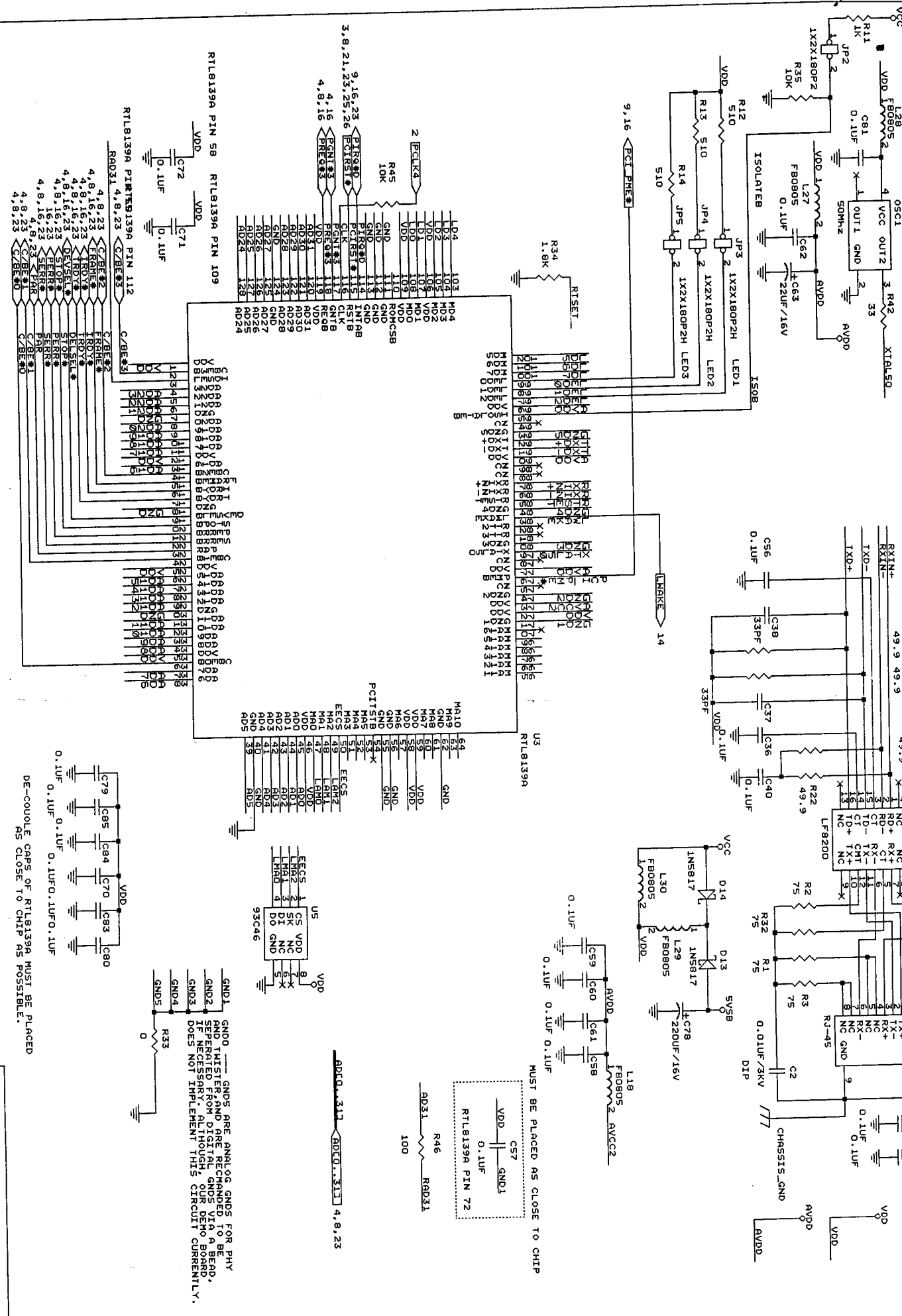
On/Off or Wake-Up function power
Resistor off ; Diode on Wake-Up function
Resistor on ; Diode off Non Wake-Up function
IOVSB 19,20





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NOTE: TO DISABLE (ISOLATE) THE RTL8139A
SHORT: TO ENABLE THE RTL8139A



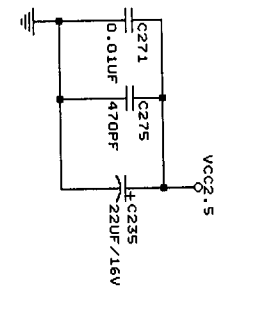
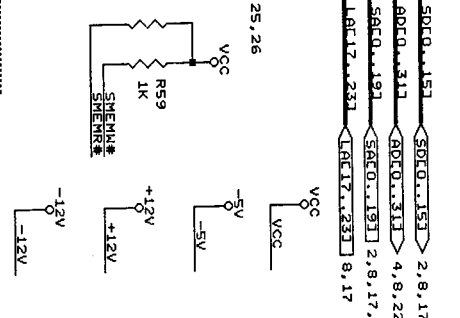
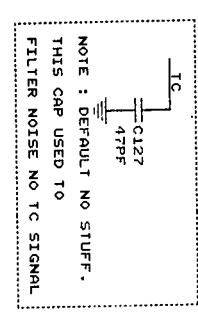
DE-COUPLE CAPS OF RTL8139A MUST BE PLACED AS CLOSE TO CHIP AS POSSIBLE.

GND1, GND2, GND3, GND4, GND5 ARE ANALOG GND'S FOR PHY AND TWISTER, AND ARE RECOMMENDED TO BE SEPARATED FROM DIGITAL GND'S ON BOARD. IF NECESSARY, ALTHOUGH OUR DEMO BOARD DOES NOT IMPLEMENT THIS CIRCUIT CURRENTLY.

MUST BE PLACED AS CLOSE TO CHIP

Size	Document Number	REV
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Pin	Signal	Function	Value	Pin	Signal	Function	Value
95	GND			1	IOCHK#	8, 17	
94	BRSTDRV			2	GND		
93	GND			3	IO		
92	VCC#C	100	85	4	IO		
91	TRG3#D	100	86	5	PIRQA	9, 16, 25	
90	PIR3#D	100	87	6	PIRQB	9, 16, 25	
89	+12V			7	PIRQC		
88	VCC	100	88	8	PIRQD		
87	VCC	100	89	9	PIRQA		
86	VCC	100	90	10	PIRQB		
85	VCC	100	91	11	PIRQC		
84	VCC	100	92	12	PIRQD		
83	VCC	100	93	13	PIRQA		
82	VCC	100	94	14	PIRQB		
81	VCC	100	95	15	PIRQC		
80	VCC	100	96	16	PIRQD		
79	VCC	100	97	17	PIRQA		
78	VCC	100	98	18	PIRQB		
77	VCC	100	99	19	PIRQC		
76	VCC	100	100	20	PIRQD		
75	VCC	100	101	21	PIRQA		
74	VCC	100	102	22	PIRQB		
73	VCC	100	103	23	PIRQC		
72	VCC	100	104	24	PIRQD		
71	VCC	100	105	25	PIRQA		
70	VCC	100	106	26	PIRQB		
69	VCC	100	107	27	PIRQC		
68	VCC	100	108	28	PIRQD		
67	VCC	100	109	29	PIRQA		
66	VCC	100	110	30	PIRQB		
65	VCC	100	111	31	PIRQC		
64	VCC	100	112	32	PIRQD		
63	VCC	100	113	33	PIRQA		
62	VCC	100	114	34	PIRQB		
61	VCC	100	115	35	PIRQC		
60	VCC	100	116	36	PIRQD		
59	VCC	100	117	37	PIRQA		
58	VCC	100	118	38	PIRQB		
57	VCC	100	119	39	PIRQC		
56	VCC	100	120	40	PIRQD		
55	VCC	100	121	41	PIRQA		
54	VCC	100	122	42	PIRQB		
53	VCC	100	123	43	PIRQC		
52	VCC	100	124	44	PIRQD		
51	VCC	100	125	45	PIRQA		
50	VCC	100	126	46	PIRQB		
49	VCC	100	127	47	PIRQC		
48	VCC	100	128	48	PIRQD		
47	VCC	100	129	49	PIRQA		
46	VCC	100	130	50	PIRQB		
45	VCC	100	131	51	PIRQC		
44	VCC	100	132	52	PIRQD		
43	VCC	100	133	53	PIRQA		
42	VCC	100	134	54	PIRQB		
41	VCC	100	135	55	PIRQC		
40	VCC	100	136	56	PIRQD		
39	VCC	100	137	57	PIRQA		
38	VCC	100	138	58	PIRQB		
37	VCC	100	139	59	PIRQC		
36	VCC	100	140	60	PIRQD		
35	VCC	100	141	61	PIRQA		
34	VCC	100	142	62	PIRQB		
33	VCC	100	143	63	PIRQC		
32	VCC	100	144	64	PIRQD		
31	VCC	100	145	65	PIRQA		
30	VCC	100	146	66	PIRQB		
29	VCC	100	147	67	PIRQC		
28	VCC	100	148	68	PIRQD		
27	VCC	100	149	69	PIRQA		
26	VCC	100	150	70	PIRQB		
25	VCC	100	151	71	PIRQC		
24	VCC	100	152	72	PIRQD		
23	VCC	100	153	73	PIRQA		
22	VCC	100	154	74	PIRQB		
21	VCC	100	155	75	PIRQC		
20	VCC	100	156	76	PIRQD		
19	VCC	100	157	77	PIRQA		
18	VCC	100	158	78	PIRQB		
17	VCC	100	159	79	PIRQC		
16	VCC	100	160	80	PIRQD		
15	VCC	100	161	81	PIRQA		
14	VCC	100	162	82	PIRQB		
13	VCC	100	163	83	PIRQC		
12	VCC	100	164	84	PIRQD		
11	VCC	100	165	85	PIRQA		
10	VCC	100	166	86	PIRQB		
9	VCC	100	167	87	PIRQC		
8	VCC	100	168	88	PIRQD		
7	VCC	100	169	89	PIRQA		
6	VCC	100	170	90	PIRQB		
5	VCC	100	171	91	PIRQC		
4	VCC	100	172	92	PIRQD		
3	VCC	100	173	93	PIRQA		
2	VCC	100	174	94	PIRQB		
1	VCC	100	175	95	PIRQC		



LANWORK at PC14 IDSEL AD31 PREQ#3
 PC11 IDSEL A49 AD26 PREQ#0
 PC12 IDSEL A46 AD29 PREQ#2
 PC13 IDSEL A46 AD29 PREQ#3