

VCCP

U17A

- H\_D0 B21 D0
- H\_D1 B22 D1
- H\_D2 A23 D2
- H\_D3 A23 D3
- H\_D4 A25 D4
- H\_D5 D22 D5
- H\_D6 B24 D6
- H\_D7 C23 D7
- H\_D8 C24 D8
- H\_D9 B25 D9
- H\_D10 G22 D10
- H\_D11 H21 D11
- H\_D12 C26 D12
- H\_D13 D23 D13
- H\_D14 J21 D14
- H\_D15 H22 D15
- H\_D16 D23 D16
- H\_D17 E24 D17
- H\_D18 G23 D18
- H\_D19 F23 D19
- H\_D20 F24 D20
- H\_D21 E25 D21
- H\_D22 F26 D22
- H\_D23 D26 D23
- H\_D24 L21 D24
- H\_D25 G26 D25
- H\_D26 H24 D26
- H\_D27 M21 D27
- H\_D28 L22 D28
- H\_D29 J24 D29
- H\_D30 K23 D30
- H\_D31 H25 D31
- H\_D32 M23 D32
- H\_D33 N22 D33
- H\_D34 P21 D34
- H\_D35 M24 D35
- H\_D36 N23 D36
- H\_D37 M26 D37
- H\_D38 N26 D38
- H\_D39 N25 D39
- H\_D40 R21 D40
- H\_D41 P24 D41
- H\_D42 R25 D42
- H\_D43 R24 D43
- H\_D44 T26 D44
- H\_D45 T25 D45
- H\_D46 T22 D46
- H\_D47 T23 D47
- H\_D48 U26 D48
- H\_D49 U24 D49
- H\_D50 U23 D50
- H\_D51 V25 D51
- H\_D52 V22 D52
- H\_D53 V24 D53
- H\_D54 V24 D54
- H\_D55 W26 D55
- H\_D56 Y26 D56
- H\_D57 Y23 D57
- H\_D58 Y23 D58
- H\_D59 Y24 D59
- H\_D60 Y21 D60
- H\_D61 AA25 D61
- H\_D62 AA22 D62
- H\_D63 AA24 D63

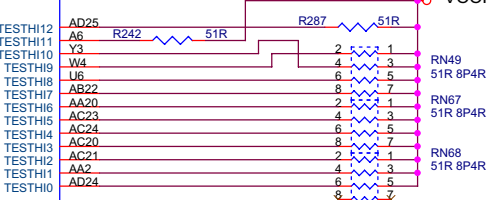


NORTHWOOD

- DEP3 X
- DEP4 X
- DEP5 X
- DEP6 X

- A35 AB1 X
- A34 Y1 X
- A33 W2 X
- A32 V3 X
- A31 U4 H A31
- A30 W1 H A29
- A29 R6 H A28
- A28 V2 H A27
- A26 T4 H A26
- A25 U3 H A24
- A24 R5 H A23
- A23 U1 H A22
- A22 T2 H A21
- A21 R3 H A19
- A20 P4 H A19
- A19 R2 H A18
- A18 I1 H A17
- A17 N5 H A16
- A16 N4 H A15
- A15 N2 H A14
- A14 M1 H A13
- A13 M1 H A12
- A12 M4 H A11
- A11 M3 H A10
- A10 L2 H A9
- A9 M6 H A8
- A8 L3 H A7
- A7 K1 H A6
- A6 L6 H A5
- A5 K4 H A4
- A4 K2 H A3

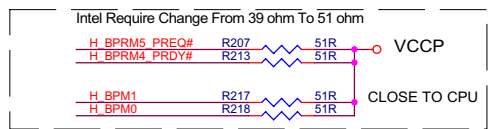
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- VID1 AE4 CPUVID1 <33>
- VID2 AE2 CPUVID2 <33>
- VID4 AE1 CPUVID4 <33>
- REQ4 H3 H\_REQ4 <7>
- REQ3 J4 H\_REQ3 <7>
- REQ2 K5 H\_REQ2 <7>
- REQ0 J1 H\_REQ0 <7>
- BPM5 AB4 H\_BPRM5\_PREQ#
- BPM4 AA5 H\_BPRM4\_PRDY#
- BPM3 Y6
- BPM2 AC4 H\_BPM1
- BPM1 AB5 H\_BPM0
- BPM0 AC6

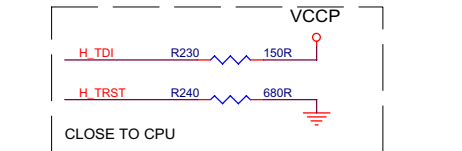
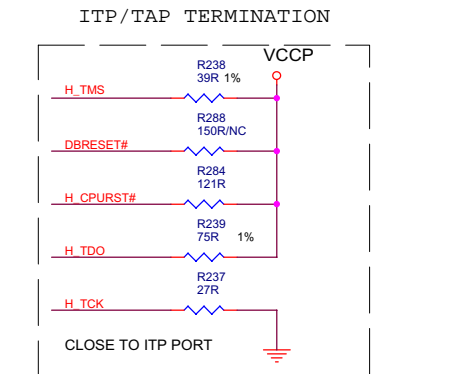
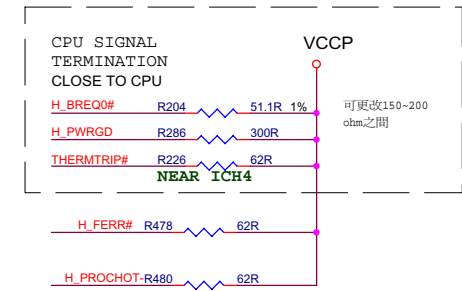
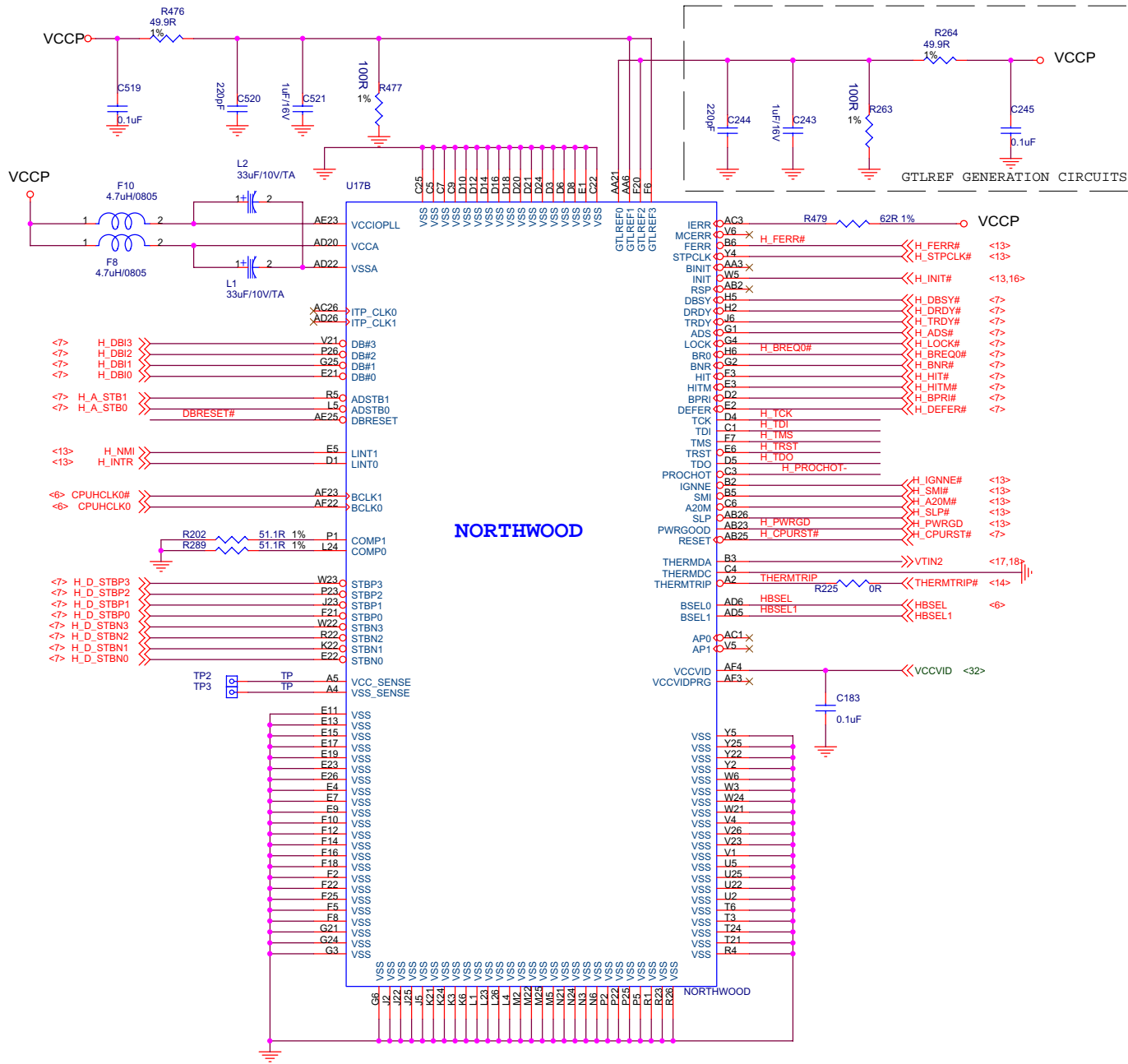


NORTHWOOD

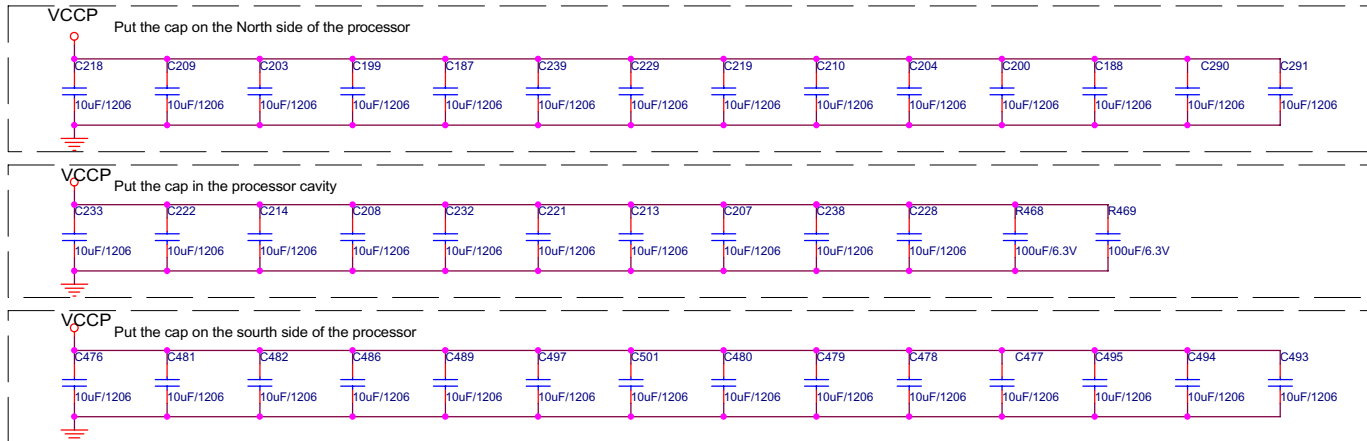
- H\_RS0#
- H\_RS1#
- H\_RS2#

- H\_D[0..63] H\_D[0..63]
- H\_A[3..31] H\_A[3..31]





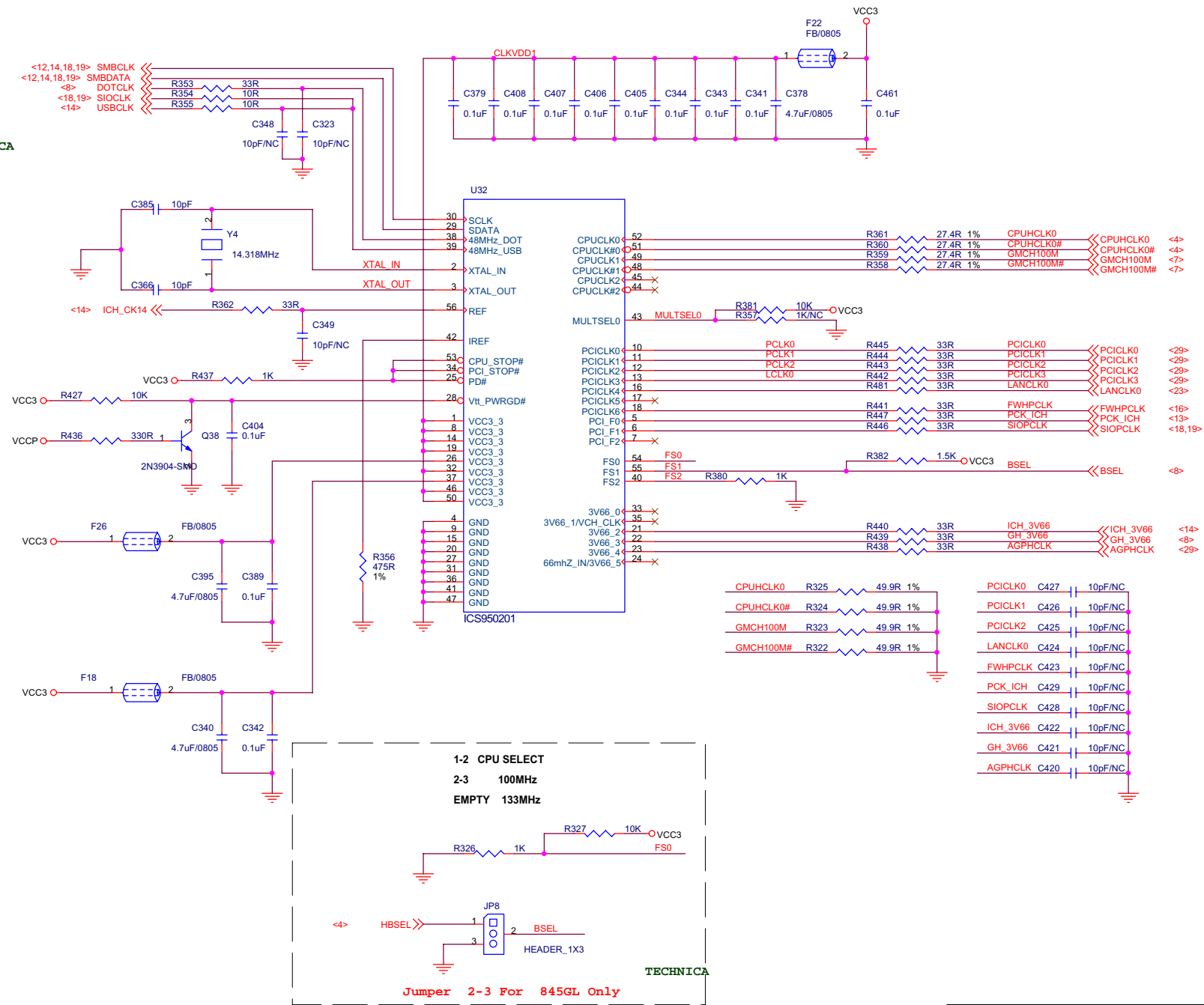
Technica House Incorporation			
Title INTEL Brookdale_G_PE CHIPSET			
Size	Document Number 478-PIN SOCKET : PART 2	Rev 0.1	
Date:	Tuesday, February 17, 2004	Sheet	4 of 34



<b>Technica House Incorporation</b>		
File INTEL Brookdale_G_PE CHIPSET		
Size	Document Number P4 CAPACITORS	Rev 0.1
Date:	Tuesday, February 17, 2004	Sheet 5 of 34

# Clock Synthesizer

TECHNICA

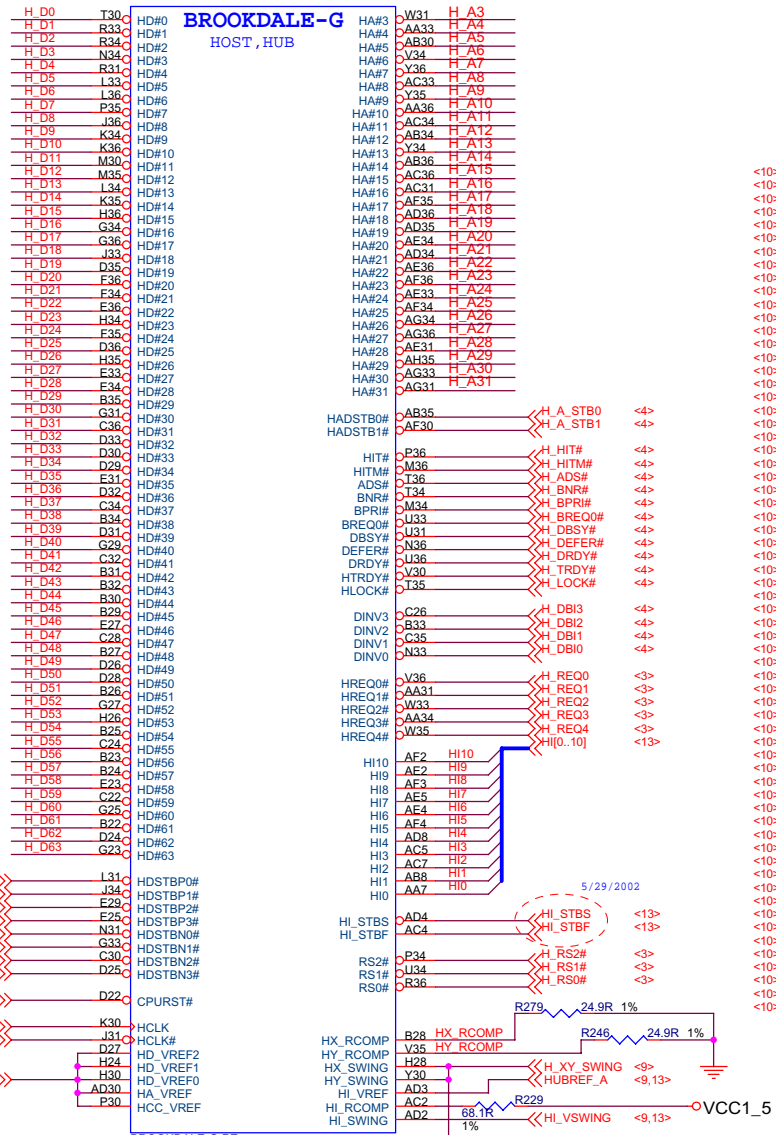


<b>Technica House Incorporation</b>			
<b>INTEL Brookdale-B CHIPSET</b>			
Size	Document Number	Rev 0.9	
<b>ICS950201_Clock Genertor - 00006</b>			
Date:	Tuesday, February 17, 2004	Sheet	8 of 34

H\_D[0..63] << H\_D[0..63] <-3>  
H\_A[3..31] << H\_A[3..31] <-3>

U16A

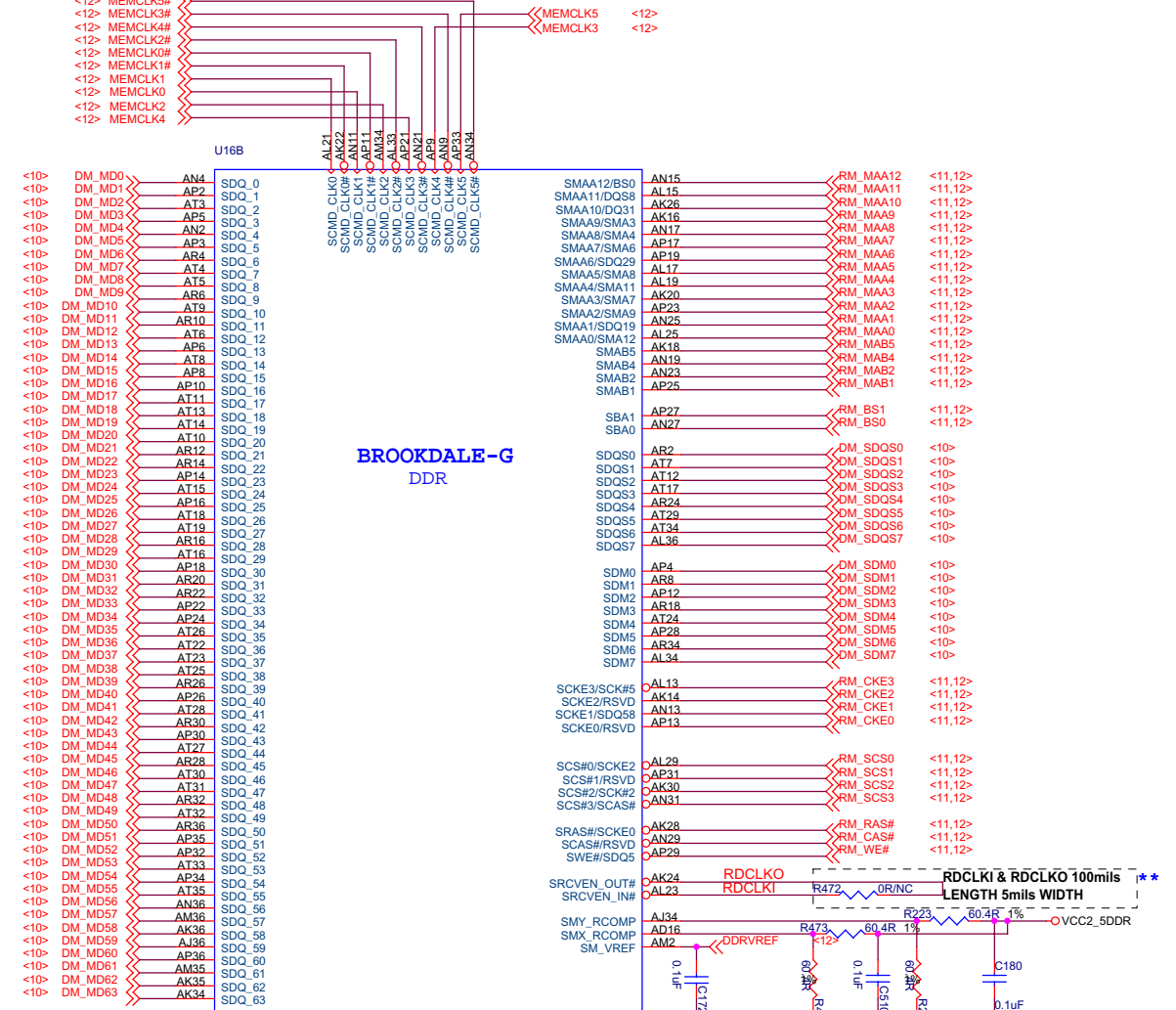
**BROOKDALE-G**  
HOST, HUB



BROOKDALE-G-PE

U16B

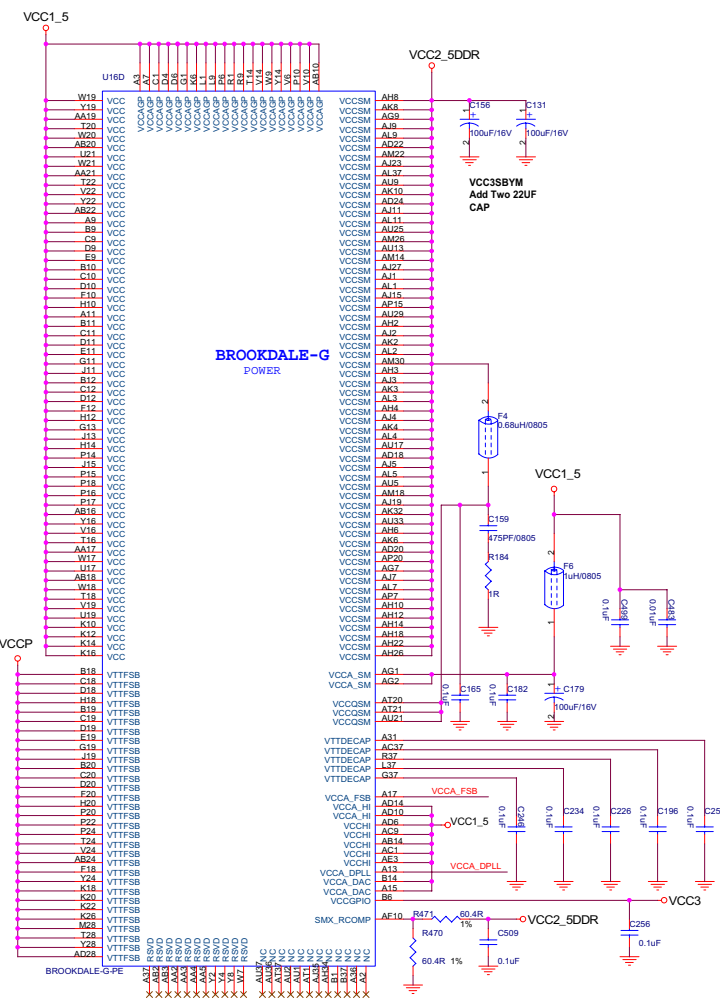
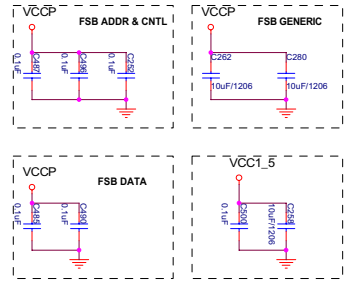
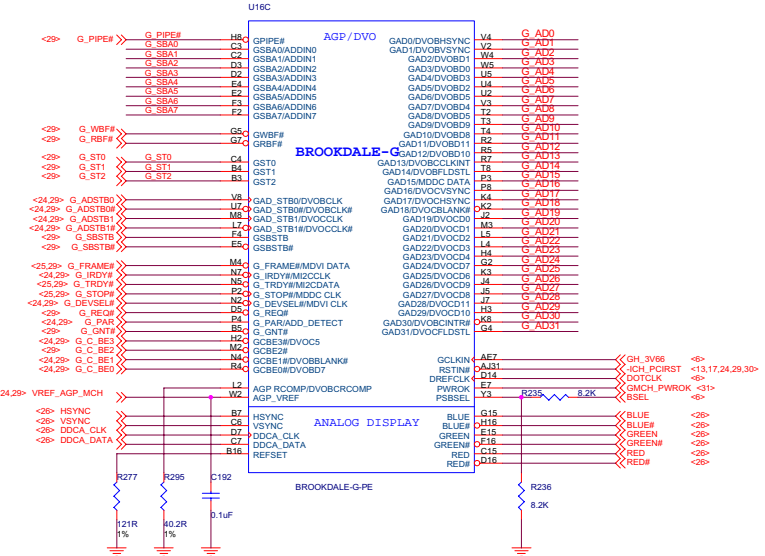
**BROOKDALE-G**  
DDR

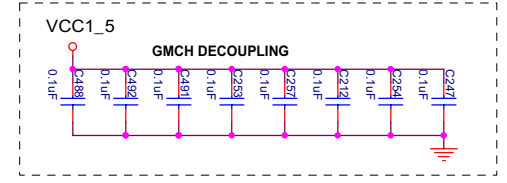
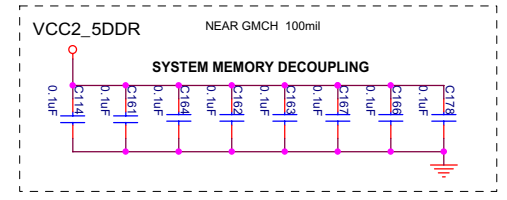
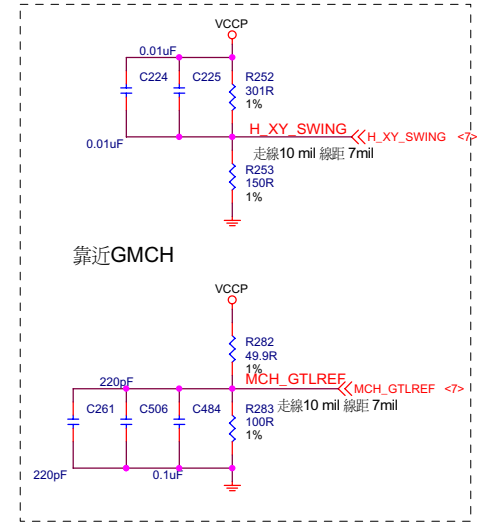
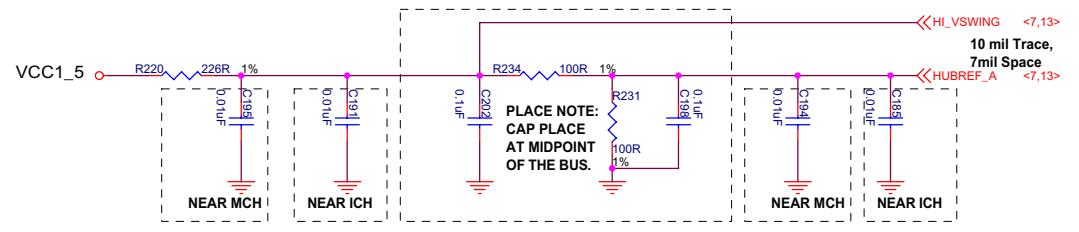
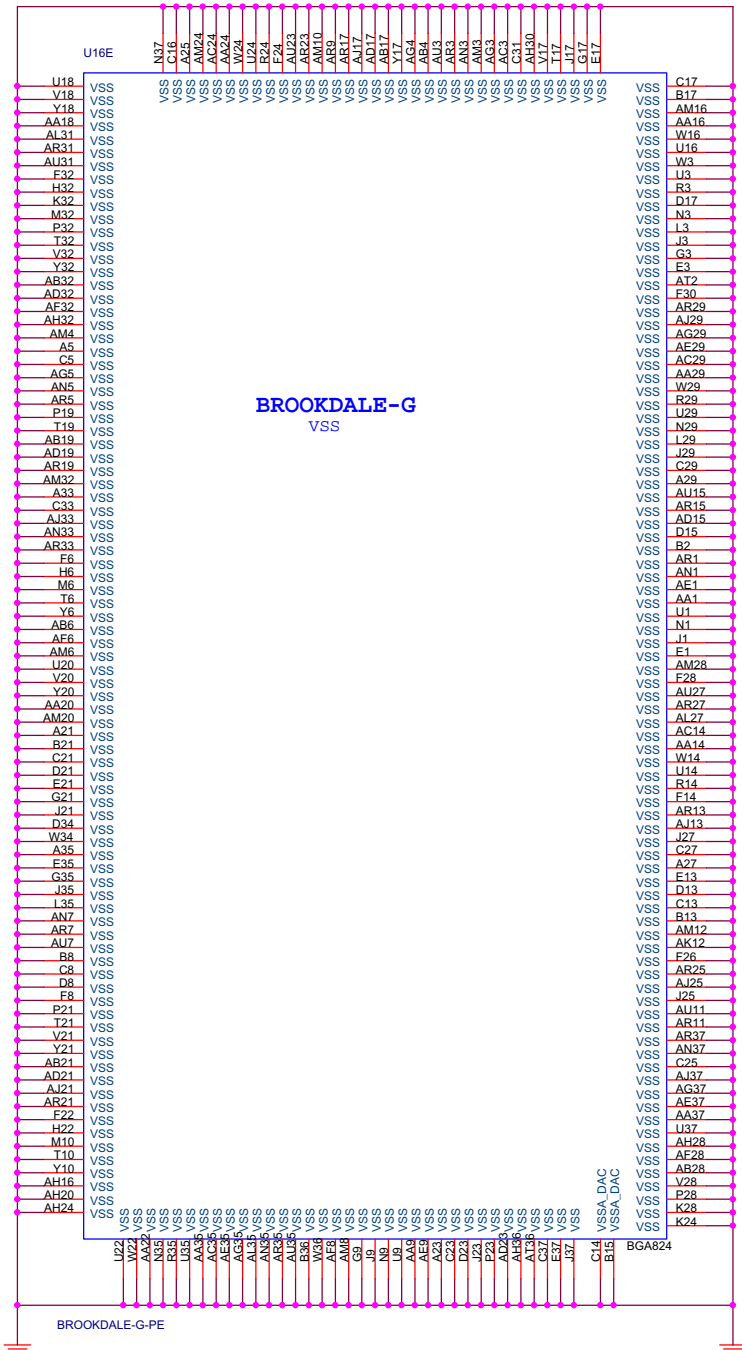


BROOKDALE-G-PE

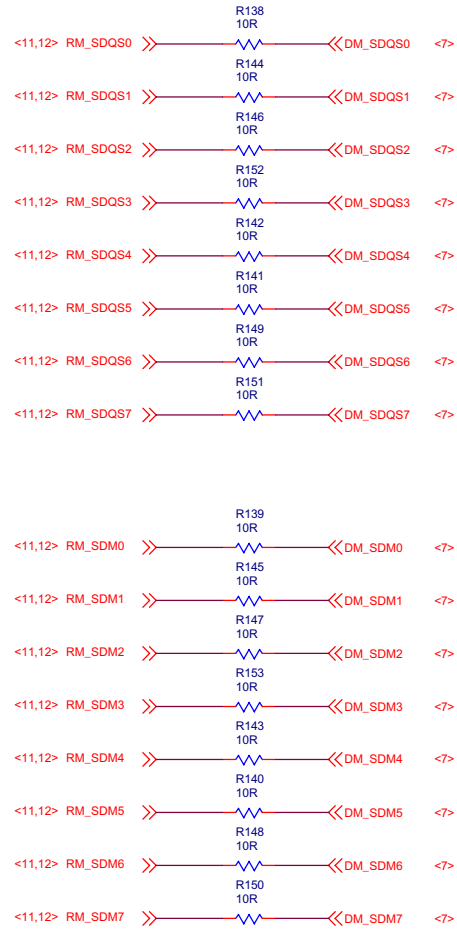
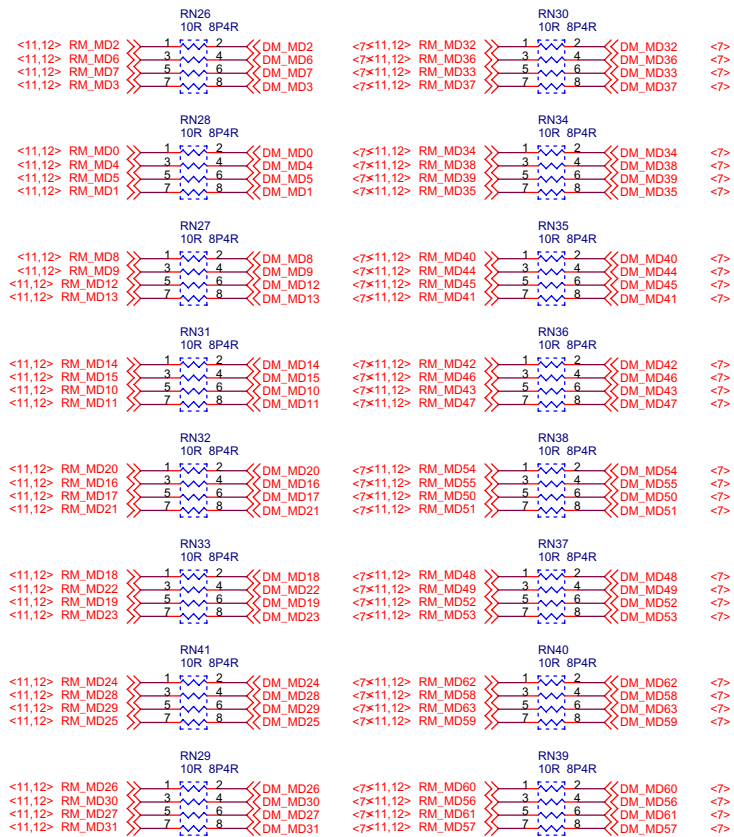
Technica House Incorporation		
Title INTEL Brookdale_G_PE CHIPSET		
Size	Document Number MCH : PART 1 (HOST INTERFACE)	Rev 0.1
Date	Tuesday, February 17, 2004	Sheet 7 of 34

<24,25,29> G\_AD0[0..31] >> G\_SBA0[0..31]  
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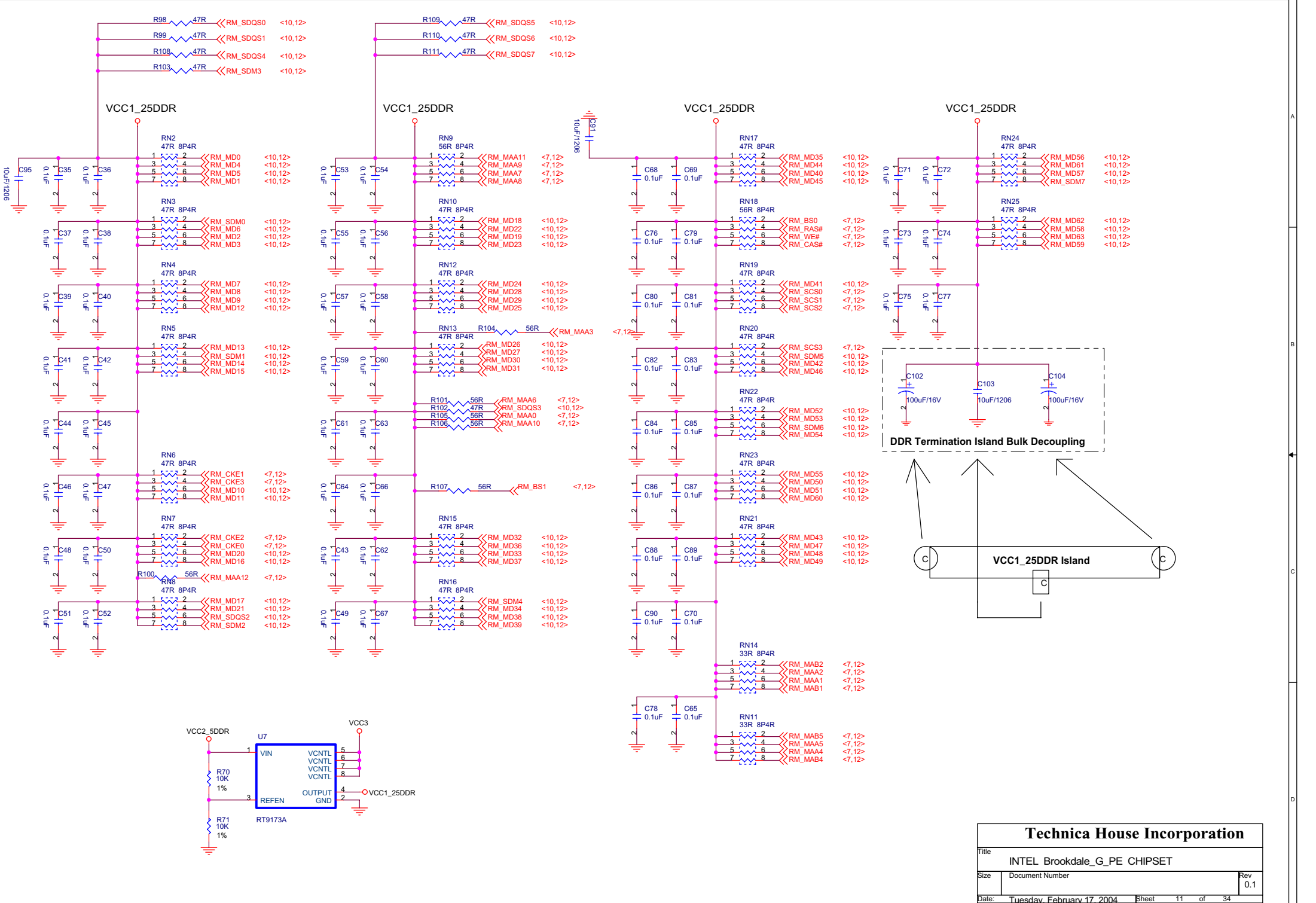


<b>Technica House Incorporation</b>		
Title INTEL Brookdale_G_PE CHIPSET		
Size	Document Number MCH : PART 3	Rev 0.1
Date:	Tuesday, February 17, 2004	Sheet 9 of 34



<b>Technica House Incorporation</b>		
Title INTEL Brookdale_G_PE CHIPSET		
Size A3	Document Number DIMM CLOCK TERMINATOR	Rev 0.1
Date: Tuesday, February 17, 2004	Sheet 10	of 34





VCC2\_5DDR

VCC2\_5DDR

<7,11> RM\_MAA0 <> RM\_MAA0 48 A0  
 <7,11> RM\_MAA1 <> RM\_MAA1 43 A1  
 <7,11> RM\_MAA2 <> RM\_MAA2 41 A2  
 <7,11> RM\_MAA3 <> RM\_MAA3 130 A3  
 <7,11> RM\_MAA4 <> RM\_MAA5 37 A4  
 <7,11> RM\_MAA5 <> RM\_MAA6 125 A5  
 <7,11> RM\_MAA6 <> RM\_MAA7 29 A6  
 <7,11> RM\_MAA7 <> RM\_MAA8 122 A7  
 <7,11> RM\_MAA8 <> RM\_MAA9 27 A8  
 <7,11> RM\_MAA9 <> RM\_MAA10 141 A9  
 <7,11> RM\_MAA10 <> RM\_MAA11 118 A10  
 <7,11> RM\_MAA11 <> RM\_MAA12 115 A11  
 <7,11> RM\_MAA12 <> 103 A12  
 <7,11> RM\_BS0 <> RM\_BS0 59 BA0  
 <7,11> RM\_BS1 <> RM\_BS1 52 BA1  
 <7,11> RM\_SCS0 <> RM\_SCS0 157 CS0  
 <7,11> RM\_SCS1 <> RM\_SCS1 158 CS1  
 <7,11> RM\_SCS2 <> RM\_SCS2 157 CS2  
 <7,11> RM\_SCS3 <> RM\_SCS3 158 CS3  
 <10,11> RM\_SDM0 <> RM\_SDM0 97 DOM0  
 <10,11> RM\_SDM1 <> RM\_SDM1 107 DOM1  
 <10,11> RM\_SDM2 <> RM\_SDM2 119 DOM2  
 <10,11> RM\_SDM3 <> RM\_SDM3 129 DOM3  
 <10,11> RM\_SDM4 <> RM\_SDM4 149 DOM4  
 <10,11> RM\_SDM5 <> RM\_SDM6 169 DOM5  
 <10,11> RM\_SDM6 <> RM\_SDM7 177 DOM6  
 <10,11> RM\_SDM7 <> 140 DOM8  
 <7,11> RM\_WE# <> RM\_WE# 63 WE  
 <7,11> RM\_CAS# <> RM\_CAS# 66 CAS  
 <7,11> RM\_RAS# <> RM\_RAS# 154 RAS  
 <7,11> RM\_CKE0 <> RM\_CKE0 21 CKE0  
 <7,11> RM\_CKE1 <> RM\_CKE1 111 CKE1  
 <7> MEMCLK0 <> MEMCLK0# 16 CK0/DNU  
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 <7> MEMCLK1 <> MEMCLK1# 137 CK1  
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 <7> MEMCLK2 <> MEMCLK2# 76 CK2/DNU  
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 <10,11> RM\_SDQS0 <> RM\_SDQS0 5 DQS0  
 <10,11> RM\_SDQS1 <> RM\_SDQS1 14 DQS1  
 <10,11> RM\_SDQS2 <> RM\_SDQS2 25 DQS2  
 <10,11> RM\_SDQS3 <> RM\_SDQS3 36 DQS3  
 <10,11> RM\_SDQS4 <> RM\_SDQS4 56 DQS4  
 <10,11> RM\_SDQS5 <> RM\_SDQS5 67 DQS5  
 <10,11> RM\_SDQS6 <> RM\_SDQS6 78 DQS6  
 <10,11> RM\_SDQS7 <> RM\_SDQS7 86 DQS7  
 <10,11> RM\_SDQS8 <> 47 DQS8  
 <6,14,78,19> SMBDATA <> SMBDATA 91 SDA  
 <6,14,18,19> SMBCLK <> SMBCLK 92 SCL

SA0 181  
 SA1 182  
 SA2 183  
 VREF 1  
 VDDID 82  
 VDDSPD 184  
 NC 9  
 NC 10  
 NC 101  
 NC 102  
 NC 173  
 NC 167  
 NC/FETEN 167  
 WP 90  
 DDR\_DIMM184 3, 11, 18, 26, 34, 42, 50, 58, 66, 74, 82, 90, 98, 106, 114, 122, 130, 138, 146, 154, 162, 170, 178

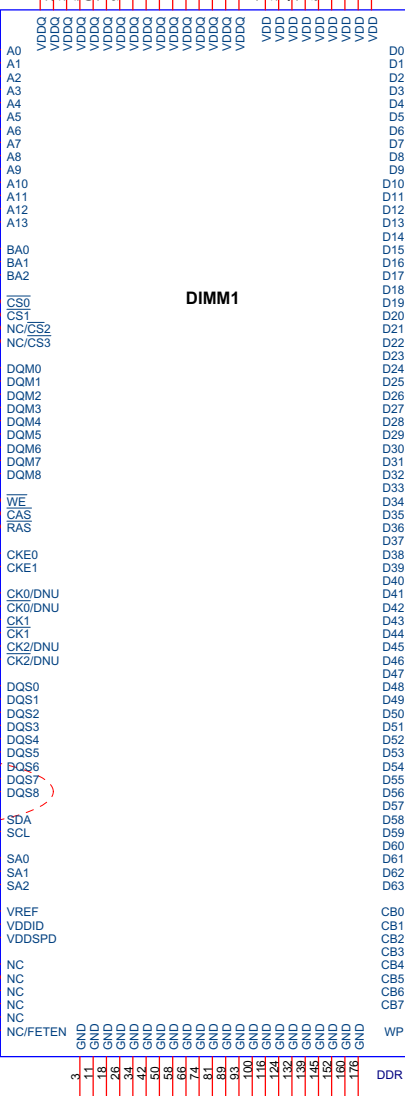
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 R125 10K  
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VCC2\_5DDR  
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VCC2\_5DDR  
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 C112 0.1uF

VCC2\_5DDR  
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 C112 0.1uF

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 C112 0.1uF



DIMM1

<7,11> RM\_MAB1 <> RM\_MAB1 48 A0  
 <7,11> RM\_MAB2 <> RM\_MAB2 41 A2  
 <7,11> RM\_MAB3 <> RM\_MAB3 130 A3  
 <7,11> RM\_MAB4 <> RM\_MAB5 37 A4  
 <7,11> RM\_MAB5 <> RM\_MAB6 125 A5  
 <7,11> RM\_MAB6 <> RM\_MAB7 29 A6  
 <7,11> RM\_MAB7 <> RM\_MAB8 122 A7  
 <7,11> RM\_MAB8 <> RM\_MAB9 27 A8  
 <7,11> RM\_MAB9 <> RM\_MAB10 141 A9  
 <7,11> RM\_MAB10 <> RM\_MAB11 118 A10  
 <7,11> RM\_MAB11 <> RM\_MAB12 115 A11  
 <7,11> RM\_MAB12 <> 103 A12  
 <7,11> RM\_BS0 <> RM\_BS0 59 BA0  
 <7,11> RM\_BS1 <> RM\_BS1 52 BA1  
 <7,11> RM\_SCS2 <> RM\_SCS2 157 CS2  
 <7,11> RM\_SCS3 <> RM\_SCS3 158 CS3  
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 <10,11> RM\_SDM0 <> RM\_SDM0 97 DOM0  
 <10,11> RM\_SDM1 <> RM\_SDM1 107 DOM1  
 <10,11> RM\_SDM2 <> RM\_SDM2 119 DOM2  
 <10,11> RM\_SDM3 <> RM\_SDM3 129 DOM3  
 <10,11> RM\_SDM4 <> RM\_SDM4 149 DOM4  
 <10,11> RM\_SDM5 <> RM\_SDM6 169 DOM5  
 <10,11> RM\_SDM6 <> RM\_SDM7 177 DOM6  
 <10,11> RM\_SDM7 <> 140 DOM8  
 <7,11> RM\_WE# <> RM\_WE# 63 WE  
 <7,11> RM\_CAS# <> RM\_CAS# 66 CAS  
 <7,11> RM\_RAS# <> RM\_RAS# 154 RAS  
 <7,11> RM\_CKE2 <> RM\_CKE2 21 CKE2  
 <7,11> RM\_CKE3 <> RM\_CKE3 111 CKE3  
 <7> MEMCLK3 <> MEMCLK3# 16 CK0/DNU  
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 <10,11> RM\_SDQS2 <> RM\_SDQS2 25 DQS2  
 <10,11> RM\_SDQS3 <> RM\_SDQS3 36 DQS3  
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 <10,11> RM\_SDQS5 <> RM\_SDQS5 67 DQS5  
 <10,11> RM\_SDQS6 <> RM\_SDQS6 78 DQS6  
 <10,11> RM\_SDQS7 <> RM\_SDQS7 86 DQS7  
 <10,11> RM\_SDQS8 <> 47 DQS8  
 <6,14,78,19> SMBDATA <> SMBDATA 91 SDA  
 <6,14,18,19> SMBCLK <> SMBCLK 92 SCL

SA0 181  
 SA1 182  
 SA2 183  
 VREF 1  
 VDDID 82  
 VDDSPD 184  
 NC 9  
 NC 10  
 NC 101  
 NC 102  
 NC 173  
 NC 167  
 NC/FETEN 167  
 WP 90  
 DDR\_DIMM184 3, 11, 18, 26, 34, 42, 50, 58, 66, 74, 82, 90, 98, 106, 114, 122, 130, 138, 146, 154, 162, 170, 178

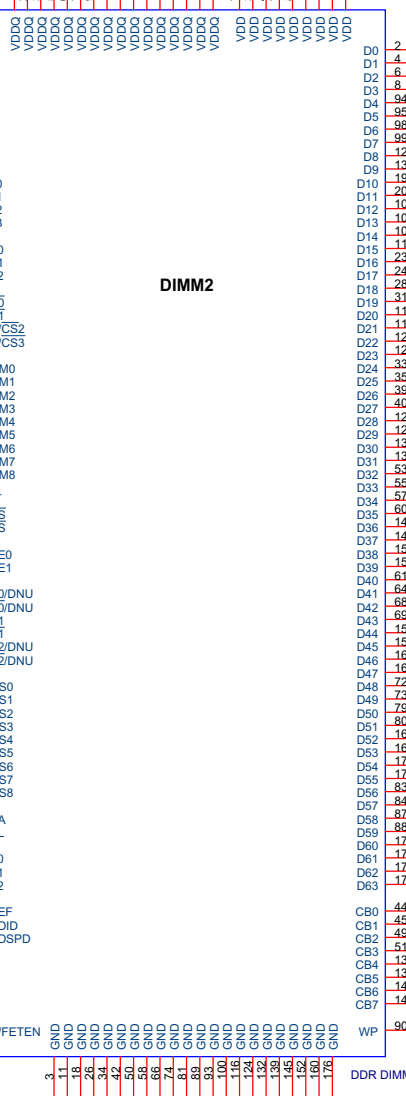
05/29/2002  
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 C113 0.1uF

VCC2\_5DDR  
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 R127 10K  
 C113 0.1uF

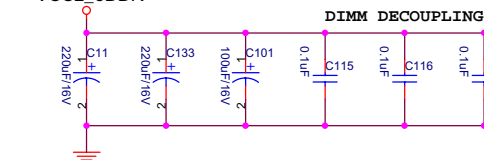
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 C113 0.1uF

VCC2\_5DDR  
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 R127 10K  
 C113 0.1uF

VCC2\_5DDR  
 <7> DDRVREF <> DDRVREF 1  
 R127 10K  
 C113 0.1uF

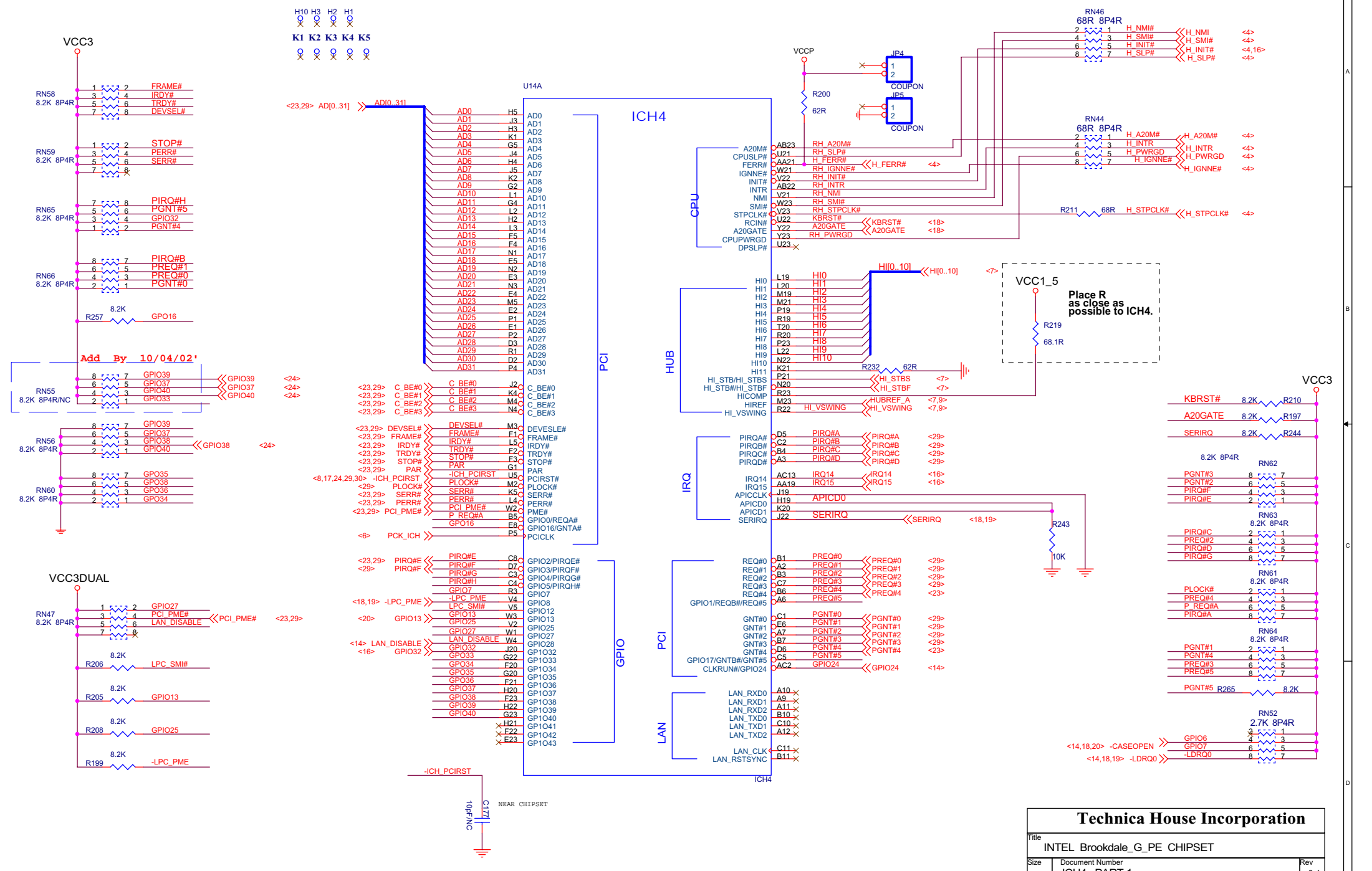


DIMM2



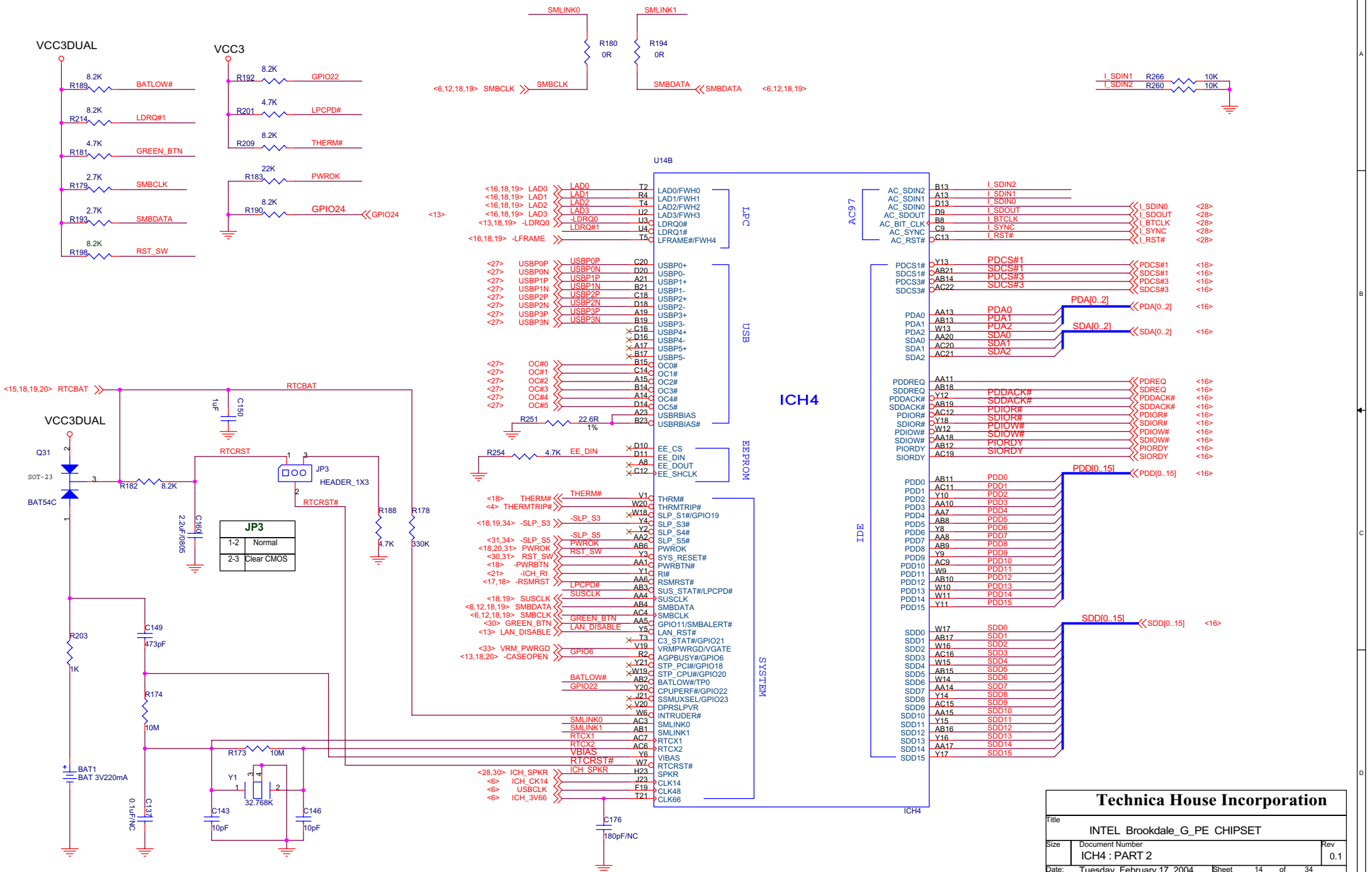
<b>Technica House Incorporation</b>		
Title INTEL Brookdale_G_PE CHIPSET		
Size	Document Number SYSTEM MEMORY : DIMM1 & DIMM2	Rev 0.1
Date:	Tuesday, February 17, 2004	Sheet 12 of 34

# ICH4 PART1



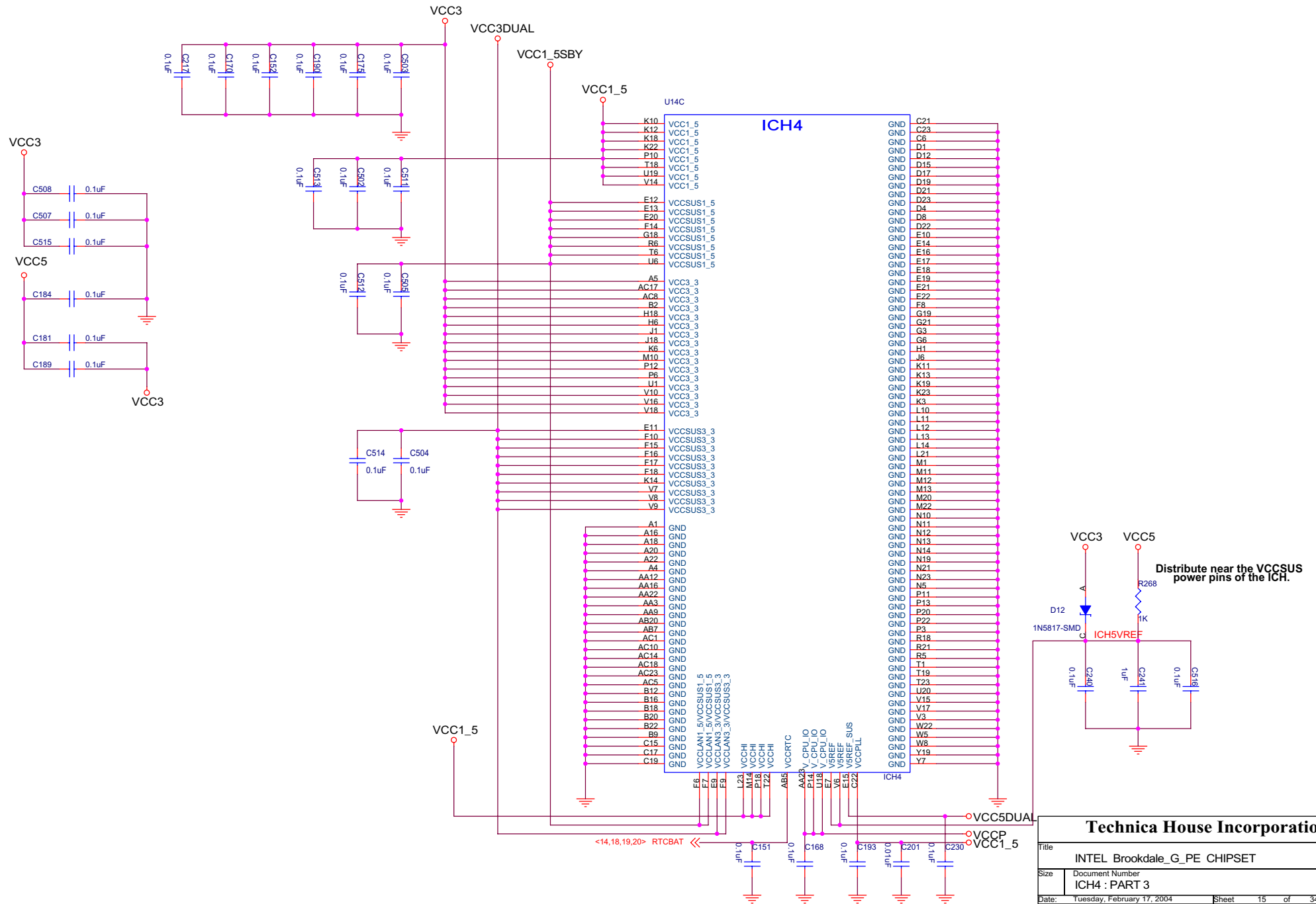
Technica House Incorporation		
Title INTEL Brookdale_G_PE CHIPSET		
Size	Document Number ICH4 : PART 1	Rev 0.1
Date: Tuesday, February 17, 2004    Sheet 13 of 34		

# ICH4 PART2



Technica House Incorporation		
Title: INTEL Brookdale_G_PE CHIPSET		
Size: Document Number	Rev: 0.1	
ICH4 : PART 2		
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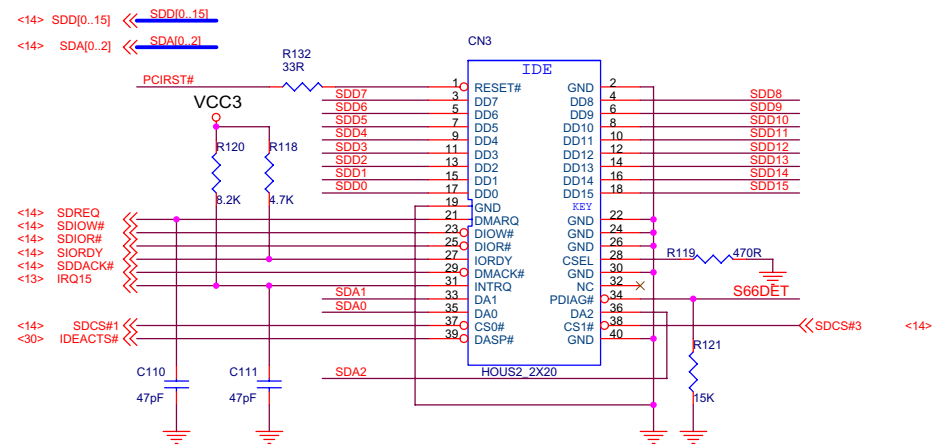
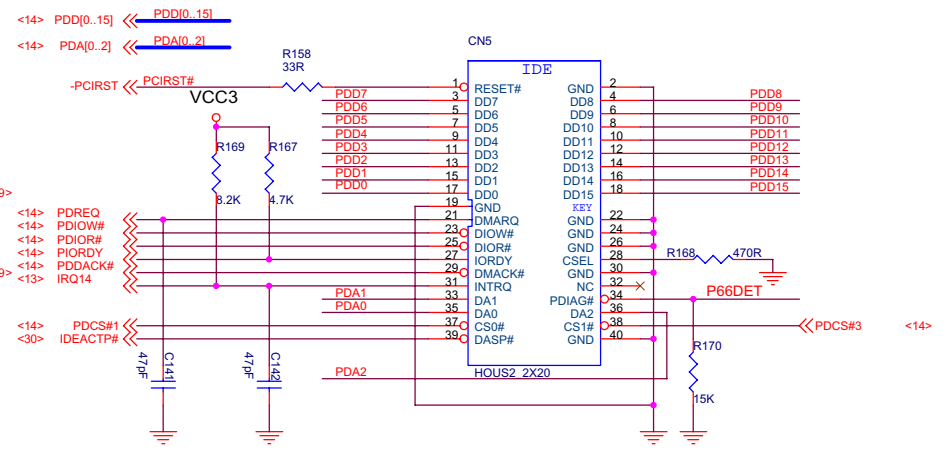
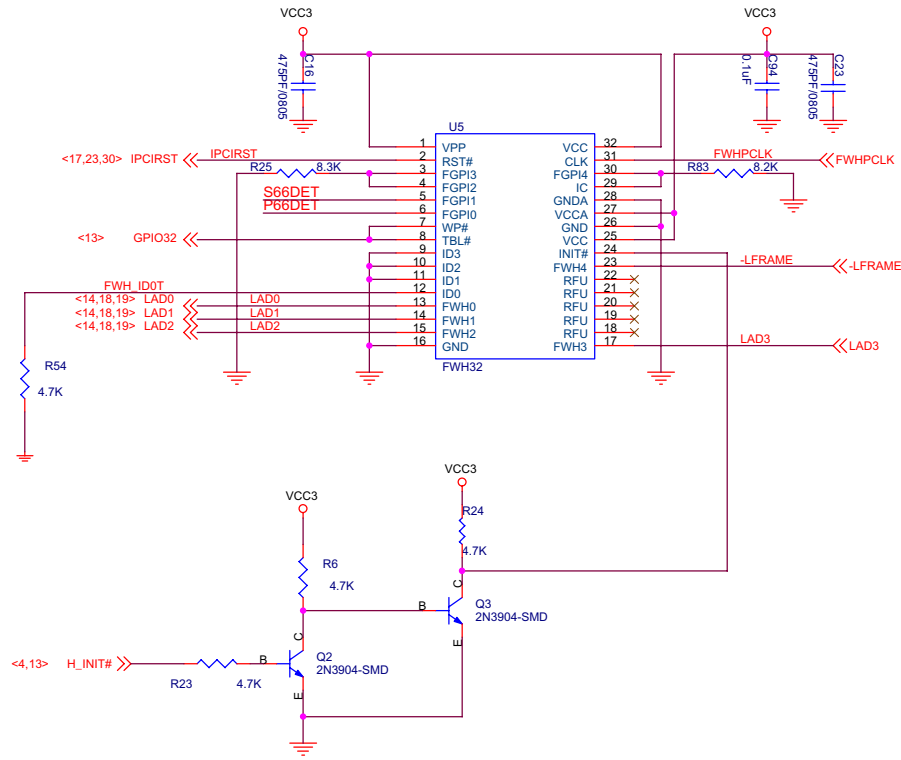
# ICH4 PART3



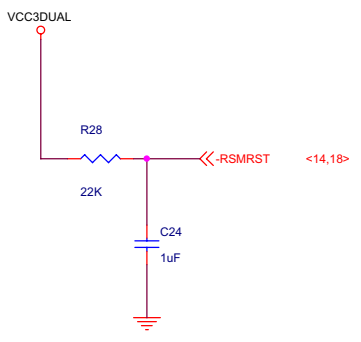
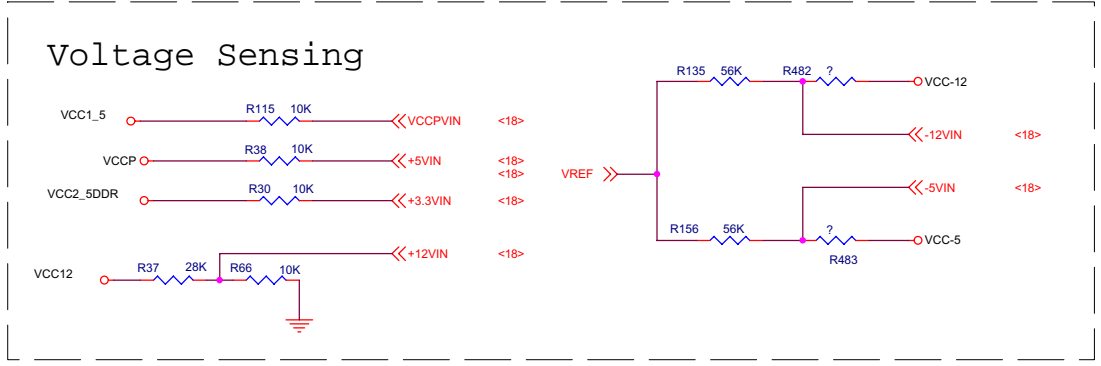
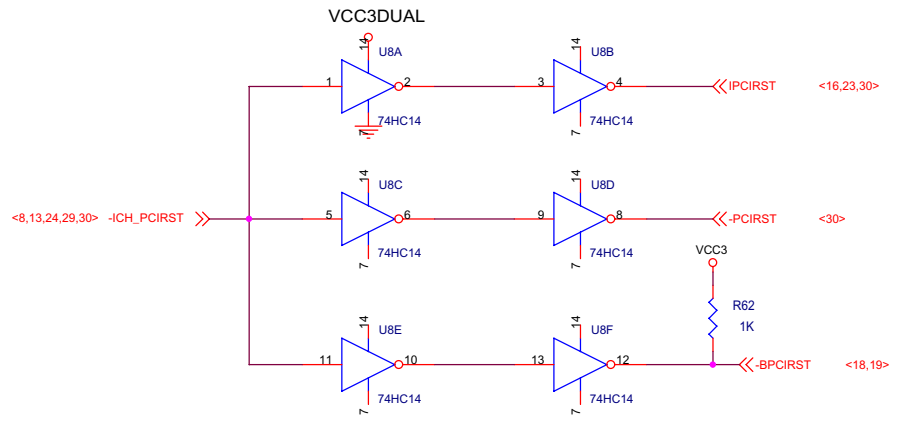
Distribute near the VCCSUS power pins of the ICH.

Technica House Incorporation		
Title INTEL Brookdale_G_PE CHIPSET		
Size	Document Number ICH4 : PART 3	Rev 0.1
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# FirmWare Hub (FWH) Socket

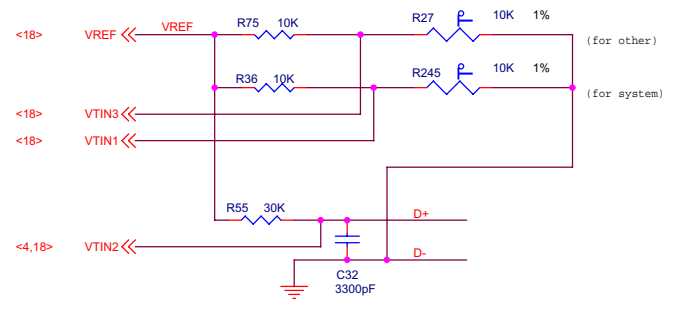


<b>Technica House Incorporation</b>		
Title		
INTEL Brookdale_G_PE CHIPSET		
Size	Document Number	Rev
	FIRMWARE HUB (FWH) / IDE(ATA100)	0.1
Date:	Tuesday, February 17, 2004	Sheet 16 of 34

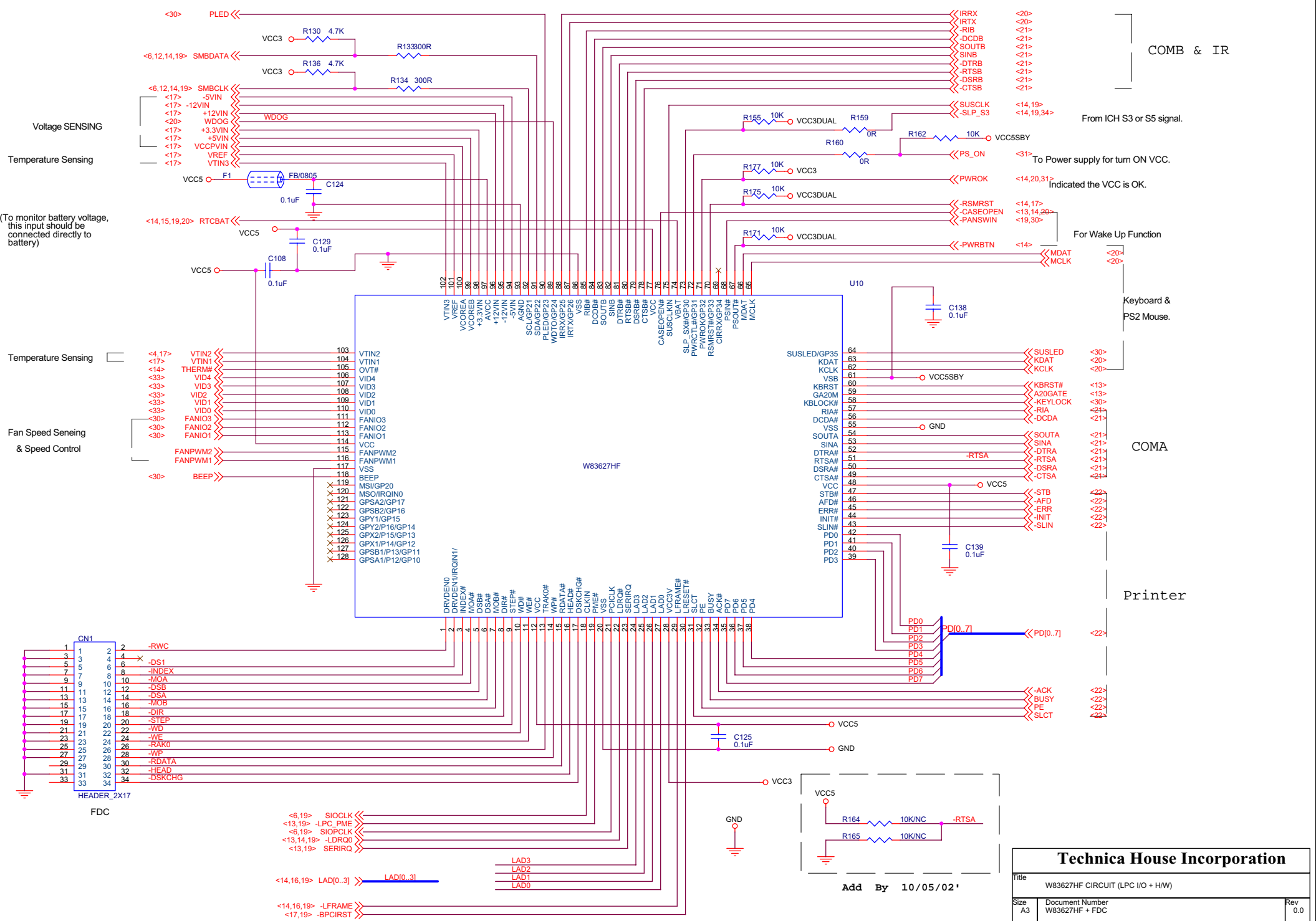


# Hardware Monitor circuits

## Temperature Sensing



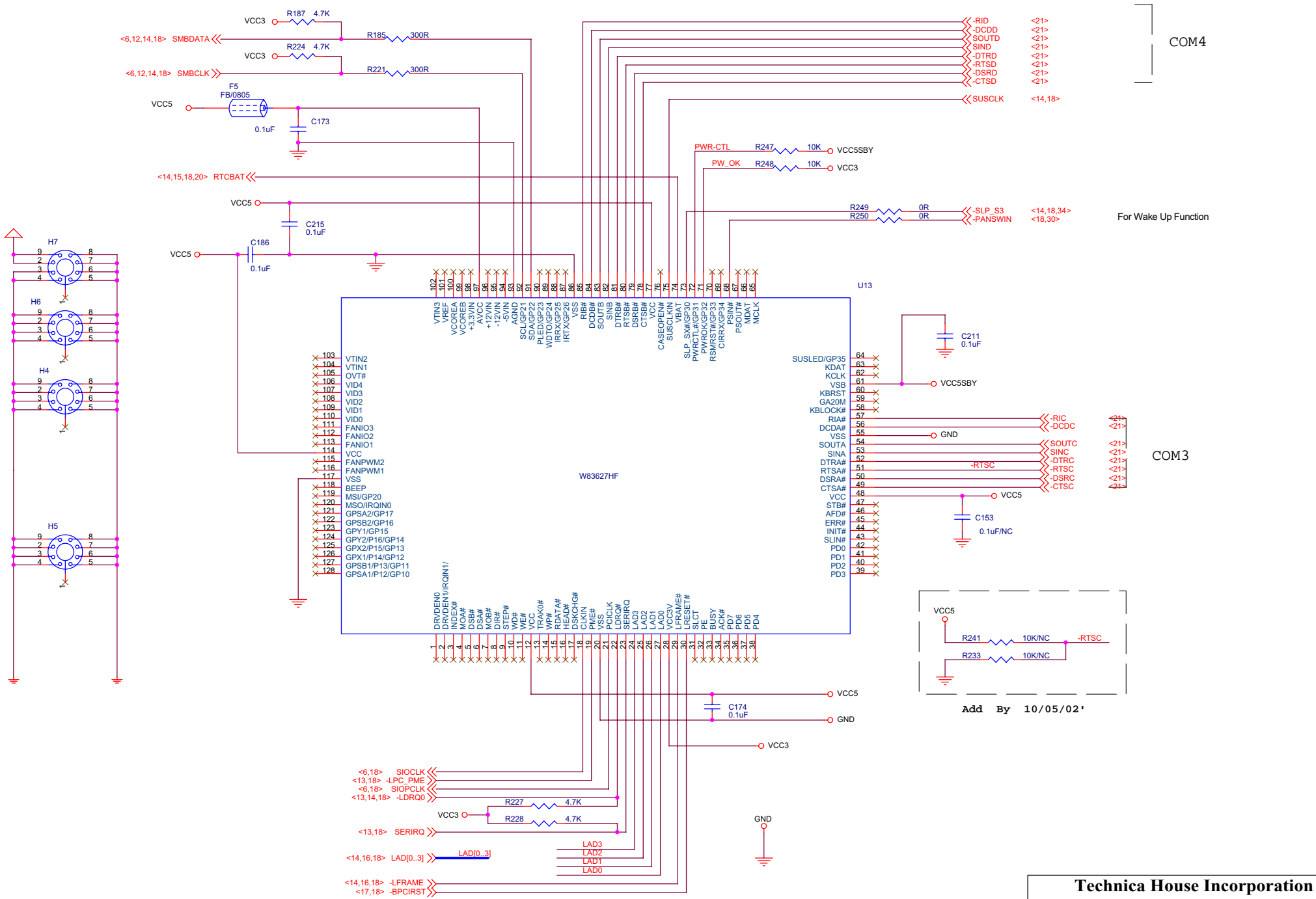
<b>Technica House Incorporation</b>		
Title: THERMISTOR, SMART CARD READER		
Size: A3	Document Number: ITTM-CG-99008	Rev: 0.0
Date: Tuesday, February 17, 2004	Sheet: 17	of 34



<b>Technica House Incorporation</b>		
Title	W83627HF CIRCUIT (LPC I/O + HW)	
Size	Document Number	Rev
A3	W83627HF + FDC	0.0
Date:	Tuesday, February 17, 2004	Sheet 18 of 34

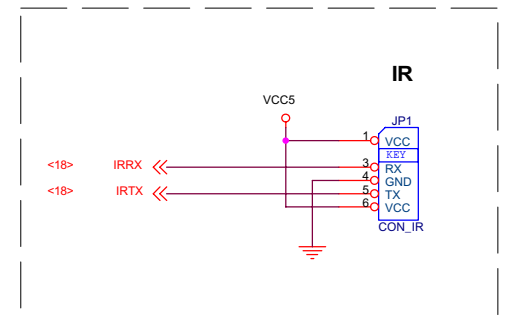
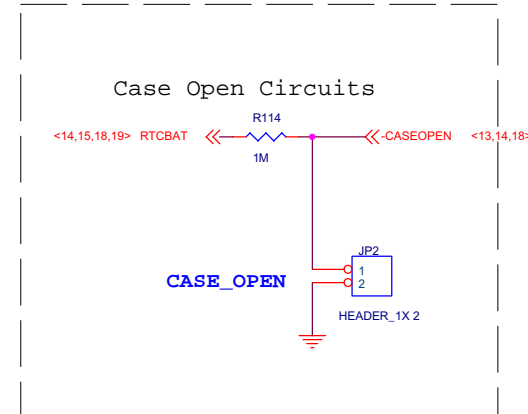
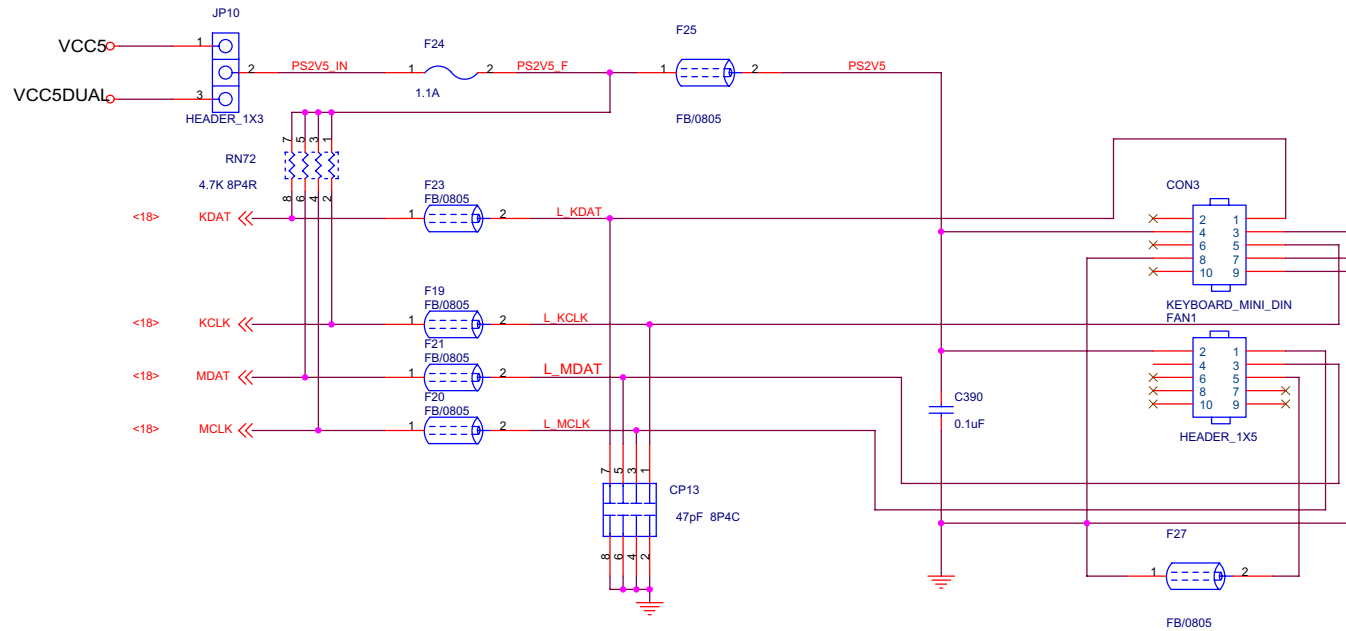
Add By 10/05/02'



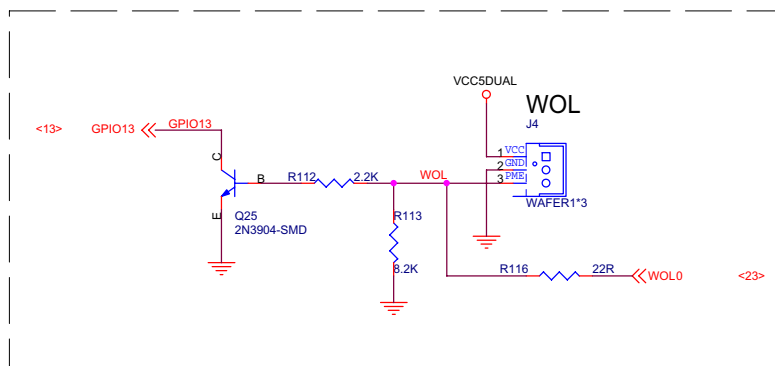
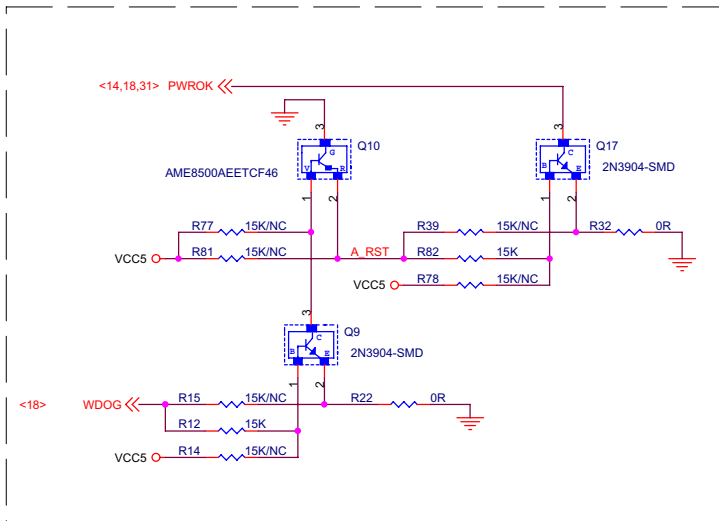


<b>Technica House Incorporation</b>		
Title	W83627HF CIRCUIT (LPC I/O + HW)	
Size	Document Number	Rev
A3	W83627HF + FDC	0.0
Date:	Tuesday, February 17, 2004	Sheet 19 of 34

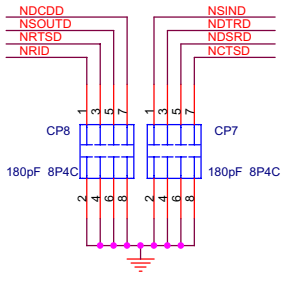
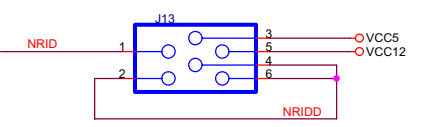
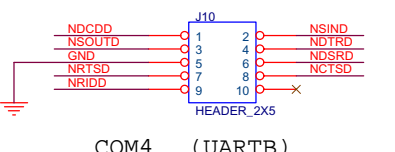
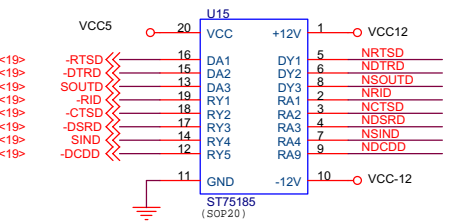
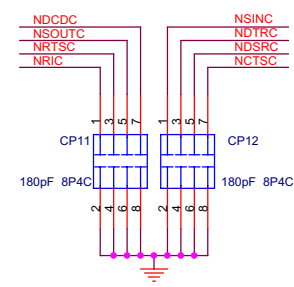
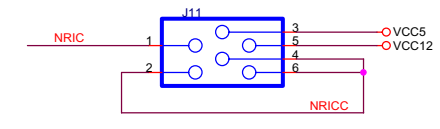
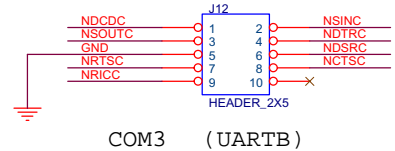
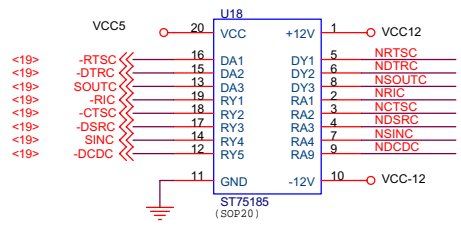
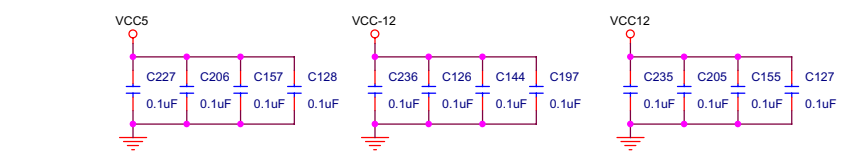
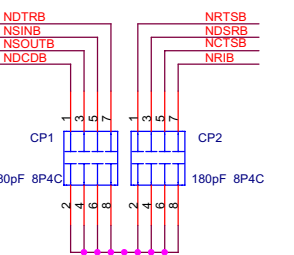
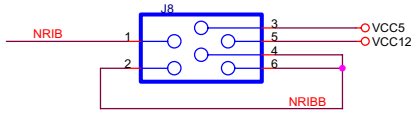
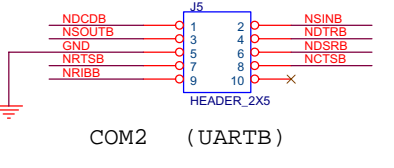
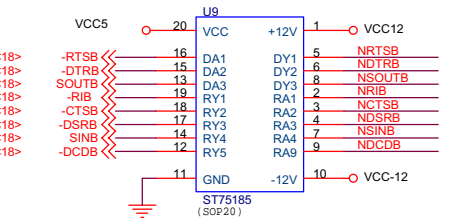
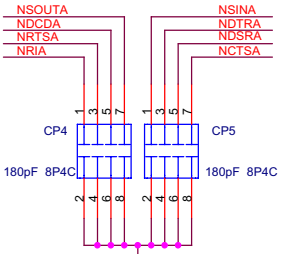
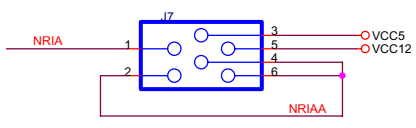
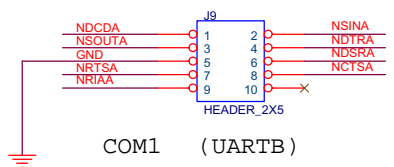
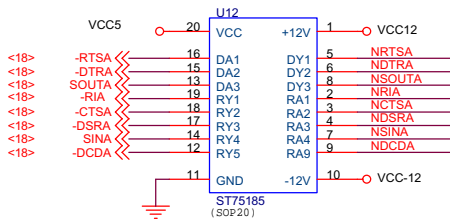
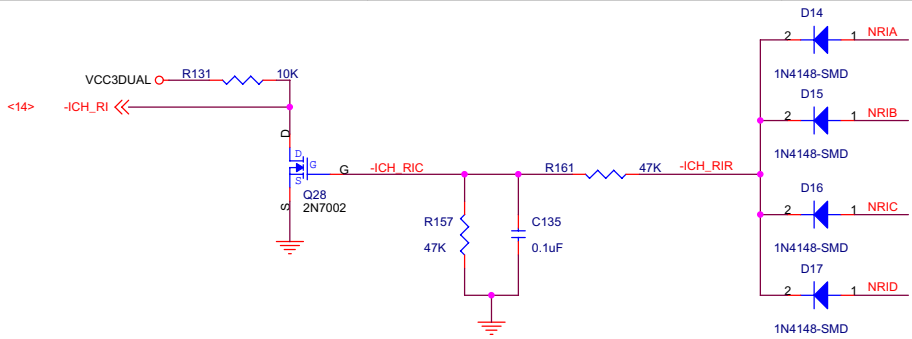
# Serial Port/COM Headers



Add By 10/04/02'

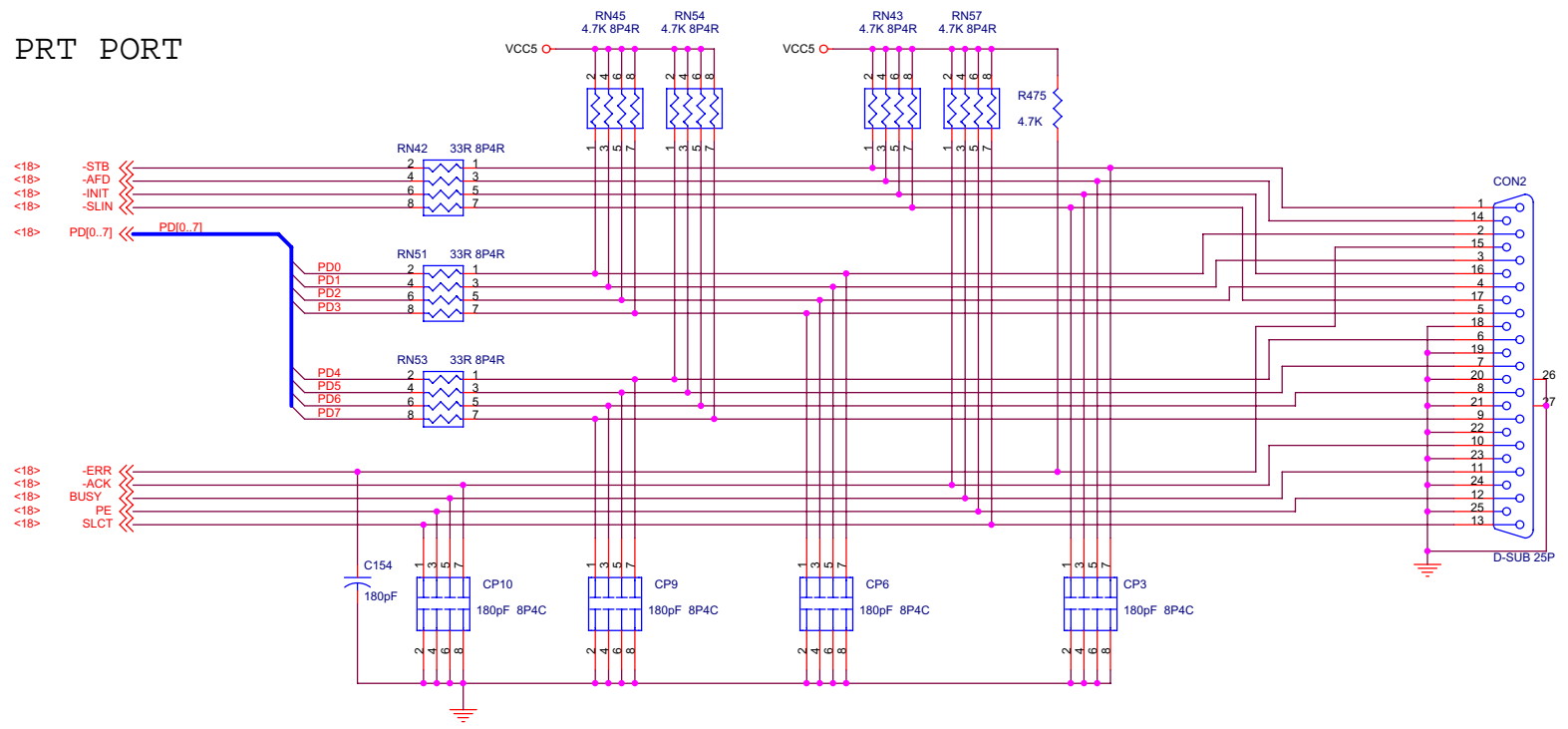


<b>Technica House Incorporation</b>		
Title	INTEL Brookdale-G CHIPSET	
Size	Document Number	Rev
	SERIAL PORT/COM/IR/CIR HEADER	0.0
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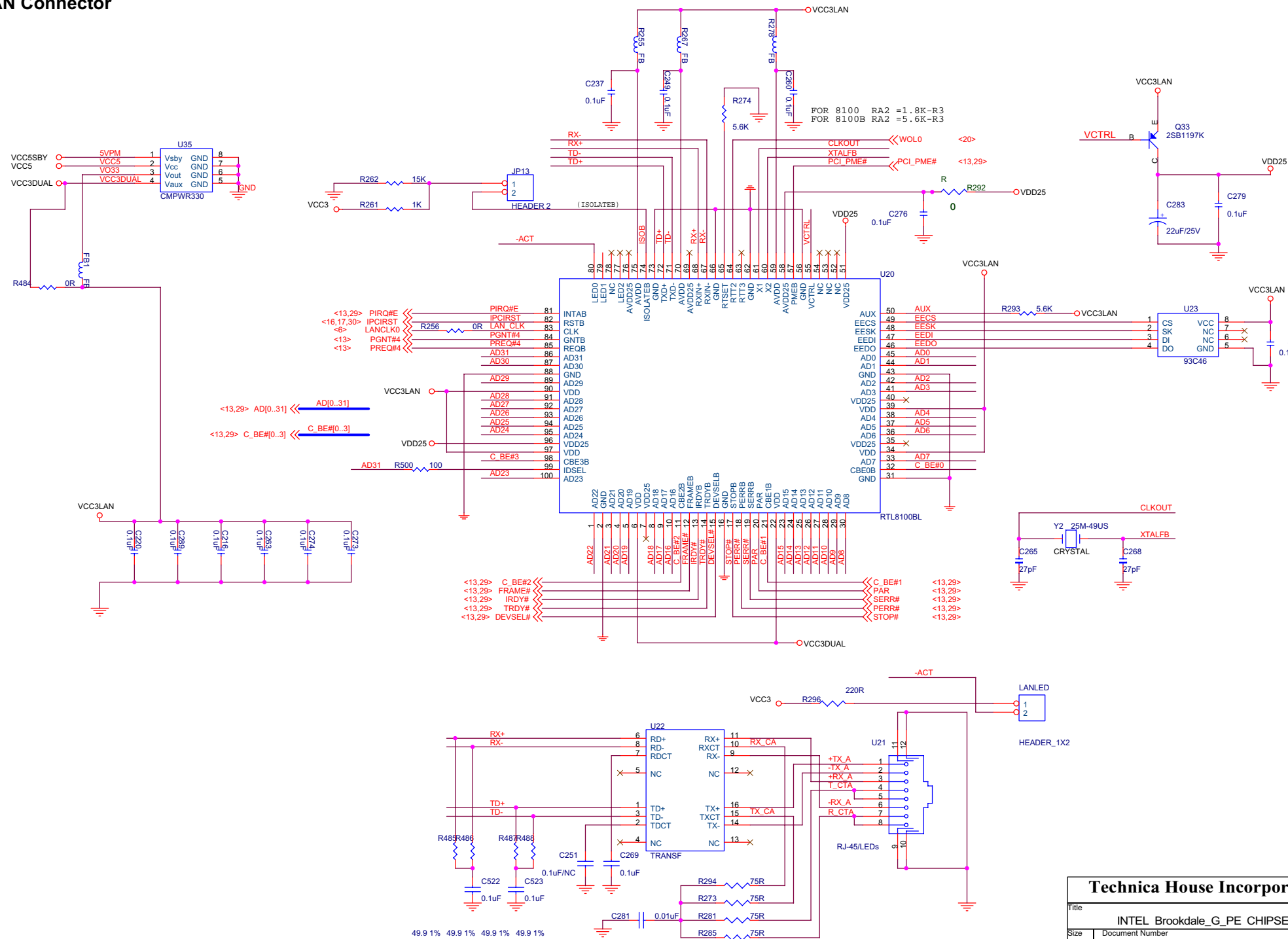
# Parallel Port Header

PRT PORT

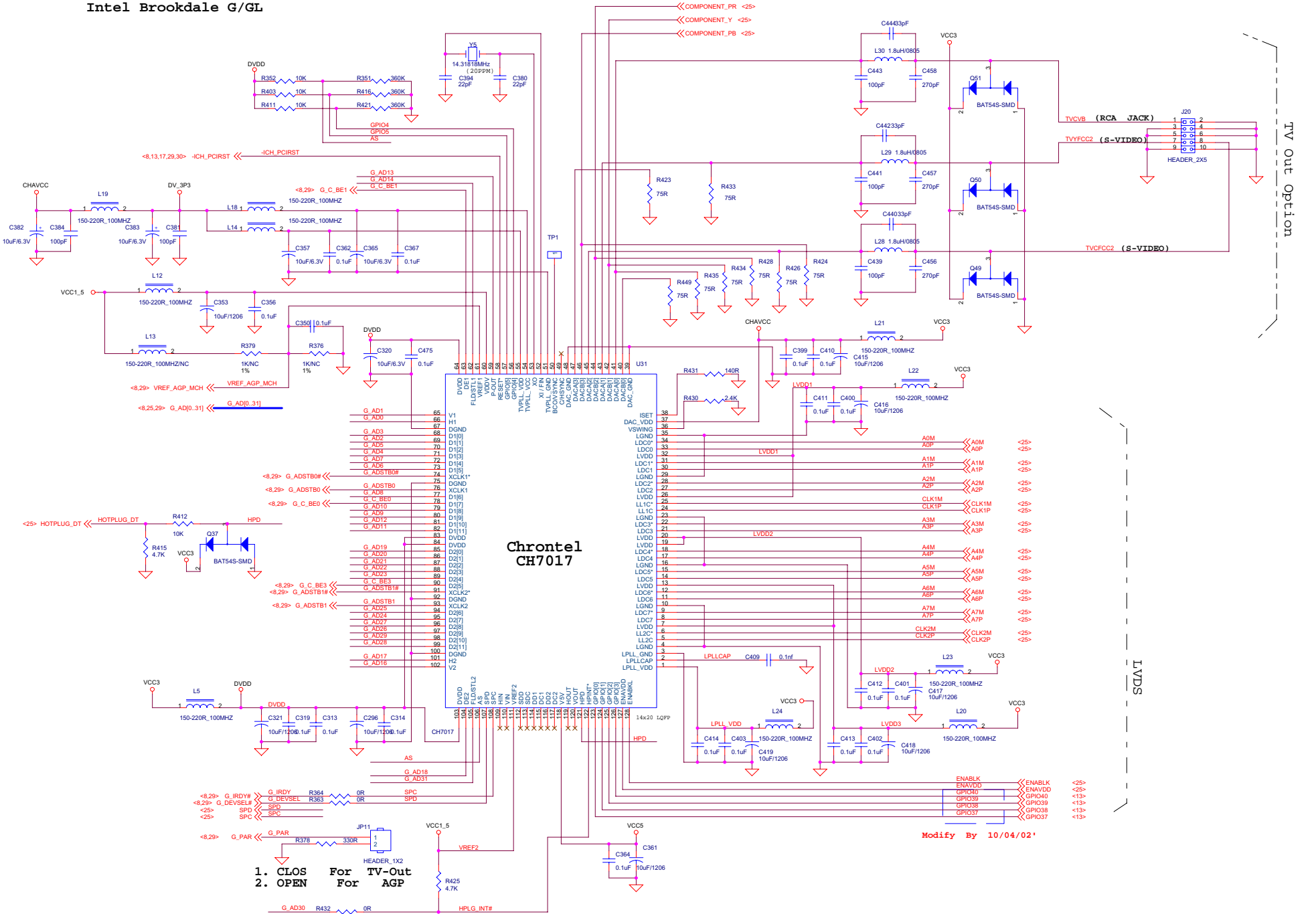


<b>Technica House Incorporation</b>		
Title INTEL Brookdale-G CHIPSET		
Size	Document Number	Rev
	PARALLEL PORT / GAME PORT	0.0
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# LAN Connector



**Preliminary Chrontel CH7017 reference design  
for  
Intel Brookdale G/GL**



**Chrontel  
CH7017**

1. CLOS For TV-Out  
2. OPEN For AGP

Modify By 10/04/02'

<b>Technica House Incorporation</b>		
Title INTEL Brookdale_G_PE CHIPSET		
Size 478-PIN SOCKET : PART 1	Document Number 478-PIN SOCKET : PART 1	Rev 0.1
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Note:  
Trace for LVDS signals should be closely-coupled and layout for 100 ohm differential impedance:  
LVDS signals pairs : ( A0x thru A7x , CLK1x and CLK2x)

+3.3V Voltage Regulator circuit for CH7017's DAC\_VDD and TVPLL

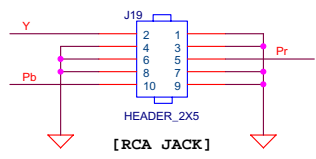
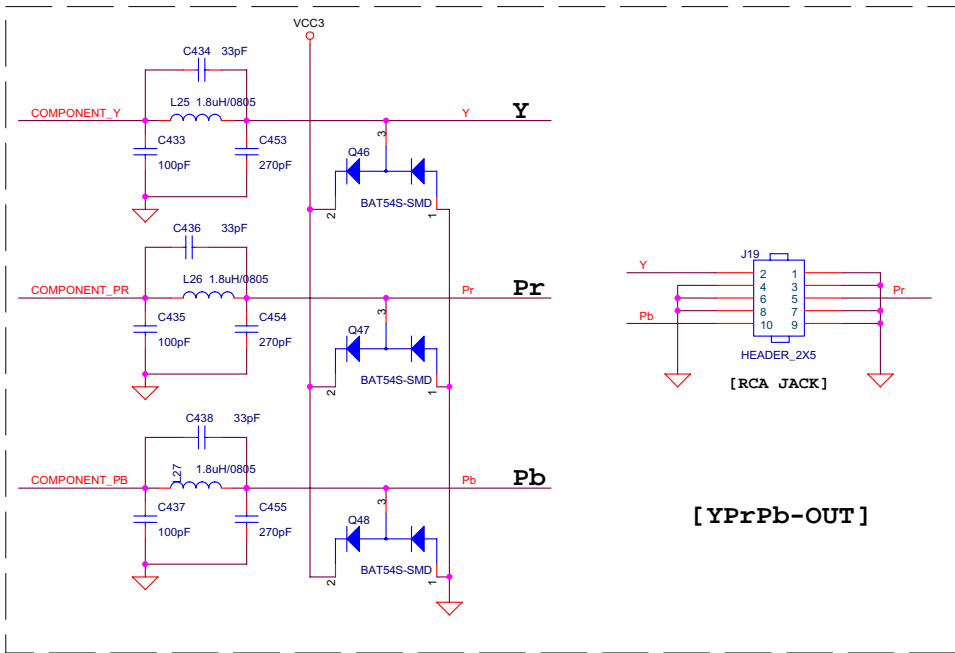
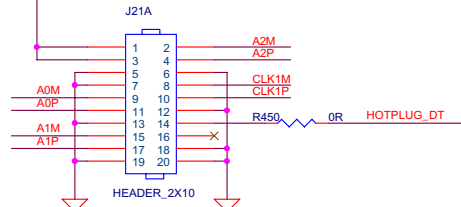
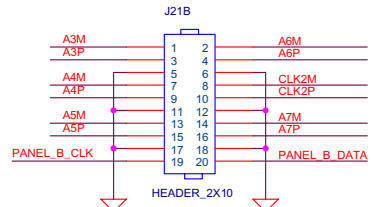
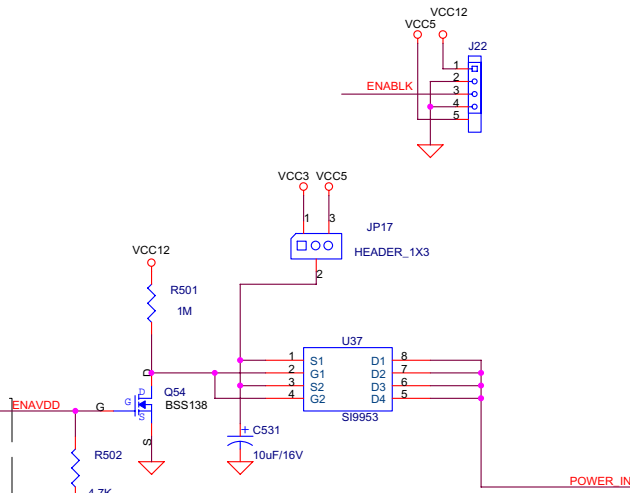
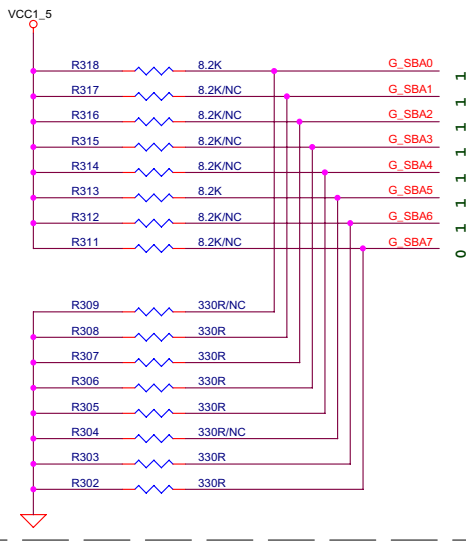
[LVDS Connector]

- <24> HOTPLUG\_DT >> HOTPLUG\_DT
- <24> A0M >> A0M
- <24> A0P >> A0P
- <24> A1M >> A1M
- <24> A1P >> A1P
- <24> A2M >> A2M
- <24> A2P >> A2P
- <24> CLK1M >> CLK1M
- <24> CLK1P >> CLK1P
- <24> A3M >> A3M
- <24> A3P >> A3P
- <24> A4M >> A4M
- <24> A4P >> A4P
- <24> A5M >> A5M
- <24> A5P >> A5P
- <24> A6M >> A6M
- <24> A6P >> A6P
- <24> A7M >> A7M
- <24> A7P >> A7P
- <24> CLK2M >> CLK2M
- <24> CLK2P >> CLK2P
- <24> ENABLK >> ENABLK
- <24> ENAVDD >> ENAVDD

- <24> COMPONENT\_Y >> COMPONENT\_Y
- <24> COMPONENT\_PR >> COMPONENT\_PR
- <24> COMPONENT\_PB >> COMPONENT\_PB

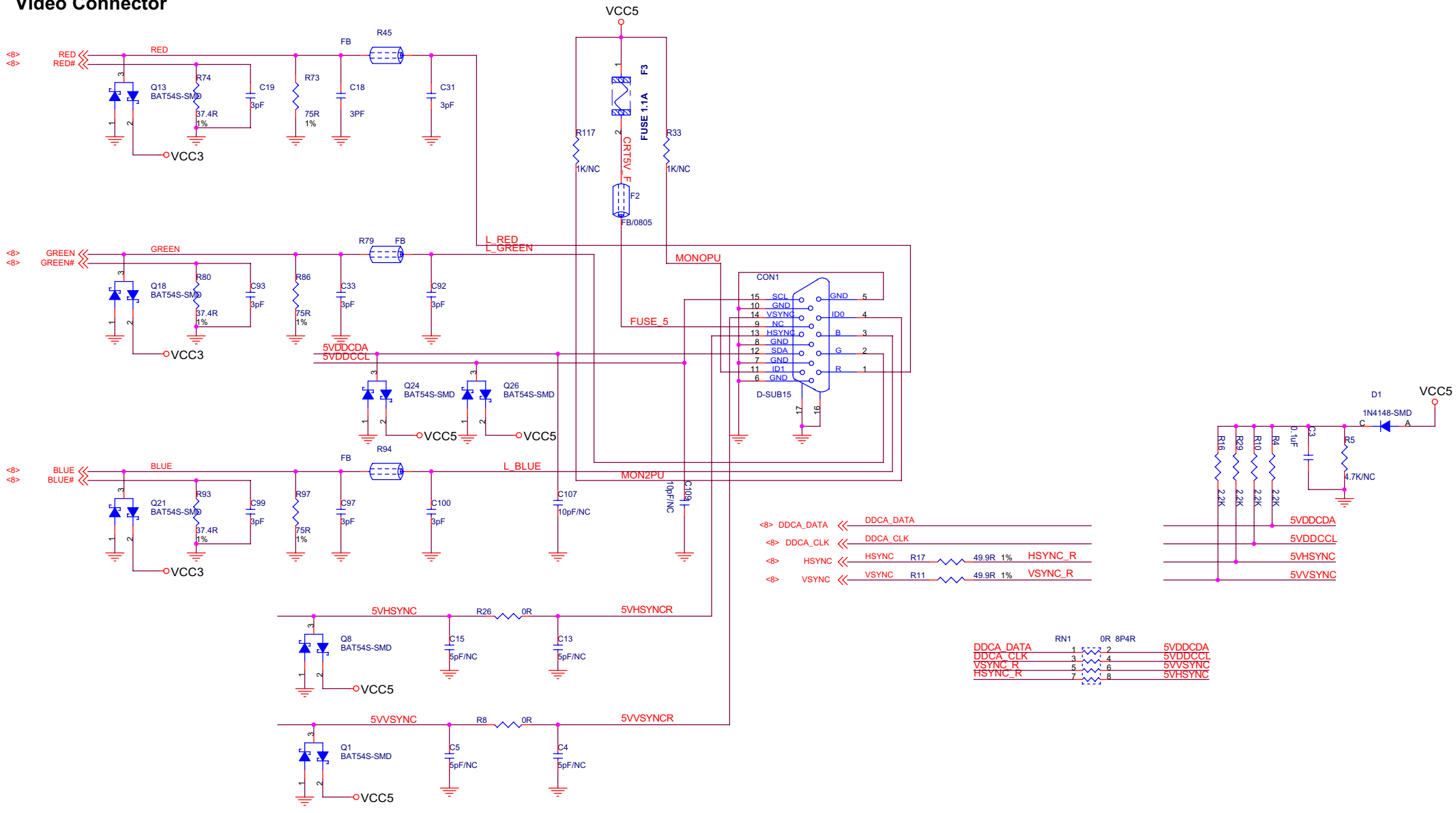
<8,29> G\_SBA[0..7] >> G\_SBA[0..7]

ADD ID Selector  
It will be provided by Intel regarding resistor stuffing option.



[YPrPb-OUT]

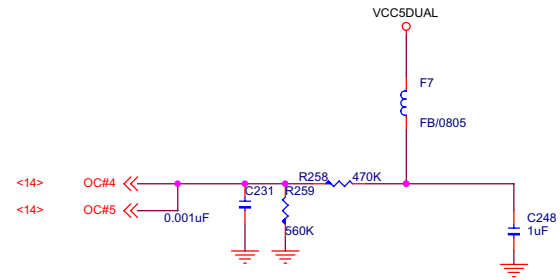
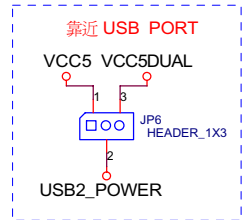
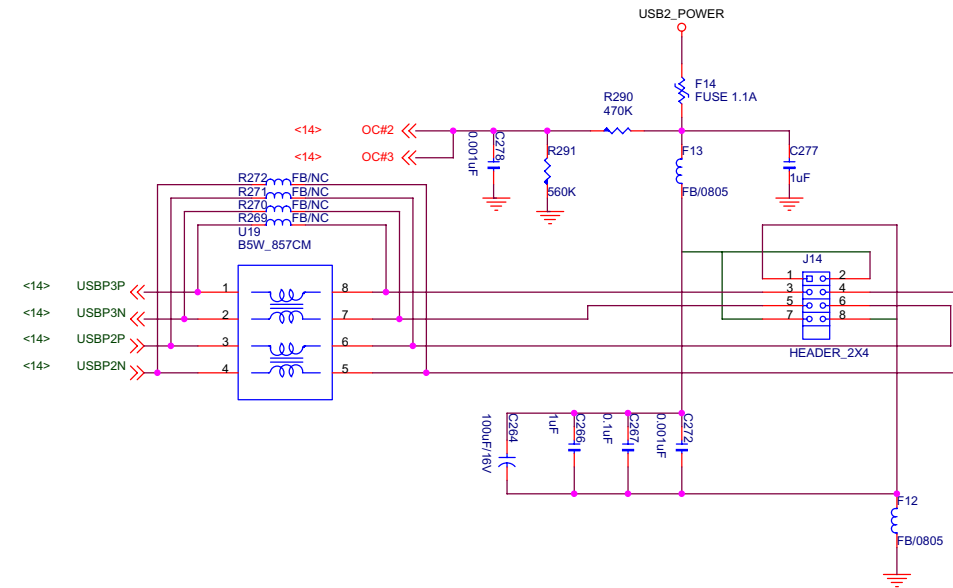
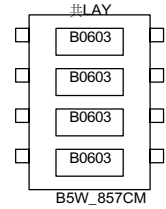
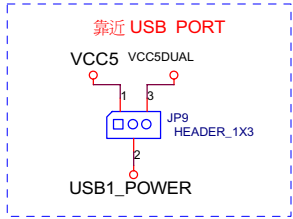
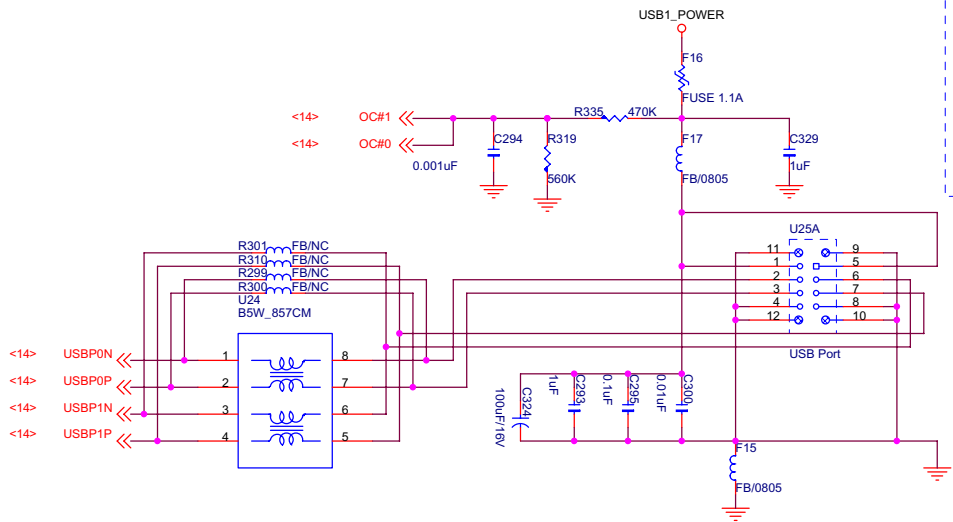
# Video Connector



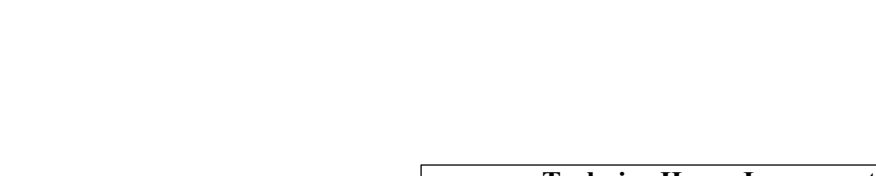
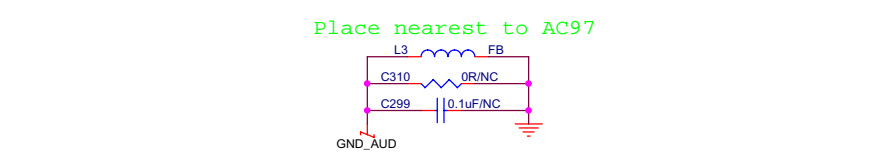
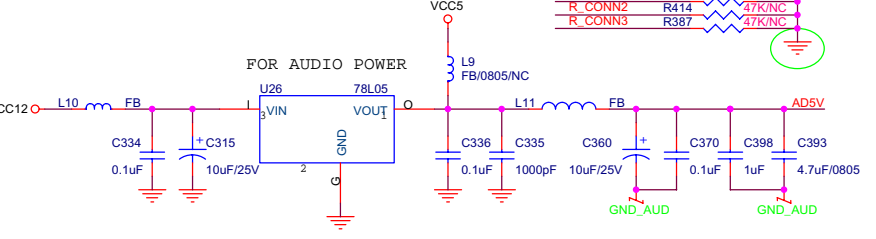
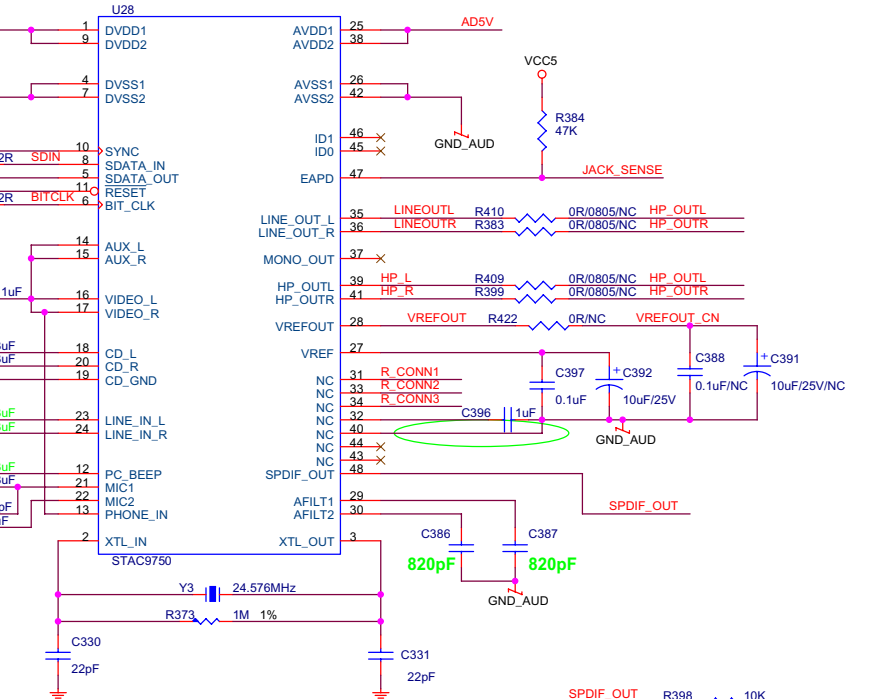
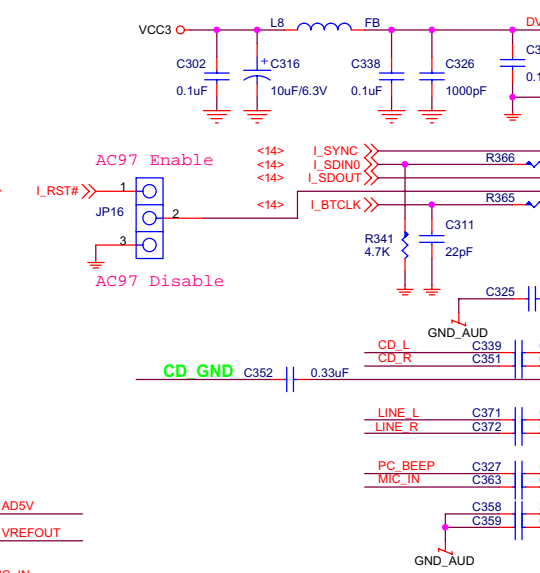
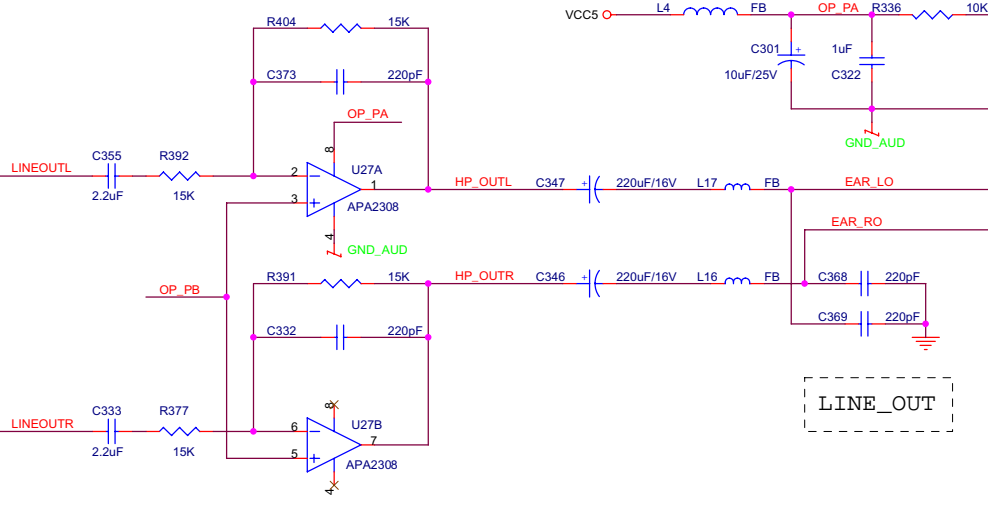
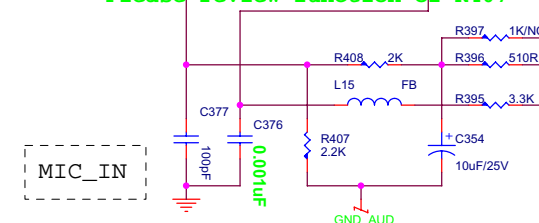
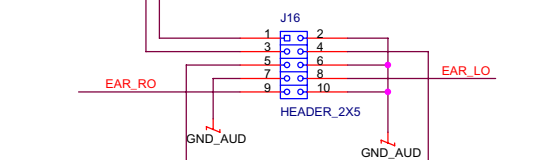
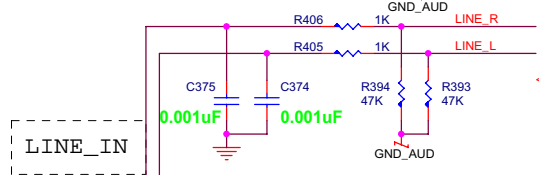
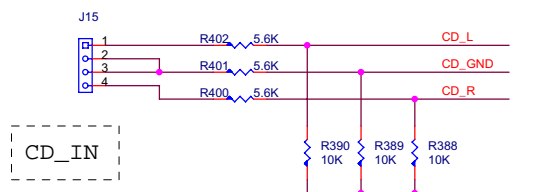
POPULATE WHEN NON LTI CONNECTOR



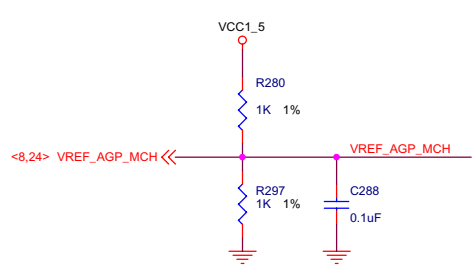
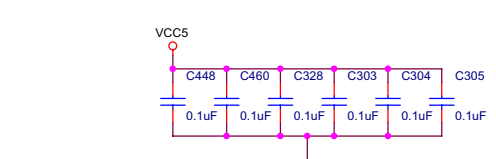
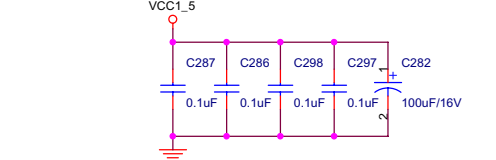
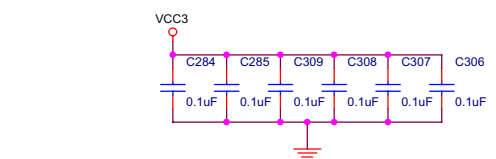
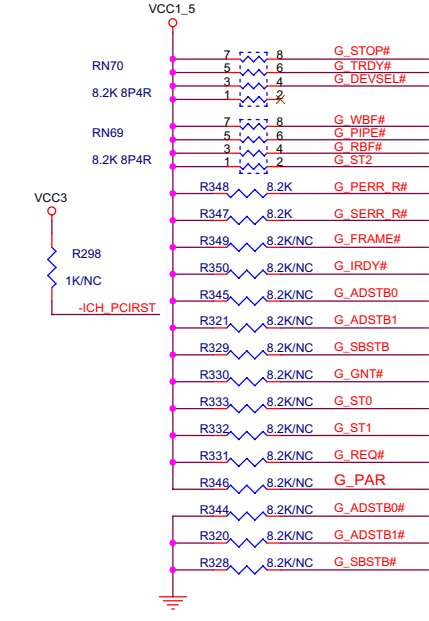
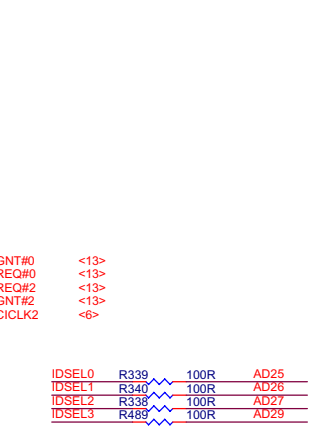
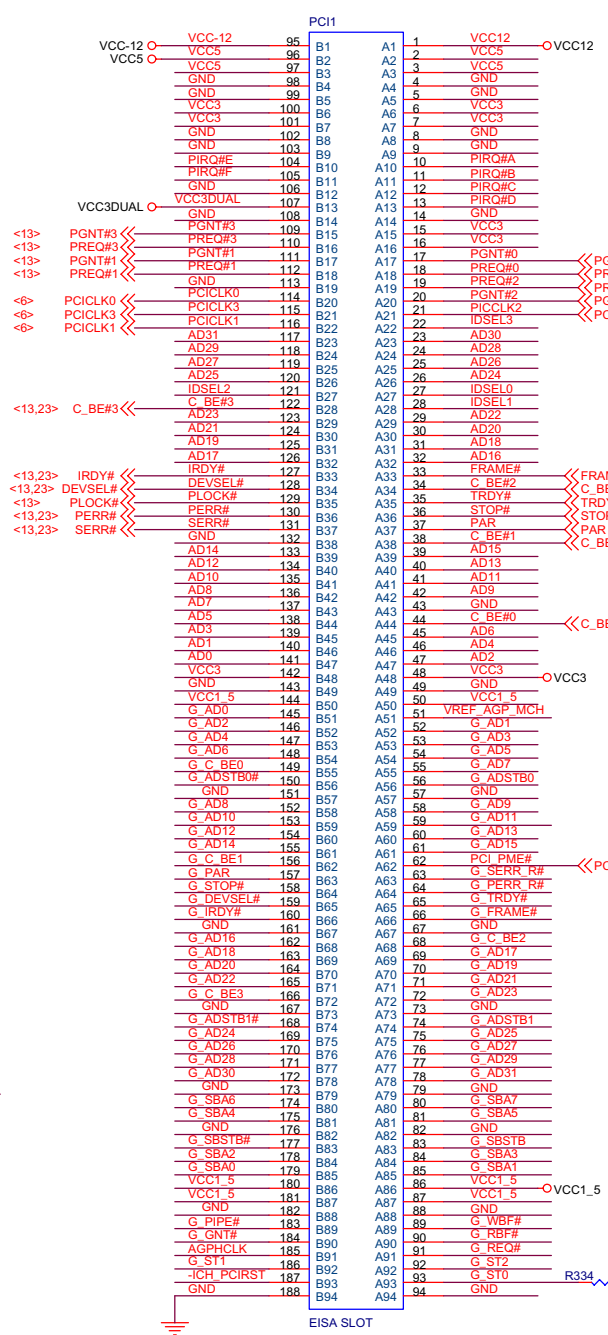
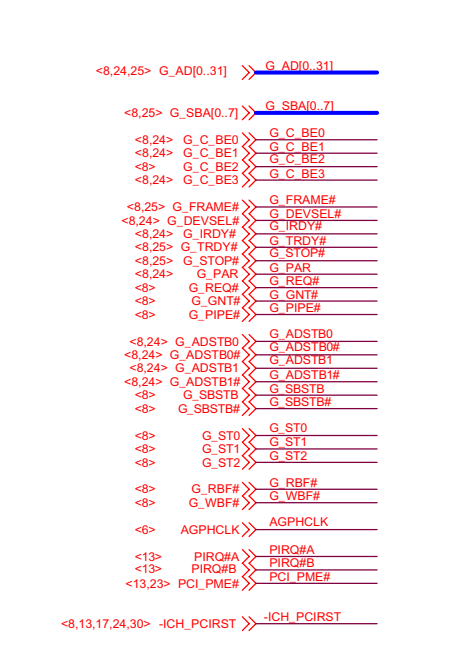
# USB Connectors



<b>Technica House Incorporation</b>		
Title INTEL Brookdale_G_PE CHIPSET		
Size	Document Number USB/RJ45 CONNECTORS	Rev 0.1
Date: Tuesday, February 17, 2004	Sheet 27	of 34

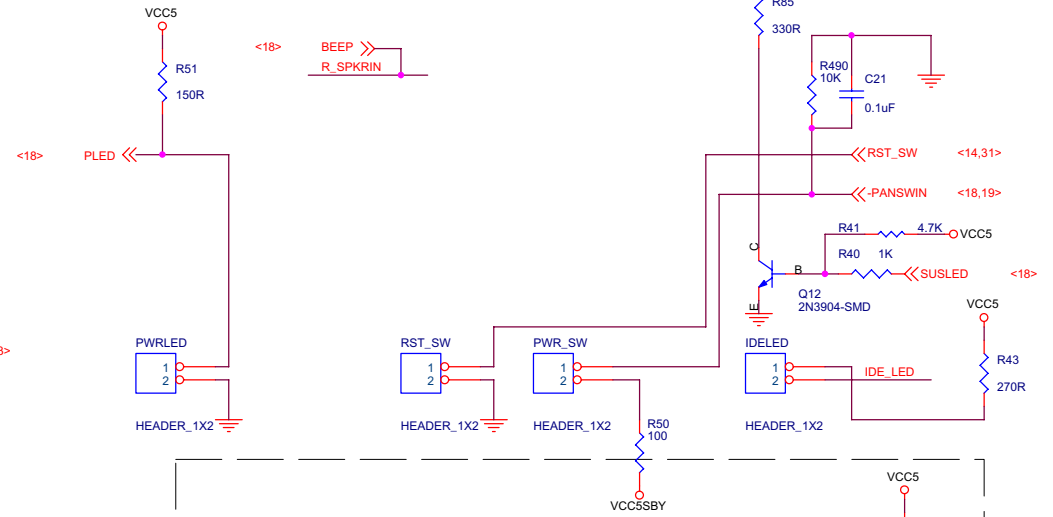
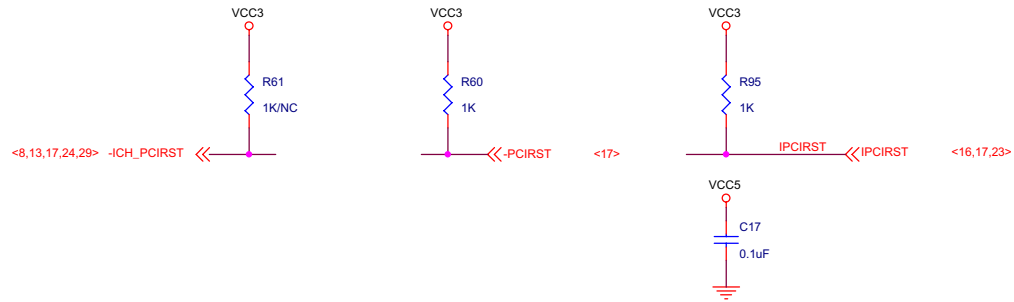
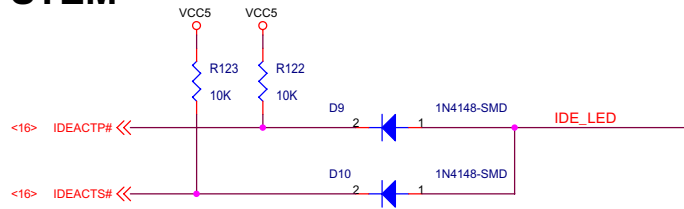


<b>Technica House Incorporation</b>		
INTEL Brookdale-G CHIPSET		
Size	Document Number	Rev
	CODEC	3.1
Date:	Tuesday, February 17, 2004	Sheet 28 of 34

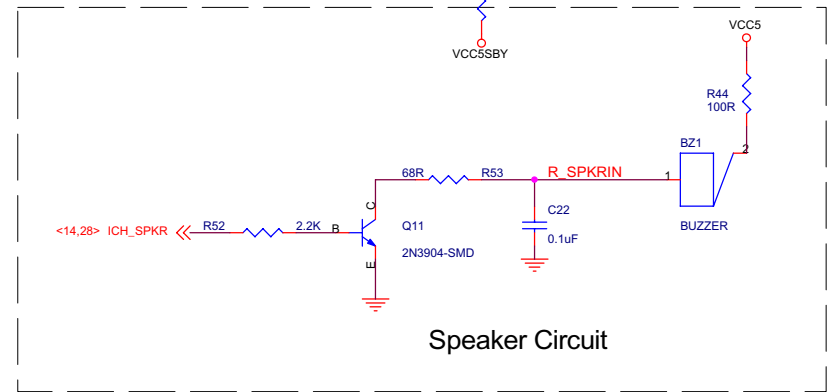
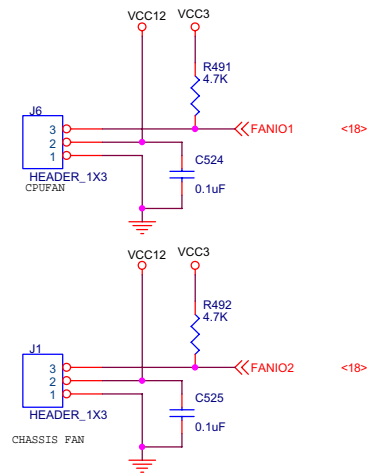


JET WAY INFORMATION			
<b>Technica House Incorporation</b>			
Title	PCI 1 & 2		
Size	Document Number	Rev	
Custom	mu-610BS	A	
Date:	Tuesday, February 17, 2004	Sheet	29 of 34

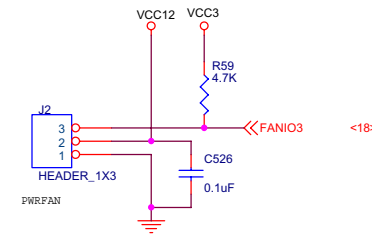
# SYSTEM



## PWM Circuit for FAN speed control

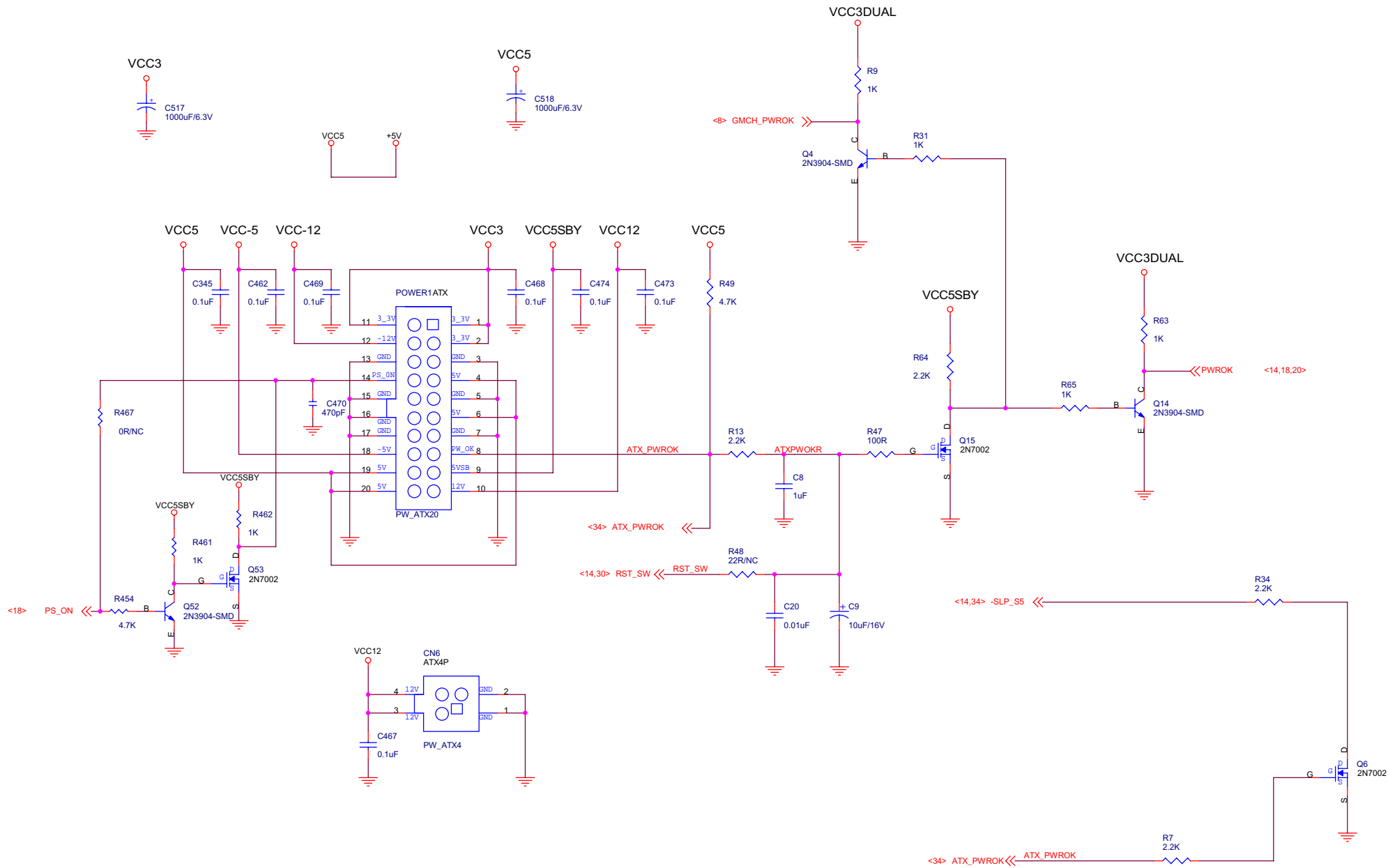


## Fan Speed Input Circuit



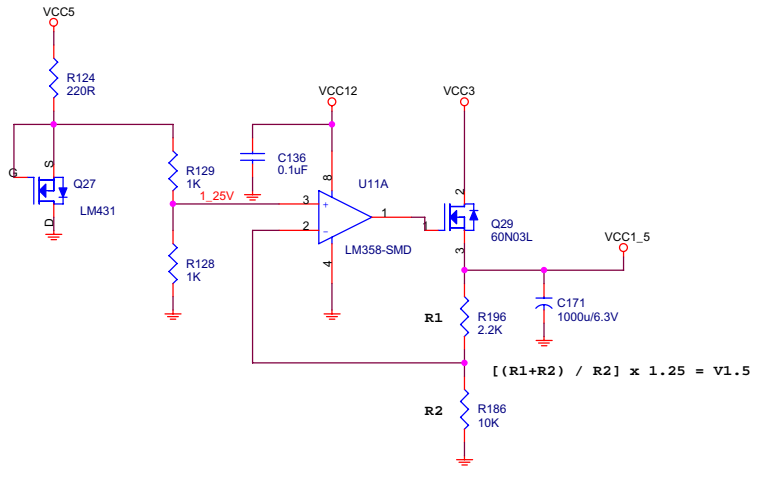
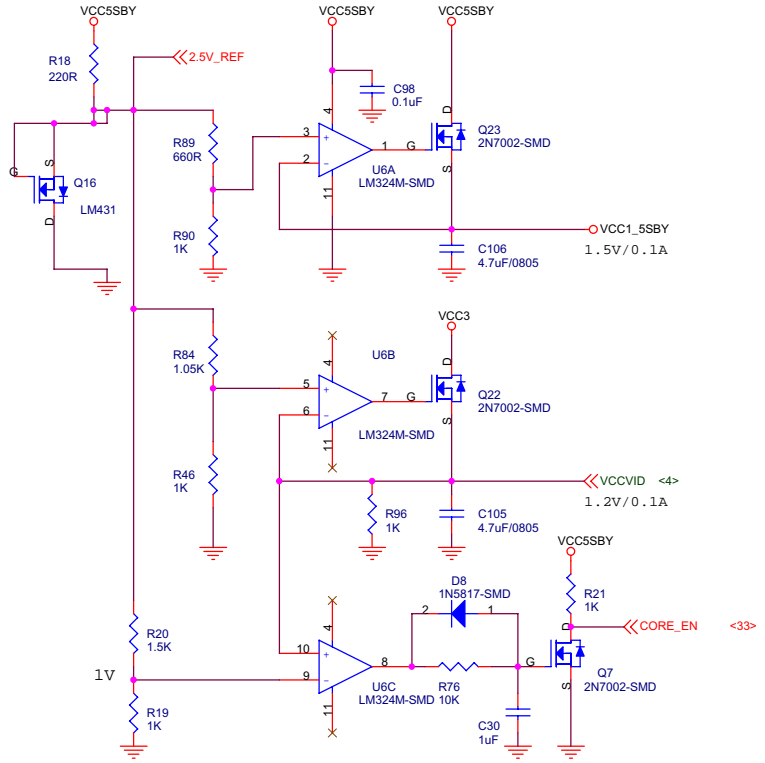
### Technica House Incorporation

Title		
INTEL Brookdale-G CHIPSET		
Size	Document Number	Rev
	SYSTEM	0.0
Date:	Tuesday, February 17, 2004	Sheet 30 of 34



<b>Technica House Incorporation</b>		
Title INTEL Brookdale-G CHIPSET		
Size	Document Number SYSTEM	Rev 0.0
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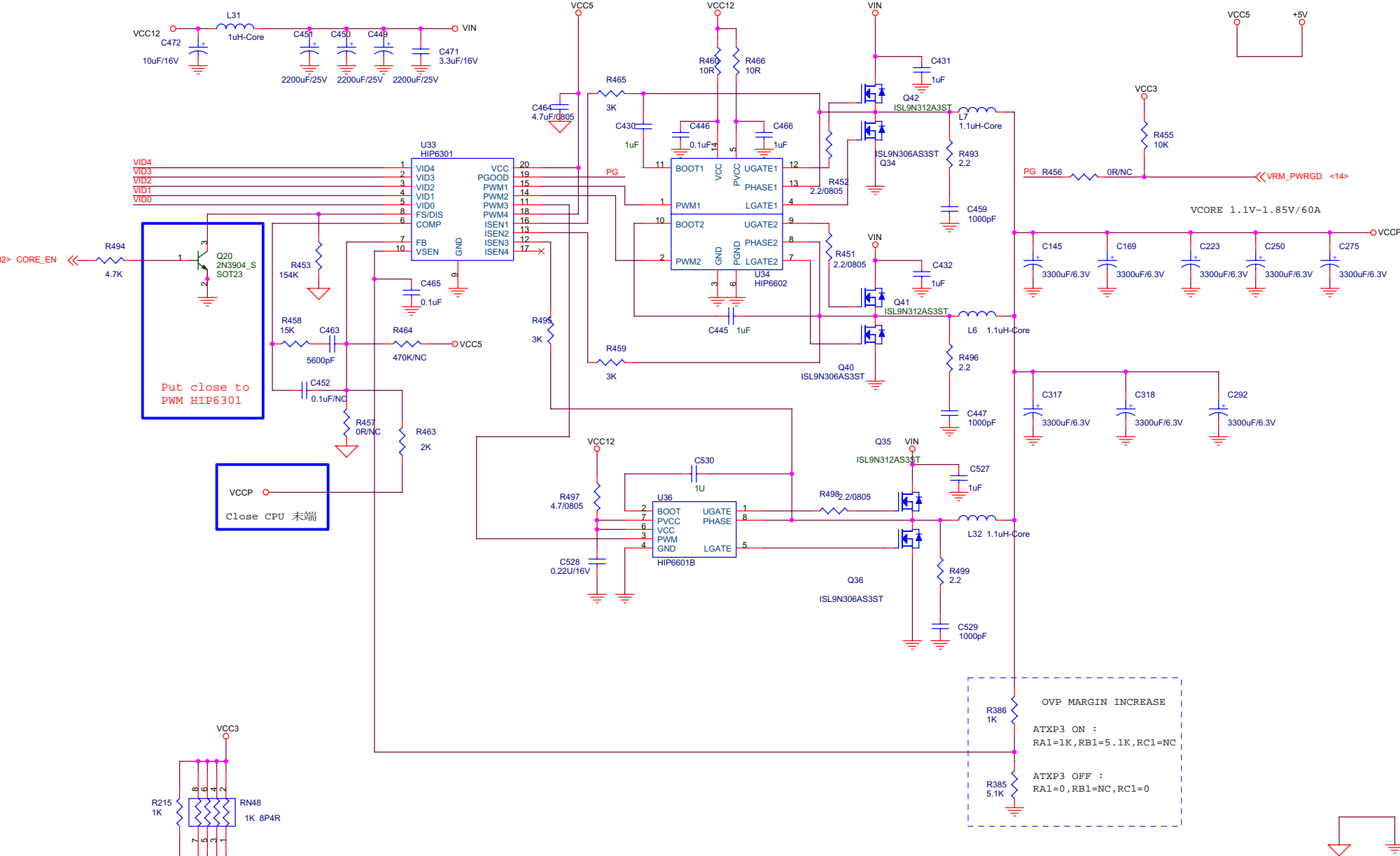
# Voltage Regulators



<b>Technica House Incorporation</b>		
Title INTEL Brookdale-G CHIPSET		
Size	Document Number	Rev
	VOLTAGE REGULATORS	0.0
Date:	Tuesday, February 17, 2004	Sheet 32 of 34

# VRM 9.0

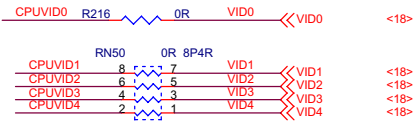
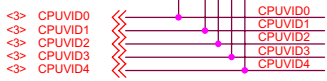
## HIP6302 FOR INTEL Brookdale/Socket478 POWER CKT



Put close to PWM HIP6301

VCCP  
Close CPU 末端

OVP MARGIN INCREASE  
ATXP3 ON :  
RA1=1K, RB1=5.1K, RC1=NC  
ATXP3 OFF :  
RA1=0, RB1=NC, RC1=0



<b>Technica House Incorporation</b>		
Title INTEL Brookdale-G CHIPSET		
Size	Document Number VRM 9.0	Rev 0.0
Date:	Tuesday, February 17, 2004	Sheet 33 of 34

