Block Diagram description

of the

+20 dBm Digianswer Bluetooth Protocol Analyser

DGABTPA101

1 Table of Contents

2 Revision History

Revision	Date	Author	Changes
1.0	30-11-00	EMN	Born

3 General

This document contains a Block description of the +20dBm Protocol Analyser. The main focus is based on the radio module, which is more thoroughly described than the rest of the module.
The chapters in this document refers to the respective blocks in the block diagram on the last page of the document.

4 Radio Description

This section is a description of the +20dBm Digianswer Bluetooth generation 1 radio block diagram.
The +20dBm radio is shown as the content inside the hatched block in the block diagram below.

4.1 LMX3162 transceiver IC

The main block of the radio is the National Semiconductor LMX3162 radio transceiver, which in fact is an upbanded DECT transceiver.

The LMX3162 radio transceiver consists of a phase locked loop PLL, transmit and receive functions. The 1,3GHz PLL is shared between the transmit and receive sections. The data is transmitted and received in different time slots. The time length is dependent upon the packet type transmitted and received. The PLL is able to hop to the desired carrier frequency in a given amount of time before data transmission and reception starts.

The transmitter part of the LMX3162 includes a frequency doubler and it employs direct VCO modulation.
The receiver part consists of a 2,5GHz low noise converting mixer, an intermediate frequency amplifier, a high gain limiting amplifier, a frequency discriminator, and a received signal-strength indicator (RSSI) circuit. The RSSI circuit is in this implementation used for channel quality monitoring and link regulation of transmitter power as required in the power class 1 Bluetooth standard.

The receiver section has a simple heterodyne receiver, ie. single conversion architecture and the received signal is demodulated using a quadrature discriminator. The transceiver IC has on-chip regulators in order to allow supply ranges from 3.0VDC to 5.5VDC.

The frequency reference to the transceiver IC is a divide by 4 version of the onboard 16MHz main clock. This main clock is fed to the radio controller (BTIC2/LMX5001), and internal divided by 4 and then fed as the PLL_OSC (4MHz reference) signal to the transceiver IC.

The signals SER_CLK, SER_LE, SER_DATA, REC_CE, RX_PD, TX_PD and PLL_PD are transceiver control signals to and from BTIC2.

4.2 Transmit Operation

A transmit RF signal is generated by very simple frequency modulation of the VCO. The VCO is seen external to the transceiver IC at the block diagram. The VCO is a none band-switching VCO, which in transmit mode varies in the frequency range of 1201-1247.5MHz dependent of the hopping scheme. It is done in open loop operation. The TX_DATA transmitted from the BTIC2 IC is Gaussian filtered using a discrete filter before entering the VCO. The amplitude of the signal generated by BTIC2 (TX_DATA) is adjusted by a resistive divider

in order to obtain and control the amplitude, such that frequency deviation within the Bluetooth specification is achieved.

The output of the VCO is fed to the LMX3162 transceiver IC, where the frequency is doubled and used as PLL input. The frequency-doubled signal is buffered and the output power of LMX3162 before entering the first PA stage is app. –7dBm nominal. This signal is now amplified in a two-stage amplifier, which has controllable gain by varying the PA Supply DC voltage. The output power can be set to 4 different power levels according to the power class 1 requirements. These power levels are defined from the receiver side in order to control the link power. The PAON_BAR signal and the PWM_QUAD signal fed from the BTIC2 to the PA supply switches the PA on/off and define the DC values according to the selected power step respectively.

At the output of PA the signal is slightly “low-pass” filtered before passing through the RX/TX switch. The signal is band-pass filtered in order to reduce harmonic, sub-harmonic and the VCO signal power at the output. Finally the signal enters the diversity switch before it is fed to one of the antennas. The construction uses antenna diversity and the decision upon which antenna to use is performed by the receiver by selecting using a well defined algorithm the polarization with the currently highest power content. The two antennas have vertical and horizontal polarization respectively. The frequency range at the antenna output covers the entire Bluetooth band, ie. from 2402-2495MHz.

4.3 Receiver Operation

In receive mode the signal enters the selected antenna. The selection is performed by the internal diversity algorithm, which is based upon the RSSI detector output and to receive the polarization with the instantly highest amount of power. The signal first enters the band-pass filter, which attenuates the limit and secures immunity to out of band blockers. After having passed the TX/RX switch the signal enters the LNA, which is build around the BFP420 from Siemens, which can achieve 13dB gain and 2dB noise figure.

After being amplified by the LNA the signal enters the LMX3162 down-converting mixer. In receive mode the VCO covers the frequency band 1146-1192,5MHz due to the heterodyne receiver structure. Due to frequency doubling in the LMX3162 the “doubled” VCO signal at the input of the mixer covers the frequency range 2292-2385MHz. The signal is bandpass filtered in an 110,0MHZ SAW filter. The only purpose of this filter is to secure as high as possible resistance for adjacent channel interferers. The bandwidth of this filter is approximately 1,2MHz.

The signal is now amplified and limited prior to quadrature detection at the output of LMX3162. The detected signal is now fed to the bit slicer, which consists of a 5.order lowpass filter, and a comparator. The 5. order filter will along with the 110.0MHz SAW filter secure that the Bluetooth ACI receiver requirements are fulfilled.

The bit slicer uses a fast and a slow time constant in order to have carrier track on only 4 preamble bit’s, and at the same time detect long sequences of 0’s and 1’s in the packet payload. These time constant’s are changed using S_FIELD2_BAR from BTIC2. The hardcoded detected bits are transferred to BTIC2 as RX_DATA.

5 Bluetooth Base Band

The Base Band Circuit consists of a single chip solution.
The main feature of this chip is to establish the communication between the DSP and the Radio. This means that the Base Band chip uses two different sets of very different interfaces.

The interface with the DSP is a general synchronous serial data communication using a DSP Sport. Through the serial connection with the Base Band chip, the DSP controls the Bluetooth settings and transmit/receive data from the Bluetooth Radio connection.

The interface with the Radio consists a serial connection, which provides communication with the radio chip. There are several special connections regarding the Bluetooth Radio. These connections are more thoroughly described in chapter 4.1.

The Base Band chip is configured by the DSP. This means that the DSP makes a setup of the Base Band chip. In other cases the DSP tells the Base Band chip whether to transmit or receive data from the Bluetooth Radio or in general the Bluetooth neighborhood and thereby other Bluetooth devices.
When transmitting or receiving data the Base Band converts the DSP data into Bluetooth packages and vice versa, as defined in the Bluetooth standard.

Furthermore the Base Bans chip controls the power down mode of the USB device.
When running in normal mode the Base Band chip runs on a 16MHz clock crystal. This generates the main clock in the system and therefore needs to be very accurate.

The Power Down mode is initiated from the DSP. The Base Band chip then shuts down the Power Supply for all the devices not needed, and puts the DSP in Power Down mode. After a certain amount of time the Base Band chip wakes up the system again.
When the Base Band chip is in power down mode, the chip shifts to the 128kHz clock to lower the power consumption of the chip.

6 Memory

This block contains a Flash memory. All the user software is saved in Flash memory.
Splitting up the software, the Flash contains the application software and a debugger, the latter used for development purposes. The application software can again be divided into two software parts: the first part contains the application specific software, which is unique for each product, in this case the software for the USB module, and the second part is the general Bluetooth Base Band software.

7 DSP

The DSP has interfaces to 3 surrounding segments:

- the Flash memory through the Address and Data bus through which the DSP loads the user software from the Flash memory and executes the loaded program, controlling the other segments and data transmission on the board.

- the USB Bus using an USB controller. For interfacing the USB controller the DSP uses the Address, Data lines an RD,WR. The USB controller is mapped into the DSP's internal memory. The USB controller is described further in chapter 8 (USB Controller). Because the USB controller needs a 24MHz clock to function, the DSP also needs to use this clock.

- the Base Band chip using a SPORT. The Base Band functionality is described in chapter 5 (Bluetooth Base Band). As shown in the Block diagram the Base Band uses a 16Mhz clock for the Radio. The communication between the DSP and Base Band only works, because the SPORT is a synchronous serial connection and therefore independent of the system clock.

8 USB Controller

The USB controller on the module enables the DSP to communicate with other USB hosts using the USB rev. 1.1 protocol. This USB module is listed as a high-speed device (12 Mbit) which supports remote wake up. This means that the USB Bus can activate the module when it is in sleep mode.
The USB controller is driven from a 24 MHz clock.

9 Power Supply

The power supply consists of two general blocks. One block for the 'general' part, of the module and one for the 'Radio' part.
Both the General supply and the Radio supply uses the 5V supplied direct from the USB Bus.

9.1 General supply

The General supply consists of two voltage regulators, who converts the 5V input voltage to a 3.3V and 2.5V, which is used by the DSP, Flash, USB controller and Base Band.

9.2 Radio supply

As shown on the Block diagram the Radio supply consists of a main supply (The dotted box) and two additional blocks.

The main Radio supply is based on the 5V USB voltage, which is slightly filtered to avoid interference.
This is then converted into the main supply voltage for the Radio.

The VCO supply is driven from the main Radio supply and enables the Base Band to turn the VCO on and off.

The PA supply is driven directly from the filtered USB voltage to ensure enough voltage to the PA stages. This is a common FET switch, which is PWM controlled. The output voltage of the switch is then low pass filtered, which gives a variable voltage source. This is used to control the power level of the PA.
As for the VCO supply this enables the Base Band to turn the PA stages on and off. When the Radio is either not in use or the module is in power down mode, this feature is used to save power.

10 USB Interface

This is the interface to the USB Bus. Refer to the USB specification rev. 1.1 for detailed description.
An additional protection circuit has been implemented to this interface.

11 +20dBm Protocol Analyser Block Diagram