4 CIRCUIT DESCRIPTION

4.1 PLL FREQUENCY SYNTHESIZER

The PLL frequency synthesizer is composed of a X-tal oscillator(X301), VCO, phase comparator, prescaler, PLL IC(U301) with programmable divider, and RC LPF. It produces the frequency controlled by CPU.

1. X-TAL OSCILLATOR

The frequency of X-tal oscillator (X301) is used as a reference freq. of PLL IC(U301) and a local frequency of IF IC (U101).

2. PLL IC

The PLL IC(U301) is controlled by CPU and receives the Rx/Tx frequency of each channel. It divides the VCO frequency through U301 Pin 5 using a prescaler and a programmable divider, compares the phase of a VCO frequency with that of a reference frequency, then finally the frequency is decided. The detected output from an internal phase comparator is sent to R322, C325, C324, R330, C326, R323, C329 composed of PLL LPF through U301 Pin 7, and it makes the DC voltage vary the VCO output frequency.

3. PLL LOCK DETECTOR

The internal phase comparator of PLL IC (U301) compares frequency and phase of a reference signal with those of VCO signal. Via U301 pin 7, The DC voltage, a difference of two signals is applied to VT terminal of VCO and makes a frequency changed. At this time, the stability of that frequency is equal to X301 and this is said to LOCK.

4. VOLTAGE CONTROLLED OSCILLATOR

The VCO is varied by DC voltage through PLL LPF. The Rx local oscillated frequency and Tx carrier frequency are decided by L302,C327,L303,C331, and voltage variable capacitor D306. The Rx local signal generated by Q304, Q305, Q306 is applied to a mixer Q102. The Tx carrier signal generated by Q304, Q305, Q306 is applied to TX amplified driver, Q203.

4.2 RECEIVER

1. TX/RX SWITCHING CIRCUIT

Receives signal from the antenna is fed to antenna switching circuit through low-pass filter consisting L216 ~ L218, C235, 236, 238, 239. D220 turns off and it makes isolation from the transmitter circuit, and the in coming signal is fed to the Band Pass Filter(SAW Filter).

2. FRONT END

Front end consists of a pair of SAW(Surface Acoustic Wave) filters and LNA(Low Noise Amplifier)

3. FIRST MIXER CIRCUIT

The received signal is fed to the GATE 1 of the first mixer Q102, And output of RX VCO is fed to the GATE 2 of the Q102. Therefore the first IF signal of 21.7 MHz is taken from the DRAIN of Q102.

4. MCF(Monolithic Crystal Filter)

MCF consists of a pair of X101 and matching capacitor, has narrow pass band of ±3.75 MHz. And eliminates ripple in pass band. So, it only passes 21.7 MHz signal of many signals from Mixer output.

5. IF AMP

The Q103 amplifies output of MCF to compensate the loss of MCF and make proper level to IF IC U101.

6. IF IC

The IF IC(U101) has second Mixer, IF AMP, OSC, FM detection, Noise squelch, and RSSI circuit. It generates second IF signal of 450kHz, using first IF signal of 21.7MHz and second local signal X301 of 21.25MHz. The signal of 450KHz is applied and filtered to 450KHz ceramic filter(X103) through pin3 and applied and amplified at second IF AMP(450KHz) pin 5. And then, a signal is sent to an internal detector circuit. The way of demodulation is a quadrature detector and It is demodulated by a resonator X104 connected IC pin 8, audio signal is taken from pin 9 via internal LPF. The noise signal of audio signal is applied to an internal filter, pin 8 of U101, and amplified and band-passed by R123, R124, R129, C148, C147, VR101. A squelch operation is controlled by varying a noise quantity of U101 which is adjusted by VR101. If a squelch is opened, the SQ detector, pin 13 of U101 is applied to CPU as a logic high and it sends the signal to disable a mute operation, so you can hear audio signal. If a squelch is closed, pin 13 is applied as a logic low and prevents the signal output.

7. AUDIO HIGH-PASS FILTER AND AUDIO AMPLIFIER

The detected audio signal is fed to speaker via de-emphasis circuit of –6dB/OCT frequency characteristic and U5, audio amplifier which output is more than 0.5W. And VR1 adjusts audio output.

4.3 TRANSMITTER

A transmitter consists of a driver AMP high frequency RF power IC. When PTT button is pressed, the output of VCO is amplified by Q203, Q204, Q205 and transmits to ANT via LPF.

1. PTT DETECTOR AND CPU CONTROL

The CPU recognizes the beginning of a transmission as a MIC level is transferred to A/D converter port pin 64 of U1. In the VOX mode, the MIC level is amplified by Q4 and U1 recognizes the PTT according to VOX level. The CPU recognized PTT signal decodes the channel frequency and other optional data. It controls the optional control circuit, transfers data to PLL IC, and radiates the low signal (TX enable signal (U1 pin 54) controls TX power).

2. MIC AMP AND MODULATION

The audio signal made by an internal condenser MIC or an external MIC is amplified by U2 and it has the characteristic of pre-emphasis 6dB/OCT. The U2 has –36dB/OCT more than 3.6KHz frequency. The audio signal through a limitting circuit is transferred to VR2, limits the maximum modulation deviation, applied to VCO, and modulated.

3. POWER AMP AND LPF

The TX RF signal generated from TX VCO is supplied to a drive AMP Q203, 204, amplified as much as a required input level, and applied to Q205. It gains the output more than 2.5W(DC 7.5V).The signal supplies to LPF and an Ant connector and radiates to ANT. The LPF removes the harmony frequency as well as improves the characteristic of TX spurious.

4.4 MICROPROCESSOR UNIT

All controls of radio is assigned by CPU program and Tx/Rx frequency and options are operated by CPU and interface circuit

1. CPU PORT ASSIGNMENT

NO	NAME	CIRCUIT SIGN	I/O	STATUS	OPERATION
1	PB1/AN1	BATT	A/D		BATTERY CHECK
2	PB0/AN0	VOX	A/D		DETECT THE MIC INPUT SIGNAL TO DECIDE VOX
3	AVSS	AVSS			GROUND
4	TEST	TEST	I	X	FLASH
5	X2				
6	X1	XIN	I		PULL-UP 10K TO CPU POWER
7	VSS	VSS			GROUND
8	OSC1	OSC1	I		3.6864MHz
9	OSC2	OSC2	O		X-TAL OUTPUT (CONNECT TO AK2345)

10	/RES	REST	O	L	RESET
11	P9_0	DTM0	O		FOR VMFFOTNL/DTM0
12	P9_1	DTM1	O		DTMF1
13	P9_2	DTM2	O		DTMF2
14	P9_3	DTM3	O		DTMF3
15	P9_4				
16	/IRQ0				
17	P6_0	TXLP	O	L	TRANSMITTING LED (0 :ON 1 :OFF)
18	P6_1	ASDO	O		DCS SIGNAL OUTPUT TERMINAL
19	P6_2	AMUT	O	L	BLOCK AUDIO OUTPUT
20	P6_3				
21	P6_4				
22	P6_5	STRB	O		AK2345 STROBE
23	P6_6				
24	P6_7	RXP	O		RECEIVER POWER (0 :OFF 1 :ON)
25	P5_0//INT0				
26	P5_1//INT1	MON	I	L	MON SWITCH INPUT
27	P5_2//INT2	SQD	I		SQUELCH DETECT(0 :DET 1 :NO DET)
28	P5_3//INT3	CTC	I		CTCSS DETECT(0 :DET 1 :NO DET)
29	P5_4//INT4	DCSH	I		DCS SIGNAL INPUT TERMINAL
30	P5_5//INT5	DCSL	I		DCS SIGNAL INPUT TERMINAL
31	P5_6//INT6	LD	I		PLL LOCK DETECT
32	P5_7//INT7				
33	VCC	C5V			SUPPLY POWER TO CPU
34	P7_3				
35	P7_4/TMRIV				
36	P7_5/TMCIV				
37	P7_6/TM0V	BEEP	O		ALARM OUTPUT TERMINAL
38	P7_7				
39	P8_0/FTCI	CH2	I		ROTARY SW 2
40	P8_1/FTOA	CH3	I		ROTARY SW 3
41	P8_2/FTOB	CH0	I		ROTARY SW 0
42	P8_3/FTIA	CH1	I		ROTARY SW 1
43	P8_4/FTIB	RXLP	O		RECEIVING LED (0 :OFF 1 :ON)
44	P8_5/FTIC	MICMT	O		
45	P8_6/FTID	MODCTC	O		
46	P8_7	DO			PLL DATA OUT
47	P2_0/SCK3	CK			PLL CLOCK OUT
48	P2_1/RXD	RXD	I		FOR DEBUGGING,FLASH
49	P2_1/TXD	TXD	O		FOR DEBUGGING,FLASH
50	P3_2/SO_1	SDO	O		CONNECT TO SDO(EEPROM)

51	P3_1/SI_1	SDI	I		CONNECT TO SDI(EEPROM)
52	P3_0/SCK1	SCK	O		CONNECT TO SCK(EEPROM,AK2345)
53	P1_0/TMOW				
54	P1_4/PWM	TXE	O	H	SUPPLY POWER TO TX (0 :OFF 1 :ON)
55	P1_5//IRQ1	ECS	O	L	93C46 CHIP SELECT
56	P1_6//IRQ2	LE	O		PLL LATCH ENABLE
57	P1_7//IRQ3				
58	AVCC	C5V			POWER INPUT
59	PB7/AN7				
60	PB6/AN6				
61	PB5/AN5				
62	PB4/AN4				
63	PB3/AN3				
64	PB2/AN2	APTT	A/D		PTT INPUT

4.5 ALIGNMENTS

1. PLL IC VCO

Voltmeter connect to PLL IC 7th pin and check the range of DC voltage.

462.55000MHz	RECEIVE	0.5V – 1.5V
	TRANSMIT	2.4V – 3.9V

2. TRANSMITTER (measuring frequency : 462.55000MHz)

1) Adjust VC301 for an exact transmitted frequency.
2) Adjust VR201 for 2.5 W(7.5V) as a transmitted output.
3) Apply 100mVrms, 1.0 KHz without tone to MIC+ terminal and adjust VR2 for 2.0 KHz deviation.
4) Check tone modulated rate around 0.35 ~ 0.55 KHz, Check that it is not over + 2.5 KHz and –2.5 KHz when an audio signal of 1 KHz and a signal with tone are modulated

3. RECEIVER (measuring frequency : 462.55000 MHz)

1) The SG set channel frequency 462.55000 MHz, 1 mV, 1 KHz to 1.5 KHz FM, connect to ANTENNA JACK.
2) It checks the SINAD to be 12dB.
3) Adjust VR101 to operate the threshold SQ around 8 ~ 10dB SINAD by varying SG signal level.

5. CRYSTAL SPEC.

FREQUENCY (MHz)	
462.5500	467.5500
462.5625	467.5625
462.5750	467.5750
462.5875	467.5875
462.6000	467.6000
462.6125	467.6125
462.6250	467.6250
462.6375	467.6375
462.6500	467.6500
462.6625	467.6625
462.6750	467.6750
462.6875	467.6875
462.7000	467.7000
462.7125	467.7125
462.7250	467.7250