SYNTHESIZER BLOCK DIAGRAM

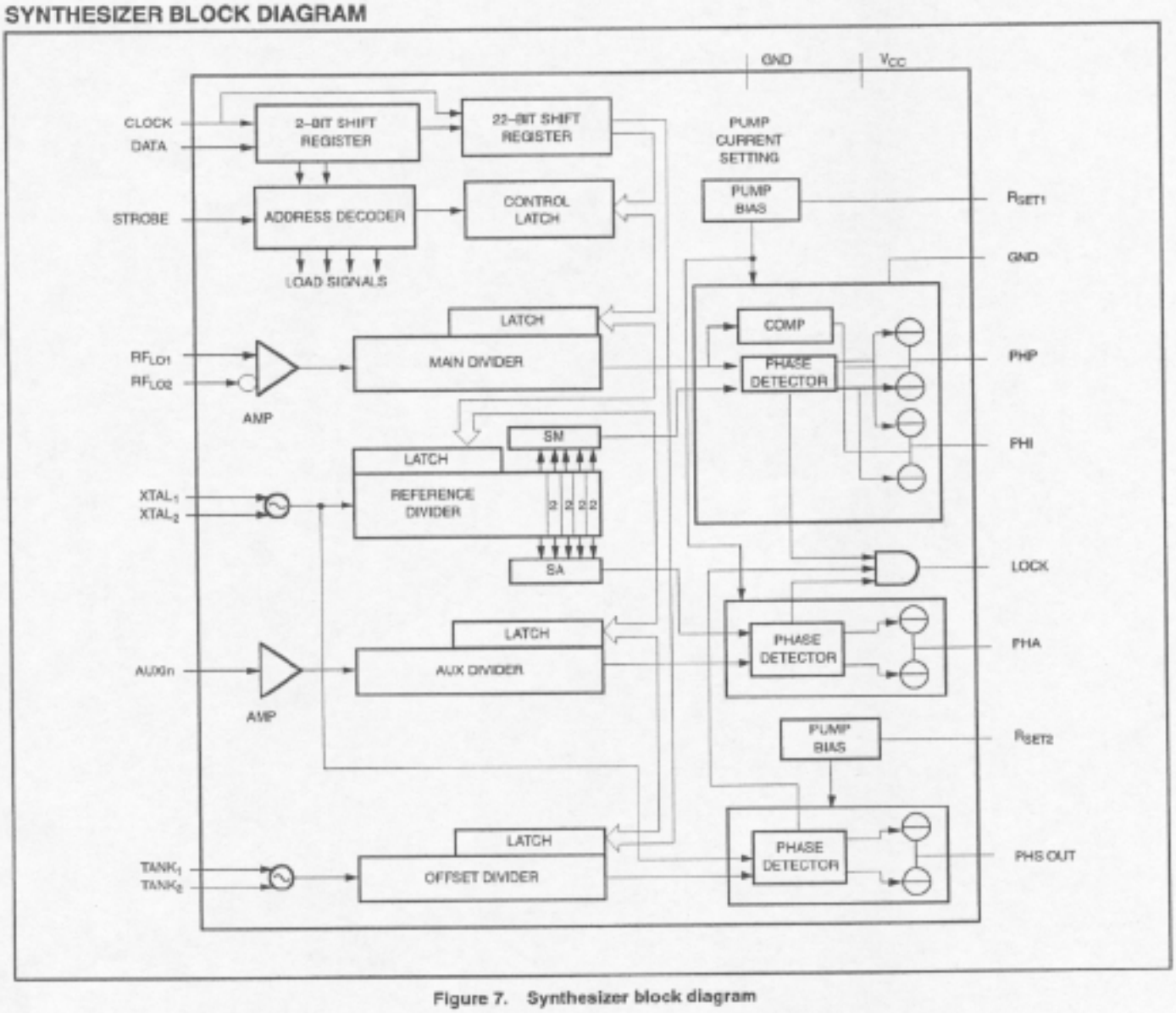


Figure 7. Synthesizer block diagram

SYNTHESIZERS AND CONTROL OPERATIONS

Main Fractional-n Divider

The RFin inputs drive a pre-amplifier to provide the clock to the first divider stage. For single ended operation, the signal should be fed to one of the inputs while the other one is AC grounded. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from –18 dBm to +0 dBm, and at frequencies as high as 2.5 GHz. The divider consists of a fully programmable bipolar prescaler followed by a CMOS counter. Total divide ratios range from 512 to 65535.

At the completion of a main divider cycle, a main divider output pulse is generated which will drive the main phase comparator. Also, the fractional accumulator is incremented by the value of NF. The accumulator works with modulo Q set by FMOD. When the accumulator overflows, the overall division ratio N will be increased by 1 to N + 1, the average division ratio over Q main divider cycles (either 5 or 8) will be

$$Nfrac = N + \frac{NF}{Q}$$

The output of the main divider will be modulated with a fractional phase ripple. The phase ripple is proportional to the contents of the fractional accumulator and is nulled by the fractional compensation charge pump.

The reloading of a new division ratio or new NF value is synchronized to the state of the main divider to avoid introducing a phase disturbance.

Auxiliary Divider

The AUXin input drives a pre-amplifier to provide the clock to the first divider stage. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The circuit operates with signal levels from –18 dBm to +0 dBm (80 to 632 mVpp), and at frequencies as high as 550 MHz. The divider consists of a fully programmable bipolar prescaler followed by a CMOS counter. Total divide ratio range is from 128 to 16383.

Reference Divider

The reference divider consists of a divider with programmable values between 4 and 1023 followed by a three bit binary counter. The 3-bit SM (SA) register (see Figure 8) determines which of the 5 output pulses are selected as the main (auxiliary) phase detector input.

Offset Divider and Phase Detector

The output of the offset VCO is fed to a programmable prescaler M with user selectable divide ratio of 6, 7, 8, 9 (all divides configure to provide 50% duty cycle). The output of the offset divider is fed into the input of the offset phase detector. The reference input for this phase detector is internally fed from the signal at the XTAL1, 2 input. The offset phase detector compares these two phases based on a multiplier principle and locks these signals, therefore, with 90 degree phase difference.

Phase Detector: Main and Auxiliary

The reference and main (aux) divider outputs are connected to a phase/frequency detector that controls the charge pump (see Figure 9). The pump current is set by a an external resistor in conjunction with control bits CP0 and CP1 in the C-word (see Charge Pump table). The dead zone (caused by finite time taken to switch the current sources on or off) is cancelled by forcing the pumps ON for a minimum time at every cycle (backlash time) providing improved linearity.

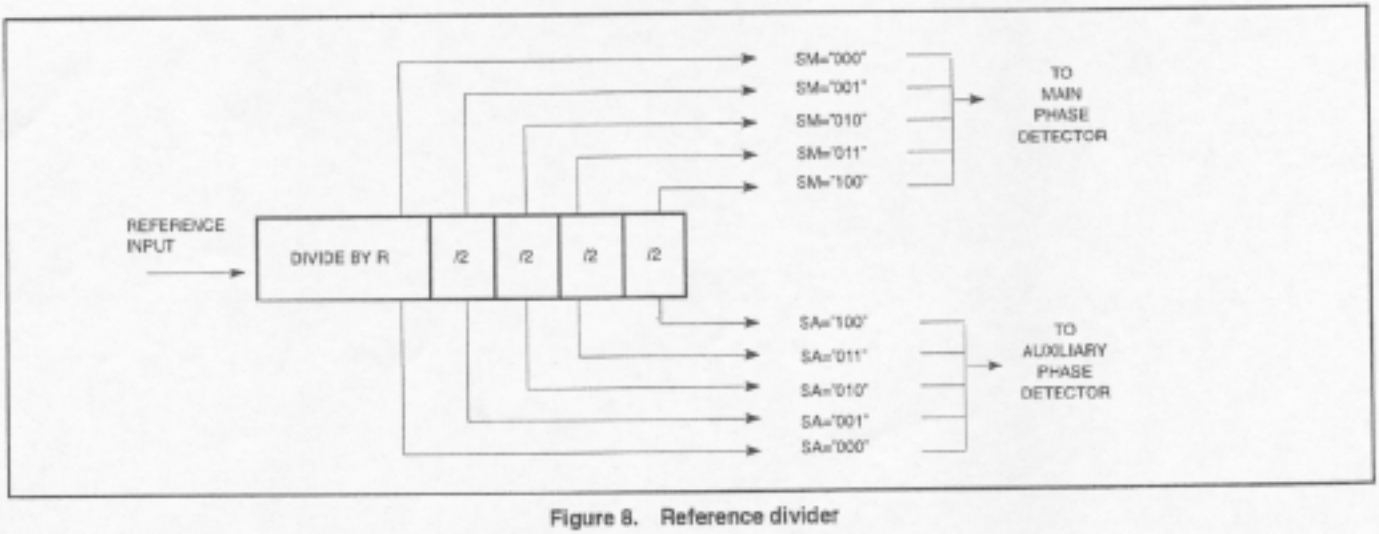


Figure 8. Reference divider

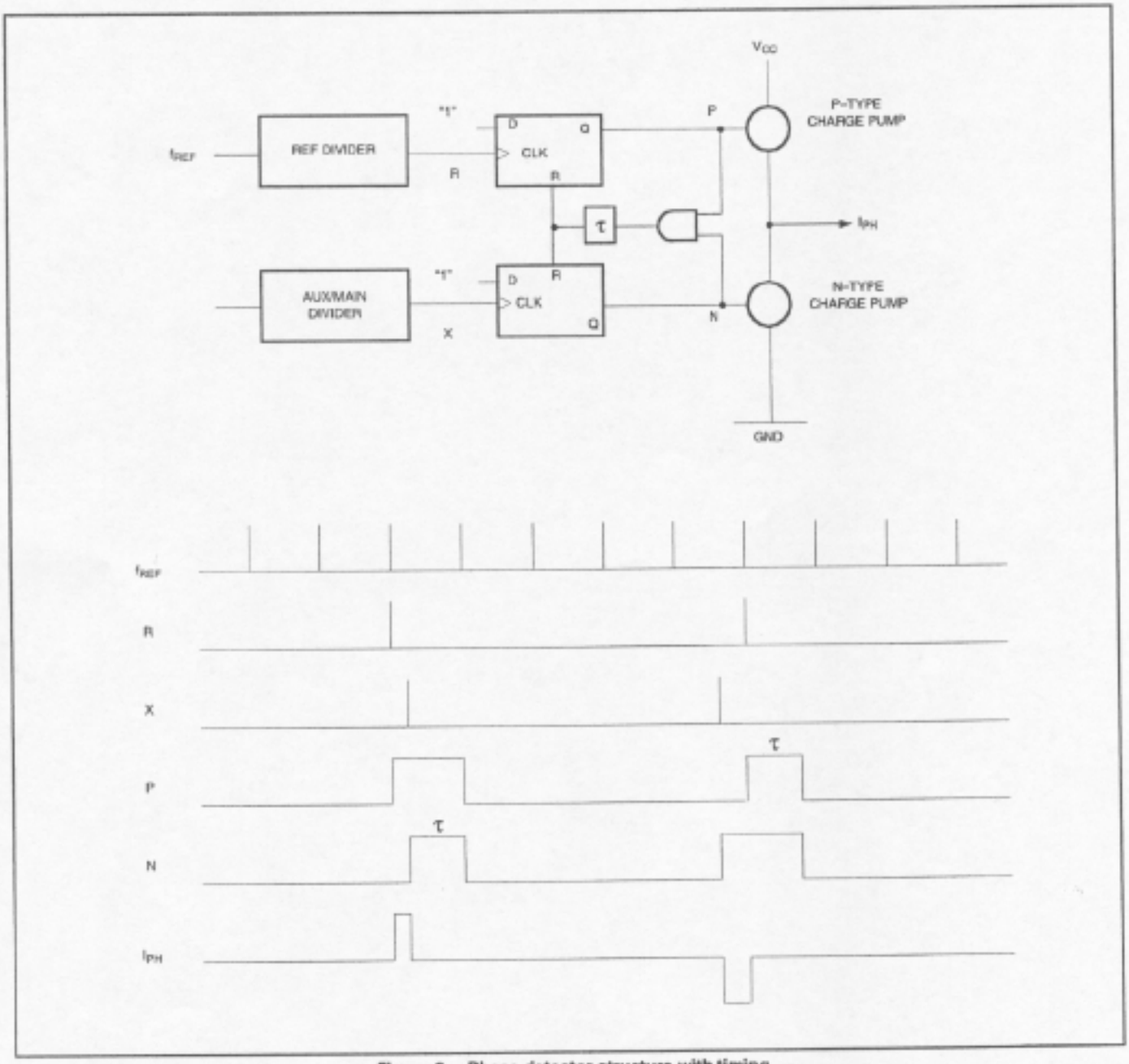


Figure 9. Phase detector structure with timing

Main Output Charge Pumps and Fractional Compensation Currents

The main charge pumps on pins PHP and PHI are driven by the main phase detector and the charge pump current values are determined by the current at pin R_{SET1} (see table of charge pump ratios). The fractional compensation is derived from the current at R_{SET1}, the contents of the fractional accumulator FRD and by the program value of the FDAC. The timing for the fractional compensation is derived from the main divider. Figure 10 shows the waveforms for a typical case and shows that for proper fractional compensation, the area of the fractional compensation current pulse must be equal to the area of the charge pump ripple output.

Principle of Fractional Compensation

The fractional compensation is designed into the circuit as a means of reducing or eliminating fractional spurs that are caused by the fractional phase ripple of the main divider. If I_{COMP} is the compensation current and I_{PUMP} is the pump current, then for each charge pump:

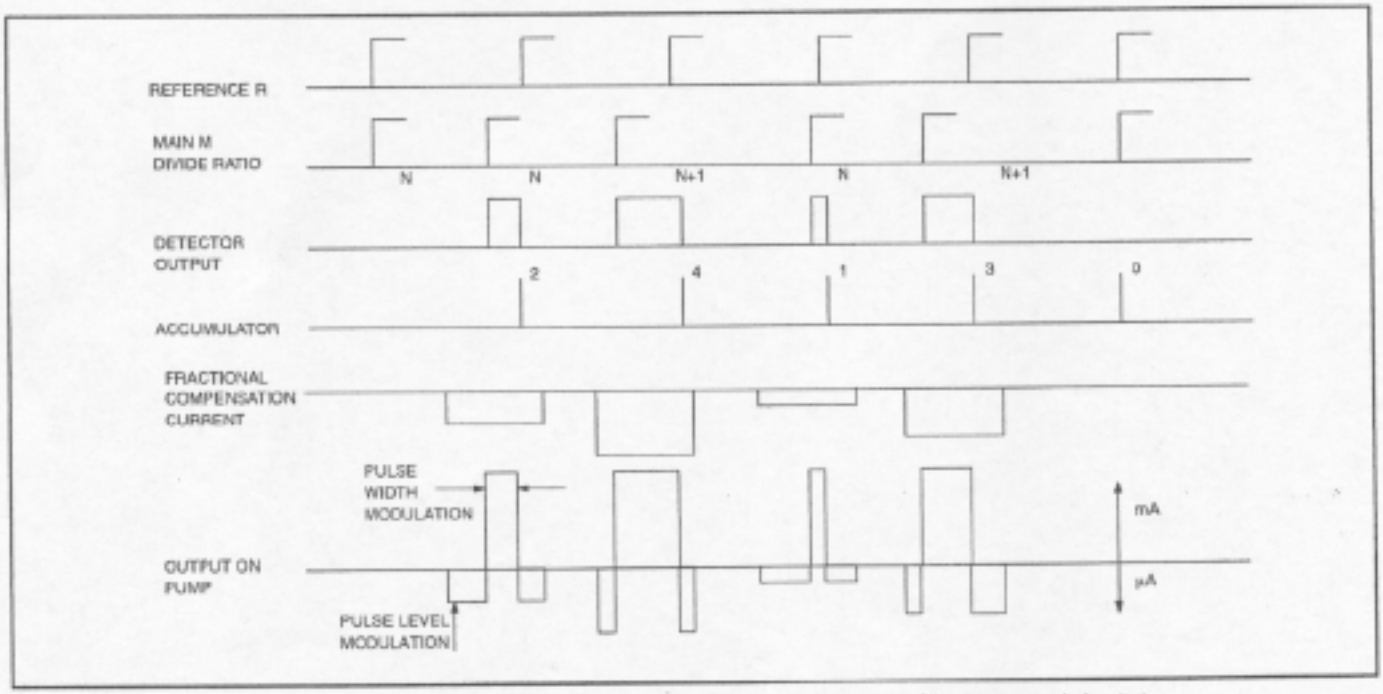
$$I_{PUMP\_TOTAL} = I_{PUMP} + I_{COMP}$$

The compensation is done by sourcing a small current, I_{COMP}, that is proportional to the fractional error phase (see Figure 11). For proper fractional compensation, the area of the fractional compensation current pulse must be equal to the area of the fractional charge pump ripple. The width of the fractional compensation pulse is fixed to 128 VCO cycles, the amplitude is adjusted by FDAC values (bits FDAC7-0 in the B-word). The fractional compensation current is derived from the main charge pump in that it follows all the current scaling through external resistor setting, R_{SET}, programming or speed-up operation. For a given pump:

$$I_{COMP} = (I_{PUMP} / 128) * (FDAC / 5*128) * FRD$$

FRD is the fractional accumulator value.

The target values for FDAC are: 128 for FMOD = 1 (modulo 5) and 80 for FMOD = 0 (modulo 8).



NOTE: For a proper fractional compensation, the area of the fractional compensation current pulse must be equal to the area of the charge pump ripple output.

Figure 10. Waveforms for NF = 2 Modulo 5 → fraction = $^2/_5$

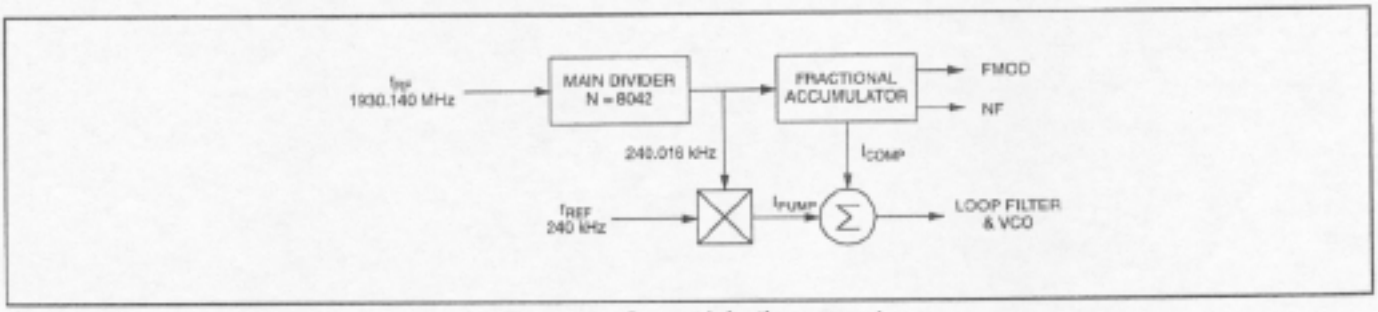


Figure 11. Current injection concept

High-speed and Adaptive Mode

The main charge pumps will enter speed up mode after the A-word is send and the strobe signal goes high and stays high. When strobe goes low again, the charge pumps will exit the speed up mode.

In the "normal mode" the current output PHP is:

$$I_{PHP\_N} = I_{PHP} + I_{PHP\_COMP}$$

The current in PHI is zero in "normal mode".

In "speed-up mode" the current in output PHP is:

$$I_{PHP\_SU} = I_{PHP} + I_{PHP\_COMP}$$

In "speed-up mode" the current in output PHI is:

$$I_{PHI\_SU} = I_{PHI} + I_{PHI\_COMP}$$

PHI pump is meant for switching only. Current and compensation are not as accurate as PHP.

Auxiliary Output Charge Pumps

The auxiliary charge pumps on pin PHA are driven by the auxiliary phase detector and the current value is determined by the external resistor attached to pin R_{SET1}.

Main and auxiliary charge pump currents

CP1	CP0	I_{PHA}	I_{PHP}	I_{PHP_SU}	I_{PHI}
0	0	$1.6xI_{SET1}$	$3xI_{SET1}$	$15xI_{SET1}$	$36xI_{SET1}$
0	1	$0.5xI_{SET1}$	$1xI_{SET1}$	$5xI_{SET1}$	$12xI_{SET1}$
1	0	$1.5xI_{SET1}$	$3xI_{SET1}$	$15xI_{SET1}$	0
1	1	$0.5xI_{SET1}$	$1xI_{SET1}$	$5xI_{SET1}$	0

NOTES
$I_{SETx} = V_{SETx}/R_{SETx}$: bias current for charge pumps.
CP1 is used to disable the PHI pump. I_{PHP_SU} is the total current at pin PHP during speed up condition.

Offset Output Charge Pumps

The offset charge pump on pin PHS is driven by the offset loop phase detector and the current value is determined by the external resistor attached to pin R_{SET2}. The charge pump current is hardware fixed to $24 * I_{SET2}$ and can not be programmed to different ratios.

Lock Detect

The output LOCK maintains a logic '1' when the auxiliary in lock indication 'AND' the main in lock condition 'AND' the offset loop lock detection is fullfilled.

Lock Condition for Main and Auxiliary

If the main PLL is in lock the main divider output signal and the reference divider output signal will have the same frequency and will also have close to zero phase difference at the input of the phase detector (the same will hold for the auxiliary divider output signal and the reference divider output signal, should the auxiliary section be powered up).

This zero phase difference constitutes the lock condition in an ideal PLL system. The CD8455 lock detect circuit indicates a lock condition, as long as this phase difference between the two divider output signals is smaller than +/– of 1 period of the signal at the input of the reference divider.

Lock Condition for Offset Loop

The offset loop lock detector indicates out of lock for offset frequencies f_{OFFin} which are lower than:

$$\frac{f_{REF}}{7} * 6 * N_O$$

or higher than:

$$\frac{f_{REF}}{7} * 6 * N_O$$

N_O: offset divider ratio; f_{REF}: reference frequency. For all other (smaller) frequency errors the lock detector will show the difference of the frequencies f_{REF} and $\frac{f_{OFFin}}{N_O}$.

Serial programming bus

The serial input is a 3-wire input (CLOCK, STROBE, DATA) to program all counter divide ratios, fractional compensation DAC, selection and enable bits. The programming data is structured into 24-bit words; each word includes 2 or 3 address bits. Figure 12 shows the timing diagram of the serial input. When the STROBE goes active HIGH, the clock is disabled and the data in the shift register remains unchanged. Depending on the address bits, the data is latched into different working registers or temporary registers. In order to fully program the CD8455 words must be sent: D, C, B, and A. Table 1 shows the format and the contents of each word. The data for the fractional compensation DAC, FC is stored by the B word in temporary registers. When the A word is loaded, the data of these temporary registers is loaded together with the main divider ratio.

Serial bus timing characteristics. See Figure 12.

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
Serial programming clock; CLK					
t_r	Input rise time	–	10	40	ns
t_f	Input fall time	–	10	40	ns
T_{cy}	Clock period	100	–	–	ns
Enable programming; STROBE					
t_{START}	Delay to rising clock edge	40	–	–	ns
t_W	Minimum inactive pulse width	1/fcomp	–	–	ns
$T_{SU;\overline{E}}$	Enable set-up time to next clock edge	30	–	–	ns
Register serial input data; DATA					
$t_{SU;DAT}$	Input data to clock set-up time	30	–	–	ns
$t_{HD;DAT}$	Input data to clock hold time	30	–	–	ns

Application information

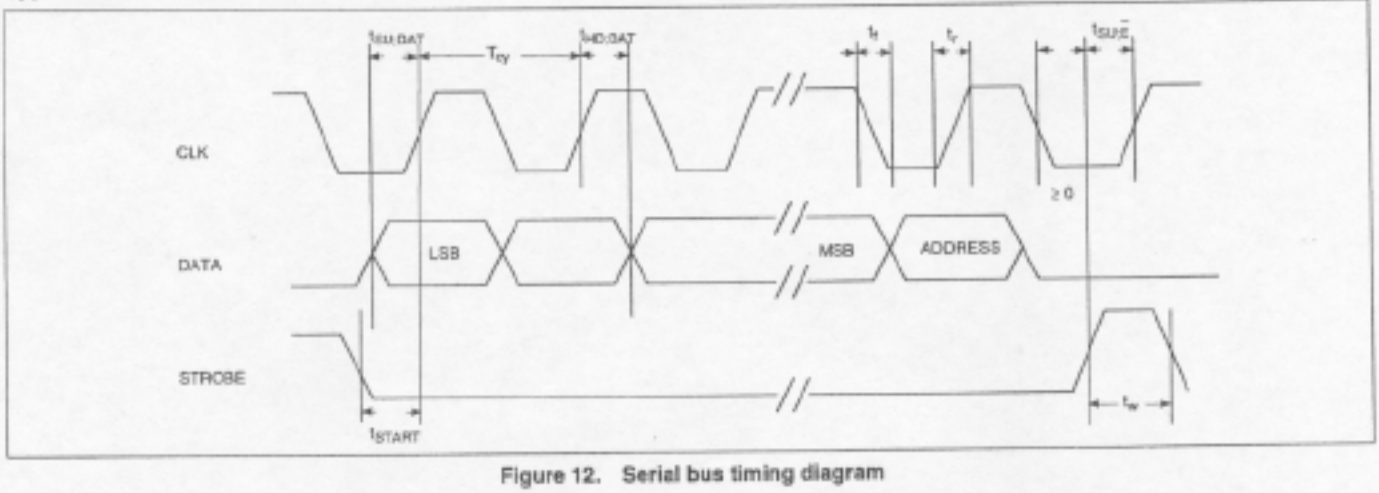


Figure 12. Serial bus timing diagram

LOOP FILTER

Component Designator	Value DUAL Mode
R1	4.3k Ω
R2	No Load
C1	33 nF
C2	3.3 nF
C3	No Load
R_{SET}	7.5 kΩ

Typical Filter Network

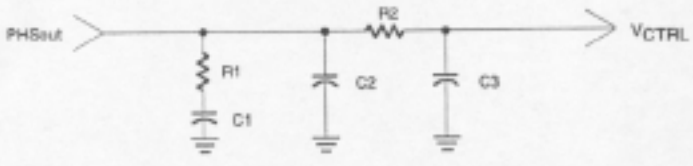


Figure 13. PLL loop filter

Reference Input

For cellular radio applications, the CD8455 will most likely utilize an external reference TCXO in order to provide the frequency stability necessary to operate to system requirements. The output of the system TCXO can be AC coupled to the $XTAL_1$ input. However, for applications that do not require such accuracy the crystal oscillator circuit can be configured as a Colpitts type oscillator with the addition of two external capacitors along with the reference crystal and a trim capacitor as shown in Figure 14.

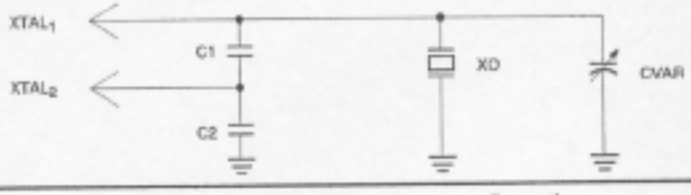


Figure 14. Crystal oscillator configuration

Component Designator	Value DUAL Mode
R1	4.7k Ω
R2	50 Ω
R3	10k Ω
C1	100 pF
C2	50 pF

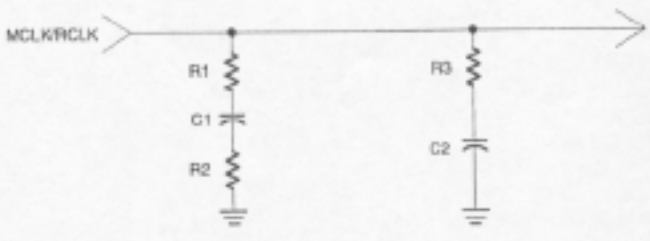


Figure 15. Reference buffer output test circuit

Data format

Table 1. Format of programmed data

LAST IN		MSB	SERIAL PROGRAMMING FORMAT				FIRST IN LSB
p23	p22	p21	p20	../..	../..	p1	p0

Table 2. A word, length 24 bits

Last in					MSB															LSB	First IN	
Address		fmod	Fractional-N		Main Divider ratio– Nmain																Spare	
0	0	Fmod	NF2	NF1	NF0	N15	N14	N13	N12	N11	N10	N9	N8	N7	N6	N5	N4	N3	N2	N1	N0	sk1	sk2
Default:		0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	1	0	0	0	0	0	0

A word select	Fixed to 00.
Fractional Modulus select	FM 0=modulo 8, 1=modulo 5.
Fractional-N Increment	NF2...0 Fractional N increment values 000 to 111.
N-Divider	N0...N15, Main divider values 512 to 65535 allowed for divider ratio.

Table 3. B word, length 24 bits

ADDRESS		REFERENCE DIVIDER NREF										RSM		RSA		FRACTIONAL COMPENSATION DAC							
0	1	R9	R8	R7	R6	R5	R4	R3	R2	R1	R0	RSM 1	RSM 0	RSA 1	RSA 0	Fdac 7	Fdac 6	Fdac 5	Fdac 4	Fdac 3	Fdac 2	Fdac 1	Fdac 0
Default:		0	0	0	1	0	1	0	0	0	1	0	0	0	0	x	x	x	x	x	x	x	x

B word select	Fixed to 01
R-Divider	R0...R9, Reference divider values 4 to 1023 allowed for divider ration.
Charge pump current Ratio	CP1, CP0: Charge pump current ratio, see table of charge pump currents.
Main comparison select	RSM Comparison divider select for main phase detector.
Aux comparison select	RSA Comparison divider select for auxiliary phase detector.
Fractional Compensation	Fdac7...0, Fractional compensation charge pump current DAC, values 0 to 255. FDAC = 77 for best op MOD8.

Table 4. C word, length 24 bits

ADDRESS		AUXILIARY DIVIDER NAUX													CP		LOCK		PD		SPARE	
1	0	A13	A12	A11	A10	A9	A8	A7	A6	A5	A4	A3	A2	A1	A0	CP1	CP0	LD1	LD0	PD1	PD2	PD3	LDO
Default		0	0	0	0	0	1	1	1	0	0	1	0	1	0	1	1	0	0	TX_{EN}	TX_{EN}	0	0

C word select	Fixed to 10
A-Divider	A0...A13, Auxiliary divider values 128 to 16384 allowed for divider ratio.
Charge pump current Ratio	CP1, CP0: Charge pump current ratio, see table for charge pump currents.
Lock detect output	LD1 LD0 0 0 Combined main, aux. & offset loop lock detect signal present at the LOCK pin. 0 1 Combined main and aux. lock detect signal present at the LOCK pin. 1 0 Main lock detect signal present at the LOCK pin. 1 1 Auxiliary loop lock detect signal present at the LOCK pin. When a section is in power down mode, the lock indicator for that section is high.
Power down	PD1=1: power to N-divider, reference divider, main charge pumps, PD1=0 to power down. PD2=1: power to Aux divider, reference divider, Aux charge pump, PD2=0 to power down.

Table 5. D word, length 24 bits

Address			Power Control								M divider		SE	TM	AD	Sleep Mode		Test pa_current					
1	1	0	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0	M1	M0	SE	TM	AD	SM1	SM2	pai5	pai4	pai3	pai2	pai1	pai0
Default:			x	x	x	x	x	x	x	x	0	0	0	0	0	0	0	0	0	0	0	0	0
D0 word select			Fixed to 110.																				
Output Power Control			PC7(msb)...PC0(lsb) Provides output power attenuation for DUAL mode amplifier outputs in 0.18 dB steps. Fx = 45.9 dB.																				
M Divider			00 = 6, 01 = 7, 10 = 8, 11 = 9																				
Offset loop power down			SE Offset loop synthesizer power down, SE = 1 power on, SE = 0 power down (sleep mode).																				
DUAL mode select			TM = 0 DUAL-mode																				
AMPS/DAMPS mode select			AD = 1 DAMPS mode. AD = 0 AMPs mode																				
TX buffers power down			SM1 TX Local oscillator buffers power down. SM1 = 1 power on, SM1 = 0 to power down. SM2 RCLK buffer power down. SM2 = 1 power on, SM2 = 0 to power down.																				
Test: pa_current pai			TX test bits for controlling the current in the power amp. Should be 0 during normal operation.																				

Table 6. Function Table

Symbol	Bits	Function
FMOD	1	Fractional-N modulus selection flag: '0' = modulo 8 '1' = modulo 5
NF	3	Fractional-N increment
NMAIN	16	Main divider ratio; 512 to 65,535 allowed
NREF	10	Reference divider ratio; 4 to 1,023 allowed, RSM, RSA = "0 0"
RSM	2	Reference select for main phase detector
RSA	2	Reference select for auxiliary phase detector
FDAC	8	Fractional compensation charge pump current DAC
NAUX	14	Auxiliary divider ratio; 128 to 16,384 allowed
CP	2	Charge pump current ratio select (see Table NO TAG)
LD	2	Lock detect output select (see Table 1)
PD1	1	PD1 = 0 for power down; shuts off power to main divider and main charge pumps, anded with PD2 to turn off ref. divider.
PD2	1	PD2 = 0 for power down; shuts off power to auxiliary divider, and auxiliary charge pumps; anded with PD1 to turn off ref. divider.
PC	8	Power control (see Note 3)
M	2	+M, M = 6, 7, 8, 9 (see Note 4)
SE	1	Transmit offset synthesizer on/off
TM	1	Transmit mode: '0' = DUAL
AD	1	Mode control, 1 = digital; 0 = analog
SM1	1	Sleep mode 1
SM2	1	Sleep mode 2

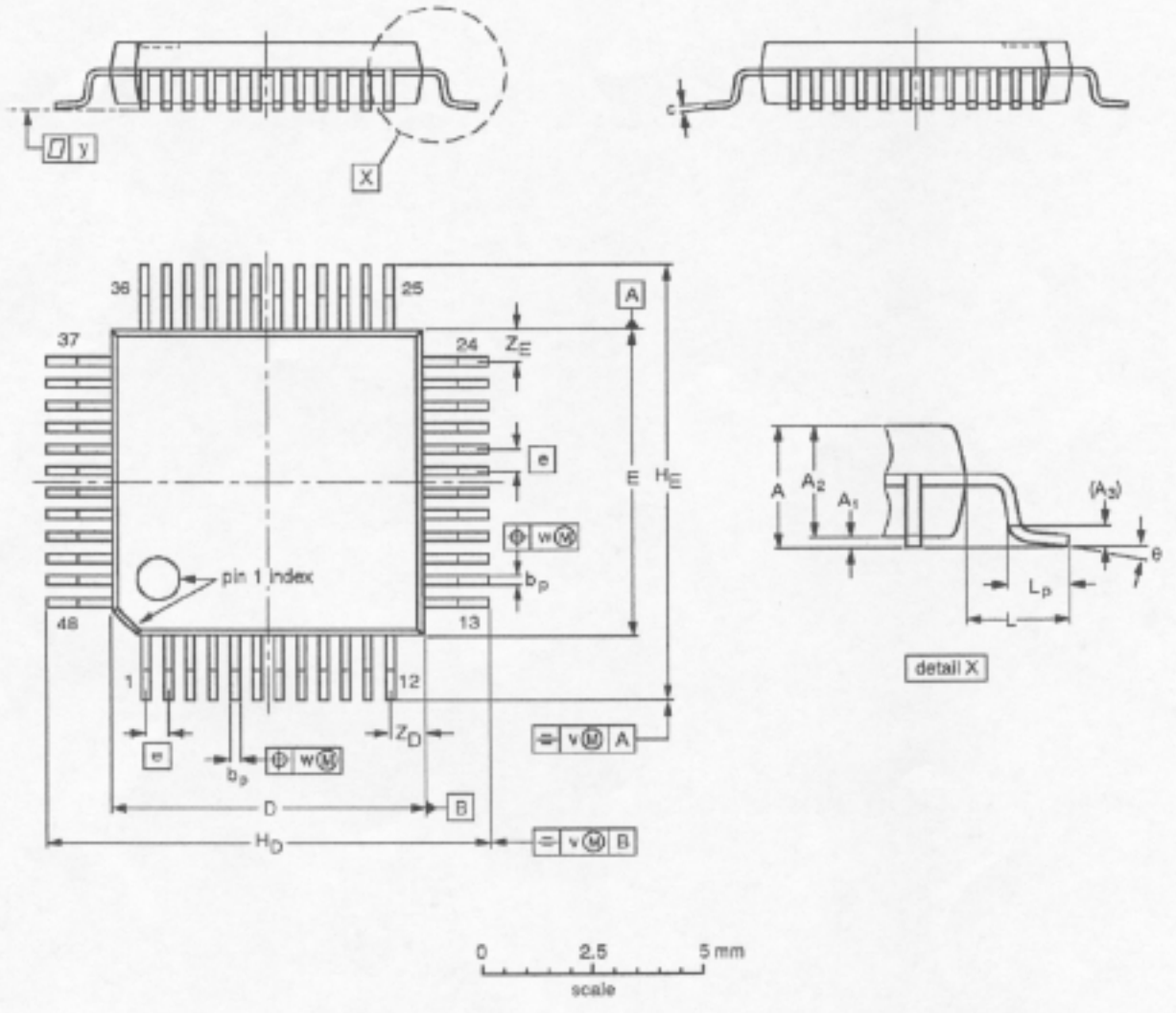
NOTES:

1. Data bits are shifted in on the the leading clock edge, with the least significant bit (LSB) first and the most significant bit (MSB) last.
2. On the rising edge of the strobe and with the address decoder output = 1, the contents of the input shift register are transferred to the working registers. The strobe rising edge comes one half clock period after the clock edge on which the MSB of a word is shifted in.
3. The PC bits are used for the power control function. Eight (8) bits of data allows for appropriate resolution of the power control. 00000000 = 0 dB; 11111111 = −45.9 dB (= 255 ÷ 0.18).
4. The M bits are used to program the ÷M counter for integer values between 6 and 9. 00 = 6, 01 = 7, 10 = 8, 11 = 9.
5. The TM bit is used to put the CD8455 into DUAL mode operation. In DUAL mode (TM = 0).
6. The AD bit allows a reduction in the linearity of the DUAL output driver while in AMPS mode.
7. The SM1 bit is used to shut down the TX_{LO} buffers. SM1 = 1, buffers on; SM1 = 0, buffers off.
8. The SM2 bit is used to shut down the RCLK buffer. SM2 = 1, buffer on; SM2 = 0, buffer off.
9. The SE bit turns on and off the offset loop synthesizer circuits. SE = 1, synthesizer on; SE = 0, synthesizer off.
10. The LOCK bits determine what signal is present on the LOCK pin as follows:

900 MHz transmit modulator and 2.5 GHz fractional-N synthesizer

CD8455

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_D	H_E	L	L_p	v	w	y	$Z_D^{(1)}$	$Z_E^{(1)}$	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2						~~94-12-19~~ 97-08-01