DATA SHEET

CD8455

900 MHz transmit modulator and 2.5 GHz fractional-N dual synthesizer

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TeLLUS Technology Inc.

DESCRIPTION

The CD8455 combines a 900 MHz transmit modulator with gain control, a 2.5 GHz fractional-N synthesizer, an auxiliary synthesizer, and an offset loop synthesizer. It is fabricated in a BiCMOS process—QUBiC2. The variable gain pre-driver amplifier delivers +10.0 dBm output power, which can attenuate 46 dB in 0.18 dB steps. The synthesizer section uses a fractional-N main divider that operates to 2.5 GHz, providing fast switching in narrow-band applications. The integer type auxiliary divider operates up to 550 MHz. The third synthesizer provides the offset frequency needed between transmit and receive modes. By using an external upconvert mixer, a PCS frequency signal can be obtained for high-band operation. A 3-wire bus is used to program all operational modes of the CD8455. The CD8455 is intended for IS-136 standard.

FEATURES

- I/Q modulator, direct modulation of RF
- +10.0 dBm output power
- 46 dB variable gain predriver
- Fractional-N main synthesizer with fractional compensation
- Three synthesizers: main, auxiliary, and offset loop
- 3-wire serial bus (CLK, STROBE, DATA)
- Control logic for programming
- Reference clock and buffers
- Power down modes

APPLICATIONS

- IS-136 standard
- Wireless communications

PIN CONFIGURATION

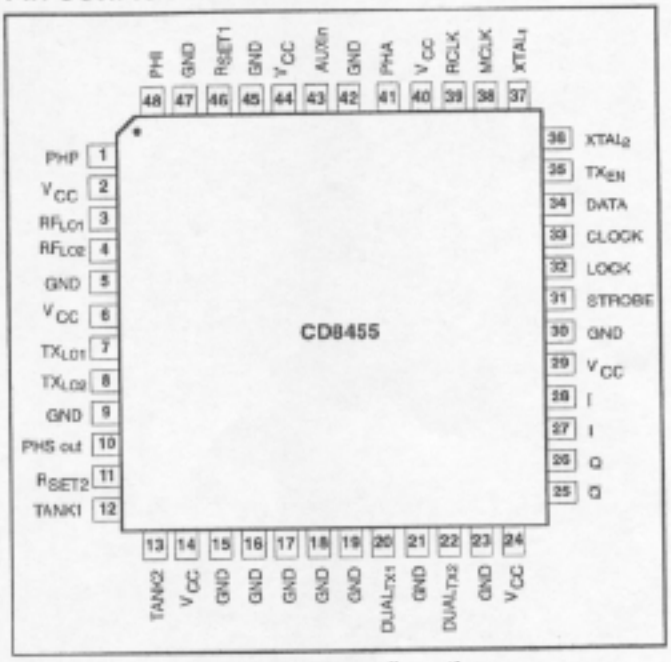


Figure 1. Pin configuration

QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{CC}	Supply voltage	V_{CC}	3.6	3.75	3.9	V
I_{CC}	Supply current	full power analog	–	105	120	mA
		full power digital	–	122	142	mA
I_{CC_sleep}	Total supply current in power-down mode		–	2.3	3.5	mA
f_{Main}	Input frequency, main divider		800	–	2200	MHz
f_{Aux}	Input frequency, auxiliary divider		40	–	200	MHz
f_{Offset}	Input frequency, offset divider		90	–	180	MHz
f_{Ref}	Reference input frequency		10	–	40	MHz
T_{amb}	Operating ambient temperature		−40	–	+85	°C

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
CD8455	LQFP48	Plastic low profile quad flat package; 48 leads; body 7x7x1.4 mm	SOT313-2

CONNECTIONS

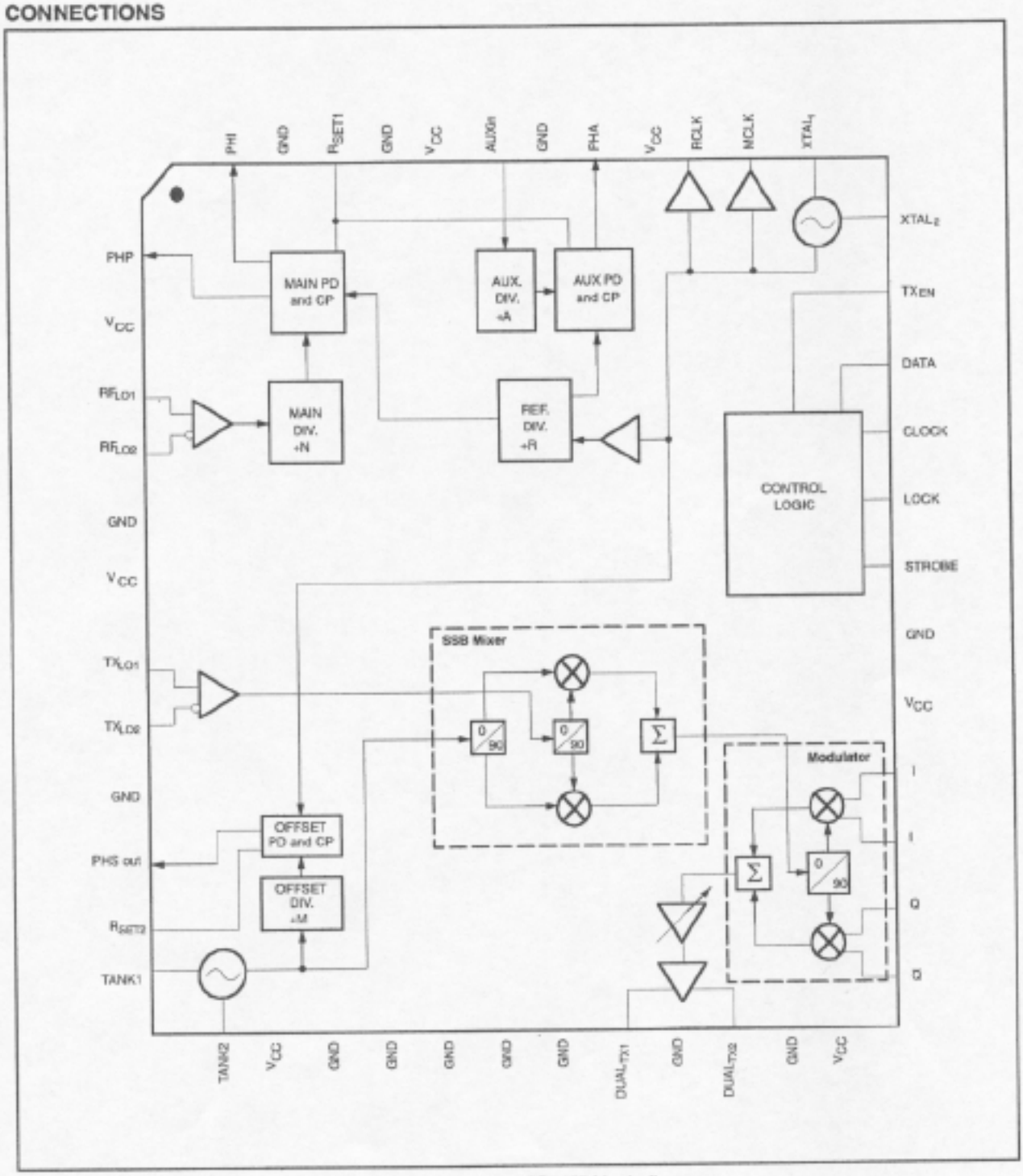


Figure 2. CD8455 block diagram

PIN DESCRIPTIONS

PIN NO.	PIN	DESCRIPTION
1	PHP	Proportional charge pump output
2	V_{CC}	Digital supply voltage
3	RF_{LO1}	Differential LO input
4	RF_{LO2}	Differential LO input
5	GND	Digital Ground
6	V_{CC}	Offset synthesizer supply voltage
7	TX_{LO1}	Differential Transmit LO Input
8	TX_{LO2}	Differential Transmit LO Input
9	GND	Offset synthesizer ground
10	PHS out	Charge pump output (transmit offset)
11	R_{SET2}	PHS out current set resistor
12	TANK1	VCO differential tank
13	TANK2	VCO differential tank
14	V_{CC}	Tx supply voltage
15	GND	Tx Ground
16	GND	Tx Ground
17	GND	Tx Ground
18	GND	Tx Ground
19	GND	Tx Ground
20	$DUAL_{TX1}$	Dual mode RF output
21	GND	Tx Ground
22	$DUAL_{TX2}$	Dual mode RF output
23	GND	Tx Ground
24	V_{CC}	Tx supply voltage
25	$\overline{Q}$	Inverting quadrature input
26	Q	Non-Inverting quadrature input
27	I	Non-inverting in phase modulation input
28	$\overline{I}$	Inverting in phase modulation input
29	V_{CC}	Tx supply voltage
30	GND	Tx Ground
31	STROBE	Data input latch enable
32	LOCK	Lock detect
33	CLOCK	Serial clock input
34	DATA	Serial data input
35	TX_{EN}	Transmit enable
36	$XTAL_2$	Crystal Oscillator emitter input
37	$XTAL_1$	Crystal Oscillator base input
38	MCLK	Buffered oscillator output
39	RCLK	Buffered oscillator output
40	V_{CC}	REF supply voltage
41	PHA	Auxiliary charge pump output
42	GND	REF Ground
43	AUXin	RX_{IF} input
44	V_{CC}	Main and aux. CP supply voltage
45	GND	Main and aux. CP Ground
46	R_{SET1}	Main and aux. CP current set resistor
47	GND	Main and aux. CP Ground
48	PHI	Integral charge pump output

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER	VALUE		UNIT
		MIN.	MAX.	
V_{CC}	Supply voltage	−0.3	+4.5	V
V_{IN}	Voltage applied to any other pin	−0.3	V_{CC}+0.3	V
P_N	Power dissipation, T_A = 25°C (still air)		980	mW
T_{JMAX}	Operation junction temperature		150	°C
P_{MAX}	Power input/output		+10/+14	dBm
I_{MAX}	DC current into any I/O pin	−10	+10	mA
T_{STG}	Storage temperature	−65	+150	°C
T_o	Operating temperature	−40	+85	°C

DC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.75 V; T_A = +25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
V_{CC}	Power supply range		3.6	3.75	3.9	V
I_{CC}	Supply current	Sleep mode		2.3	3.5	mA
		Standby mode		18.5	20	
		Operating: full power analog		105	120	
		Operating: full power digital DUAL (CW Mode)		122	142	
V_{IL}	Clock, Data, Strobe, TX_{EN}	Input logic low	−0.3		$0.3V_{CC}$	V
V_{IH}	Clock, data, strobe, TX_{EN}	Input logic high	$0.7V_{CC}$		V_{CC}+0.3	V

AC ELECTRICAL CHARACTERISTICS

V_{CC} = +3.75 V; f_{OFFin} = 155.52 MHz; f_{LO} = 992.02 MHz; I/Q Level= 0.9 V_{P-P}; T_A = +25°C; unless otherwise stated.

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNITS
			MIN	–3.	TYP	+3.	MAX	
MODULATOR								
$TX_{LO\ 1/2}$	Transmit LO input (AC-coupled; 50 Ω single-ended, 100 Ω differential)	Input power Frequency range	–13 900				–10 1100	dBm MHz
$XTAL_1$	Osc. transistor base	Osc. frequency			20			MHz
$XTAL_2$	Osc. transistor emitter	Osc. frequency			20			MHz
XO	Negative resistance				–100			Ω
RCLK, MCLK	Reference buffer output Frequency range Output levels Harmonic content	Z_{LOAD} = see test circuit	 10 0.4		 0.6		 40 1.4 –7	 MHz V_{P-P} dBc
Q / $\overline{Q}$ I / $\overline{I}$	Baseband in-phase differential inputs	Input frequency Diff. mod. level Diff. input impedance DC bias point	 0.8 10.0 1.6		0.2 0.9 $0.5V_{CC}$		1.8 1.0 2.0	MHz V_{P-P} kΩ V
$DUAL_{TX}$	DUAL output SE=1, TX_{EN}=1 (with external matching) (50 Ω)	AMPS/DAMPS	824				849	MHz
$DUAL_{TX}$	Differential output, ($DUAL_{TX}$) open-collector, matched to 200 Ω differential impedance	Output level (avg. min., I and Q quad., 0 dB VGA) Gain flatness	+9.0		+10.0 1			dBm dB
$DUAL_{TX}$	VGA dynamic range	VGA = 00 to VGA = FF	43		45.9		49	dB
$DUAL_{TX}$	Linearity worst case intermod. products (0 dB VGA OR +9 dBm, whichever is less, I & Q in-phase)	3rd-order 5th-order 7th-order			–42 –55 –65		–34 –45	dBc
$DUAL_{TX}$	Carrier suppression (I & Q in quadrature)	VGA = 00 VGA = FF	–34		–40 –33			dBc
$DUAL_{TX}$	Sideband suppression (I & Q in quadrature)		–35		–45			dBc
$DUAL_{TX}$	Broad-band noise (0 dB VGA or +9 dBm, whichever is less)	869 to 894 MHz			–125			dBm/Hz
$DUAL_{TX}$	Adjacent channel noise power	@ ±30 kHz			–95			dBc/Hz
$DUAL_{TX}$	Alternate channel noise power	@ ±60 kHz			–101			dBc/Hz
	Spurious output	824 to 849 MHz			–56			dBc
		869 to 894 MHz			–56			dBc

SYNTHESIZER ELECTRICAL CHARACTERISTICS

V_{CC} = +3.75 V, T_A = +25°C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
RFin main divider input						
f_{Main}	Main divider input frequency		800	–	2200	MHz
$V_{RFin(rms)}$	AC-coupled input signal level	R_S = 50 Ω; single-ended drive; MAX. limit is indicative	–15	–	0	dBm
N_M	Main divider ratio		512	–	65535	
Auxiliary reference divider input						
f_{AUXin}	Input frequency range		40	–	200	MHz
V_{AUXin}	AC-coupled input signal level	R_S = 50 Ω; MAX. limit is indicative	–18	–	0	dBm
			80	–	632	mVpp
Z_{AUXin}	Input impedance (real part)		–	10	–	kΩ
C_{AUXin}	Typical pin input capacitance	indicative, not tested	–	1	–	pF
N_A	Auxiliary division ratio		128	–	16383	
Reference divider input						
f_{REFin}	Input frequency range from TCXO		10	–	40	MHz
VRFin	AC-coupled input signal level	single-ended drive; MAX. limit is indicative	800	–		mVpp
N_R	Reference division ratio	SA = SM = "000"	4	–	1023	
Offset divider input						
f_{OFFin}	Input frequency range		90	–	180	MHz
N_O	Offset division ratio: 6, 7, 8, 9		6	–	9	
Charge pump current setting resistors input						
R_{SET1}	External resistor from pin to ground		6	7.5	15	kΩ
V_{SET1}	Regulated voltage at pin	R_{SET1} = 7.5 kΩ	–	1.25	–	V
R_{SET2}	External resistor from pin to ground		4.7		5.6	kΩ
Charge pump outputs (including fractional compensation pump); R_{SET1} = 7.5 kΩ, FC = 76						
I_{CP}	Charge pump current ratio to I_{SET1}	CURRENT GAIN I_{PH}/I_{SET1}	–15		+15	%
I_{MATCH}	Sink-to-source current matching	V_{PH} = 0.5 V_{CC}	–10		+10	%
I_{ZOUT}	Output current variation versus V_{PH}[1]	V_{PH} in compliance range	–10		+10	%
I_{LPH}	Charge pump off leakage current	V_{CP} = 0.5 V_{CC}	–10		+10	nA
V_{PH}	Charge pump voltage compliance		0.6	–	V_{CC}–0.8	V
Offset Loop Charge Pump Outputs R_{SET2} = 4.7 kΩ						
I_{OPH}	Charge pump current ratio to I_{SET2}		–25		25	%
I_{MATCH}	Sink to source current matching	V_{PHS} = 0.5 V_{CC}	–15		15	%
I_{ZOUT}	Current output variation versus V_{PH}[1]	V_{PHS} in compliance range	–25		25	%
V_{PH}	Charge pump voltage compliance		0.7		V_{CC}–0.7	V

CHARACTERISTICS (CONTINUED)

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Phase noise (condition R_{SET1} = 7.5 kΩ, CP = 00)						
$\mathcal{L}(f)$	Synthesizer's contribution to close-in-phase noise of 2100 MHz RF signal at 1 kHz offset.	fref = 19.44 MHz; 632 mV_{pp} fcomp = 240 kHz indicative, not tested	–	–71	–	dBc/Hz
Interface logic input signal levels						
V_{IH}	HIGH level input voltage		0.7 V_{CC}	–	V_{CC}+0.3	V
V_{IL}	LOW level input voltage		–0.3	–	0.3 V_{CC}	V
Lock detect output signal (in push/pull mode)						
V_{OL}	LOW level output voltage	I_{sink} = 2 mA	–	–	0.4	V
V_{OH}	HIGH level output voltage	I_{source} = –2 mA	V_{CC}–0.4	–	–	V

1. The relative output current variation is defined thus:
$\Delta I_{out}/I_{out} = 2x(I_2-I_1)/|(I_2+I_1)|$; with V_1=0.7 V, V_2=V_{CC}–0.8 V or V_2 = V_{CC}–0.7 V (see Figure 3)

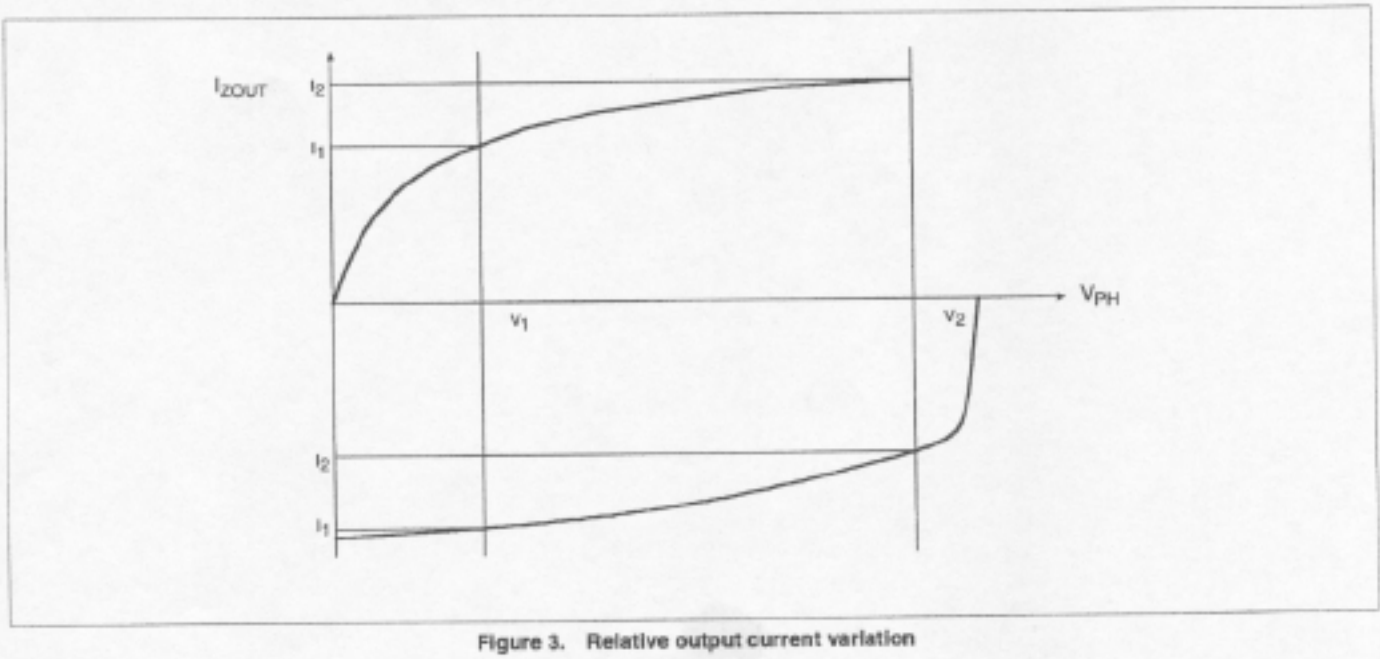


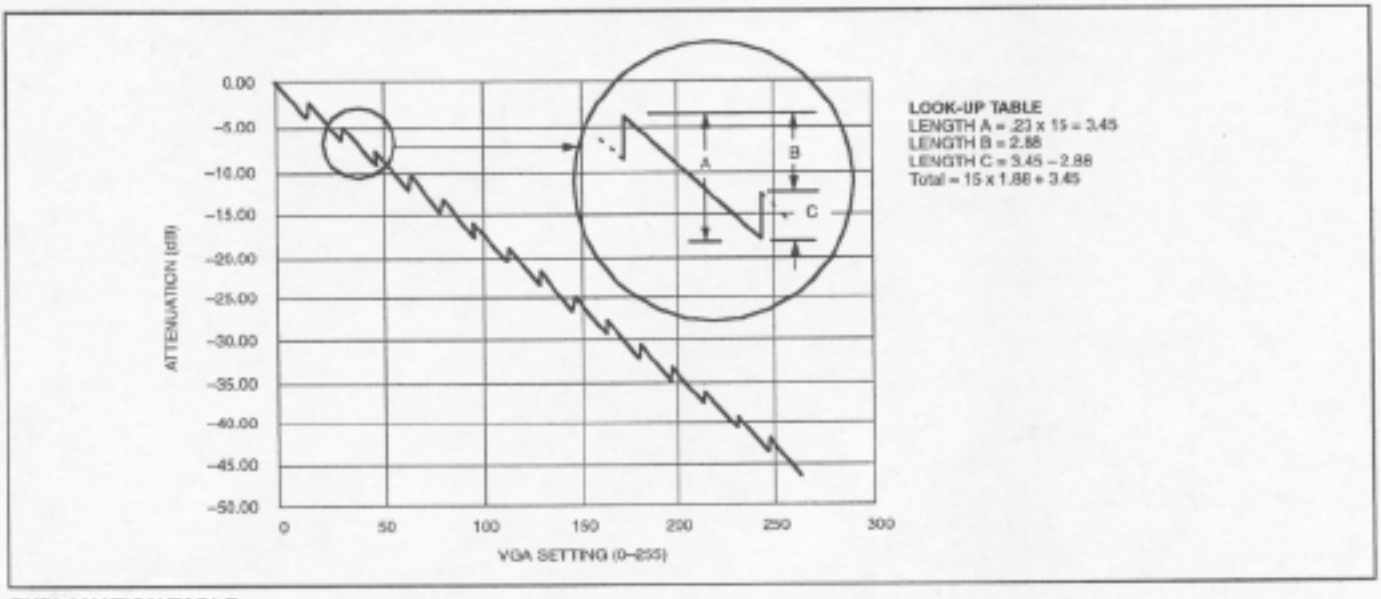
Figure 3. Relative output current variation

OPERATING MODES & POWER DOWN CONTROL

The CD8455 has two power saving modes of operation: sleep mode and stand-by mode. The intention of these modes is to disable circuitry that is not in use at the time of operation to reduce power consumption. During sleep mode, only circuitry that is required to provide master clock (MCLK) to the digital portion of the system is enabled. During stand-by mode, circuitry that supports receiving functionality, such as MCLK, RCLK, synthesizers and input buffers are enabled. In transmit mode, all the functions of the device are enabled.

I/Q MODULATOR AND POWER CONTROL

CD8455 is comprised an offset VCO, a buffer amplifier, an image reject mixer or upconverter, an I/Q modulator, a Variable Gain Amplifier (VGA), and a pre-driver. The offset oscillator generates the transmitter IF signal, which can be modulated in the AMPS mode. The transmitter local oscillator (TX_LO) signal is amplified to the required level in the local oscillator buffer and is mixed with the offset frequency in the upconverter. The upconverter output frequency is equal to the difference of the local oscillator and the offset frequencies. This signal can be modulated in an I/Q modulator and applied to the VGA, which has a 46 dB dynamic range. The VGA gain can be controlled via PC bits (PC7 to PC0). The LSB (PC3 to PC0) adjust the output power in fine steps, 0.23 dB/step, while the MSB (PC7 to PC4) provide coarse adjustment, 2.88 dB/step. The pre-driver provides sufficient gain to deliver +9 dBm linear power to a 50 Ω load via an external matching circuit.



EXPLANATION TABLE

- Each segment covers 16 LSB (0 . 15) of the VGA and provides 3.45 dB (= 15*0.23 dB).
- The discontinuities happen whenever one of the 4 MSB bits changes at 2.88 dB intervals (C).
- The magnitude of the discontinuities are nominally 0.57 dB; and they may vary by the accuracy of the VGA. The magnitude is always positive, A = 0.57 +0.53, or 0.57 −0.22 dB.

Figure 4. Power control monotonicity

DIGITAL MODE OPERATION

In the digital mode of operation, the AD control bit should be set to high (=1). The offset loop synthesizer is controlled via the SE bit. The transmitter path is enabled by the positive edge of the TXEN. This signal is used to control the operation of the transmitter within the required time slots in TDMA standards. The digital modulation is implemented by applying the baseband signal to the I/Q input pins and the output power is adjusted via the VGA.

AMPS MODE OPERATION

In the AMPS mode, the FM signal can be implemented either by modulating the frequency of the offset loop or modulating the carrier at RF in the I/Q modulator. In order to modulate the offset frequency, the baseband signal is applied to the offset VCO. The offset frequency is much higher than the bandwidth of the baseband, therefore, the loop can be kept locked while its frequency is modulated by the baseband with an appropriate loop filter. In this case, the offset loop behaves like a high pass filter and is not able to modulate the DC or the very low frequency components of the baseband. Then the modulated signal is upconverted to the desired output frequency and applied to the I/Q modulator. In this implementation, a DC voltage should be applied to the I/Q modulator inputs enabling this block to pass the signal to the VGA. If the modulation is implemented in the I/Q modulator, the modulating signal, generated by a baseband processor externally, is applied the the I/Q input pins. The modulated signal is amplified in the pre-driver and its level is controlled via the VGA control bits.

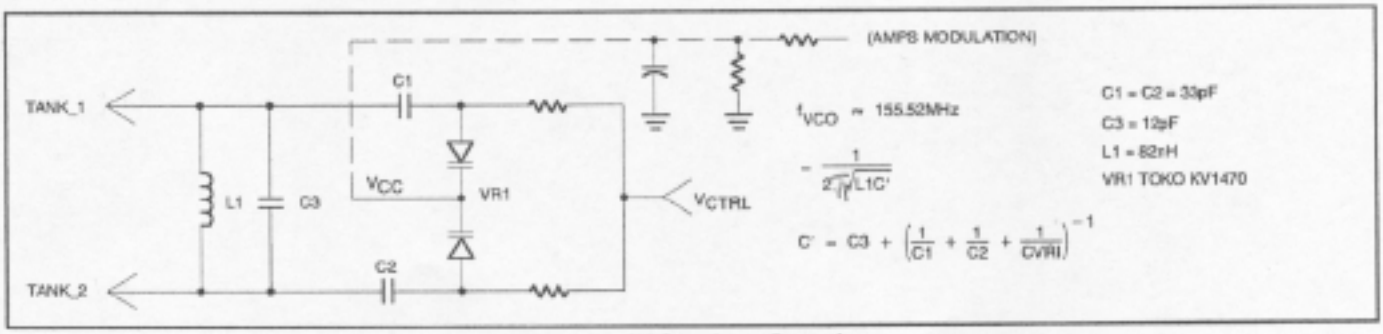


Figure 5. VCO tank configuration

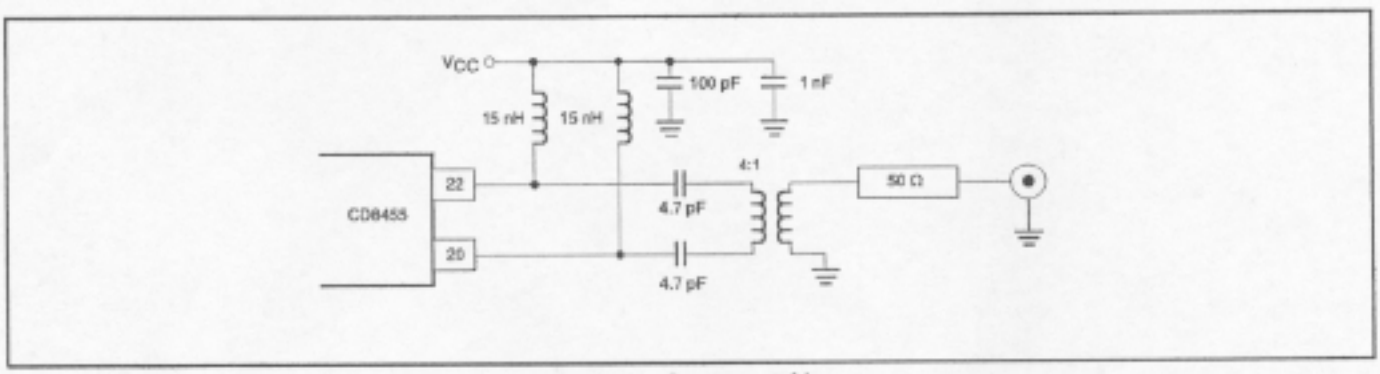


Figure 6. Output matching