RF2402

UHF QUADRATURE MODULATOR

Typical Applications

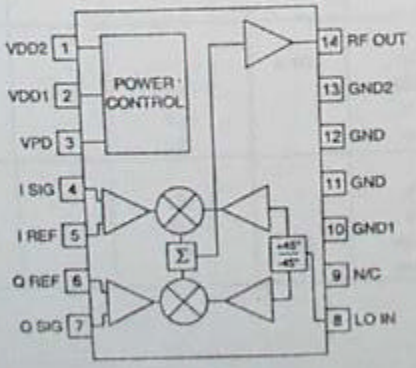
- Digital and Spread Spectrum Systems
- GMSK, QPSK, DQPSK, QAM Modulation
- GSM and D-AMPS Cellular Systems
- AM, SSB, DSB Modulation
- Image-Reject Upconverters

Product Description

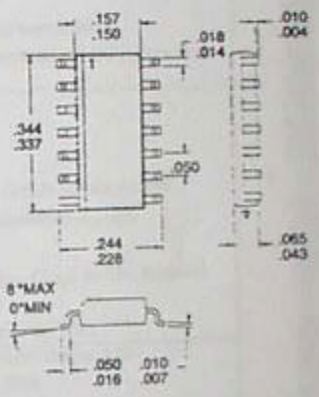
The RF2402 is a monolithic integrated universal modulation system capable of generating modulated AM, PM, or compound carriers in the UHF frequency range. The IC contains all of the required components to implement the modulation function including differential amplifiers for the baseband inputs, a 90° hybrid phase splitter, limiting LO amplifiers, two balanced mixers, a combining amplifier, and an output RF amplifier which will drive a 50Ω load. Component matching, which can only be accomplished with monolithic construction, is used to full advantage to obtain excellent amplitude balance and high phase accuracy. The unit features low power consumption, single power supply operation, and adjustment free operation with no external parts required to operate the part as specified.

Optimum Technology Matching™ Applied

☐ Si BJT ☐ GaAs HBT ☑ GaAs MESFET
☐ Si Bi-CMOS



Functional Block Diagram



Package Style: SOP-14

Features

- Single 3V to 5V Power Supply
- Low Power and Small Size
- CMOS Compatible Power Down Control
- Excellent Amplitude and Phase Balance
- Low Broadband Noise Floor
- 600MHz to 1000MHz Operation

Ordering Information

RF2402	UHF Quadrature Modulator
RF2402 PCBA	Fully Assembled Evaluation Board

RF Micro Devices, Inc.
7625 Thorndike Road
Greensboro, NC 27409, USA
Tel (910) 664 1233
Fax (910) 664 0454
http://www.rfmd.com

Rev A3 970227

Absolute Maximum Ratings

Parameter	Rating	Unit
Supply Voltage (V_{DD})	-0.5 to +7.5	V_{DC}
Power Down Voltage	-0.5 to V_{DD}+0.4	V_{DC}
Input LO and RF Levels	+6	dBm
Operating Ambient Temperature	-40 to +85	°C
Storage Temperature	-40 to +150	°C

Caution! ESD sensitive device.

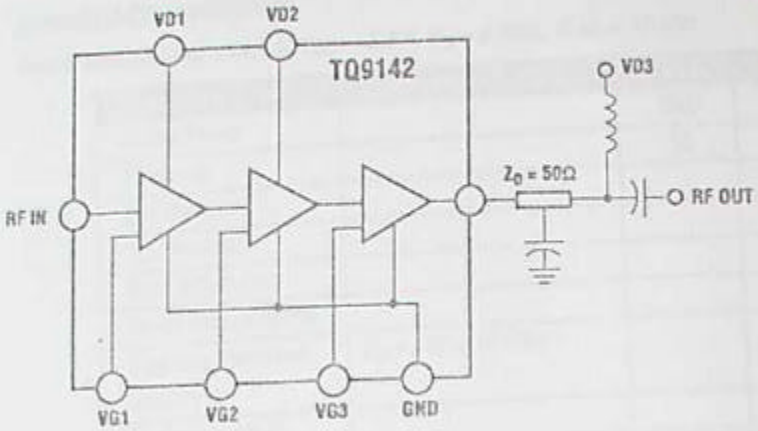
Parameter	Specification			Unit	Condition
	Min.	Typ.	Max.		
Carrier Input					T=25°C, V_{CC}=5V_{DC}, I&Q inputs=2V_{PP}
Frequency Range		600 to 1000		MHz	
Power Level		-3 to +6		dBm	
Input VSWR		1.2:1			With external 50Ω termination.
Input Impedance		200-j200		Ω	At 900MHz, without external 50Ω termination.
Modulation Input					
Frequency Range		DC to 100		MHz	
Reference Voltage (V_{REF})		2.0 to 3.0		V	
Modulation (I&Q)		V_{REF}±2		V	I & Q signals for 0dBm output power.
Maximum Modulation (I&Q)		V_{REF}±2.5		V	In-phase and quadrature signals.
Input Resistance		3000		Ω	
DC Offset		50	150	mV	I_{SIG}-I_{REF} and Q_{SIG}-Q_{REF} for DC balance
Amplitude Error (I/Q)		0.2		dB	
Quadrature Phase Error		±3		°	From 800MHz to 1000MHz.
RF Output					V_{DD}=5V, LO Power=0dBm, LO Freq=900MHz, SSB
Output Power		0		dBm	
Output Impedance		50		Ω	
Output VSWR		1.5:1			
Broadband Noise Floor		-155		dBm/Hz	
Sideband Suppression		25		dB	
Carrier Suppression		40		dB	Modulation DC offset externally adjusted for optimum suppression. Suppression is typically better than 25dB without adjustment.
Power Down					
Turn On/Off Time			<100	ns	
PD Input Resistance		>1		MΩ	
Power Down "ON"		V_{CC}		V	Threshold voltage
Power Down "OFF"		0		V	Threshold voltage
Power Supply					
Voltage		5		V	Specifications
		3 to 5.5		V	Operating Limits
Current		28	39	mA	Operating
		0.5	2	mA	Power Down

TRIQUINT SEMICONDUCTOR, INC.

TQS WIRELESS COMMUNICATIONS

TQ9142B

High-Efficiency 3-Stage AMPS Power Amplifier IC



The TQ9142B is a highly efficient 3-stage power amplifier developed for handsets and portable terminals operating in the AMPS cellular band (824-849 MHz). The part is designed to require minimal external circuitry for matching or bias, simplifying design and keeping board space and cost to a minimum. Access to each stage's gate and drain voltages is provided for maximum flexibility in selection of output power control method, making output power vs. efficiency tradeoffs, or for implementing alternative biasing schemes. The amplifier is packaged in a space-efficient SOIC-16 plastic package with specially modified central thermal tabs. These tabs provide reliable operation for the 1.4 Watt power output.

Electrical Specifications

Test Conditions: V_{DD} = +4.8 V, V_{GG} = −3.5 V, T_A = 25 °C, P_{IN} = 0 dBm

Parameter[1]	Min	Typ	Max	Units
Frequency Range	824		849	MHz
Output Power	30.0	31.0		dBm
Efficiency	55	60		%
Input Return Loss		10		dB
Supply Voltage		4.8		V

1. Min/max values listed here are 100% production tested.

Features

- 60% drain efficiency
- +31.0 dBm power output @ 4.8 V
- 4.8 V to 6.0 V battery operation
- SO-16 package
- 50-Ω matched input
- Monolithic construction

Applications

- Analog cellular handsets
- CDPD terminals

Operating Range

Parameter	Conditions	Min	Typ	Max	Units
Frequency Range	Matched for cellular band	824		849	MHz
Supply Voltage (V_{DD})	Output power varies w/supply voltage	2.7	5.0	7.0	V
Temperature	Measured at case	-40	25	110	°C

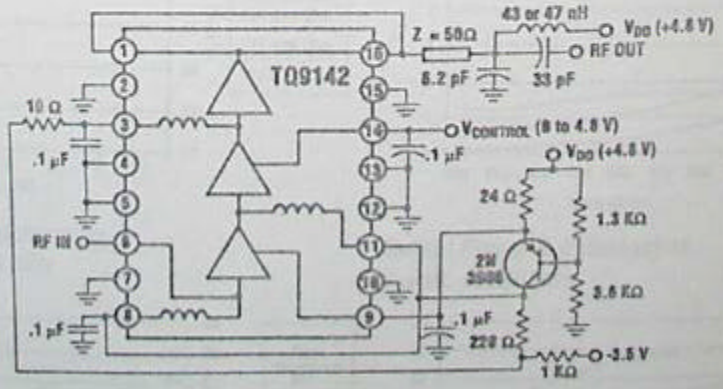
Electrical Characteristics

Test Conditions: V_{DD} = +4.8 V, V_{GG} = −3.5 V, P_{IN} = 0 dBm, B.W. = 30 KHz

Parameter	Conditions	Min	Typ	Max	Units
Output Power		30.0	31.0		dBm
Efficiency		55	60		%
2nd Harmonic			-35		dBc
3rd Harmonic			-45		dBc
Input Return Loss			10		dB
Power Control Range			25		dB
Spurious Levels and Stability (1)	P_{IN} = -40 to +0 dBm		-80		dBc
Rx Band Noise (2)			-88		dBm
Gain (small signal)	P_{IN} = -10 dBm		40		dB
Negative Supply Current			2	5	mA
Ruggedness (3)		No Degradation			

Notes: 1. Load VSWR set to 7:1 and the angle is varied 360°. All spurious outputs will be less than -80 dBc. No large-signal oscillations permitted.
2. Noise power is measured in 30 KHz bandwidth at the transmit frequency plus 45 MHz.
3. Burnout testing. Load set to 50 ohms, output power is measured at nominal test conditions. Load VSWR set to 10:1 and the angle varied 360° over 60 seconds. Load set to 50 ohms, output power is measured again and compared with the first measurement to check for no degradation from first measurement.

Test Circuit

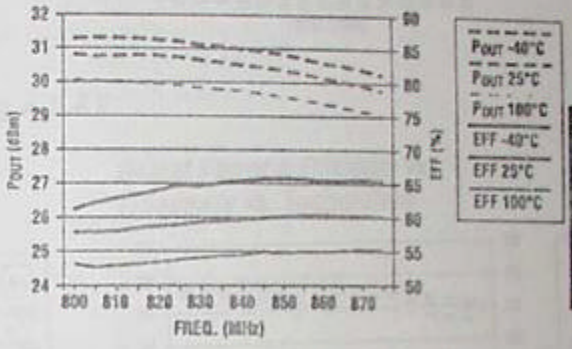


Bias Circuit Description

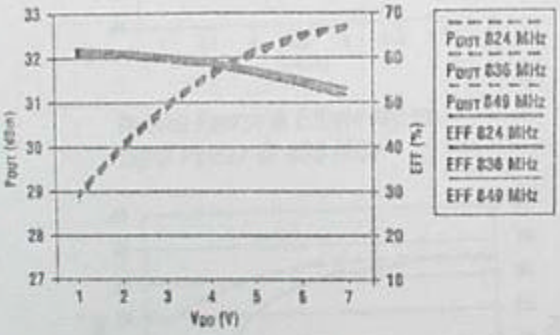
The TQ9142B is tested with the bias stabilization circuit shown in the test circuit schematic above. This circuit accurately sets the bias point for the power amplifier and provides low quiescent current and excellent efficiency at all operating voltages and output powers. Output power may be controlled by varying the supply voltage marked $V_{CONTROL}$. TriQuint recommends this circuit be incorporated into designs to provide the most predictable performance and the most robust performance in high-volume applications. The PNP transistor may be a 2N3906 or equivalent. A small footprint, dual PNP transistor such as the Rohm UMT1N, may also be used. The second PNP can be connected as a diode to temperature compensate the bias circuit.

Typical Performance – Tuned for V_{DD} (nom) = 4.8 V

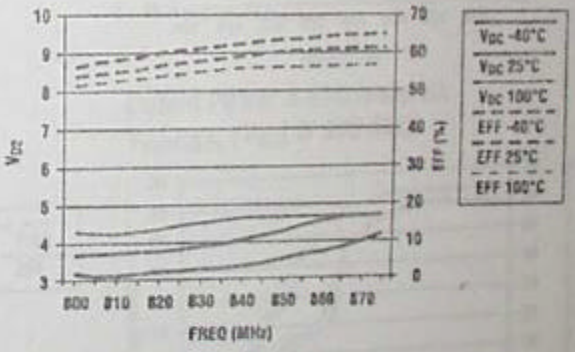
Output Power & Efficiency vs. Frequency vs. Temperature



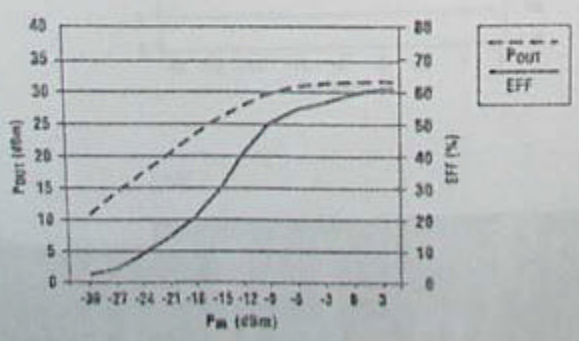
Output Power & Efficiency vs. V_{DD} vs. Frequency



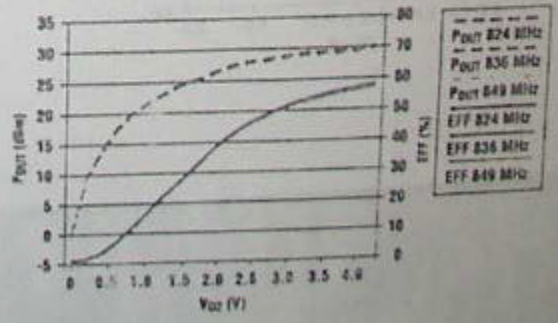
V_{D2} & Efficiency vs. Frequency vs. Temperature at Constant P_{OUT} of 30 dBm



Output Power & Efficiency vs. Input Power @ 836 MHz

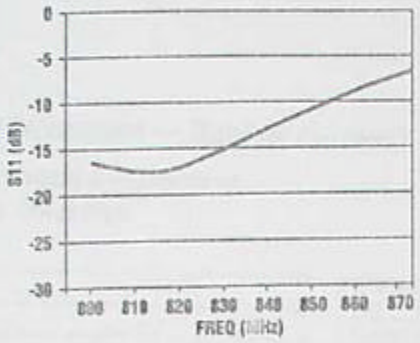


Output Power & Efficiency vs. V_{D2} vs. Frequency

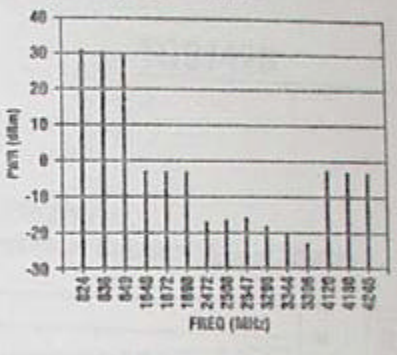


Typical Performance — Tuned for V_{DD} (nom) = 4.8 V

S11 vs. Frequency

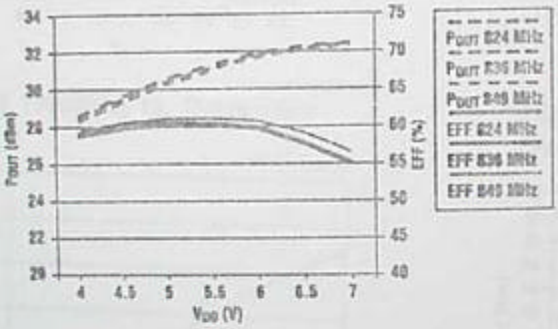


Fundamental & Harmonics vs. Frequency @ T = 25°C

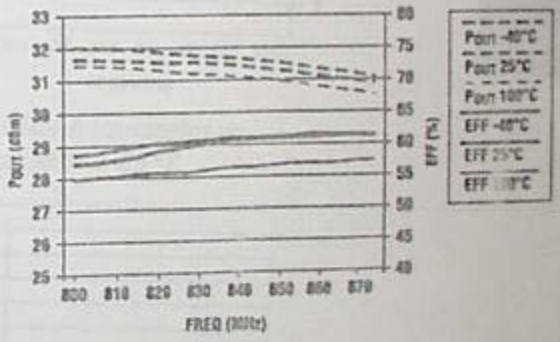


Typical Performance — Tuned for V_{DD} (nom) = 5.8 V

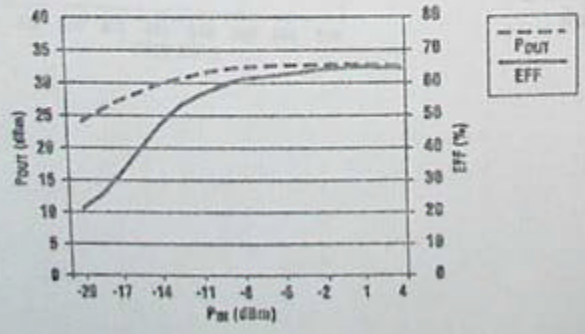
Output Power & Efficiency vs. V_{DD} vs. Frequency



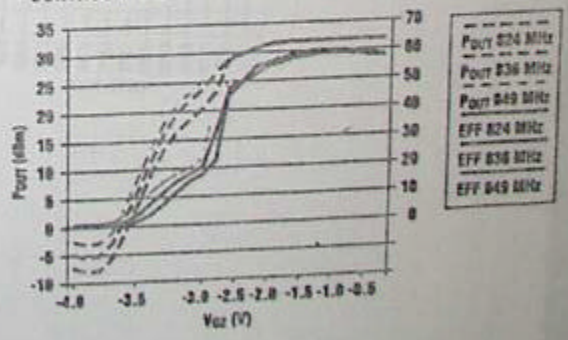
Output Power & Efficiency vs. Frequency vs. Temperature



Output Power & Efficiency vs. Input Power @ 836 MHz

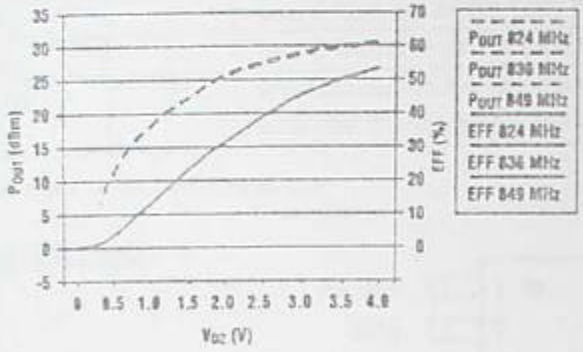


Output Power & Efficiency vs. $V_{CONTROL}$ (V_{G2}) @ 836 MHz

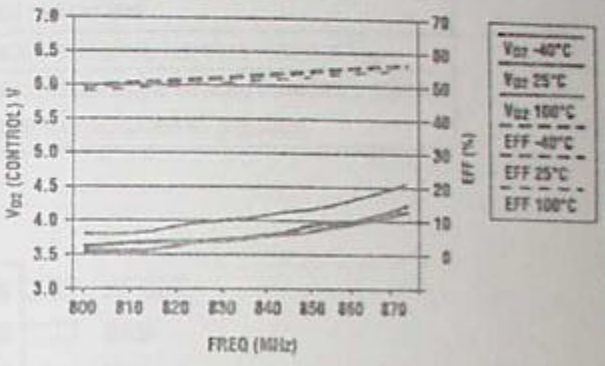


Typical Performance — Tuned for V_{DD} (nom) = 5.8 V

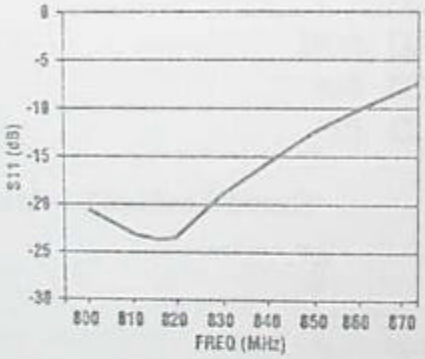
Power Output & Efficiency vs. V_{D2} vs. Frequency



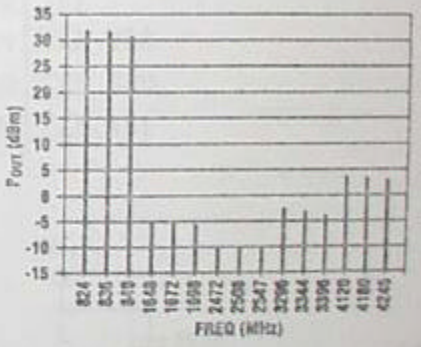
V_{D2} & Efficiency vs. Temperature at Constant P_{OUT} of 30 dBm



S11 vs. Frequency vs. Temperature



Fundamental & Harmonics vs. Frequency @ T = 25°C

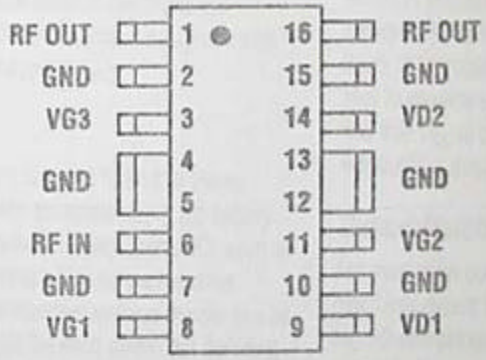


Pin Descriptions

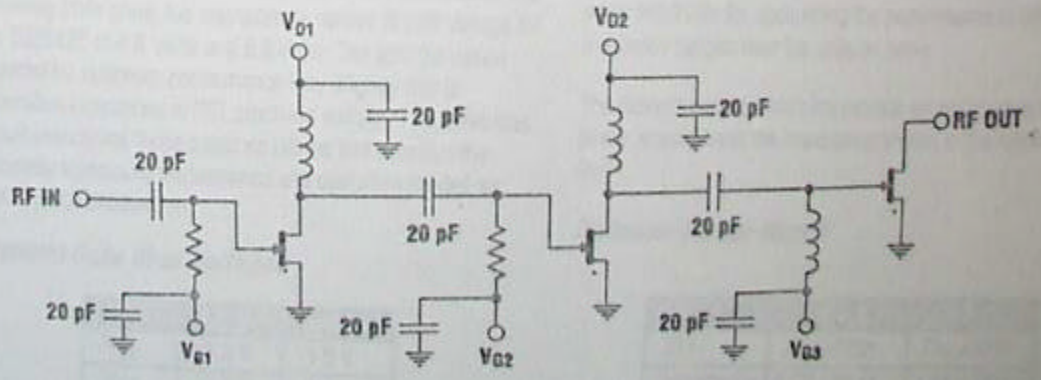
Pin Name	Pin #	Description
RF OUT	1,16	Power amplifier output. Critical, but simple, matching circuit required.
V_{G3}	3	Output-stage gate voltage. Requires 51 Ω series resistor near device for stability. Local bypass cap required.
RF IN	6	Power amplifier input. Matched to 50 ohms. Internal DC block.
V_{G1}	8	First-stage gate voltage. Set V_{G1} = -1.5 V or use bias stabilization circuit.
V_{D1}	9	Input-stage supply voltage. Local bypass cap recommended. Use same voltage as V_{D3} or use bias stabilization circuit.
V_{G2}	11	Second-stage gate voltage. Local bypass cap required.
V_{D2}	14	Second-stage drain voltage. Local bypass cap required. Use same voltage as V_{D3}.
GND	(1)	Ground connection. It is very important to place multiple via holes immediately adjacent to the pins. Provides thermal path for heat dissipation and RF grounding

Note: 1. GND Pins are: 2, 4, 5, 7, 10, 12, 13, 15.

TQ9142B Pinout



TQ9142B — Simplified Schematic



General Description

The TQ9142B is a gallium arsenide (GaAs) power FET amplifier. It has three stages of gain and features 1 Watt output power at 60% drain efficiency. It can operate at supply voltages from 4.8 to 6.0 V. The device is optimized for operation at frequencies from 824 to 849 MHz. The input is matched to 50 ohms and a simple output match and bypassing completes the minimal external circuitry required for normal operation. The output match and all gate and drain voltages are accessible, allowing the device to be optimized for V_{DD}, output power and efficiency.

The TQ9142B is packaged in a low-cost SOIC-16 package with thermal tabs. It is optimized for use as the transmit amplifier in analog cellular (AMPS) phones and for Cellular Digital Packet Data (CDPD) wide-area network (WAN) applications. Its high efficiency, high output power and ease of use make the TQ9142B an excellent solution for RF system designers with tight time-to-market and cost requirements.

Gate Biasing

A negative voltage is required to bias the TQ9142B Power Amplifier properly. This is usually generated from the battery voltage with a commercially available charge pump IC, such as the Harris 7660 or one of the Maxim 850 series Negative Supply Generator ICs. A simple resistive voltage divider can be used to produce the gate voltages for each stage, but the most consistent operation of the amplifier will be obtained by using the active bias circuit shown in the Test Circuit Schematic. The following table gives the approximate values of gate voltage for the TQ9142B at 4.8 Volts and 5.8 Volts. The specific values required for optimum performance vary slightly due to fabrication tolerances in FET pinch-off voltage. The active bias circuit overcomes these small variations and provides the extremely repeatable performance and operation needed for high-volume production.

Nominal Gate Bias Voltages

V_{DD}	4.8 V	5.8 V
V_{G1}	-1.3 V	-1.0 V
V_{G2}	-1.3 V	-1.4 V
V_{G3}	-1.8 V	-1.7 V

For a fixed output matching network, output power increases monotonically but gradually as gate voltage becomes more positive. Efficiency tends to rise to a peak, then to decrease with more positive gate voltage. See the P_{OUT} and efficiency vs. V_{G2} plots at each supply voltage.

Quiescent current, the total drain current flowing with no RF drive, also tends to increase with more positive gate voltage, and must be considered when selecting "optimum" gate bias voltages. The bias stabilization circuit used in the Test Circuit schematic does an excellent job of controlling quiescent current with variations in FET pinch-off voltage.

As with all GaAs power FETs, it is imperative to ensure that the gate bias is present before applying the drain voltage. Without the gate control, the drain current will rise to full I_{DSS} (~1.5 A) which is potentially destructive to power FETs which are designed to operate at 20% to 50% of I_{DSS}. This is usually more of a problem in a lab test environment, but it is a good idea to provide safeguards in the circuit design to minimize the risk that V_{DD} is applied for any significant length of time without V_{GG} applied.

Output Match

For maximum output power and efficiency, the output matching circuit for the TQ9142B is implemented off-chip with high-Q components. The use of external matching elements allows for some tradeoff adjustments to be made between supply voltage, output power and efficiency. It also allows some flexibility for optimizing the performance in different frequency ranges near the cellular band.

The desired output match impedance for optimum output power should have the impedance shown in the following table:

Optimum Power Match

V_{DD}	4.8 V	5.8 V
S11	.76∠-179°	.73∠+178°
Impedance	6.77-j.36 Ω	7.74+j.74Ω

Pin Descriptions

Pin Name	Pin #	Description
RF OUT	1,16	Power amplifier output. Critical, but simple, matching circuit required.
V_{G3}	3	Output-stage gate voltage. Requires 51 Ω series resistor near device for stability. Local bypass cap required.
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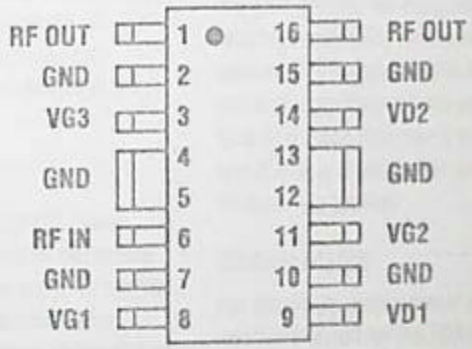
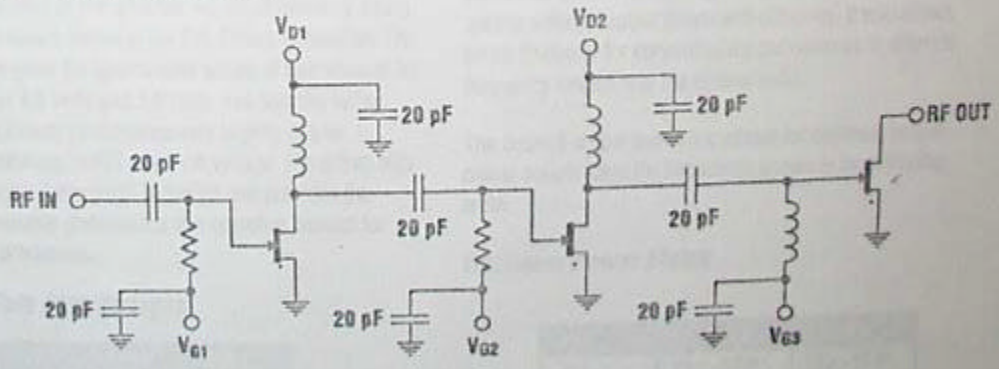
TQ9142B Pinout



TQ9142B — Simplified Schematic



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Gate Biasing

A negative voltage is required to bias the TQ9142B Power Amplifier properly. This is usually generated from the battery voltage with a commercially available charge pump IC, such as the Harris 7660 or one of the Maxim 850 series Negative Supply Generator ICs. A simple resistive voltage divider can be used to produce the gate voltages for each stage, but the most consistent operation of the amplifier will be obtained by using the active bias circuit shown in the Test Circuit Schematic. The following table gives the approximate values of gate voltage for the TQ9142B at 4.8 Volts and 5.8 Volts. The specific values required for optimum performance vary slightly due to fabrication tolerances in FET pinch-off voltage. The active bias circuit overcomes these small variations and provides the extremely repeatable performance and operation needed for high-volume production.

Nominal Gate Bias Voltages

V_{DD}	4.8 V	5.8 V
V_{G1}	-1.3 V	-1.0 V
V_{G2}	-1.3 V	-1.4 V
V_{G3}	-1.8 V	-1.7 V

For a fixed output matching network, output power increases monotonically but gradually as gate voltage becomes more positive. Efficiency tends to rise to a peak, then to decrease with more positive gate voltage. See the P_{OUT} and efficiency vs. V_{G2} plots at each supply voltage.

Quiescent current, the total drain current flowing with no RF drive, also tends to increase with more positive gate voltage, and must be considered when selecting "optimum" gate bias voltages. The bias stabilization circuit used in the Test Circuit schematic does an excellent job of controlling quiescent current with variations in FET pinch-off voltage.

As with all GaAs power FETs, it is imperative to ensure that the gate bias is present before applying the drain voltage. Without the gate control, the drain current will rise to full I_{DSS} (~1.5 A) which is potentially destructive to power FETs which are designed to operate at 20% to 50% of I_{DSS}. This is usually more of a problem in a lab test environment, but it is a good idea to provide safeguards in the circuit design to minimize the risk that V_{DD} is applied for any significant length of time without V_{GG} applied.

Output Match

For maximum output power and efficiency, the output matching circuit for the TQ9142B is implemented off-chip with high-Q components. The use of external matching elements allows for some tradeoff adjustments to be made between supply voltage, output power and efficiency. It also allows some flexibility for optimizing the performance in different frequency ranges near the cellular band.

The desired output match impedance for optimum output power should have the impedance shown in the following table:

Optimum Power Match

V_{DD}	4.8 V	5.8 V
S11	.76∠-179°	.73∠+178°
Impedance	6.77-j.36 Ω	7.74+j 74Ω

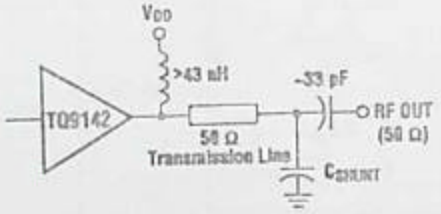
ICs

The basic output network for the TQ9142B, (and for most GaAs FET power amplifiers), consists of a series inductor followed by a shunt capacitor. An RF choke for bringing the output stage supply voltage and a DC blocking capacitor are also needed.

The series inductance can be realized using a series transmission line or a combination of a series transmission line with a lumped element inductor. The transmission line characteristic impedance should be kept at 50 Ω.

The preferred topology for the output match is shown in the following figures for both the transmission line approach and the combination transmission line/lumped inductor approach.

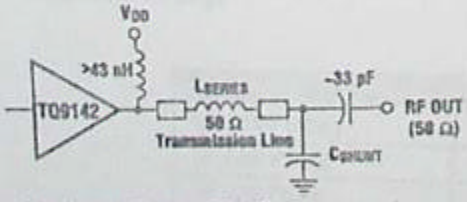
Output Match Topology - Transmission Line



Transmission Line Power Match

V_{DD}	4.8 V	5.8 V
Line Length	338 mils	365 mils
C_{SHUNT}	8.2 pF	6.8 pF

Output Match Topology - Lumped Inductance



Lumped Inductor Power Match

V_{DD}	4.8 V	5.8 V
L_{SERIES}	3.3 nH	3.9 nH
C_{SHUNT}	10 pF	8.2 pF

Please note that the value shown in the table for L_{SERIES} includes the equivalent inductance of any transmission line connecting the power amplifier to the inductor and any transmission line connecting the inductor to the shunt capacitor. Since these lines vary significantly from layout to layout, no attempt has been made here to estimate the approximate value of the physical lumped inductor. The closest standard values of lumped inductors that are lower than the required values are 2.2 nH and 1.8 nH. The connecting transmission lines must be kept fairly short since lumped inductors with values of less than 1.2 nH are not available in most sizes.

Power Control

The best method of power control for the TQ9142B is to vary V_{D2}. It is also possible to vary any of the gate voltages to achieve the same result, but the bias stabilization circuit shown in the Test Schematic works best if VD2 is the control voltage.

Power Down Function

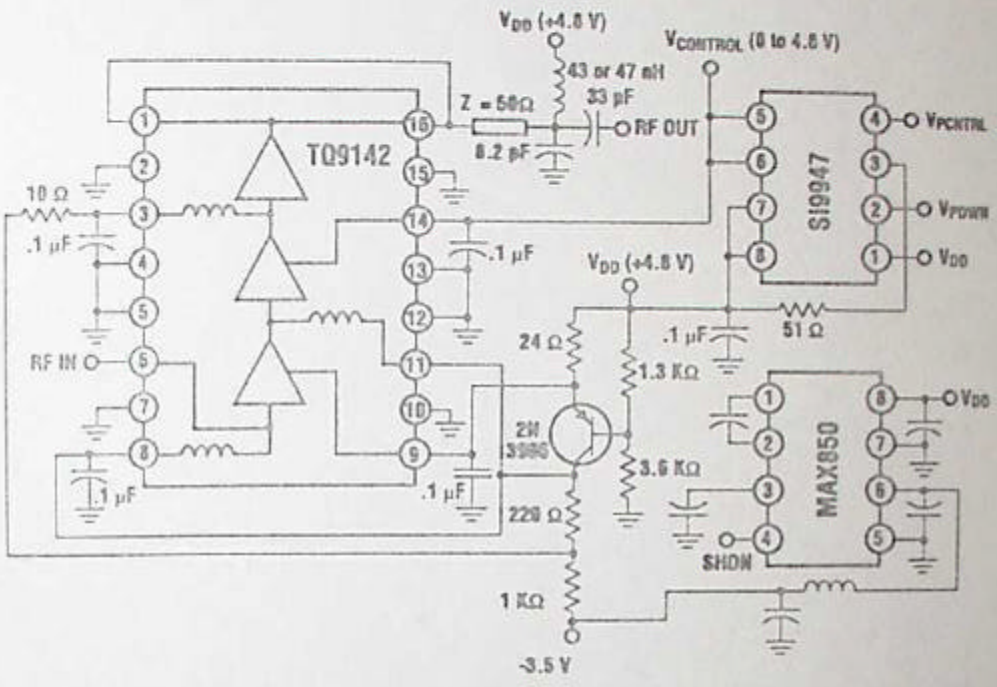
To achieve minimum current leakage in standby mode, a silicon PMOS switching FET (PFET), such as the Siliconix Si9947, can be used in series with the supply voltage. When $V_{STANDBY}$ (active high) is applied to the gate of the PFET, the switch is turned off and only a few microamperes of current will flow. When $V_{STANDBY}$ = 0, the switch is turned on and V_{DD} is applied to the power amplifier. Typically, the switch will drop the supply voltage by 0.1 to 0.2 V.

The turn-on and turn-off times for the TQ9142B using a PFET are 3 µs and 13 µs, respectively.

Single Supply Operation (Negative Voltage Generators)

Depletion-mode GaAs power FETs require a negative gate bias voltage (with respect to the grounded source). Several highly efficient negative supply generator ICs are available, such as the Maxim MAX850. The Typical Application Circuit figure includes the negative supply, the Silicon PFET and the bias circuit to illustrate a complete solution suitable for many cellular telephone designs.

Typical Application Circuit



Absolute Maximum Ratings

Parameter	Min.	Typ.	Max.	Units
DC Power Supply			8.0	V
DC Gate Voltage	-5.0		-0.5	V
RF Input Power			+10	dBm
Storage Temperature	-55		+150	°C
Operating Temperature (case)	-40		+125	°C

ESD-sensitive device - Class 1