MODEL *PCS2000* BDA
Circuit Description

Uplink

The uplink RF circuit consists of three (3) stages of gain. Each gain stage is a monolithic integrated circuit (mmic) mounted to a printed circuit board (PCB). The signal received by the inside antenna is directed to the 1st mmic stage by a frequency diplexer, which separates the uplink frequency (1850-1910 MHz) from the downlink frequency (1930-1995 MHz). This signal is amplified by the mmic stages and directed to an identical diplexer at the output of the 2nd stage. A total of four (4) band-pass Surface Acoustic Wave (SAW) filters are used between active stages to provide adequate isolation of the downlink chain. All stages are biased for linear operation. The overall gain from the inside antenna terminal to the outside antenna terminal is a maximum 40 dB. Each diplexer / filter combination provides 50 dB of rejection between the uplink amplifier chain and the downlink.

Downlink

The downlink circuit is identical in operation to the uplink. The only differences are the downlink frequency (1930-1945 MHz) and signal flow in the opposite direction.

Power Supply

All the mmic amplification stages, in both the uplink and downlink, operate from a single supply voltage of +5 Vdc. A "Wall" power supply and dc-dc converter is used to provide a regulated 5 volts from an input of 110 Vac. All internal dc circuits are filtered and de-coupled from the RF circuits. The overall current at 5 Vdc is less than 1.0 Amp.