MODEL 110 Mini-BDA
Circuit Description

Uplink

The uplink rf circuit consists of two stages of gain. Each gain stage is a monolithic integrated circuit (mmic) mounted to a printed circuit board (PCB). The signal received by the inside antenna is directed to the 1st mmic stage by a frequency diplexer, which separates the uplink frequency (806-821 MHz) from the downlink frequency (851-866MHz). This signal is amplified by both mmic stages and directed to an identical diplexer at the output of the 2nd stage. Both stages are biased for linear operation. The overall gain from the inside antenna terminal to the outside antenna terminal is nominally 40 dB. Each diplexer provides 60 dB of rejection between the uplink amplifier chain and the downlink.

Downlink

The downlink circuit is similar in operation to the uplink, in that it also uses two stages of mmic amplification. The major differences are the downlink frequency (851-866 MHz), the overall gain (30 dB) and signal flow in the opposite direction.

Power Supply

All the mmic amplification stages, in both the uplink and downlink, operate from a single supply voltage of +5 Vdc. A linear regulator is used to provide the 5 volts from an input of 12 Vdc. All internal dc circuits are filtered and de-coupled from the rf circuits. A 115 Vac to 12 Vdc "Wall" supply is provided as part of the unit. The overall current at 12 Vdc is less than 1.0 Amp.