

TADIRAN-Telematics Proprietary

Tulip – US

Technical Description

Proposed for
FCC Type Approval

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Tulip-US Technical Description

1. General.

This document describes TADIRAN TELEMATICS Vehicle Location Unit (VLU). The commercial brand name of this product is: TULIP -US.

The TULIP –US (VLU) is the mobile portion of Location and Messaging system. In this document we use the name VLU for the Tulip-US unit.

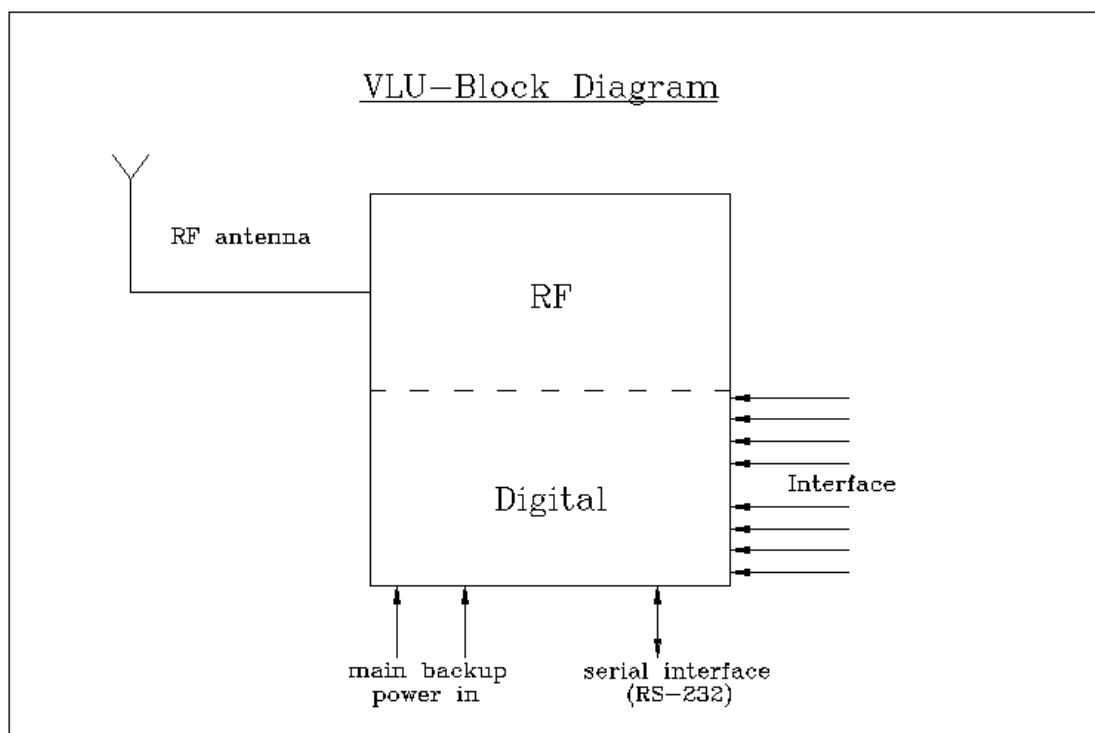
1.1 System Description

The system uses RF signals to provide a mean of locating vehicles equipped with the Location system. The system based on Forward Channel (Paging) transmitted from Pagers to the mobile units and based on Reverse Channel used for Location signal and messaging (from the mobile units to Base-Station).

The VLU is the in-vehicle transmitter / receiver element of the system. The VLU has an Omni-directional antenna to receive and transmit signals. The VLU implements a Paging channel receiver, POCSAG format, FSK modulated at a carrier frequency of 927.778266 MHz to address, program, control the VLU and messages transmission to the VLU. The VLU is ready to receive the proper address from the paging channel and to reply in the reverse channel with location signal (Pseudo-Noise sequence, ~1.5 Mchip Rate) and status response. The reverse channel is phase shaping BPSK modulated signal at 907.997333 MHz in the proper time slot.

2. VLU Description.

The VLU is based on one board with two main parts: Digital portion and RF portion.

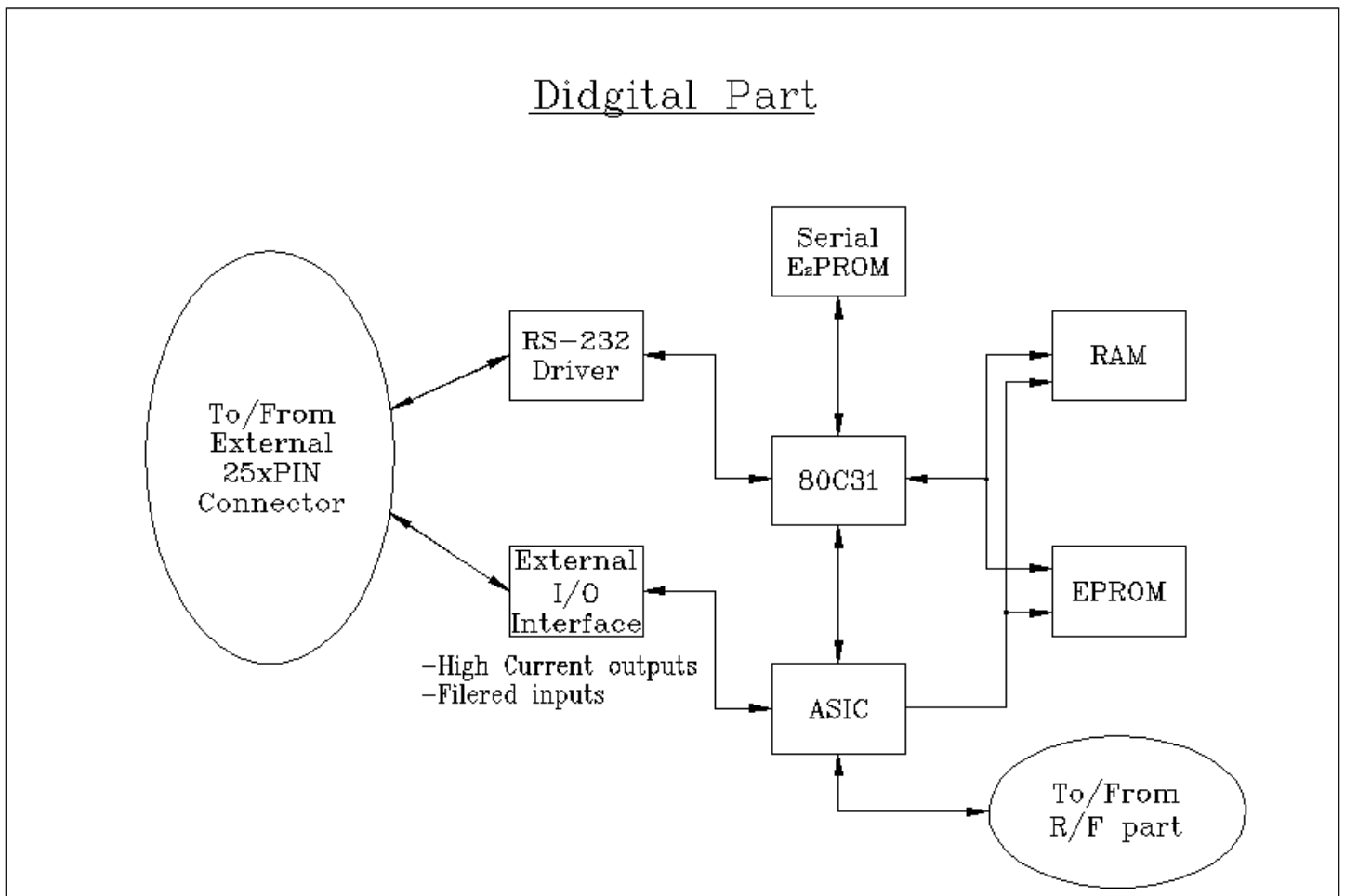


2.1 Digital Part

The digital part of the VLU contains the following functions:

- VLU Controller and peripherals.
- External interfaces
- Custom ASIC for timing and processing.
- Power supply

The block diagram of the digital part described in the following figure.



2.1.1 VLU External Interface

The VLU digital interface consists of:

- Serial wired interface.
- Main battery input and Backup battery input.
- I/O interface with up to 10 I/Os.

2.1.2 Custom digital LSI

The Custom digital LSI contain the following function:

- Decoding the received POCSAG paging data.
- POCSAG batch structure tracking logic.
- Generate the Location PN code sequence.
- Transmit data and timing control.
- RF control.
- Alarm I/O interface.

2.1.3 Micro Controller

The VLU digital control is based on 80C32 μ C. The VLU controller main functions are as follow.

- Program and Parameters in an external FLA84.
- UART link to external device.
- VLU watchdog control.
- VCTCXO control.

2.1.4 Power supply

The VLU power supply meets fully the SAE-J1211 tables 3 and 4.

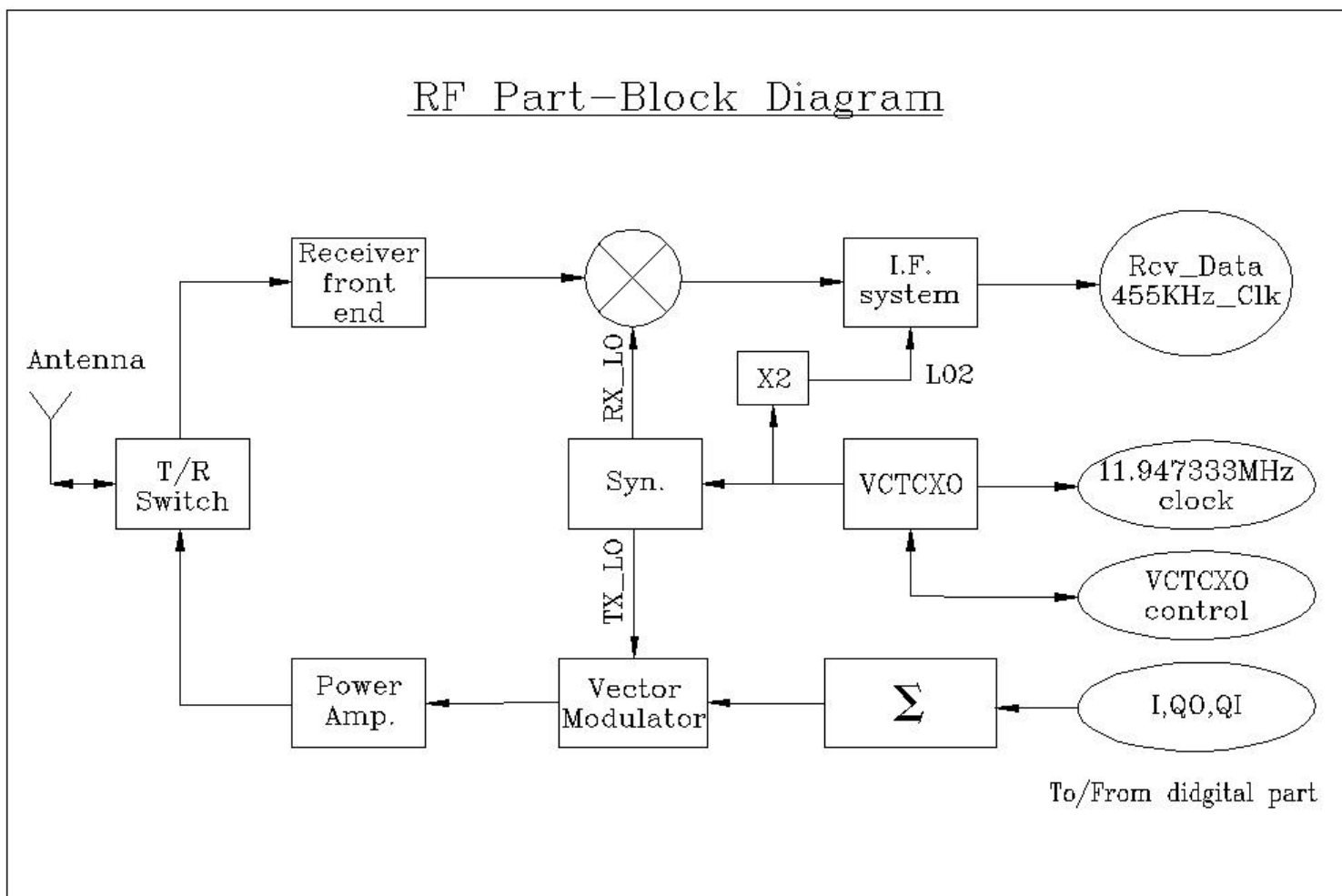
2.2 VLU RF PART

The RF part consist of 3 main functions compatible with location network system. The main functions are:

- FSK Receiver (RF to base-band)
- PSK Transmitter (base band to RF)
- Frequency Generator (LO frequency generator)

The following figure describes the block diagram of the RF part.

The antenna input is connected by T/R switch to the receiver or transmitter according to the CPU control. The received RF signal pass through filter and LNA in the receiver front end and down converted to the IF receiver. The IF receiver demodulates the signal and generates the data signal.



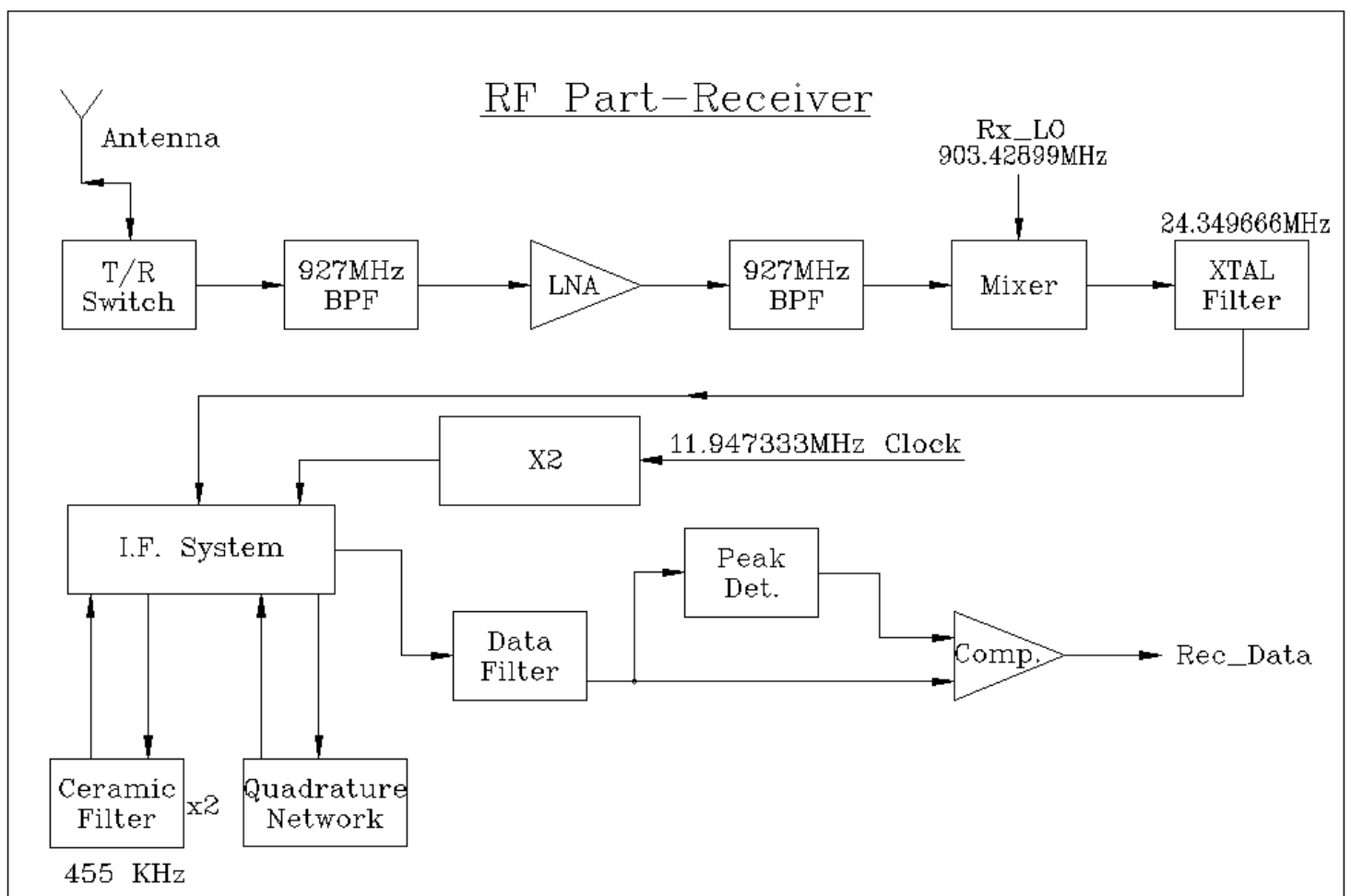
In the transmission branch, the RF part receives base band signal in quadrature mode I,Q of the transmitted signal. The base band signal enters to transversal filter that generates band limited base band signal with the required spectrum. The output of the transversal filter is modulated by vector modulator. The vector modulator output is the RF signal that enters to the power amplifier. The T/R switch controls the connection of the transmitted signal to the antenna. The Local Oscillator for down conversion is the same LO (Local Oscillator) signal that modulate the transmission. The LO is generated from TCXO reference by PLL and multiplier.

2.2.1 VLU Receiver

The VLU receiver is a FSK receiver with the following parameters:

- Center frequency - 927.778266 Mhz.
- Modulation - FSK
- Bit rate - 2400 BPS.
- Frequency deviation - ± 4.5 kHz.

The following figure describes the receiver block diagram. The input signal is filtered and entered to Low Noise Amplifier (LNA). The amplified RF signal pass through band pass filter and down converted to IF level. The LO1 frequency is of 24.349666 MHz.



The IF signal enter to crystal filter (BPF) and entered to standard FM discriminator integrated circuit. The output of the discriminator enters to threshold comperator that generates the data signal.

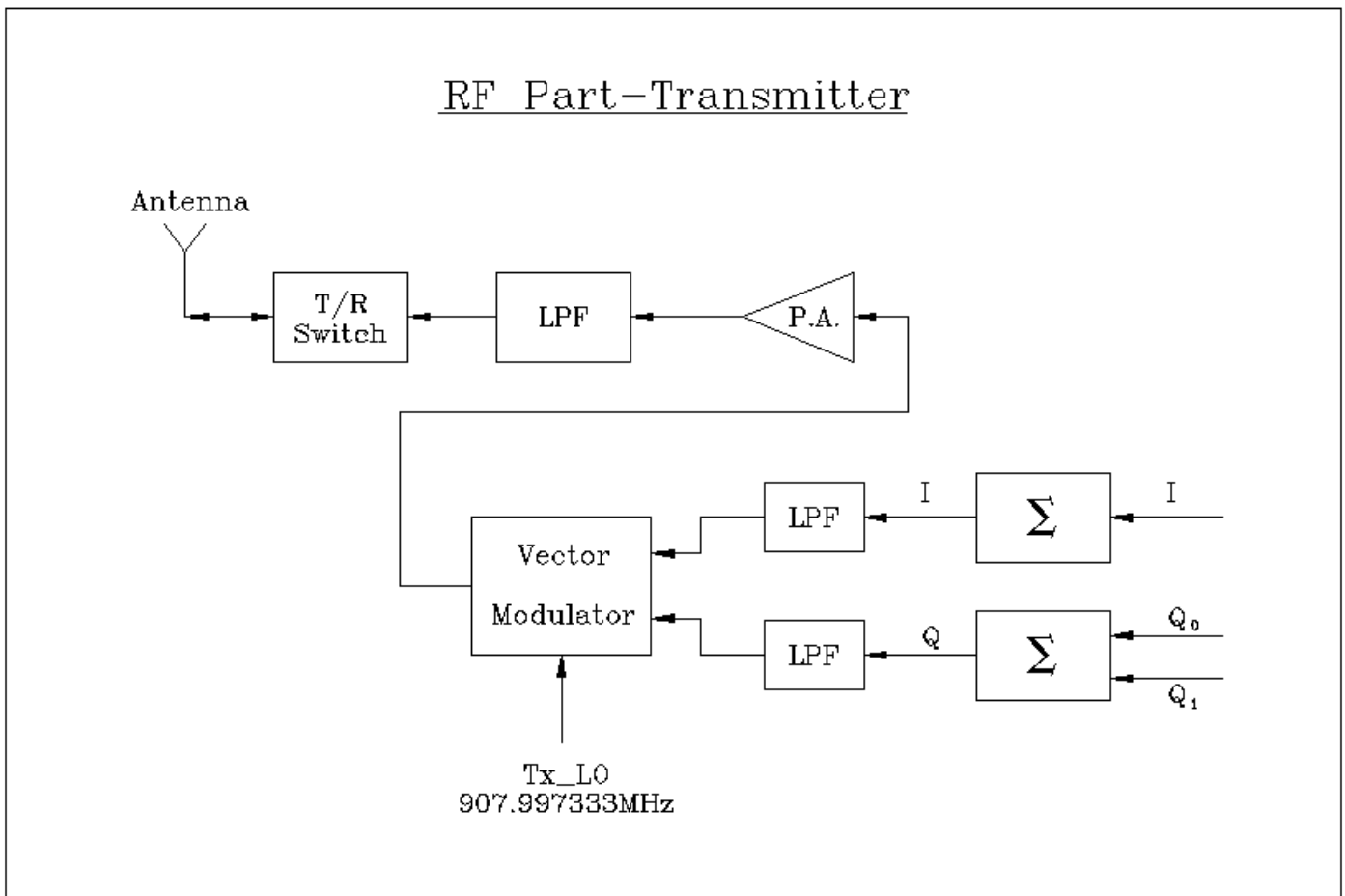
2.2.2 VLU Transmitter

The VLU transmitter parameters:

- Center frequency - 907.997333 MHz.
- Bit rate - 1.49140625 Mbps or ~11.7 Kbps
- Modulation - CPSK with constant envelop for the ~1.5 Mbps bit rate.
BPSK for the 11.7 Kbps bit rate.
- Power output - 5 (Min) to -9 (Max) Watt.

The power is not adjustable

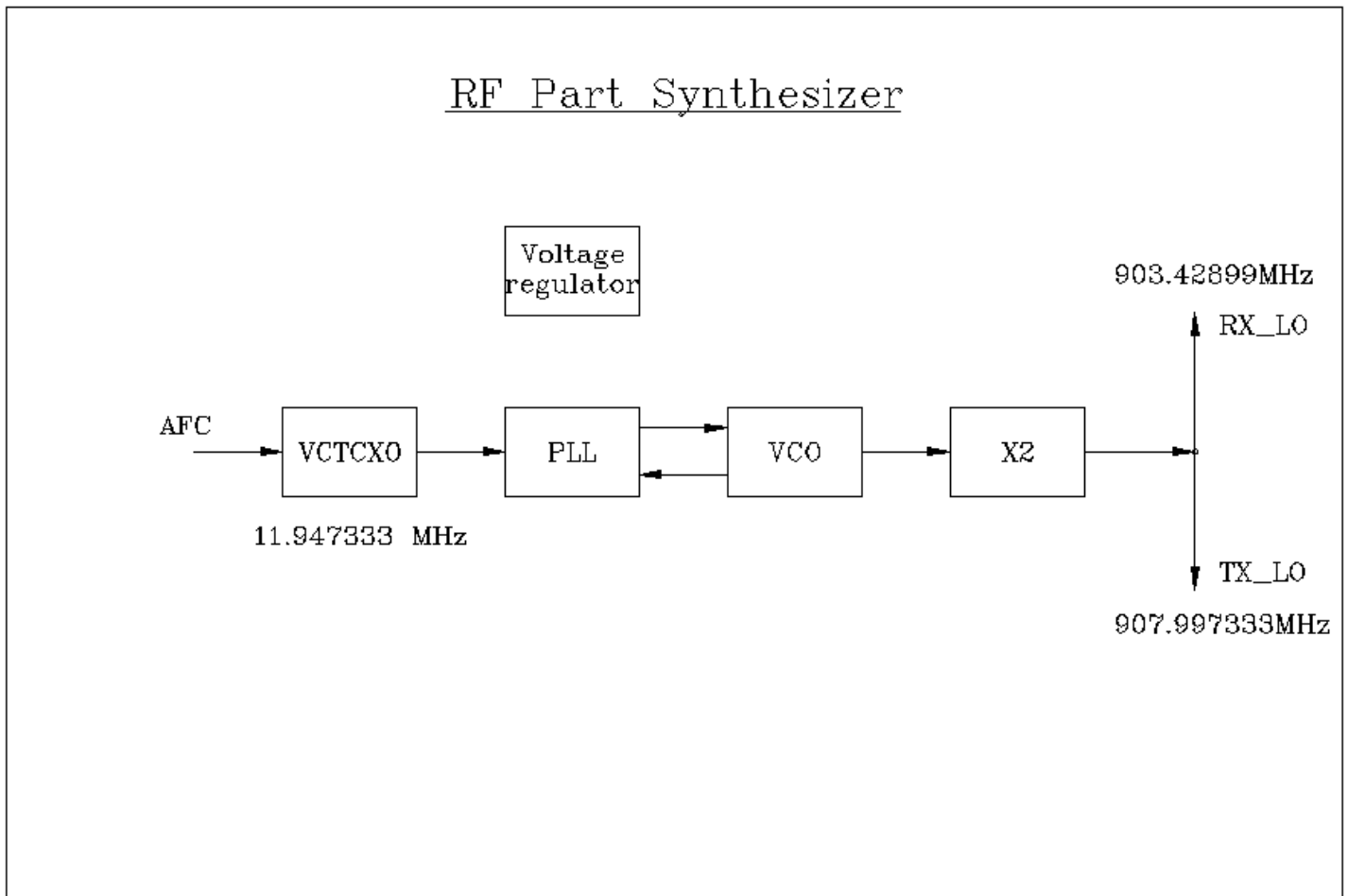
The RF transmitter transmits two types of signals, narrow band of ~11.7 Kbps and wide-band of ~ 1.5 Mcps. The narrow band signal is the messages data signal and the wide-band signal is the PN signal for location processing. The transmitter block diagram is described in the following figure.



The data signal for transmission that is generated in the digital part and pass the first process that generates I,Q signal. To achieve the required spectrum, the IQ signals pass through transversal filter. The transversal filter is implemented inside the ASIC by shift registers outputs that are combining through resistors. The transversal filter output signals pass through LPF at the input of the vector modulator for receiving the final shaping. The shaped IQ signal is modulated by vector modulator (IQ quadrature modulator). The modulator output is amplified to the required output power and pass through LPF and T/R switch to the antenna.

2.2.3 VLU “Synthesizer”

The LO frequencies for transmission and down conversion are generated by the “synthesizer” block. The RF frequency is based on PLL and multiplier that multiplies the VCTCXO frequency to receive the LO frequency. The synthesizer is based on TCXO with these convert accuracy of at least ± 2.5 ppm at power down mode.



The clock source based on a standard VCTCXO controlled by the CPU. The compensation value is calculated and it is using to control the VCTCXO.
The multiplier output is filtered by BPF to achieve the requirements of the LO.