General Description.

The component is a low power, high sensitivity ASK/OOK Superheterodyne receiver with high selectivity designed as a Single Inline Package (SIP) for use in conjunction with a host CPU module in low bit rate wireless communication applications. Two end items exist operating at different frequencies to cover applications in Europe under ETSI –ETS 300-220 and the United States under FCC Part 15 and Canada under DOC RSS. Radio Type approvals (RTA) are also available in other countries.

The SIP features a RF integrated circuit with crystal based PLL local oscillator, a narrow SAW front end filter, a self duty cycle circuit for reduced average current draw and a data present filter which keeps the data output quiet when no RF signal is present allowing the host CPU to sleep for further current savings.