System technical description : (Handheld Unit)

1.In Handheld, HT48CU80 is main controller,any message transfer by RF between Handheld and Dongle.

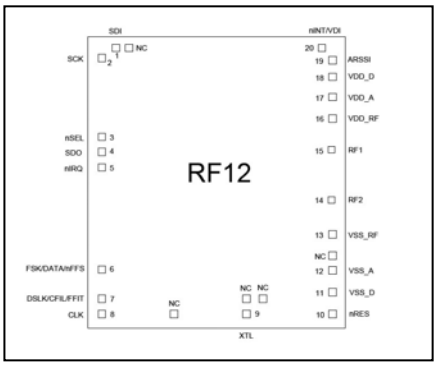
- RF (RF IC: RF12) is a low power, multi-channel FSK transceiver designed for use in applications requiring FCC conformance for unlicensed use in the 906/909/912/915 MHz。The chip is a complete analog RF and base band transceiver including a multi-band PLL synthesizer with PA, LNA, I/Q down converter mixers, baseband filters and amplifiers, and an I/Q demodulator. All required RF functions are integrated. Only an external crystal (10MHz) and bypass filtering are needed for operation.
- The HT48CU80 are 8-bit high performance , RISC architecture microcontroller devices specifically designed for multiple I/O control product applications.The advantages of low power consumption ,I/O flexibil-ity, timerfunctions, oscillator options , HALT and wake-up functions, watchdog timer, buzzer driver
- LCD modul: The ST7565P is a single-chip dot matrix LCD driver that can be connected directly to a microprocessor bus. 8-bit parallel or serial display data sent from the microprocessor is stored in the internal display data RAM and the chip generates a LCD drive signal independent of the microprocessor. Because the chips in the ST7565P contain 65x132 bits of display data RAM and there is a

1-to-1 correspondence between the LCD panel pixels and the internal RAM bits, these chips enable displays with a high degree of freedom. The ST7565P chips contain 65 common output circuits and 132 segment output circuits, so that a single chip can drive a 65x132 dot display (capable of displaying 8 columnsx4 rows of a 16x16 dot kanji font).

RF12 Universal ISM Band FSK Transceiver

DESCRIPTION

RF12



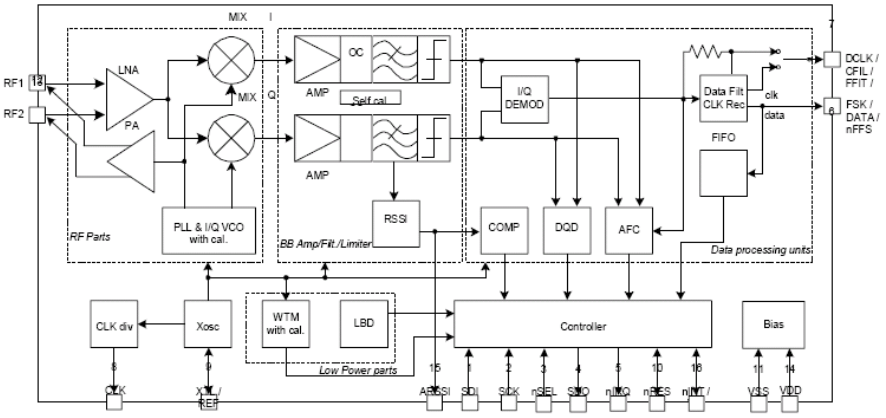
ETEK's RF12 is a single chip, low power, multi-channel FSK transceiver designed for use in applications requiring FCC or ETSI conformance for unlicensed use in the 315, 433, 868 and 915 MHz bands. The RF12 transceiver is a part of ETEK's product line, which produces a flexible, low cost, and highly integrated solution that does not require production alignments. The chip is a complete analog RF and baseband transceiver including a multi-band PLL synthesizer with PA, LNA, I/Q down converter mixers, baseband filters and amplifiers, and an I/Q demodulator. All required RF functions are integrated. Only an external crystal and bypass filtering are needed for operation.

The RF12 features a completely integrated PLL for easy RF design, and its rapid settling time allows for fast frequency-hopping, bypassing multipath fading and interference to achieve robust wireless links. The PLL's high resolution allows the usage of multiple channels in any of the bands. The receiver baseband bandwidth (BW) is programmable to accommodate various deviation, data rate and crystal tolerance requirements. The transceiver employs the Zero-IF approach with I/Q demodulation. Consequently, no external components (except crystal and decoupling) are needed in most applications.

The RF12 dramatically reduces the load on the microcontroller with the integrated digital data processing features: data filtering, clock recovery, data pattern recognition, integrated FIFO and TX data register. The automatic frequency control (AFC) feature allows the use of a low accuracy (low cost) crystal. To minimize the system cost, the RF12 can provide a clock signal for the microcontroller, avoiding the need for two crystals.

For low power applications, the RF12 supports low duty cycle operation based on the internal wake-up timer.

FUNCTIONAL BLOCK DIAGRAM



PRELIMINARY

FEATURES

- Fully integrated (low BOM, easy design-in)
- No alignment required in production
- Fast-settling, programmable, high-resolution PLL synthesizer
- Fast frequency-hopping capability
- High bit rate (up to 115.2 kbps in digital mode and 256 kbps in analog mode)
- Direct differential antenna input/output
- Integrated power amplifier
- Programmable TX frequency deviation (15 to 240 KHz)
- Programmable RX baseband bandwidth (67 to 400 kHz)
- Analog and digital RSSI outputs
- Automatic frequency control (AFC)
- Data quality detection (DQD)
- Internal data filtering and clock recovery
- RX synchron pattern recognition
- SPI compatible serial control interface
- Clock and reset signals for microcontroller
- 16 bit RX Data FIFO
- Two 8 bit TX data registers
- Low power duty cycle mode
- Standard 10 MHz crystal reference
- Wake-up timer
- Low power consumption
- Low standby current (0.3 μA)

TYPICAL APPLICATIONS

- Remote control
- Home security and alarm
- Wireless keyboard/mouse and other PC peripherals
- Toy controls
- Remote keyless entry
- Tire pressure monitoring
- Telemetry
- Personal/patient data logging
- Remote automatic meter reading

DETAILED FEATURE-LEVEL DESCRIPTION

The RF12 FSK transceiver is designed to cover the unlicensed frequency bands at 315, 433, 868 and 915 MHz. The devices facilitate compliance with FCC and ETSI requirements.

The receiver block employs the Zero-IF approach with I/Q demodulation, allowing the use of a minimal number of external components in a typical application. The RF12 incorporates a fully integrated multi-band PLL synthesizer, PA with antenna tuning, an LNA with switchable gain, I/Q down converter mixers, baseband filters and amplifiers, and an I/Q demodulator followed by a data filter.

PLL

The programmable PLL synthesizer determines the operating frequency, while preserving accuracy based on the on-chip crystal-controlled reference oscillator. The PLL's high resolution allows the usage of multiple channels in any of the bands.

The RF VCO in the PLL performs automatic calibration, which requires only a few microseconds. Calibration always occurs when the synthesizer starts. If temperature or supply voltage changes significantly, VCO recalibration can be invoked easily. Recalibration can be initiated at any time by switching the synthesizer off and back on again.

RF Power Amplifier (PA)

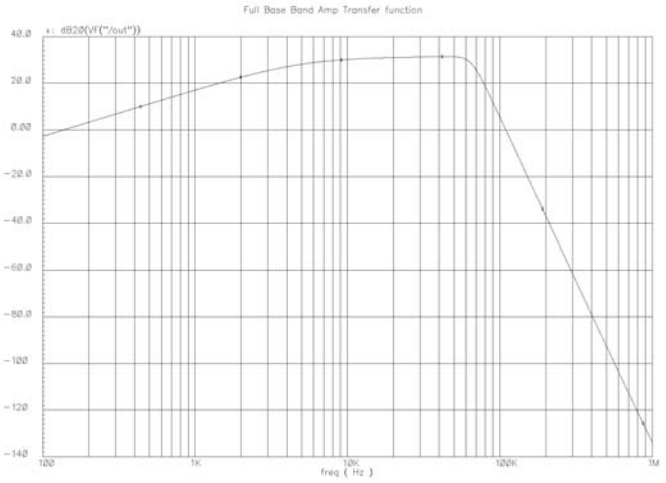
The power amplifier has an open-collector differential output and can directly drive a loop antenna with a programmable output power level. An automatic antenna tuning circuit is built in to avoid costly trimming procedures and the so-called "hand effect."

LNA

The LNA has 250 Ohm input impedance, which functions well with the proposed antennas If the RF input of the chip is connected to 50 Ohm devices, an external matching circuit is required to provide the correct matching and to minimize the noise figure of the receiver.

The LNA gain can be selected (0, –6, –14, –20 dB relative to the highest gain) according to RF signal strength. It can be useful in an environment with strong interferers.

Baseband Filters



The receiver bandwidth is selectable by programming the bandwidth (BW) of the baseband filters. This allows setting up the receiver according to the characteristics of the signal to be received.

An appropriate bandwidth can be chosen to accommodate various FSK deviation, data rate and crystal tolerance requirements. The filter structure is 7th order Butterworth low-pass with 40 dB suppression at 2*BW frequency. Offset cancellation is done by using a high-pass filter with a cut-off frequency below 7 kHz.

Data Filtering and Clock Recovery

Output data filtering can be completed by an external capacitor or by using digital filtering according to the final application.

Analog operation: The filter is an RC type low-pass filter followed by a Schmitt-trigger (St). The resistor (10 kOhm) and the St are integrated on the chip. An (external) capacitor can be chosen according to the actual bit rate. In this mode, the receiver can handle up to 256 kbps data rate. The FIFO can not be used in this mode and clock is not provided for the demodulated data.

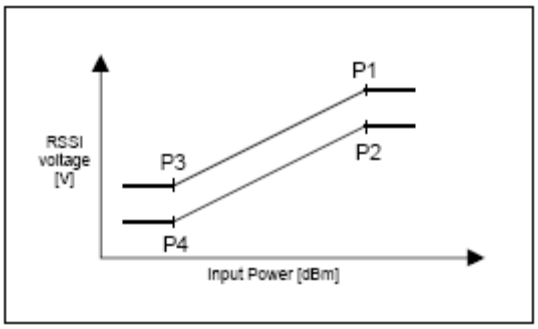
Digital operation: A digital filter is used with a clock frequency at 29 times the bit rate. In this mode there is a clock recovery circuit (CR), which can provide synchronized clock to the data. Using this clock the received data can fill a FIFO. The CR has three operation modes: fast, slow, and automatic. In slow mode, its noise immunity is very high, but it has slower settling time and requires more accurate data timing than in fast mode. In automatic mode the CR automatically changes between fast and slow mode. The CR starts in fast mode, then after locking it automatically switches to slow mode (Only the digital data filter and the clock recovery use the bit rate clock. For analog operation, there is no need for setting the correct bit rate.)

Data Validity Blocks

RSSI

A digital RSSI output is provided to monitor the input signal level. It goes high if the received signal strength exceeds a given preprogrammed level. An analog RSSI signal is also available. The RSSI settling time depends on the external filter capacitor. Pin 19 is used as analog RSSI output. The digital RSSI can be can be monitored by reading the status register.

Analog RSSI Voltage vs. RF Input Power



P1	-65 dBm	1300 mV
P2	-65 dBm	1000 mV
P3	-100 dBm	600 mV
P4	-100 dBm	300 mV

DQD

The Data Quality Detector is based on counting the spikes on the unfiltered received data. For correct operation, the “DQD threshold” parameter must be filled in by using the Data Filter Command.

AFC

By using an integrated Automatic Frequency Control (AFC) feature, the receiver can minimize the TX/RX offset in discrete steps, allowing the use of:

1, Inexpensive, low accuracy crystals 2, Narrower receiver bandwidth (i.e. increased sensitivity) 3, Higher data rate

Crystal Oscillator

The RF12 has a single-pin crystal oscillator circuit, which provides a 10 MHz reference signal for the PLL. To reduce external parts and simplify design, the crystal load capacitor is internal and programmable. Guidelines for selecting the appropriate crystal can be found later in this datasheet.

The transceiver can supply the clock signal for the microcontroller; so accurate timing is possible without the need for a second crystal.

When the microcontroller turns the crystal oscillator off by clearing the appropriate bit using the Configuration Setting Command, the chip provides a fixed number (196) of further clock pulses (“clock tail”) for the microcontroller to let it go to idle or sleep mode.

Low Battery Voltage Detector

The low battery detector circuit monitors the supply voltage and generates an interrupt if it falls below a programmable threshold level. The detector circuit has 50 mV hysteresis.

Wake-Up Timer

The wake-up timer has very low current consumption (1.5 uA typical) and can be programmed from 1 ms to several days with an accuracy of ±5%.

It calibrates itself to the crystal oscillator at every startup, and then at every 30 seconds. When the crystal oscillator is switched off, the calibration circuit switches it back on only long enough for a quick calibration (a few milliseconds) to facilitate accurate wake-up timing.

Event Handling

In order to minimize current consumption, the transceiver supports different power saving modes. Active mode can be initiated by several wake-up events (negative logical pulse on nINT input, wake-up timer timeout, low supply voltage detection, on-chip FIFO filled up or receiving a request through the serial interface).

If any wake-up event occurs, the wake-up logic generates an interrupt signal, which can be used to wake up the microcontroller, effectively reducing the period the microcontroller has to be active. The source of the interrupt can be read out from the transceiver by the microcontroller through the SDO pin.

Interface and Controller

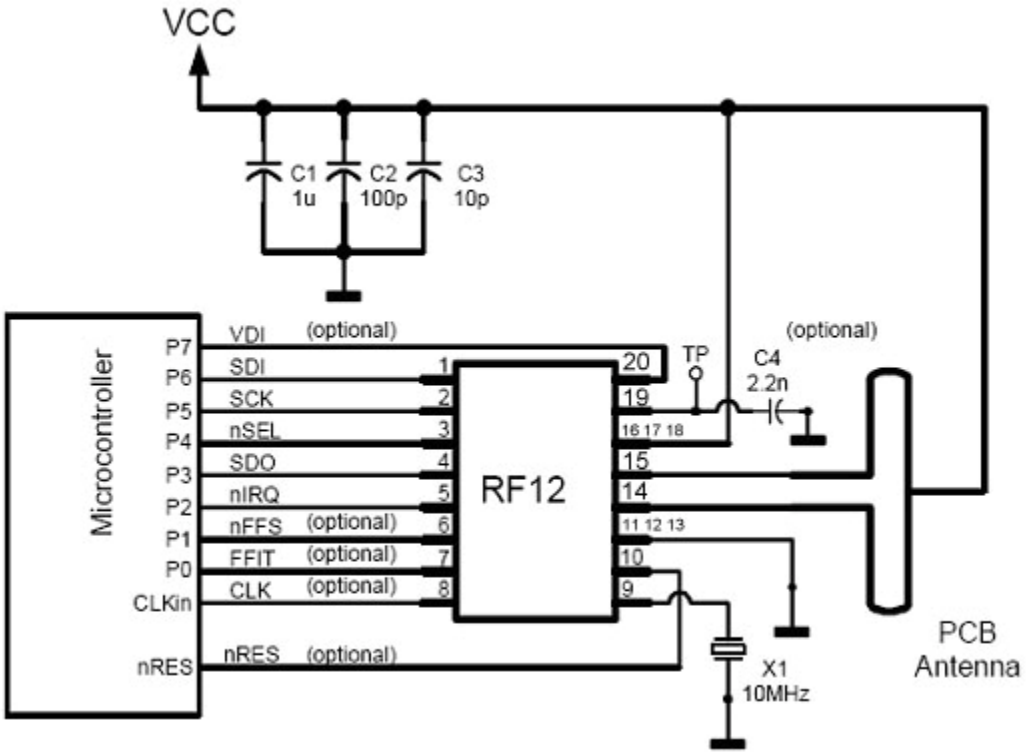
An SPI compatible serial interface lets the user select the frequency band, center frequency of the synthesizer, and the bandwidth of the baseband signal path. Division ratio for the microcontroller clock, wake-up timer period, and low supply voltage detector threshold are also programmable. Any of these auxiliary functions can be disabled when not needed. All parameters are set to default after power-on; the programmed values are retained during sleep mode. The interface supports the read-out of a status register, providing detailed information about the status of the transceiver and the received data.

The transmitter block is equipped with an 8 bit wide TX data register. It is possible to write 8 bits into the register in burst mode and the internal bit rate generator transmits the bits out with the predefined rate.

It is also possible to store the received data bits into a FIFO register and read them out in a buffered mode.

Typical Application

Typical application with FIFO usage



	Pin 6	Pin 7
Transmit mode el=0 in Configuration Setting Command	TX Data input	-
Transmit mode el=1 in Configuration Setting Command	Connect to logic high	-
Receive mode ef=0 in Configuration Setting Command	RX Data output	RX Data clock output
Receive mode ef=1 in Configuration Setting Command	nFFS input	FFIT output

GENERAL DEVICE SPECIFICATION

All voltages are referenced to V_{ss}, the potential on the ground reference pin VSS.

Absolute Maximum Ratings (non-operating)

Symbol	Parameter	Min	Max	Units
V_{dd}	Positive supply voltage	-0.5	6	V
V_{in}	Voltage on any pin (except RF1 and RF2)	-0.5	V_{dd}+0.5	V
V_{oc}	Voltage on open collector outputs (RF1, RF2)	-0.5	V_{dd}+1.5 (Note 1)	V
I_{in}	Input current into any pin except VDD and VSS	-25	25	mA
ESD	Electrostatic discharge with human body model		1000	V
T_{st}	Storage temperature	-55	125	oC
T_{ld}	Lead temperature (soldering, max 10 s)		260	oC

Recommended Operating Range

Symbol	Parameter	Min	Max	Units
V_{dd}	Positive supply voltage	2.2	5.4	V
V_{ocDC}	DC voltage on open collector outputs (RF1, RF2)		V_{dd}+1.5 (Note 2)	V
V_{ocAC}	AC peak voltage on open collector outputs (RF1, RF2)	V_{dd}-1.5 (Note 1)	V_{dd}+1.5	V
T_{op}	Ambient operating temperature	-40	85	^{o}C

Note 1: At maximum, V_{dd} +1.5 V cannot be higher than 7 V. At minimum, V_{dd} -1.5 V cannot be lower than 1.2 V.

Note 2: At maximum, V_{dd} +1.5 V cannot be higher than 5.5 V.

ELECTRICAL SPECIFICATION

(Min/max values are valid over the whole recommended operating range. Typical conditions: T_{op} = 27 °C; V_{dd} = V_{oc} = 2.7 V)

DC Characteristics

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
$I_{dd\_TX\_0}$	Supply current (TX mode, Pout = 0 dBm)	315/433 MHz bands 868 MHz band 915 MHz band		13 16 17	14 18 19	mA
$I_{dd\_TX\_PMAX}$	Supply current (TX mode, Pout = Pmax)	315/433 MHz bands 868 MHz band 915 MHz band		21 23 24	22 25 26	mA
I_{dd_RX}	Supply current (RX mode)	315/433 MHz bands 868 MHz band 915 MHz band		11 12 13	13 14 15	mA
I_{pd}	Standby current (Sleep mode)	All blocks disabled		0.3		µA
I_{lb}	Low battery voltage detector current consumption			0.5		µA
I_{wt}	Wake-up timer current consumption			1.5		µA
I_x	Idle current	Crystal oscillator and baseband parts are on		3	3.5	mA
V_{lb}	Low battery detect threshold	Programmable in 0.1 V steps	2.2		5.3	V
V_{lba}	Low battery detection accuracy			±75		mV
V_{il}	Digital input low level voltage				0.3*V_{dd}	V
V_{ih}	Digital input high level voltage		0.7*V_{dd}			V
I_{il}	Digital input current	V_{il} = 0 V	-1		1	µA
I_{ih}	Digital input current	V_{ih} = V_{dd}, V_{dd} = 5.4 V	-1		1	µA
V_{ol}	Digital output low level	I_{ol} = 2 mA			0.4	V
V_{oh}	Digital output high level	I_{oh} = -2 mA	V_{dd}-0.4			V

AC Characteristics (PLL parameters)

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
f_{ref}	PLL reference frequency	(Note 1)	8	10	12	MHz
f_o	Receiver LO / Transmitter carrier frequency	315MHz band,2.5kHz resolution 433MHz band,2.5kHz resolution 868MHz band,5.0kHz resolution 915MHz band,7.5kHz resolution	310.24 430.24 860.48 900.72		319.75 439.75 879.51 929.27	MHz
t_{lock}	PLL lock time	Frequency error < 1kHz after 10MHz step		20		us
t_{st}, P	PLL startup time	With a running crystal oscillator			250	us

AC Characteristics (Receiver)

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
BW	Receiver bandwidth	mode 0 mode 1 mode 2 mode 3 mode 4 mode 5	60 120 180 240 300 360	67 134 200 270 350 400	75 150 225 300 375 450	kHz
BR	FSK bit rate	With internal digital filters	0.6		115.2	kbps
BRA	FSK bit rate	With analog filter			256	kbps
Pmin	Receiver Sensitivity	BER 10^{-3}, BW=67kHz, BR=1.2kbps (Note 2)		-109	-100	dBm
AFC_{range}	AFC locking range	df_{FSK}: FSK deviation in the received signal		$0.8*df_{FSK}$		
$IIP3_{inh}$	Input IP3	In band interferers in high bands(868, 915 MHz)		-21		dBm
$IIP3_{outh}$	Input IP3	Out of band interferers l f-f_o l > 4 MHz		-18		dBm
$IIP3_{inl}$	IIP3 (LNA –6 dB gain)	In band interferers in low bands (315, 433 MHz)		-15		dBm
$IIP3_{outl}$	IIP3 (LNA –6 dB gain)	Out of band interferers l f-f_o l > 4 MHz		-12		dBm
P_{max}	Maximum input power	LNA: high gain	0			dBm
C_{in}	RF input capacitance			1		pF
RS_a	RSSI accuracy			+/-5		dB
RS_r	RSSI range			46		dB
C_{ARSSI}	Filter capacitor for ARSSI		1			nF
RS_{step}	RSSI programmable level steps			6		dB
RS_{resp}	DRSSI response time	Until the RSSI signal goes high after the input signal exceeds the preprogrammed limit CARRSI = 5 nF		500		us

AC Characteristics (Transmitter)

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
I_{OUT}	Open collector output DC current	Programmable	0.5		6	mA
P_{max}	Available output power with optimal antenna impedance (Note 3, 4)	In low bands In high bands		8 4		dBm
P_{out}	Typical output power	Selectable in 3 dB steps (Note 5)	P_{max}-21		P_{max}	dBm
P_{sp}	Spurious emission	At max power with loop antenna (Note 6)			-50	dBc
C_o	Output capacitance (set by the automatic antenna tuning circuit)	In low bands In high bands	2 2.1	2.6 2.7	3.2 3.3	pF
Q_o	Quality factor of the output capacitance	In low bands In high bands	13 8	15 10	17 12	
L_{out}	Output phase noise	100 kHz from carrier 1 MHz from carrier		-75 -85		dBc/Hz
BR	FSK bit rate				256	kbps
df_{fsk}	FSK frequency deviation	Programmable in 15 kHz steps	15		240	kHz

AC Characteristics (Turn-on/Turnaround timings)

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
tsx	Crystal oscillator startup time	Crystal ESR < 100			5	ms
$T_{tx\_rx\_XTAL\_ON}$	Transmitter - Receiver turnover time	Synthesizer off, crystal oscillator on during TX/RX change with 10 MHz step		450		us
$T_{rx\_tx\_XTAL\_ON}$	Receiver -Transmitter turnover time	Synthesizer off, crystal oscillator on during RX/TX change with 10 MHz step		350		us
$T_{tx\_rx\_SYNT\_ON}$	Transmitter - Receiver turnover time	Synthesizer and crystal oscillator on during TX/RX change with 10 MHz step		425		us
$T_{rx\_tx\_SYNT\_ON}$	Receiver -Transmitter turnover time	Synthesizer and crystal oscillator on during RX/TX change with 10 MHz step		300		us

AC Characteristics (Others)

Symbol	Parameter	Conditions/Notes	Min	Typ	Max	Units
C_{xl}	Crystal load capacitance, see crystal selection guide	Programmable in 0.5 pF steps, tolerance +/- 10%	8.5		16	pF
t_{POR}	Internal POR timeout	After V_{dd} has reached 90% of final value (Note 7)			100	ms
t_{PBt}	Wake-up timer clock period	Calibrated every 30 seconds	0.95		1.05	ms
C_{in}, D	Digital input capacitance				2	pF
t_r , f	Digital output rise/fall time	15 pF pure capacitive load			10	ns

Note 1: Not using a 10 MHz crystal is allowed but not recommended because all crystal referred timing and frequency parameters will change accordingly.

Note 2: See the BER diagrams in the measurement results section for detailed information (Not available at this time).

Note 3: See matching circuit parameters and antenna design guide for information.

Note 4: Optimal antenna admittance/impedance:

RF12	Yantenna [S]	Zantenna [Ohm]	Lantenna [nH]
315 MHz	1.5E-3 -j5.14E-3	52 + j179	98.00
433 MHz	1.4E-3 -j7.1E-3	27 + j136	52.00
868 MHz	2E-3 -j1.5E-2	8.7 + j66	12.50
915 MHz	2.2E-3 -j1.55E-2	9 + j63	11.20

Note 5: Adjustable in 8 steps.

Note 6: With selective resonant antennas

Note 7: During this period, commands are not accepted by the chip.

CONTROL INTERFACE

Commands to the transmitter are sent serially. Data bits on pin SDI are shifted into the device upon the rising edge of the clock on pin SCK whenever the chip select pin nSEL is low. When the nSEL signal is high, it initializes the serial interface. All commands consist of a command code, followed by a varying number of parameter or data bits. All data are sent MSB first (e.g. bit 15 for a 16-bit command). Bits having no influence (don't care) are indicated with X. The Power On Reset (POR) circuit sets default values in all control and command registers.

The receiver will generate an interrupt request (IT) for the microcontroller - by pulling the nIRQ pin low - on the following events:

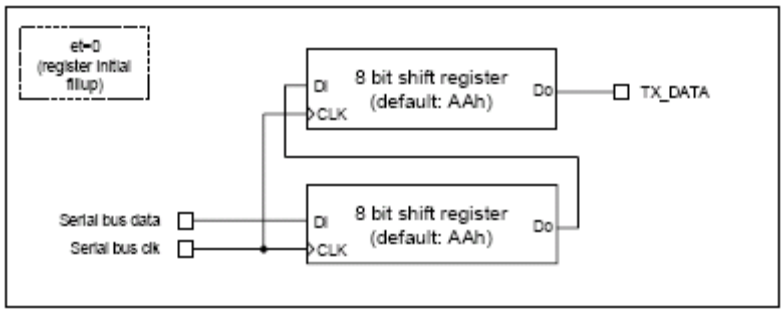
- The TX register is ready to receive the next byte (RGIT)
- The FIFO has received the preprogrammed amount of bits (FFIT)
- Power-on reset (POR)
- FIFO overflow (FFOV) / TX register underrun (RGUR)
- Wake-up timer timeout (WKUP)
- Negative pulse on the interrupt input pin nINT (EXT)
- Supply voltage below the preprogrammed value is detected (LBD)

FFIT and FFOV are applicable when the FIFO is enabled. RGIT and RGUR are applicable only when the TX register is enabled. To identify the source of the IT, the status bits should be read out.

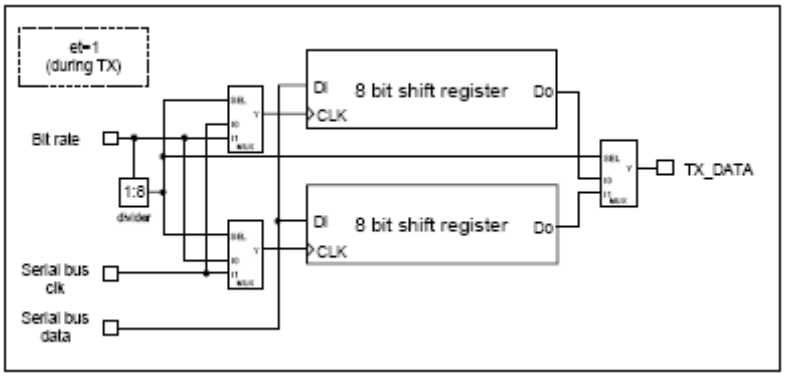
TX REGISTER BUFFERED DATA TRANSMISSION

In this operating mode (enabled by bit el, the Configuration Control Command) the TX data is clocked into one of the two 8-bit data registers. The transmitter starts to send out the data from the first register (with the given bit rate) when bit et is set with the Power Management Command. The initial value of the data registers (AAh) can be used to generate preamble. During this mode, the SDO pin can be monitored to check whether the register is ready (SDO is high) to receive the next byte from the microcontroller.

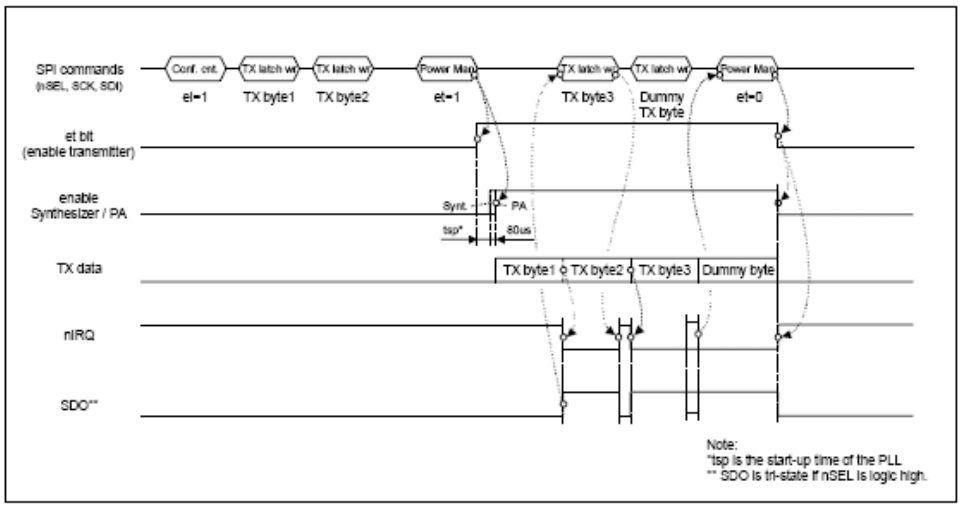
TX register simplified block diagram (before transmit)



TX register simplified block diagram (during transmit)



Typical TX register usage



Note: The content of the data registers are initialized by clearing bit et.

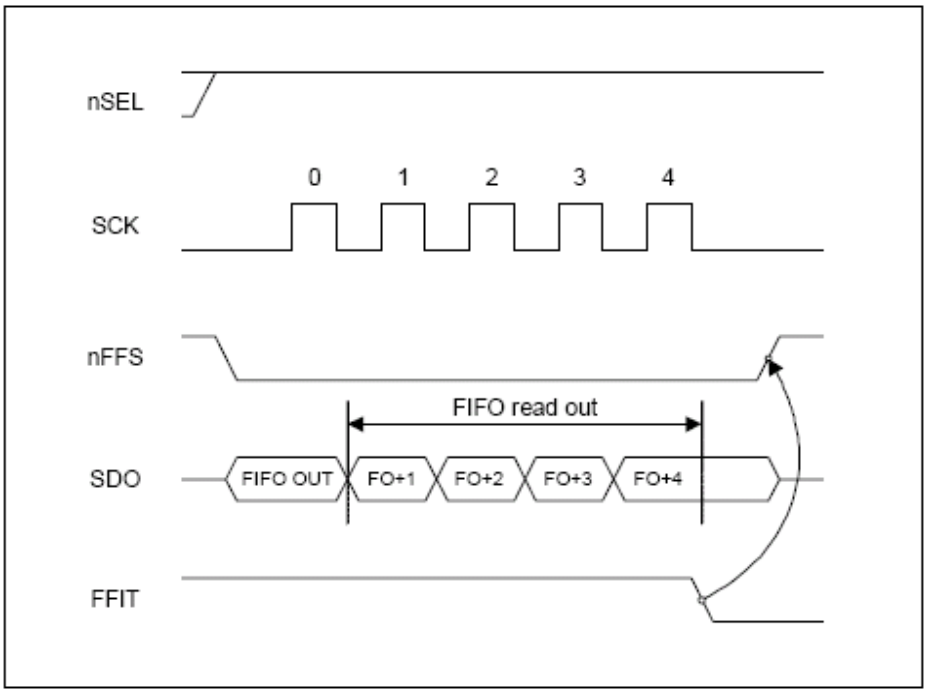
RX FIFO BUFFERED DATA READ

In this operating mode, incoming data are clocked into a 16 bit FIFO buffer. The receiver starts to fill up the FIFO when the Valid Data Indicator (VDI) bit and the synchron pattern recognition circuit indicates potentially real incoming data. This prevents the FIFO from being filled with noise and overloading the external microcontroller.

Polling Mode:
The nFFS signal selects the buffer directly and its content can be clocked out through pin SDO by SCK. Set the FIFO IT level to 1. In this case, as long as FFIT indicates received bits in the FIFO, the controller may continue to take the bits away. When FFIT goes low, no more bits need to be taken. An SPI read command is also available.

Interrupt Controlled Mode:
The user can define the FIFO level (the number of received bits) which will generate the nFFIT when exceeded. The status bits report the changed FIFO status in this case.

FIFO Read Example with FFIT Polling



During FIFO access f_{SCK} cannot be higher than f_{ref} /4, where f_{ref} is the crystal oscillator frequency.

CRYSTAL SELECTION GUIDELINES

The crystal oscillator of the RF12 requires a 10 MHz parallel mode crystal. The circuit contains an integrated load capacitor in order to minimize the external component count. The internal load capacitance value is programmable from 8.5 pF to 16 pF in 0.5 pF steps. With appropriate PCB layout, the total load capacitance value can be 10 pF to 20 pF so a variety of crystal types can be used.

When the total load capacitance is not more than 20 pF and a worst case 7 pF shunt capacitance (C_0) value is expected for the crystal, the oscillator is able to start up with any crystal having less than 300 ohms ESR (equivalent series loss resistance). However, lower C_0 and ESR values guarantee faster oscillator startup.

The crystal frequency is used as the reference of the PLL, which generates the local oscillator frequency (f_{LO}). Therefore f_{LO} is directly proportional to the crystal frequency. The accuracy requirements for production tolerance, temperature drift and aging can thus be determined from the maximum allowable local oscillator frequency error.

Whenever a low frequency error is essential for the application, it is possible to “pull” the crystal to the accurate frequency by changing the load capacitor value. The widest pulling range can be achieved if the nominal required load capacitance of the crystal is in the “midrange”, for example 16 pF. The “pull-ability” of the crystal is defined by its motional capacitance and C_0.

Maximum XTAL Tolerances Including Temperature and Aging [ppm]

Bit Rate: 2.4kbps	Deviation [+/- kHz]						
	30	**45**	**60**	**75**	**90**	**105**	**120**
315 MHz	25	50	75	100	100	100	100
433 MHz	20	30	50	70	90	100	100
868 MHz	10	20	25	30	40	50	60
915 MHz	10	15	25	30	40	50	50

Bit Rate: 9.6kbps	Deviation [+/- kHz]						
	30	**45**	**60**	**75**	**90**	**105**	**120**
315 MHz	20	50	70	75	100	100	100
433 MHz	15	30	50	70	80	100	100
868 MHz	8	15	25	30	40	50	60
915 MHz	8	15	25	30	40	50	50

Bit Rate: 38.3kbps	Deviation [+/- kHz]						
	30	**45**	**60**	**75**	**90**	**105**	**120**
315 MHz	don't use	7	30	50	75	100	100
433 MHz	don't use	5	20	30	50	75	75
868 MHz	don't use	3	10	20	25	30	40
915 MHz	don't use	3	10	15	25	30	40

RX-TX ALIGNMENT PROCEDURES

RX-TX frequency offset can be caused only by the differences in the actual reference frequency. To minimize these errors it is suggested to use the same crystal type and the same PCB layout for the crystal placement on the RX and TX PCBs.

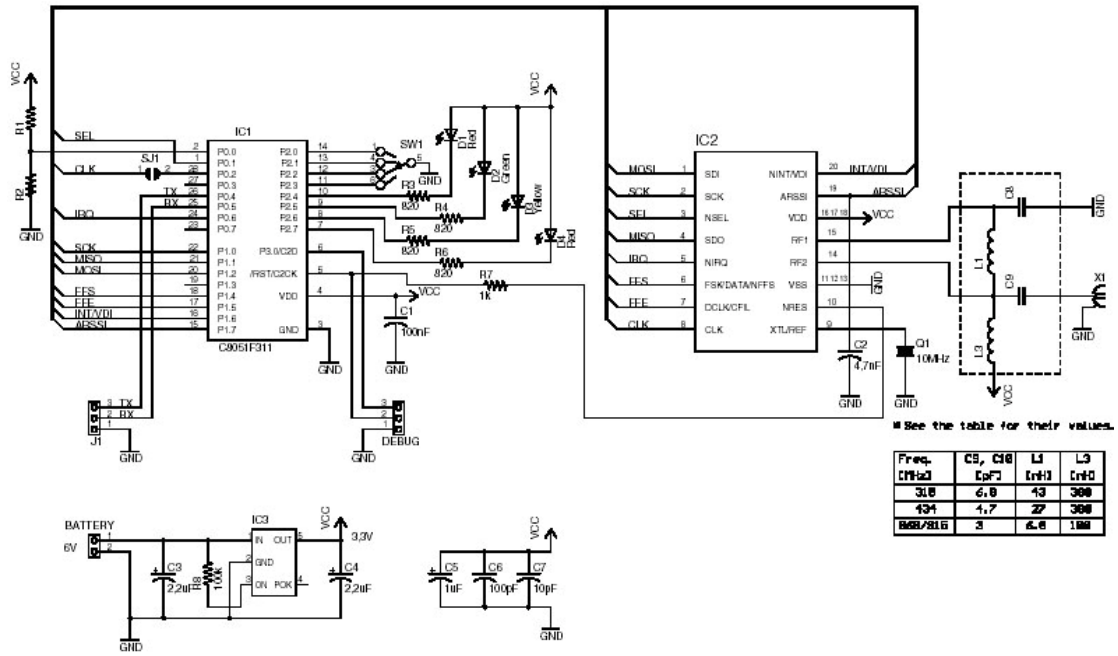
To verify the possible RX-TX offset it is suggested to measure the CLK output of both chips with a high level of accuracy. Do not measure the output at the XTL pin since the measurement process itself will change the reference frequency. Since the carrier frequencies are derived from the reference frequency, having identical reference frequencies and nominal frequency settings at the TX and RX side there should be no offset if the CLK signals have identical frequencies.

It is possible to monitor the actual RX-TX offset using the AFC status report included in the status byte of the receiver. By reading out the status byte from the receiver the actual measured offset frequency will be reported. In order to get accurate values the AFC has to be disabled during the read by clearing the "en" bit in the AFC Control Command (bit 0).

TYPICAL APPLICATIONS

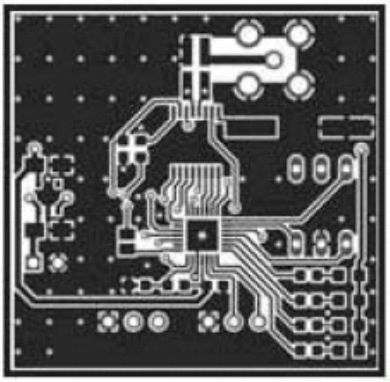
REPEATER DEMO (915 MHZ)

Schematics

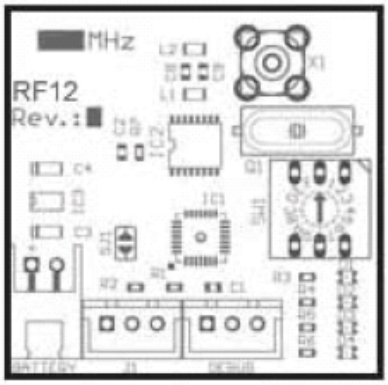


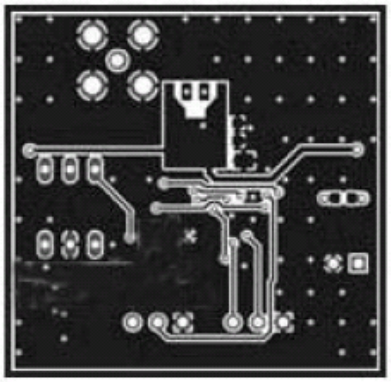
Freq. [MHz]	C8, C10 [pF]	L1 [nH]	L3 [nH]
315	6.8	43	300
434	4.7	27	300
868/915	3	6.8	100

PCB Layout



Top View





Bottom View