Technical Description

The brief circuit description is listed as below:

1) **U5 acts as 2.4GHz RF Module (MY85SPK02M2).**
   a. **U6 acts as Sound Circuitry and audio amplifiers(NS4158/NS4150)**
2) **U3 acts as a DC to DC regulator.**
3) **X1 16MHz Crystal for Bluetooth module IS1685S.**
5) **U2 acts as EEPROM (ACE24C32)**

Antenna Type: Internal antenna
Antenna Gain: 0dBi
Nominal rated field strength: 95.3 dBμV/m at 3m
Maximum allowed field strength of production tolerance: 89.2 to 99.2 dBμV/m at 3m

Bluetooth Mono Audio IC with A2DP Streaming

GENERAL DESCRIPTION

IS1685S is a compact, highly integrated, CMOS single-chip RF and baseband IC for Bluetooth v3.0 with Enhanced Data Rate 2.4GHz applications. This chip is fully compliant with Bluetooth specification and completely backward-compatible with Bluetooth 1.1, 1.2, 2.0 or 2.1 systems.

It incorporates Bluetooth 1M/2M/3Mbps RF, single-cycle MCU, MODEM, UART interface, and ISSC's own Bluetooth software stack to achieve the required BT v3.0+EDR functions.

To provide the superior audio and voice quality, it also integrates a DSP co-processor, a PLL, and a CODEC for voice and audio applications. For voice, not only basic A-law/μ-law/CVSD encoding/decoding but also enhanced noise reduction and echo cancellation were implemented by the built-in DSP to reach the better quality in the both sending and receiving sides. For enhanced audio applications, SBC decoding function is also carried out by DSP to satisfy A2DP requirements.

The device incorporates built-in self-test (BIST) and auto-calibration functions to simplify production test.

A wider input voltage range for adaptor can achieve better reliability.

FEATURES

- Bluetooth v3.0 + EDR which is backward-compatible with BT2.0 and 1.2.
- ISSC's own Bluetooth software stack for the headset or speaker application. It supports following profiles :
  - Hands Free 1.5
  - Handset 1.2
  - A2DP 1.0
  - AVRCP 1.0
  - PBAP 1.0
- Integrated DSP that supports:
  - Noise suppression
  - Echo suppression
  - Wind-noise suppression
  - Automatic volume control for speaker side
- Connection to two phones with HFP/A2DP profiles
- Support microphone and speaker equalization
- Built-in Chinese/English voice prompt
- Built-in firmware support external NFC (Near Field Connection) tag
- Support standard HCI commands for test requirements
- Capable charging voltage from an empty battery and sustain a direct DC input voltage up to 7V
- Charging current up to 350mA
- 7x7 mm^2 standard QFN 48 package

APPLICATIONS

- Bluetooth mono headset with A2DP music streaming
- Bluetooth mono speaker
- Bluetooth mono speaker phone
- Bluetooth mono car audio unit

Table of Contents

1 Overview

The ISSC IS1685S is a monolithic IC for Bluetooth v3.0 with EDR (Enhanced Data Rate) 2.4GHz applications. It incorporates a stand-alone baseband processor and with an integrated 2.4GHz transceiver. The IS1685S is designed to support high quality voice application; an audio engine and a high performance mono CODEC are integrated for this purpose. The internal Digital Signal Processor provides the enhanced noise reduction and echo suppression to offer the superior voice quality. A Power Manager Unit inside the chip minimizing the footprint and reducing the system cost.

FEATURES

System Specification

- Compliant with Bluetooth Specification v.3.0 (EDR) in 2.4 GHz ISM band

Baseband Hardware

- 16MHz main clock input
- Built-in internal ROM for program memory
- Support to connect to two hosts (phones, tablets…) with HFP or A2DP profiles simultaneously
- Adaptive Frequency Hopping (AFH) avoids occupied RF channels
- Fast Connection supported

RF Hardware

- Fully Bluetooth 3.0 (EDR) system in 2.4 GHz ISM band.
- Combined TX/RX RF terminal simplifies external matching and reduces external antenna switches.
- Max. +4dBm output power with 20 dB level control from register control.
- Built-in T/R switch for Class 2/3 application

- To avoid temperature variation, temperature sensor with temperature calibration is utilized into bias current and gain control.
- Fully integrated synthesizer has been created. There requires no external VCO, varactor diode, resonator and loop filter.
- Crystal oscillation with built-in digital trimming for temperature/process variations.

Audio processor

- Support 64 kb/s A-Law or μ-Law PCM format, or CVSD (Continuous Variable Slope Delta Modulation) for SCO channel operation.
- Noise suppression
- Echo suppression
- SBC decoding
- Packet loss concealment

Audio Codec

- 16 bit mono codec
- 94dB SNR DAC playback
- Integrate headphone amplifier for 16/32Ω speakers

Peripherals

- Built-in Lithium-ion battery charger
- Integrate 3V, 1.8V LDO and Switching mode regulator
- Built-in ADC for battery monitor and voltage sense.
- LED drivers

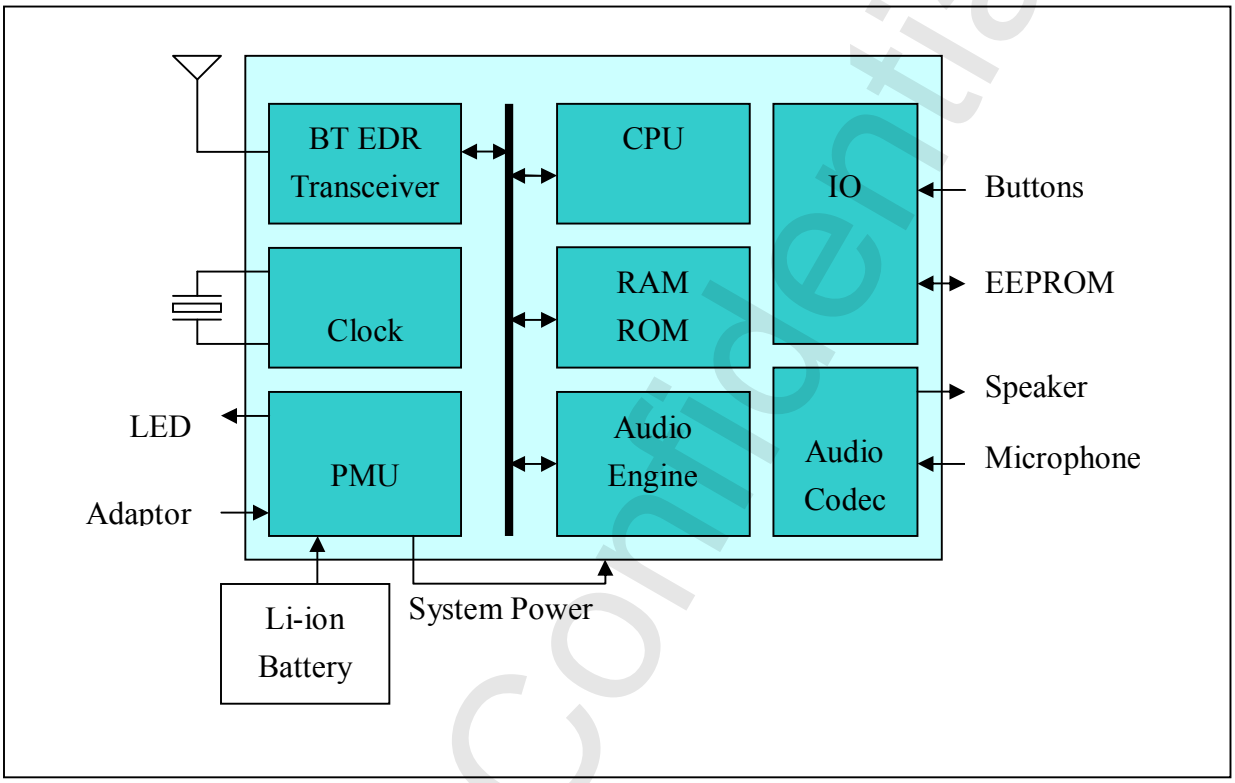
Flexible HCI interface

- High speed HCI-UART (Universal Asynchronous Receiver Transmitter) interface

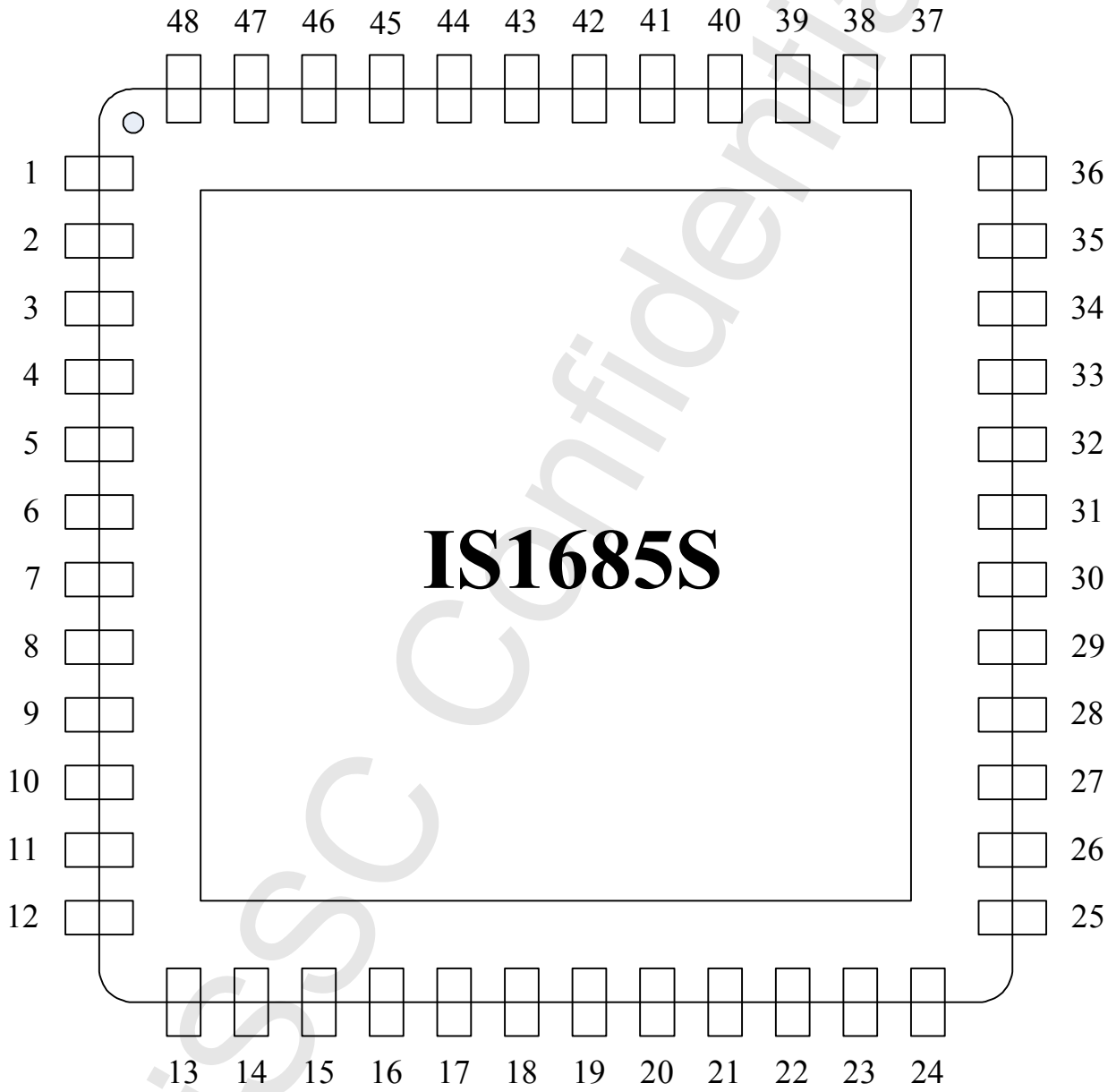
Package

- 7x7mm^2 48QFN standard package

APPLICATION DIAGRAM



2 PIN ASSIGNMENTS



Pin No.	I/O	Pin Name	Pin Descriptions
1	AO	AOHPM	Headphone common mode output/sense input
2	AO	AOHPL	Mono channel analog headphone output
3	P	VDDA	Positive power supply/reference voltage for CODEC
4	AO	VCOM	Internal biasing voltage for CODEC
5	AI	MICP1	Mono differential analog positive input
6	AI	MICN1	Mono differential analog negative input
7	P	MIC_BIAS	Electric microphone biasing voltage
8	P	VDD_IO	Power supply input for IO pads
9	I/O	P2_3	GPIO, default pull-high input
10	I/O	P1_5	GPIO, default pull-high input
11	AI	RST_N	System Reset Pin
12	I/O	P1_2	EEPROM clock SCL
13	I/O	P1_3	EEPROM data SDA
14	P	1V8	Core 1.8V power input
15	P	3V1_O	3.1V LDO output
16	P	CODEC_VO	3.1V LDO output for CODEC power
17	P	3V1_VIN	3.1V LDO input
18	P	ADAP_IN	Power adaptor input
19	P	BAT_IN	Battery input
20	P	SAR_AVDD	SAR 1.8V input
21	P	SYS_PWR	System Power Output
22	P	BK_VDD	Buck VDD Power Input
23	P	BK_LX	Buck switching node
24	P	BK_OUT	Buck output
25	P	MFB	Multi-Function Push Button key
26	AI	LED1	LED Driver 1
27	AI	LED2	LED Driver 2
28	I/O	P2_4	System Configuration, leave unconnected
29	I/O	P2_2	GPIO, default pull-low input
30	I/O	P0_5	GPIO, default pull-high input
31	O	HCI_TXD	HCI TX data
32	I	HCI_RXD	HCI RX data
33	I/O	P1_6	GPIO, external amplifier enable

Pin No.	I/O	Pin Name	Pin Descriptions
34	P	VDD_IO	I/O power supply input
35	I	XO_P	16MHz Crystal input positive
36	I	XO_N	16MHz Crystal input negative
37	RP	VCC_RF	RF power input for both synthesizer and TX/RX block
38	I	RX_CLASS1	Class1 RF RX path
39	I/O	RTX	Class2 RTX path; Class1/Class2 TX path
40	I/O	P0_1	Class1 TX Control signal for external TR switch
41	I/O	P0_3	Class1 RX Control signal for external TR switch
42	I/O	P3_0	GPIO, default pull-high input
43	I/O	P2_0	System Configuration, leave unconnected
44	I/O	P0_0	GPIO, default pull-low input
45	I/O	P0_4	Connect to Near Field Connection module
46	P	VDD_IO	I/O power supply input
47	I	EAN	No connection
48	P	VDDAO	Positive power supply for CODEC output amplifier
49	P	GND	Exposed pad as ground

3 RADIO TRANSCEIVER

IS1685S is design optimized for use in Bluetooth 2.4 GHz system. It provides low-power, low-cost with high receiving sensitivity and high transmitting power that extend the effective communication range. It is fully compliant with the Bluetooth Radio and EDR specifications.

TRANSMITTER

The internal PA has a maximum output power of +4dBm with level control 20dB from amplitude control. This is applied into Class2/3 radios without external RF PA. A larger output power for Class1 application, the external PA must be used.

The transmitter features IQ direct conversion to minimize the frequency drift. And it can excess 20dB power range with temperature compensation machine.

RECEVIER

The LNA can be operated into two type modes. One type is TR-combined mode for single port application. The other type is TR-separated mode for dual port application that uses an external PA/LNA application.

The ADC is utilized to sample input analogue wave to convert into digital for de-modulator analysis. Before the ADC, a channel filter has been integrated into receiver channel that can reduce the external component count and increase the anti-interference capability.

The image rejection filter is to reject image frequency for low-IF architecture. This filter for low-IF architecture is implied to reduce external BPF component for super heterodyne architecture.

There is an RSSI signal to the processor that it can control the power to make a good tradeoff for effective distance and current consumption.

SYNTHESIZER

A synthesizer generates a clock for radio transceiver operation. There is a VCO inside with tunable internal LC tank. It can reduce variation for components. A crystal oscillation with internal digital trimming circuit provides a stable clock for synthesizer.

4 MICROPROCESSOR

A single-cycle 8-bit MCU is inside IS1685S to carry out the required Bluetooth protocols. It can run at the range from 16MHz to a higher clock so that MCU firmware can dynamically consider the tradeoff between computing power and power consumption. MCU firmware is implemented in ROM (Read-Only-Memory) to minimize the power consumption of program execution and to save the cost of external flash.

EXTERNAL RESET

A watchdog timer capable of reset the chip. It has an integrated Power-On Reset (POR) circuit that resets all circuits to a known power-on state. This action can also be driven by an external reset signal that can be used to externally control the device, forcing it into a power-on reset state. The RST signal input is active low and no connection is required in most applications.

5 AUDIO

There are several stages for input and output that all can be programmed for varying gain response characteristics. At the microphone input side, you may use single-end input or differential input. One critical point in maintaining a high quality signal is to provide a stable bias voltage source for the condenser microphone's FET. DC blocking capacitors may be used at both positive and negative sides of input. Internally, this analog signal is converted to 15-bit 8 kHz linear PCM data.

The voice data taken from common memory is converted to an analogue value by a DAC. A multistage amplifier drives the audio signal and provides a differential signal between Line_out+ and Line_out-. The output amplifier is capable of driving a speaker directly if its impedance is 16/32Ω.

The IS1685S includes the capability to cancel the acoustic echo that may be present in a headset. All processing is performed by a DSP with low power consumption. This technique will most effectively cancel the incoming echo signal without impact to the desired voice signal. An outgoing signal to the speaker which level exceeds a certain threshold (and therefore deemed likely to create echo) will result in suppression of signal along the input path from the microphone. Filtering is also applied and provides for a smoother transition for a more natural user experience.

DIGITAL SIGNAL PROCESSOR

A digital signal processor (DSP) cooperates with MCU to deal with audio section. It provides audio processing with following features:

1. Internal ROM and RAM
2. 8 kHz CVSD
3. 8 kHz A–law
4. 8 kHz u-law
5. SBC decode
6. Equalization for both speaker and microphone sides
7. Noise reduction
8. Adaptive echo cancellation and echo suppression
9. Multi-band dynamic range compression

This built-in codec contains a high signal to noise (S/N) analog to digital converter (ADC) and digital to analog converter (DAC).

INTERNAL VOICE PROMPT

IS1685 stores English and Chinese voice prompts in the internal ROM. Voice prompt can be used from internal ROM or external EEPROM for every response points. There are night response points to notify user for current state.

Response points	English	Chinese
1	Power On	开机
2	Pairing	进入配接状态
3	Pairing Completed	完成配对
4	Connected	耳机已连接
5	Disconnected	耳机已断开
6	Incoming Call	远方来电
7	Pairing Not Completed	配对失败
8	Power Off	关机
9	Battery Low	电量不足

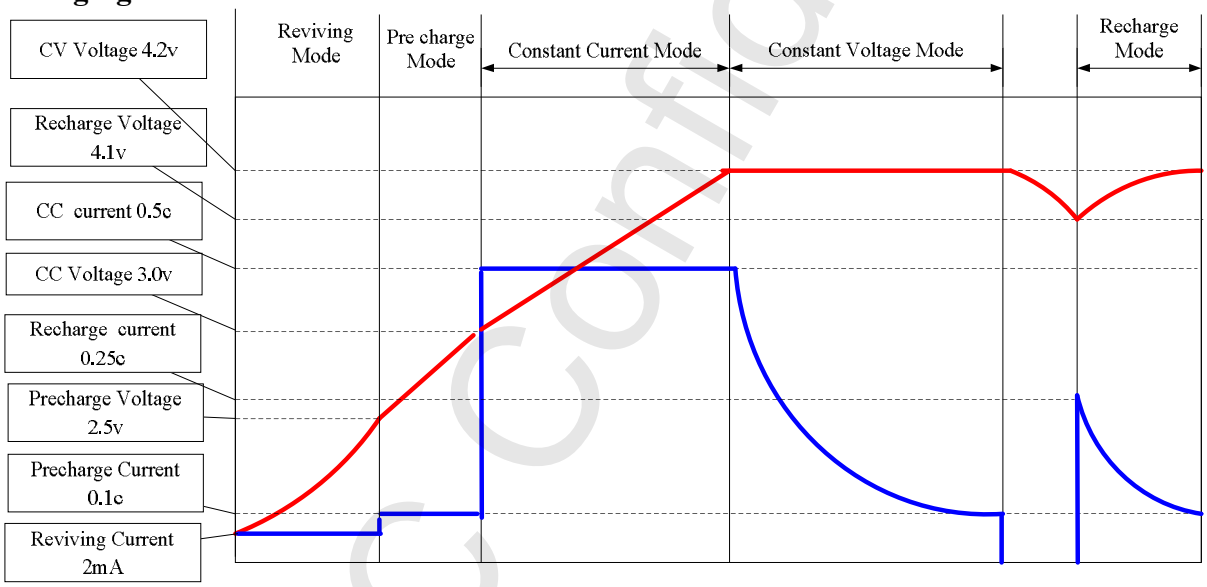
6 POWER MANAGE UNIT

The PMU inside the chip has two main features, charging a Li-ion battery and some regulators for voltage translation. A power switch is used to switch over the power source between battery and adaptor automatically. It also provides two LED drivers.

CHARGING A BATTERY

The charging current is configured in the EEPROM. Whenever the adaptor is plug-in, charging circuit is active. Reviving, Pre-charging, Constant Current and Constant Voltage modes are implemented and re-charging function is also included. The maximum charging current is 350mA.

Charging curve



VOLTAGE MONITING

A 10-bit Successive-Approximation-Register analog to digital converter (SAR ADC) provides one dedicated channel for battery voltage level detection. The warning level is programmable and stored in the EEPROM. This ADC provides a good resolution that MCU can control the charging process.

VOLTAGE REGULATION

The built-in voltage converter is used to convert the battery or adaptor power for power supply. It also integrates hardware architecture to control power on/off procedure. The built-in programmable LDOs provide power for codec and digital IO pads. It is used to buffer the high input voltage from battery or adapter. This LDO need s 1uF bypass capacitor.

There is a bulk voltage convert generating the voltage for RF and digital core power. This

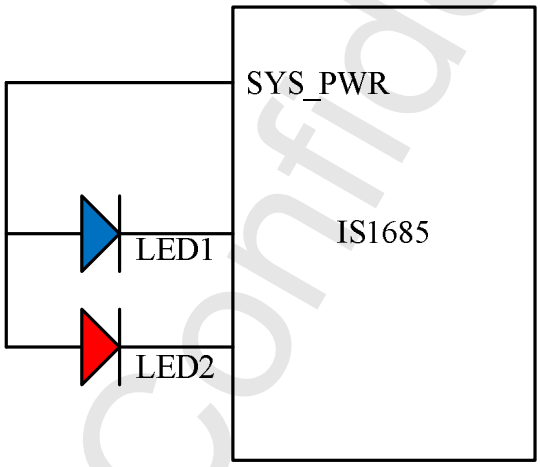
converter has good conversion efficiency to save power and fast transient response.

SWITCHING REGULATOR

The built-in programmable output voltage regulator can convert battery voltage for RF and baseband core power supply. This converter has high conversion efficiency and fast transient response.

LED DRIVER

There are two dedicate LED drivers to control the LEDs.



7 GENERAL PURPOSE IOs

IS1685 provides four general purpose IOs for keys setting. It can be saved in the EEPROM. The first button must be power key. The power on/off functions only can be set on MFB pin. There are four different operations for every button. They are short click, long click, double click and combinations.

GPIOs for Buttons

Button Name	GPIO name	Pin
Button 0	MFB	25
Button 2	P2_3	9
Button 3	P1_5	10
Button 5	P0_5	30

Buttons behaviors

Index	Description
POWERON_BUTTON_PRESS	Power on event
POWEROFF_BUTTON_PRESS	Power off event
ENTER_PAIRING_MODE	Enter pairing mode
SHS_RESET_TO_DEFAULT	Reset some EEPROM parameters to default value
CONNECT_HF_LINK	Active the HF link from headset to phone
DISCONNECT_HF_LINK	Disconnect the HF link
SHS_LED_DISABLE	Turn off LED
SHS_BUZZER_MUTE_TOGGLE	Buzzer ON/OFF toggle
SHS_LANGUAGE_CHANGE	Change voice prompt language
ANSWER	Answer an incoming call
REJECT_CALL	Reject an incoming call
END_CALL	Ending an active call if SCO exist or create the SCO link
INITIATE_VOICE_DIAL	Setup a voice dial call
CANCEL_VOICE_DIAL	Cancel ongoing voice dial call
LAST_NUMBER_REDIAL	Setup last number redial call
SWITCH_TO_SECOND_CALL	Switch to the second call
TRANSFER_TO_PHONE	Transfer the voice to phone
JOIN_TWO_CALLS	Three way talk

RELEASE_HELD_OR_WAITING_CALL	Release the call which is on hold or wait
RELEASE_ACTIVE_CALL_AND_ACCEPT_HELD_OR_WAITING_CALL	Release the active call and accept the call which is on hold or wait
MIC_MUTE	Mute microphone
MIC_UNMUTE	Un-mute microphone
MICROPHONE_GAIN_UP	Increase the microphone gain by one stage
MICROPHONE_GAIN_DOWN	Decrease the microphone gain by one stage
VOL_UP	Increase the speaker gain by one stage
VOL_DOWN	Decrease the speaker gain by one stage
AV_PLAY_PAUSE	Providing the AVRCP play/pause function while the A2DP link exist or linking back to a device with A2DP service
AV_STOP	Stop function
AV_FWD	Forward function
AV_BWD	Backward function

GPIOs for added functions

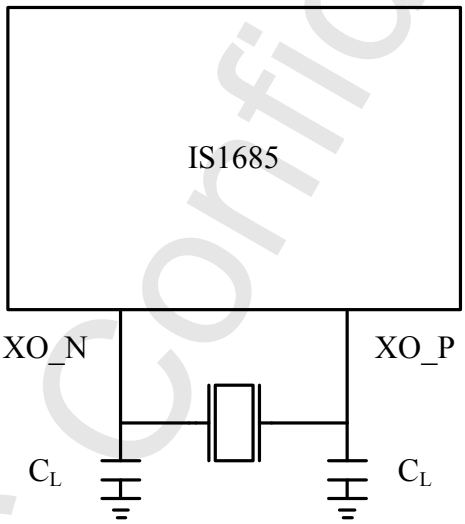
Functions	**GPIO name**	**Pin**
Slide switch	P0_0	44
Buzzer	P0_4	45
NFC detect	P0_4	45
External AMP enable	P1_6	33
3rd LED signal	P3_0	42

8 REFERENCE CLOCK

IS1685S is composed of an integrated crystal oscillation function. It used a 16 MHz external crystal and two specified load capacitors that a high quality system reference timer source is obtained. This feature is typically used to remove the initial tolerance frequency errors associated with the crystal and its equivalent load capacitance in mass production. Frequency trim is achieved by adjusting the crystal load capacitance through on-chip trim capacitors C_{trim} integrated in chip.

The value of trimming capacitance is around 200fF per LSB at 5 bits word, therefore the overall adjustable clock frequency is around 40 KHz.

C_{trim} =200fF * (1~31)



9 SPECIFICATIONS

Table 1: Absolute Maximum Voltages

Symbol	Parameter	Min	Max	Unit
VDD_CORE VDD_SAR VDD_PLL VCC_RF	Digital core supply voltage SAR ADC supply voltage PLL supply voltage RF supply voltage	1.7	1.98	V
VDD_IO	I/O supply voltage		3.6	V
VDD_CODEC	CODEC supply voltage	1.7	3.3	V
LDO_IN	3V1_VIN		4.5	V
BK_IN	BUCK supply voltage		4.3	V
ADP_IN	Input voltage for adaptor	4.3	7.7	V
BAT_IN	Input voltage for battery		4.3	V
T_{STORE}	Storage temperature	-40	+85	ºC

Table 2: Recommended operate condition

Symbol	Parameter	Min	Typical	Max	Unit
VDD_CORE VDD_SAR VDD_PLL VCC_RF	Digital core supply voltage SAR ADC supply voltage PLL supply voltage RF supply voltage	1.7	1.8	1.9	V
VDD_IO	I/O supply voltage	2.7	3.0	3.3	V
VDD_CODEC	CODEC supply voltage	1.7	2.7	3.3	V
LDO_IN	3V1_VIN	3		4.3	V
BK_IN	BUCK supply voltage	3		4.3	V
ADP_IN	Input voltage for adaptor	4.5		7	V
BAT_IN	Input voltage for battery	3		4.2	V
$T_{OPERATION}$	Operation temperature	-40	+25	+85	ºC

Table 3: BUCK switching regulator

Normal Operation		Min	Typ	Max	Unit
Input Voltage (Vin)		3		4.3	V
Default Output Voltage (Vout) (I_{load}=70mA, Vin=4V, ±5% accuracy)		1.71	1.85	1.89	V
Output ripple			10		mV_{RMS}
Transient response	I_{load} = 10 to 50mA		50		μs
	I_{load} = 50 to 10mA		50		
Conversion efficiency @BAT=3.8V	I_{load} = 50mA		86		%
Switching frequency			800		KHz
Maximum load current				100	mA
Quiescent Current				1000	μA
Output Current (peak)				200	mA
Load Regulation (I_{load} = 10 ~ 100mA)			1		mV/mA
Line Regulation (3.2V < Vin < 4.2V)			0.03 (30)		%/V (mV/V)
Shutdown Current				<1	μA

Table 4: Low Drop Regulation

Normal Operation		Min	Typ	Max	Unit
Operation Temperature		-40		85	℃
Input Voltage (Vin)		3.0		4.3	V
Output Voltage (V_{OUT}) (1) V_{OUT_CODEC} (2) V_{OUT_IO}	$V_{OUT\ CODEC}$ = 2.7V		2.7		V
	$V_{OUT\ CODEC}$ = 1.8V		1.8		
	$V_{OUT\ IO}$ = 3.1V		3.1		
	$V_{OUT\ IO}$ = 1.8V		1.8		
Output Accuracy (V_{IN}=3.7V, I_{LOAD}=100mA, 27'C)			±5		%
Transient response	I_{load} = 10 to 50mA		40	60	μs
	I_{load} = 50 to 10mA		40	60	
Output current (average)	V_{OUT}			100	mA
Output Current (peak)	V_{OUT}			150	mA
Drop-out voltage (I_{load} = maximum output current)				300	mV
Quiescent Current (excluding load, I_{load} < 100 μA)			45		μA
Load Regulation (I_{load} = 0mA to 100mA), △Vout Note: 0.4(mV/mA) * (100mA-0mA)=40mV				60 (0.6)	mV (mV/mA)
Line Regulation (Vout+0.3V<Vin<4.5V			7	10	mV/V
EN current				10	nA
Shutdown Current				<1	μA

Table 5: Battery Charger

Charging Mode (BAT_IN rising to 4.2V)	Min	Typ	Max	Unit
Input Voltage (Vin)	4.5	5.0	7.0	V
Battery trickle charge current (BAT_IN < trickle charge voltage threshold)		0.1C		mA
Programmable current range @BAT=3.6V, ADAP_IN=5V	0		350	mA
Trickle charge voltage threshold		3		V
Float voltage	4.158	4.2	4.242	V
Charging current variation	-20		+20	%

Table 6: LED driver

	Min	Typ	Max	Unit
Operation Temperature	-40		85	℃
Supply voltage	1.7	1.8	1.98	V
Open-drain Voltage			5.1	V
Open-drain Current			5.5	mA
Intensity control		16		steps
Current step		0.35		mA
Shutdown Current			1	μA

Table 7: Audio codec ADC

T= 25°C, Vdd=3.0V, 1KHz sine wave input, Bandwidth = 20~20KHz					
Parameter	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Input Level	Line/microphone input Full scale			2.2	Vpp
SNR	A-weighted 1KHz@full scale, Line input, microphone input		85		dB
	A-weighted 1KHz@full scale, Microphone boost enable		75		
Digital Gain		-54		4.85	dB
Analog Gain				26	dB
MIC Boost			20		dB
Gain Step			1.7		dB
Input resistance	$R_{L,}$ Microphone input		6	10	kOhm
Output capacitance	Cp			20	pF

Table 8: Audio codec DAC

T= 25°C, Vdd=3.0V, 1KHz sine wave input, Bandwidth= 20~20KHz					
Parameter	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Output Level	Full scale			2.1	Vpp
SNR	A-weighted 1KHz@full scale		94		dB
Max Output Power	R_L=16Ohm		34		mW
	R_L=32Ohm		17		mW
Digital Gain		-54		0	dB
Analog Gain		-28		3	dB
Analog Gain Step			1		dB
Output resistance	R_L	8	16	32	Ohm
Output capacitance	Cp			500	pF

Table 9: Transmitter section for BDR

VCC_RF = 1.8V Temperature = 25ºC						
Parameter		**Min**	**Typ**	**Max**	**Spec.**	**Unit**
Maximum RF transmit power			3	4.0	-6 to 4	dBm
RF power variation over temperature range with compensation enabled			±2			dB
RF power control range			20		≥16	dB
RF power range control resolution			0.3			dB
20dB bandwidth for modulated carrier			900		≤1000	KHz
ACP	F = F_0±2MHz		-33		≤-20	dBm
	F = F_0±3MHz		-45		≤-40	dBm
Note: F_0=2441MHz	F = F_0±>3MHz		-54		≤-40	dBm
Δf_{1avg} maximum modulation		150		165	140<Δf_{1avg}<175	KHz
Δf_{2max} maximum modulation		120		140	≥115	KHz
$\Delta f_{2avg}/\Delta f_{1avg}$		0.92	0.94		≥0.80	
ICFT (abs)		0	5	10	75	KHz
Drift rate (abs)		2		7	≤20	KHz/50us
Drift (single slot packet, abs)			12		≤25	KHz
2nd harmonic content @ Tx= 4dBm			-53		≤-47	dBm
3rd harmonic content @ Tx= 4dBm			-55		≤-47	dBm

Table 10: Transmitter section for EDR

VCC_RF = 1.8V Temperature = 25ºC						
Parameter		**Min**	**Typ**	**Max**	**Spec.**	**Unit**
Relative transmit power			-1.4		≧-4	dB
π/4 DQPSK max carrier frequency stability	$\|\omega_o\|$ freq. error		2.5	5	≤10	KHz
	$\|\omega_i\|$ initial freq. error		2.5	5	≤75	KHz
	$\|\omega_o+\omega_i\|$ block freq. error		5	10	≤75	KHz
8DPSK max carrier frequency stability	$\|\omega_o\|$ freq. error		2.5	5	≤10	KHz
	$\|\omega_i\|$ initial freq. error		2.5	5	≤75	KHz
	$\|\omega_o+\omega_i\|$ block freq. error		5	10	≤75	KHz
π/4 DQPSK modulation accuracy @ Tx= 2dBm	RMS DEVM		7		≤20	%
	99% DEVM		100		≤30	%
	Peak DEVM			25	≤35	%
8DQPSK modulation accuracy @ Tx= 2dBm	RMS DEVM		7		≤13	%
	99% DEVM		100		≤20	%
	Peak DEVM			20	≤25	%
In-band spurious emissions Note: F_0=2441MHz	F > F_0+3MHz		<-52		≤-40	dBm
	F < F_0-3MHz		<-53		≤-40	dBm

	F = F_0-3MHz		-46		≤-40	dBm
	F = F_0-2MHz		-34		≤-20	dBm
	F = F_0-1MHz		-34		≤-26	dBm
	F = F_0+1MHz		-37		≤-26	dBm
	F = F_0+2MHz		-34		≤-20	dBm
	F = F_0+3MHz		-46		≤-40	dBm
EDR differential phase encoding			100		≥99	%

Table 11: Receiver section for BDR

VCC_RF = 1.8V Temperature = 25ºC						
Parameter		**Min**	**Typ**	**Max**	**Spec.**	**Unit**
Sensitivity at 0.1% BER for all basic rate packet types	2402 MHz		-90		≤-70	dBm
	2441 MHz		-90			
	2480 MHz		-90			
Maximum received signal at 0.1% BER			-10		≥-20	dBm
C/I co-channel			4		≤11	dB
Adjacent channel selectivity C/I Note: F_0=2441MHz	F = F_0+1MHz		-7		≤0	dB
	F = F_0-1MHz		-7		≤0	dB
	F = F_0+2MHz		-36		≤-30	dB
	F = F_0-2MHz		-22		≤-9	dB
	F = F_0-3MHz		-24		≤-20	dB
	F = F_0+5MHz		-50		≤-40	dB
	F = F_{image}		-22		≤-9	dB

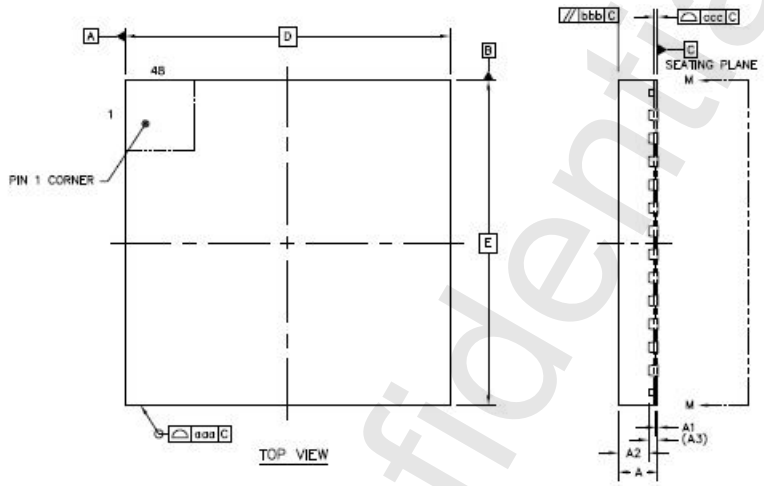
Table 12: Receiver section for EDR

VCC_RF = 1.8V Temperature = 25ºC						
Parameter		**Min**	**Typ**	**Max**	**Spec.**	**Unit**
Sensitivity (0.01% BER)	2402 MHz π/4 DQPSK		-90		≤-70	dBm
	2441 MHz π/4 DQPSK		-90			
	2480 MHz π/4 DQPSK		-90			
	2402 MHz 8DPSK		-83		≤-70	dBm
	2441 MHz 8DPSK		-83			
	2480 MHz 8DPSK		-83			
Maximum received signal (0.01% BER)	π/4 DQPSK		-10		≥-20	dBm
	8DPSK		-10		≥-20	
C/I co-channel (0.01% BER)	π/4 DQPSK		5		≤13	dB
	8DPSK		14		≤21	dB
Adjacent channel selectivity C/I Note: F_0=2441MHz	F = F_0+1MHz π/4 DQPSK		-13		≤0	dB
	F = F_0+1MHz 8DPSK		-7		≤5	dB
	F = F_0-1MHz π/4 DQPSK		-13		≤0	dB
	F = F_0-1MHz 8DPSK		-7		≤5	dB
	F = F_0+2MHz π/4 DQPSK		-38		≤-30	dB
	F = F_0+2MHz 8DPSK		-34		≤-25	dB
	F = F_0-2MHz π/4 DQPSK		-23		≤-7	dB

	F = F_0-2MHz 8DPSK		-21		≤0	dB
	F = F_0-3MHz π/4 DQPSK		-26		≤-20	dB
	F = F_0-3MHz 8DPSK		-19		≤-13	dB
	F = F_0+5MHz π/4 DQPSK		-53		≤-40	dB
	F = F_0+5MHz 8DPSK		-46		≤-33	dB
	F = F_{image} π/4 DQPSK		-23		≤-7	dB
	F = F_{image} 8DPSK		-21		≤0	dB

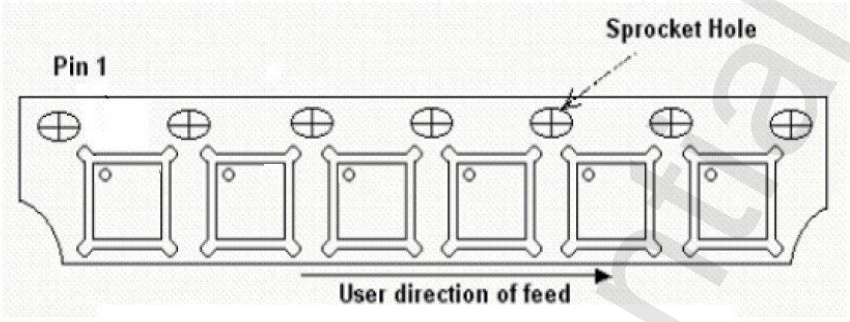
10 PACKAGE

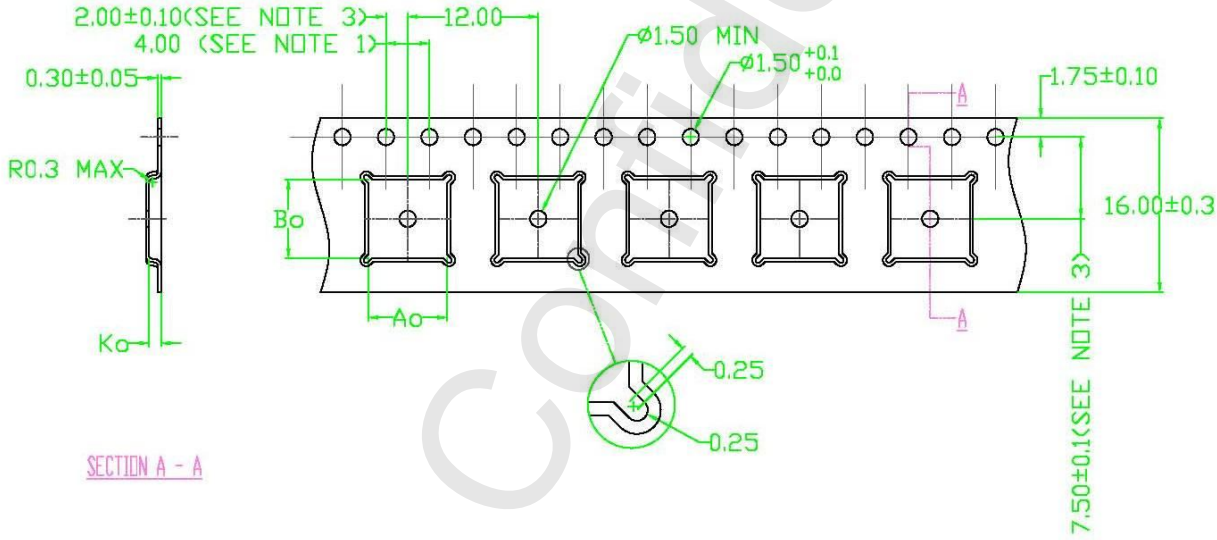
Chip Outline



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.035	0.05
MOLD THICKNESS		A2	---	0.65	0.67
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.2	0.25	0.3
BODY SIZE	X	D		7 BSC	
	Y	E		7 BSC	
LEAD PITCH		e		0.5 BSC	
EP SIZE	X	J	5.2	5.3	5.4
	Y	K	5.2	5.3	5.4
LEAD LENGTH		L	0.35	0.4	0.45
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		bbb		0.1	
COPLANARITY		ccc		0.08	
LEAD OFFSET		ddd		0.1	
EXPOSED PAD OFFSET		eee		0.1	

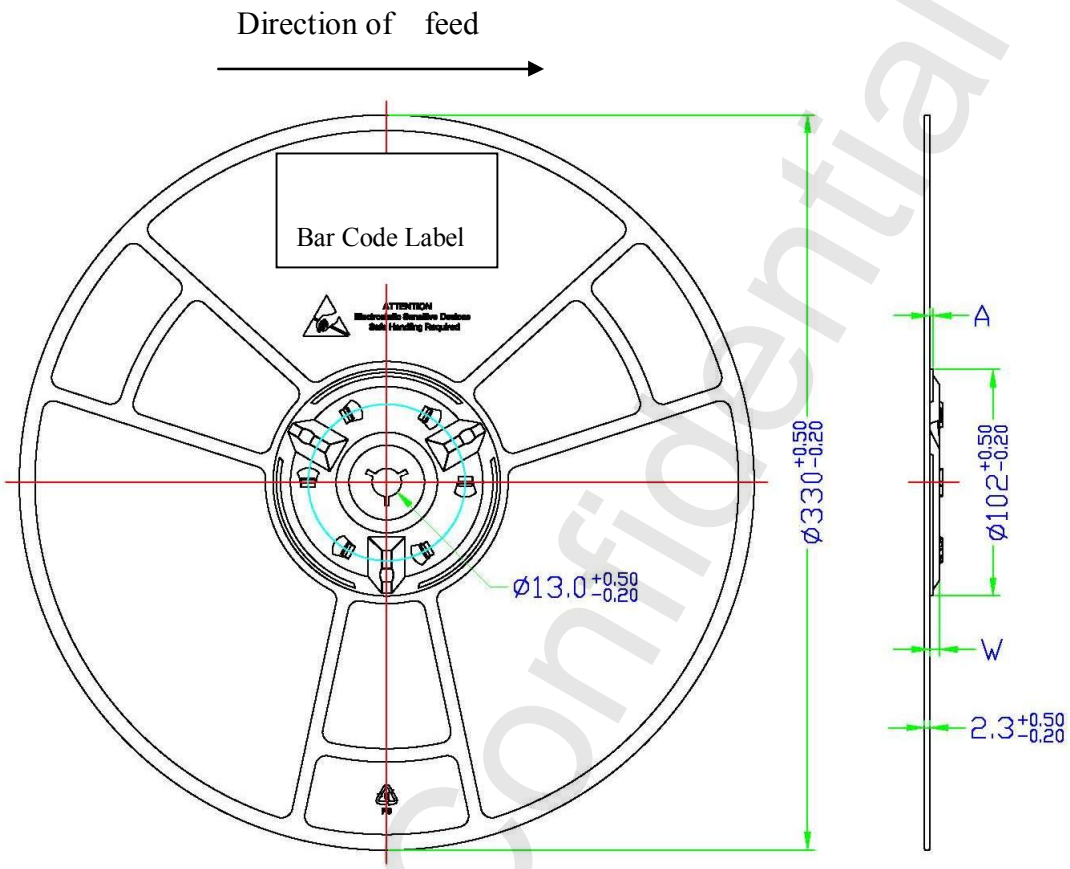
Tape Dimension





A_0	B_0	K_0	Unit	Notes
7.25	7.25	1.10	mm	1. 10 sprocket hole pitch cumulative tolerance ±0.2 2. Material: PS + C 3. Camber not to exceed 1mm in 100 mm 4. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.

Reel Information



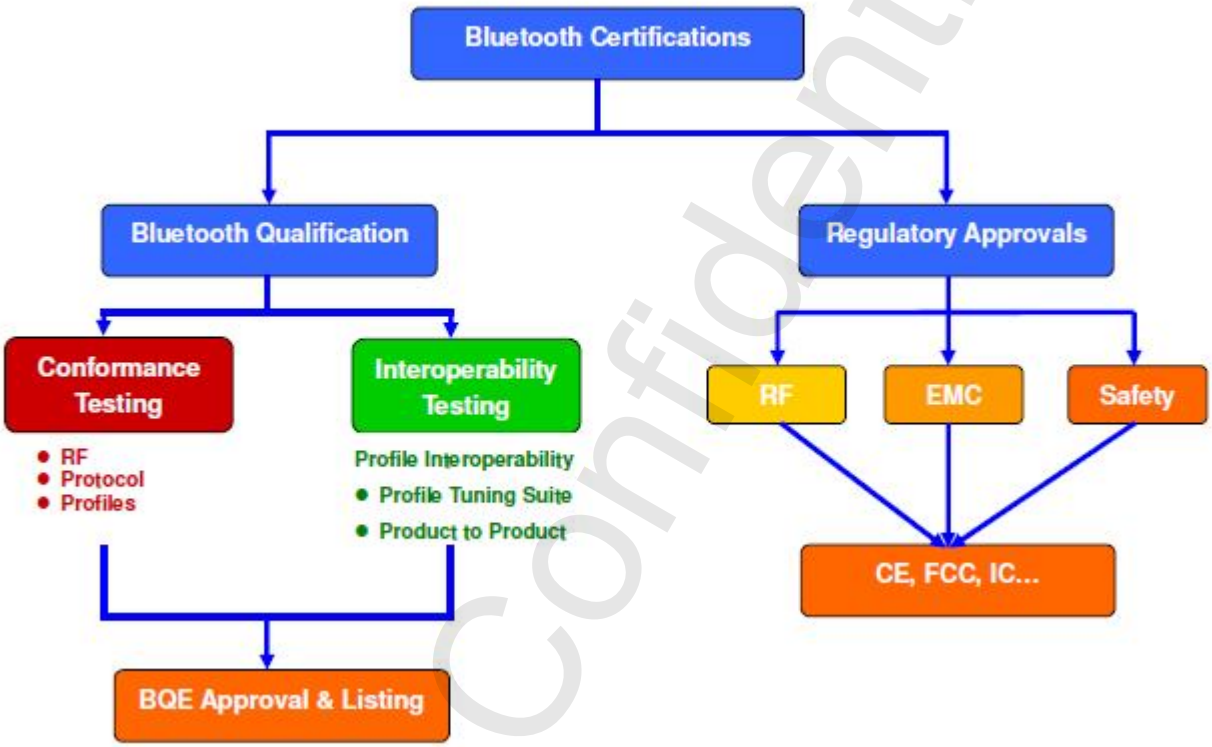
Package Type	Nominal Hub Width (Tape Width)	A	W	Units
QFN 7x7x0.9 mm	16	4.5	16.4 (+0.3/-0.2)	mm

Note:

Minimum Order Quantity is 3000 Tape & Reel

11 BLUETOOTH CERTIFICATIONS

There are some regulations to guarantee the wireless product can work properly. The following chart displayed the main certifications on the world.



Bluetooth qualification, the Bluetooth SIG certification process, is required for any product using Bluetooth wireless technology and is a precondition of the intellectual property license for use of the technology. Using this chip to create a new EPL (end product listing) has to reference some QDID (qualification device ID) come from IS1685S. IS1685S claim following QDID.

QD ID	Design Description	Product Type
B016460	ISSC Bluetooth v3.0 Embedded Host Stack	Component (Tested)
B014077	ISSC Bluetooth v2.1 Embedded Protocol	Component (Tested)
B016749	ISSC Bluetooth 3.0+EDR Single Chip	Component (Tested)

12 REFLOW PROFILES

1.) Follow: IPC/JEDEC J-STD-020 C

2.) Condition:

Average ramp-up rate (217℃ to peak): 1~2℃/sec max.
Preheat：150~200C、60~180 seconds
Temperature maintained above 217℃：60~150 seconds
Time within 5℃ of actual peak temperature: 20 ~ 40 sec.
Peak temperature：250+0/-5℃ or 260+0/-5℃
Ramp-down rate : 3℃/sec. max.
Time 25℃ to peak temperature : 8 minutes max.
Cycle interval：5 minus