Exhibit 8: User's Manual

NQE1005 TIM TRANSMITTER

Table of Contents

Declaration of Compliance

The following declaration applies to World Wireless Communications Corp NQE1005 TIM spread spectrum transmitter. This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) This device must accept any interference received, including interference that may cause undesired operation.

2. Caution

Changes or modifications not expressly approved by World Wireless could void the authority to operate this equipment.

The responsible party for this declaration is:

World Wireless Communications Corp
150 Wright Brothers Drive / Suite 560
Salt Lake City, Utah 84116
Phone: (801) 575-6600

Note to Installers

Do not install this equipment in locations that could cause RF exposure to persons where the distance is less than 20 centimeters.

Hardware Requirements

Antennas

Built in: No connections required

Power Supply

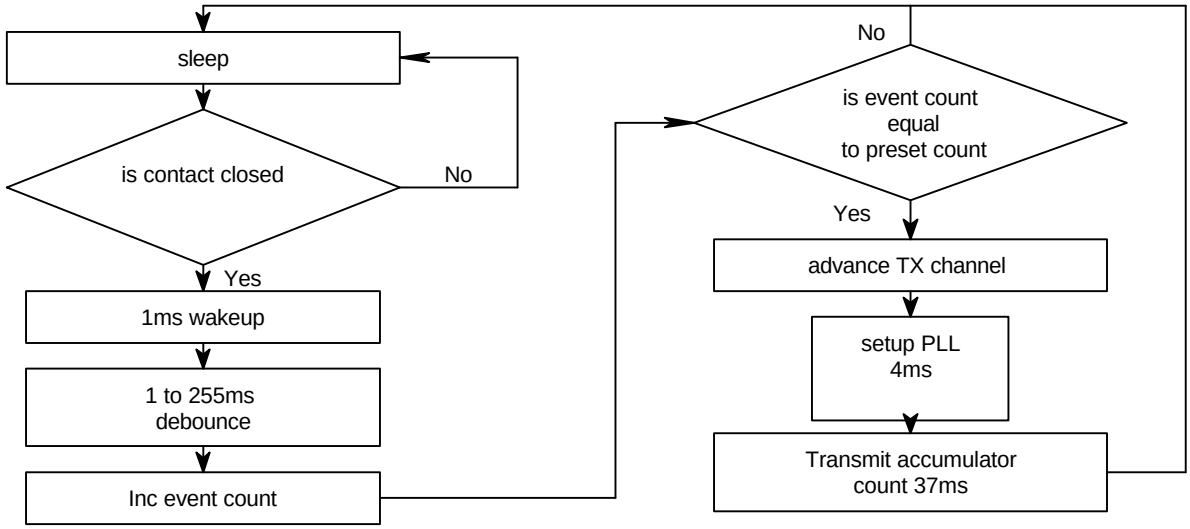
The NQE1005 Transmitter is a sealed unit with internal lithium 3.6 volt battery
designed for 10 year service under normal conditions. No maintenance required.

NQE1005 TIM TRANSMITTER
Functional Description

General Description

The TIM Transmitter remains in "sleep" mode until an input event occurs. The TIM Transmitter wakes up to monitor and accumulates switch closures. Events represent units of power or other similar items measured. Events are monitored by closures between pins 1 and 6 of connector JP2. Events are accumulated and compared to a preset number
(1 to 10,000 set at installation).When this count is reached it will trigger, transmitting a data packet containing the total accumulated count. This data is transmitted to a receiver station using FSK (Frequency Shift Keying) modulation, on 1 of 25 different frequency channels ranging from 902 to 928 MHz. The complete packet transmits within 0.043 seconds. After the data has transmitted, the transmitter returns to “sleep” mode and collects another set of data. This process is then repeated when the next preset count is reached and transmitted on the next frequency from the hop table. As an example, let’s say the meter count is at 1000 units of gas used and the preprogrammed event count is set at 10. The TIM wakes up 10 times to advance the accumulator but will only advance the transmitter channel on the tenth event. At this point the accumulated count of 1010 would be sent. All 25 transmit frequency channels are used before any given frequency is repeated. The worst case or shortest delay that the firmware allows is 0.043 seconds between channels. Accounting for switch debounce of 1ms, a wakeup time of 1ms, 4ms to setup the PLL, and 0.037 seconds to transmit. It takes 1.075 seconds to visit all 25 channels (0.043x25=1.075 seconds). Any one channel could be visited 9.3 times in 10 seconds (10\1.075 = 9.30). Total transmit time for any 10 second period is 9.3x .037 for 0.344 seconds, 0.4 seconds is

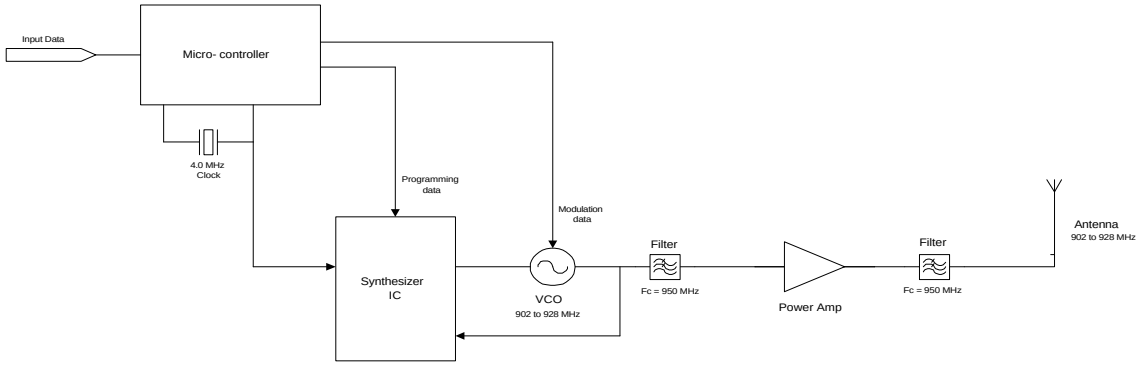
allowed.



Detailed Description

The 4 MHz crystal (Y1) will provide a reference clock for the synthesizer IC (U2) and the micro-controller (U1). U1 will program the dividers in U2 to values that will select the appropriate frequency. The output of U2 (pin 4) will be filtered (C14, R11, C15, R24, C35, C46, R33, C47, R32, and C46) and will provide the tune voltage for the Voltage Controlled Oscillator (VCO). The VCO consists of D1, D2, Q1, Q3 and their associated resistors, capacitors, and inductors. The output of the VCO (Q3) will provide the feedback (via C19 and R20) for U2 (pin 8) and will also feed the Power Amplifier. The Power Amplifier consists of a low pass filter (C49, L8, C50, L9, and C51), Q2, Q5 and their associated resistors, capacitors, and inductors. The output of the Power Amplifier (Q5) is then filtered by C33, C56, L10, C55, C24, C25, C62, C26, and C37. The output of C37 will then feed the antenna (the antenna is etched on the PCB). Serial data from U1-2 passes through a variable resistor (R2) and is low pass filtered by C41, R28, C42, R29, and C43. This signal then modulates the VCO using D1, C38, and C36. R2 sets the frequency deviation of the output frequency. When in "sleep" mode, U1 (pins 3 & 6) powers down the VCO and power amplifier by setting the base voltage on Q4 and Q6 to a high voltage (3.6 volts). Prior to transmitting, U1 pulls these two signals to a low (0 volts), which will apply power to the VCO and power amplifier. JP1 is used as an interface to do "on-board" programming of the micro-controller (U1). JP2-2 & 3 allows the battery (3.6 Volts) to be disconnected until the unit is installed out in the field. J2-4, 5, & 6 will provide an external interface to U1.

TITANIC TIM TRANSMITTER
Block Diagram



WinGate 2000 TIM RECEIVER
Functional Description

TIM RECEIVER DESCRIPTION

Overview

The TIM Receiver is a frequency-hopping receiver with an IF bandwidth of 330KHz. It continuously hops through the 25 specific frequencies it has memorized, stopping just long enough at each frequency to determine whether valid data is being received. If valid data is detected, the receiver stays on frequency long enough to accept the entire packet of data, then it continues hopping. The receiver detects frequency-modulated, Manchester-encoded, digital signals using dual down-conversion architecture. On board processors decode and verify that the data is good before passing it to a motherboard through a 24-pin (12x2) connector. Power and control signals are also passed to the receiver through this connector.

RF Front End

A RF input signal enters the receiver through a female SMA connector. The signal passes through a SAW band pass filter (915 +/- 13 MHz), an amplifier, and another SAW band pass filter. Each of these filters has approximately 3 dB of loss while the amplifier has approximately 18 dB of gain. The signal next passes through the first mixer, which provides 18 dB of conversion gain. The Local Oscillator (1^{st} LO) for this mixer comes from the Synthesizer which provides frequencies from 967.1 MHz to 985.5MHz at approximately –10 dBm. The Intermediate frequency from this mixer is 61.3 MHz. This IF passes through a three-section band pass filter, which must be manually tuned. On the output end of the band pass filter is a resonant shunt that must be tuned to 66.65 MHz to provide immunity to “half-IF spurs”. Following this shunt is an impedance match to the input of the FM Demodulator chip, MC13156.

Synthesizer

The synthesizer consists of a discrete designed Voltage Controlled Oscillator (VCO) and a Phase Locked Loop (PLL) chip, MC145191F. The heart of the VCO is a varactor and a single-loop,

air-core inductor. The PLL provides voltage in the range of 0.5V to 4.0V (measured at TP4) to the varactor for tuning the 1st LO frequency. The air inductor must be tuned by hand to center the VCO response for the given voltage input. A control voltage of 0.5 volts corresponds approximately to an output frequency of 960 MHz while a control voltage of 4.0V corresponds approximately with an output frequency of 990 MHz. The VCO output is buffered before being sent to the mixer or fed back to the PLL

Chip. The PLL receives a serial control word from one of the micro controllers to set the synthesizer frequency. The reference frequency for the PLL is 24 MHz.

FM Demodulator Chip MC13156

The 1st IF of 61.3 MHz enters the FM chip, MC12156, on pin 1, which is the input to a second mixer. The 2nd LO of 72 MHz enters the mixer on pin 24 of the chip at approximately –3 dBm. The 2nd LO is derived from the third harmonic of the 24 MHz crystal oscillator that services the PLL and micro controllers. The output of the mixer is at 10.7 MHz. This 2nd IF then passes through a narrow band ceramic filter, an on chip amplifier, another ceramic filter, and back on chip to a limiting amplifier. The filters have 3 dB of loss and a bandwidth of 330kHz; the amplifiers have 39 dB and 55 dB of gain respectively. The final stage is a demodulation using an off chip tuned circuit that must be adjusted for maximum data amplitude and duty cycle symmetry. The demodulated data signal is then lowpass filtered by an off chip op-amp circuit before passing onto the microprocessors. The chip also provides a signal strength indicator on pin 20 in the form of a current proportional to the signal strength. This current is converted to a voltage through an adjustable, external resistor and compared with hysteresis to a set level. The output of this comparator is called the “squelch” line. The squelch line goes high (+5V) for signals above the minimum sensitivity of the receiver and is low (0V) otherwise.

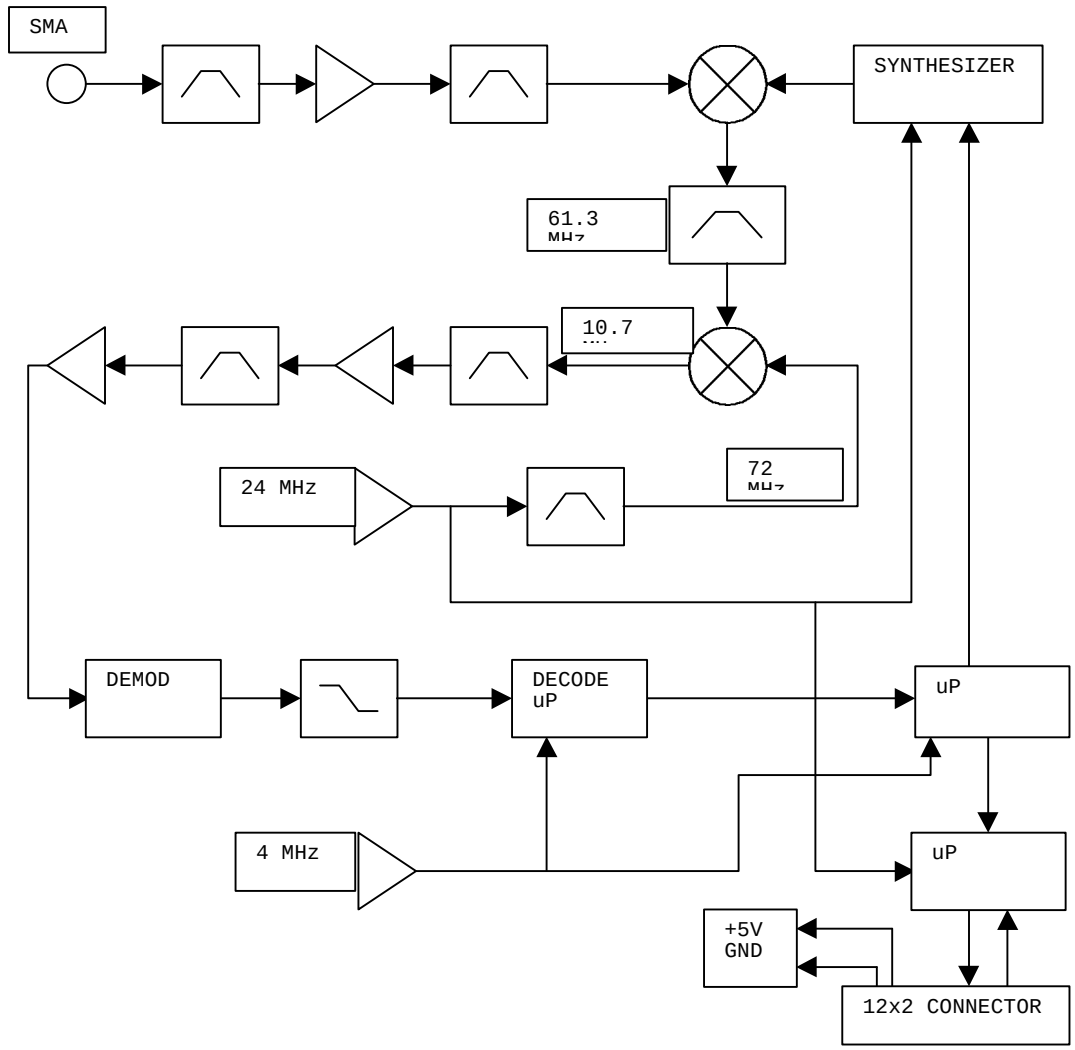
Microprocessors

There are three processors on the receiver. The first one, U5, takes the demodulated data stream and decodes the Manchester formatting. The decoded data passes along to a processor, U3, which controls the PLL hopping and performs the verification of the bit stream to determine if it is valid data. The valid data then passes to U8, which handles interface with the outside world through the 24-pin motherboard connector.

Specifications

1.1	Sensitivity:	-103 dBm
1.2	Dynamic Range:	100 dB
1.3	Data Rate :	9600 BAUD
1.4	Temperature	Range: -40 C to +85 C
1.5	Input Range:	902 to 928 MHz
1.6	Hop Frequencies:	905.8 MHz to 924.2 MHz in 600 kHz hops
1.7	Packaging:	Metal box with female SMA connector for RF input and 12x2 Socket for power and control.

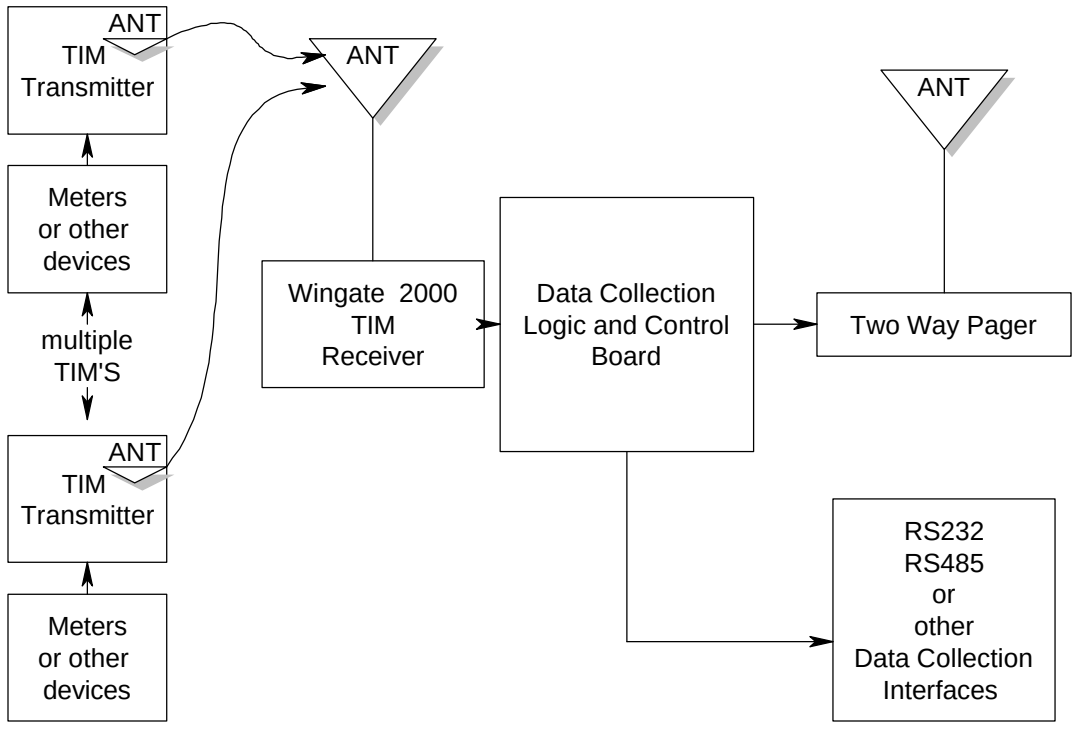
7.0 Block Diagram



Receiver and System Description

The NQE1005 is the companion to the WinGate 2000 Receiver from World Wireless Communications. This receiver fast scans all twenty-five channels listed in the hopping table. If valid data is detected from one of the Transmitters it stays on that channel long enough to accept an entire packet of data. The on board processor then passes the data out to a data collection system and continues to scan for the next transmitter. After each transmission the transmitters advance to the next frequency in the hopping table. When the input count is reached a new packet is sent. This completes the cycle. One typical implementation is illustrated below.

Typical System Using the NQE1005 Transmitters



Example System Operation

Let us assume a system with 16 TIM Transmitters and one WinGate 2000 TIM Receiver. Each TIM Transmitter is attached to meters with event counts set to allow transmitters to transmit depending on meter demand from a few minutes to several hours. As each TIM reaches the condition were the event count equals the preset count the contents of the accumulator will be sent to the receiver. Let us say the accumulator was at 1010 and the event count was set to 20 the value received would be 1030. Let us assume that either some other Transmitter or another TIM transmitted at the same time on the same frequency one packet might be lost but on the next transmit a count of 1050 would be received only the intermediate count of 1030 would be lost. Because of the random nature of count generation the over all system error rate is very acceptable.

Frequency Table Description

The frequency assignments were made on the basis of dividing the available channel allocation into 400 KHz channels. Then dropping the end channels for guard bands and the center channels next to 916 MHz for improved performance. The channels were assigned the numbers 1 – 25 then randomized as shown in figure 1.

Assigned Tx Freq		Random Table	
1	905.8MHz	8	910 MHz
2	906.4 MHz	18	920 MHz
3	907 MHz	19	920.6 MHz
4	907.6 MHz	4	919.4 MHz
5	908.2 MHz	20	921.2 MHz
6	908.8 MHz	25	924.2 MHz
7	909.4 MHz	4	907.6 MHz
8	910 MHz	2	906.4 MHz
9	910.6 MHz	13	917 MHz
10	911.2 MHz	24	923.6 MHz
11	911.8 MHz	7	909.4 MHz
12	912.4 MHz	22	922.4 MHz
13	917 MHz	6	908.8 MHz
14	917.6 MHz	23	923 MHz
15	918.2 MHz	1	905.8 MHz
16	918.8 MHz	16	918.8 MHz
17	919.4 MHz	14	917.6 MHz
18	920 MHz	15	918.2 MHz
19	920.6 MHz	9	910.6 MHz
20	921.2 MHz	10	911.2 MHz
21	921.8 MHz	11	911.8 MHz
22	922.4 MHz	12	912.4 MHz
23	923 MHz	21	921.8 MHz
24	923.6 MHz	3	907 MHz
25	924.2 MHz	5	908.2 MHz

Figure 1

NQE1005 TIM TRANSMITTER
Specifications

Data Transmission

The NQE1005 TIM Transmitter will transmit 11 bytes of data every time the event counter capture matches the programmed interval. Each transmission occurs on one of 25 distinct frequencies between 905.8 and 924.2MHz.

Sync Flags
65 sync flags (data 7Eh) will be sent out to allow receiver to synchronize on the transmission frequency.

Sync Byte
1 sync byte (data AAh) will be transmitted to indicate start of packet

Address
32 bit (4 Byte) address transmitted

Input Status
Status of external input other than pulse count input. Status of input reflected in the status byte sent at the time of transmission.

Counter
16 bit (2 Byte) up counter keeping track of switch closures (normal state of input pin is active high). Counter will increment on switch closure (negative edge).

CRC Bytes
2 bytes of CRC data transmitted to ensure accuracy of transmitted data

Programming

The TIM Transmitter is programmed using the PC parallel port to operate a synchronous serial data transfer using 3 I/O pins from the Transmitter (switch input, pclock and pdata). Data valid on rising clock edge. The data transfer format follows:

Command
1 command byte to indicate to TIM to read and send or receive and write data from/to EEPROM

Address

32 bit (4 Byte) programmable address stored in non-volatile memory

Transmission Interval

Programmable interval from 1 to 10000 used to update the next transmission capture count. Interval stored in non-volatile memory.

Pulse debounce Duration

Programmable from 1 to 255 ms with 50 ms set as factory default. Pulse duration (debounce) stored in non-volatile memory

Counter Preload

Programmable counter preloaded from 0 – 65535 (2 bytes).

TIM Options Programming Communications Format

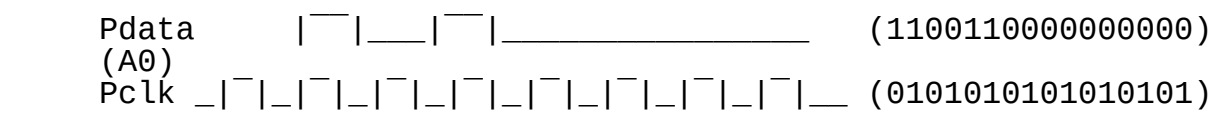
Handshake

TIM must recognize a handshake routine from the PC parallel port as follows. Pclk and Pdata are inputs to the TIM during handshake

	Parallel Port to TIM out		Tim Responds
	Pclk	Pdata	
1.	0	1	0
2.	0	0	1
3.	0	1	0
4.	1	1	1

Data Transfer – Write

After accepting the handshake sequence, the TIM will read in the next 8 bits of data that is presented on the Pdata pin when the Pclk pin transitions from low to high. If the 8 bits is a 'A0' hex, the TIM will receive the next 72 bits as data in, then store the data at the appropriate location in NVRAM.

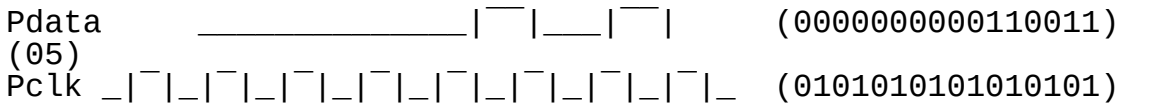


Data Sequence – Write

Pdata == [Command][Addr1][Addr2][Addr3][Addr4][IntrvlHigh[IntrvlLo][Debounce][PresetHigh[PresetLo]

Data Transfer – Read

After accepting the handshake sequence, the TIM will read in the next 8 bits of data that is presented on the Pdata pin when the Pclk pin transitions from low to high. If the 8 bits is a '05' hex, the TIM will transmit the next 72 bits as data out on the pushbutton input pin.



Data Sequence – Read

Pdata [Command]
Pushbutton[Addr1][Addr2][Addr3][Addr4][IntrvlHigh[IntrvlLo][Debounce][PresetHigh[PresetLo]

Data Transmission

The TIM Transmitter will transmit 11 bytes of data every time the event counter capture matches the programmed interval. Each transmission occurs on one of 25 distinct frequencies between 905.8 and 924.2MHz.

Frequency

The TIM Transmitter will broadcast the accumulated data on one of 25 frequencies in pseudo-random order.

Sync Flags

65 sync flags (data 7Eh) will be sent out to allow receiver to synchronize on the transmission frequency.

Sync Byte

1 sync byte (data Aah) will be transmitted to indicate start of packet

Address

32 bit (4 Byte) TIM address transmitted

Input Status

Status of secondary input reserved for future use. Status of input reflected in the status byte sent at the time of transmission

Counter

16 bit (2 Byte) up counter keeping track of switch closures (normal state of input pin is active high). Counter will increment on switch closure (negative edge).

CRC Bytes

2 bytes of CRC data transmitted to ensure accuracy of transmitted data

CRC = x^-15 + x^-13 + x^-1

Explanation 16 Bit CRC Generation:
If lsb of data byte == 1, EXOR 0xA001 into CRC
Shift data byte right
Shift CRC right on every bit (0 rotates into msb)
Shift the data byte 8 times (8 bits)
Shift the 8 bytes of data in the message through the crc.

Baud Rate

Data is transmitted using Manchester encoding (BITOUT = DATA && CLOCK) at 16129 data rate.

Deviation

150KHz – selectable using potentiometer on PCB.

IDENTIFCATION LABEL

The following label will be permanently attached to the front of the NEQ1005 TIM Transmitter, as shown below.