

# THE DESCRIPTION OF CIRCUIT

## 1. INTRODUCTION

The paging receiver has a single loop antenna which enables it to operate at around  $7\mu\text{V/m}$  in free space. The paging receivers are double conversion super-heterodyne receivers. The double conversion IF will contribute to improved selectivity and will consist of a first IF of 21.4MHz and a second IF of 455kHz.

The paging receiver consists of a RF board and a DIGITAL board. The RF board consists of a loop antenna, LNA, Mixer, Saw filter, First local oscillator, Multiplier, and FSK Receiver IC, The DIGITAL board consists of a MCU, LCD, DC-DC converter, EEPROM, Buzzer, Motor, RESET CIRCUIT and LED lamp.

## 2. THE PARTS OF RF Board

### 2.1 Loop Antenna

The loop antenna plated metal connects to the matching network (C1,2,3,75,76, TC1) between antenna and LNA(Q1,Q2). The matching network is used to tune the pager's operating frequency by making TC1 variable.

### 2.2 RF Amplifier(Q1,Q2)

The RF amplifier is a low noise amplifier, consists of the cascade transistors. The RF signal is coupled through TC1 to the input of a LNA(Q1,Q2). The RF signal is then amplified about 15dB. The amplified signal from Q1,Q2 is passed through capacitor C11, C12.

### 2.3 Band Pass Filter(SAW filter)

The band pass filter is used to reject the unwanted signal and to select the wanted channel signal. The capacitor C9,10,11,12 and inductor L1 is a matching network to adjust the impedance between a LNA and a SAW filter. The passed signal via saw filter(SAW1) have a 3MHz bandpass and is transferred to the Mixer(Q3).

### 2.4 AGC

The AGC circuit(Q6) used to control the gain of LNA by the RSSI signal of FSK receiver IC(U1), which improved the received signal ratio on the other strong electro-magnetic field.

### 2.5 Phase Locked Loop and multiplier

Phase Locked Loop Block consists of PLL IC, LPF(Low Pass Filter) VCO(Voltage Control Oscillator). Reference frequency of PLL is 12.8MHz. The trimmer capacitor(TC3) is used to adjust the pager's local frequency.

$F_i$  = Output frequency of VCO

$F_c$  = channel frequency  
 $F_{if1}$  = 1st immediate frequency = 21.4MHz

The formula of  $F_I$ ,

$$F_I = \frac{(F_c - F_{if1})}{4} \text{ (MHz)}$$

## 2.6 MIXER

The mixer(Q3) makes the first immediate frequency(21.4MHz) by combining a channel frequency via component C18 with the local oscillator frequency via component C44. The output of the mixer is matched to crystal filter(MCF1) with components L6,C22,R7. The 1st IF is transferred to the input of MCF(MCF1). The MCF is used to reject the unwanted carrier and a 15kHz bandpass filter.

The carrier passed via MCF is transferred to a IF amplifier(Q4) and a mixer input(#20, U1).

## 2.7 FSK Receiver IC(U1)

The FSK receiver IC consists of voltage regulator (#17,18), 2nd mixer, data shaper(#14,15), low battery detector(#16), RSSI(#10), 2nd local oscillator(#1,2), quad detector(#8,9) and limiting IF amplifier(#5,6), battery saving(#13).

As external component, there are a ceramic filter(CF1), Discriminator(X2), Audio low pass filter(R14,15,16,C29,30,31) and local crystal(X3).

The battery saving signal(BS) from MCU turns voltage regulator(Q5) on. The voltage regulator supply power to LNA, Mixer and Local oscillator, then the 2<sup>nd</sup> oscillator(X3) works. At this time, output of the 2nd IF mixer is routed through ceramic filter(CF1) and two internal IF amplifier stages. This reduces the unwanted signals and provides better selectivity. The received audio signal(#9, U1) is filtered by the BPF(R14,15,16,C29,30,31), and transferred into the input data of MCU by the built-in data shaper of U1.

## 3. THE PARTS OF DIGITAL BOARD

### 3.1. CODE PLUG MODE

The code plug includes an electrically erasable read-only memory (EEPROM) IC. Pager address codes, functions to which the pager will respond, and pager option(bit rate, character set , etc) are inputted with encoder(programmer).

### 3.2. DC/DC CONVERTOR(U102)

The device generates a boosted 3.0 DC voltage for MCU(U101) and EEPROM(U103).

### 3.3. MCU(U101), LCD

This devices are specially designed CMOS LSI, decodes POCSAG data from FSK receiver IC(U1) and decided whether address of pager on EEPROM is equal or not to address of data from the RF carrier. If address is equal, The MCU wakes up main clock(1MHz), then the MCU is standby mode to receive message. After the MCU receives messages according to sync. clock, gives alert, and then displays messages on LCD screen.

### **3.4. SUPPORT CIRCUIT**

The support circuit consists of a motor driver, buzzer driver, LED lamp driver. If the your pager received messages, the MCU(#44, 43) outputs high('1') for buzzer, low('0') for motor to alert beep or vibrate. Press mode button and then the MCU(#42) outputs low('1') to turn the back-light on. The reset circuit turns on Q104, by connecting your pager to battery. MCU is reset and after short time MCU is set and your pager will be initialized.