THE DISCRIPTION OF CIRCUIT

1. Introduction

The paging receiver has a double loop antenna which enables it to operate at around 7 μ v/m in free space.

The paging receivers are double conversion superheterodyne receivers.

The double conversion IF will contribute to improved selectivity and will consist of a first IF of 21.4MHz and a second IF of 455KHz.

The paging receiver consists of a RF board and a DIGITAL board. The RF board consists of a loop antena, LNA, Mixer, Saw filter, First local osillator, Multiplier, and FSK Reciever IC, The DIGITAL board consists of a MCU, LCD, DC-DC convertor, Eeprom, Buzzer, Motor, RESET CIRCUIT and LED lamp.

2. THE PARTS OF RF B'd

2.1 Loop Antena

The loop antenna plated metal connects to the matching network (C1,2,6,10,17,47, 48,L6,R17,VC1) between antenna and LNA(Q1, Q2).

The matching network is used to tune to the pager's operating frequency by making VC1 variable.

2.2 RF Amplifier(Q1,Q2)

The RF amplifier is a low noise amplifier, consists of the cascade transistors.

The RF signal is coupled through C6 to the input of a LNA(Q1,2) A protective diode D1 becomes forward biased with negative voltage and clamps the discharge to ground. The RF signal is then amplified about 15dB. The amplified signal from Q1,2 is passed through capacitor C4,5.

2.3 Band Pass Fillter(SAW filter)

The band pass filter is used to reject the unwanted signal and to select the wanted channel signal. The capacitor C4,5,11,12 and L4,5 is a maching network to adjust the impedance between a LNA and a SAW filter and Mixer(Q3).

The passed signal via saw filter(SF1) have a 3MHz bandpass and is transfered to the Mixer(Q3).

2.4 AGC

The AGC circuit(Q5) used to control the gain of LNA by the rssi signal of FSK reciever IC(U1), which improved the receive ratio on the other strong electro-magnetic fild.

2.5 Fist local oscillator and multiplier

The oscillator consists of ther third overtone oscillator(Q7) and multiplier(Q8) and accessory components.

The trimer capacitor(VC2) is used to adjust the pager's local frequency.

Fl = local oscillator frequency

Fc = channel frequency

F_{in} = lst intermediate frequency, 21.4MHz

The fomula of Fl,

$$FL = \frac{(Fc - 21.4)}{12} \text{ (MHz)}$$

The multiplier is to emphasize a 12th harmonic frequency by the accessory components, which outputs to the mixer(Q3).

2.6 MIXER

The mixer(Q3) makes the first intermediate frequency(21.4MHz) by combining a channel frequency via component C12 with the local oscillator frequency via component C13. The output of the mixer is mached to crystal filter(F2) with components C14, R22, L7. The lst I.F is transfered to the input of MCF(F2).

The MCF is to used to reject the unwanted carrier and a 15KHz bandpass filter.

The carrier passed via MCF is transfered to a mixer intput(#20, U1).

2.7 FSK Reciever IC(U1)

The FSK reciever IC consists of voltage regulator (#17,18), 2nd mixer, data shaper(#14,15), low battery detector(#16), RSSI(#10), 2nd local oscillator(#1,2), quad detector(#8,9) and limitting if amplifier(#5,6), battery saving(#13).

As external component, there are a ceramic filter(CF1), Discreminator(X3), Audio low pass filter(R19,20,21,C43,44,45) and local crystal(X2).

The battery saving signal(BS) from decoder IC(#1) turns voltage regulator(Q4) on.

The regulutor voltage supply to LNA, Mixer, Local oscillator, then the 2nd oscillator (X1) works, at this time , output of the 2nd IF mixer is routed through ceramic filter(CF1) and two internal IF amplifier stages. This reduces the unwanted signals and provides better selectivity.

The received audio signal(#9, U1) is filtered by the BPF(R19,20,21,C43,44,45), transfered to the data input of MCU(#15) via the built-in data shaper of U1.

3. THE PARTS OF DIGITAL B'd

3.1. CODE PLUG MODE

The code plug includes an electrically erasable read-only memory(EEPROM) IC. It is programmed your pager's address codes, functions to which the pager will respond, and pager option(bit rate, charactor set , etc) by encoder programmer.

3.2. DC DC CONVERTOR(U102)

The device generates a boostered 3.0 dc voltage for MCU(U101), and EEPROM (U103).

3.3. MCU(U101), LCD

These devices are specially designed CMOS LSI, decodes pocsag data from FSK reciever IC(U1) whether is equal or not to address of pager on EEPROM and address of data from the RF carrier. If address is equal, MCU wakes up main clock(1MHz), then the MCU will be a active mode to recieve message. After the MCU recieves messages according to syncronous clock, gives alert, and then displays messages on LCD screen.

3.4. SUPPORT CIRCUIT

The support circuit consists of a Motor driver, Buzzer driver, LED lamp driver.
If the your pager recieved messages , the MCU(#44, 43) outputs high('1) for buzzer, low('0') for motor to alert beep or vibrate, press mode button and then the MCU(#42) outputs low('1') to turn the backlight on.
The reset circuit (Q104) turns on Q104, by connecting your pager to battery. MCU is reset and after short time MCU is set and your pager will be initialized.