DESCRIPTION OF CIRCUITRY

RULE PART NUMBER: 2.983 (d)(10)

THEORY OF OPERATION

1.0 PURPOSE

This report has been prepared to support the application for FCC Type Acceptance PER CODE OF FEDERAL REGULATIONS, TITLE 47, PARTS 2, 90 AND 101 for the transmitter subsystem of the JDT Model 242-3492-XYZ Transceiver. The report presents necessary information concerning electrical circuit description, measured performance and physical construction and configuration.

2.0 DL-3492 TRANSCEIVER

2.1 GENERAL

The main subassemblies of this transceiver include the RF board, and Modem board. The RF board provides frequency modulation and demodulation of the radio frequency signal. The main components of the RF board include the Frequency Synthesizer/VCO, dual conversion superheterodyne receiver, RF exciter/power amplifier, and a Temperature compensated crystal oscillator as a frequency reference. The main components of the modem board include the microprocessor, transmit audio processing circuitry, and receive audio processing circuitry. A block diagram of the transceiver is located at the end of this section in Figure 2.

2.2 TRANSCEIVER CIRCUIT DESCRIPTION

The transmitter produces a nominal RF output power output of 5W at 13.3V DC. Frequency modulation of the transmit signal occurs in the synthesizer. Transmit audio processing circuitry is contained in the modem board.

DRIVER (Q500)

The VCO RF output signal is applied to R846, R847 and R848 that form a resistive splitter for the receive first local oscillator and the transmitter. The VCO signal is then applied to a 50 ohm pad formed by R500, R501, and R502. The RF signal is applied to Q500 which provides amplification and additional isolation between the VCO and transmitter. Biasing for this stage is provided by R503 and L500, C505 provides RF decoupling. The RF signal is then applied to the power amplifier module Q500.

FINAL (U510)

The RF signal from Q500 is applied to the input port of the RF power amplifier module, U510, which provides 5 watts (nominal) at the antenna connector J501. U510 operates on an input voltage from 10-16Vdc.

POWER CONTROL (U130C)

Power control is provided by U520, U130, Q520 and a stripline directional coupler. The power is adjust by Power Set Control R525 which provides a reference voltage to U130C. U130C drives Q520 and PA module U510. The stripline directional coupler is connected to a forward RF peak detector formed by R535, CR520, C531 and U520A. The other end of the stripline directional coupler is connected to a reverse RF peak detector formed by R593, CR592, C593 and U520B.

If the power output of U510 decreases due to temperature variations, etc., the forward peak detector voltage decreases. The detector voltage drop is buffered by U520A and applied to inverting amplifier U130C which increases the forward bias on Q520. The increased bias voltage on Q520 increases the

power output level of U510. If the power output of U510 increases, the forward peak detector voltage increases and U130C decreases the forward bias on Q520. The decreased bias voltage on Q520 decreases the output power of U510. The output of CR520 and CR592 are applied to U520. If the output of either buffer increases, the increase is applied to the inverting input of U130C. The output of U130C then decreases and Q520 decreases the input voltage to U510 to lower the power. The control voltage is isolated from RF by ferrite bead EP513 and C513 decouples RF. The forward/reverse power voltages from U520A/B are also applied to U913/U912 for outputs on J201.

LOW PASS FILTER

The low-pass filter consists of L540, C541, L541, C542, L542, C543, and C544. The filter attenuates spurious frequencies occurring above the transmit frequency band. The transmit signal is then fed through the antenna switch to antenna jack J501.

ANTENNA SWITCH (CR540, CR541)

The antenna switching circuit switches the antenna to the receiver in the receive mode and the transmitter in the transmit mode. In the transmit mode, +9V is applied to L543 and current flows through diode CR540, L544, diode CR541 and R540. When a diode is forward biased, it presents a low impedance to the RF signal; conversely, when it is reverse biased (or not conducting), it presents a high impedance. Therefore, when CR540 is forward biased, the transmit signal has a low-impedance path to the antenna through coupling capacitor C546. L544, and C552 form a discrete quarter- wave line. When CR540 is forward biased, this quarter-wave line is effectively AC grounded on one end by C552. When a quarter-wave line is grounded on one end, the other end presents a high impedance to the quarter-wave frequency. This blocks the transmit signal from the receiver. C545 and C551 matches the antenna to 50 ohms in transmit and receive.

TRANSMITTER KEY-UP CONTROL

Q130, Q131, and Q132 act as switches which turn on with the RX_EN line. When the line goes low Q130 is turned off which turns Q131 on turning Q132 on. This applies 13.3V to U130 before the TX_EN line goes high. U130A/B provides the key-up and key-down conditioning circuit. C116 and R117 provide a ramp up and ramp down of the 9.0TX during key-up and key-down which reduces load pull of the VCO during key-up. The conditioning provides a stable 5.5V output by balancing the 5.5V reference with the 5.5V regulated supply. The output on U130B, pin 7 is applied to comparator U130D, pin 12, the non-inverting input. The output of U130D, pin 14 is applied to the base of current source Q135. The output of Q135 is on the emitter and is applied back to the inverting input of comparator U130D, pin 13. A decrease or increase at U130D, pin 13 causes a correction by U130D to stabilize the 9V transmit output. R140/141 establish the reference voltage on U130D, pin 13. C143 and C144 provide RF decoupling and C145 stabilizes the output. The 9V transmit voltage is then distributed to the circuits.

2.3 POWER SUPPLIES

REGULATED +9.6V

The RF enable signal applied on J201, pin 5 and to the base of Q110 turning the transistor on. This causes the collector to go low and applies a low to the control line of U111, pin 1 and R110 is a pull up resistor. The 13.3V from J201, pin 2 is on U111, pin 6 to produce a +9.6V reference output on U111, pin 4. C120 stabilizes the voltage and C122 provides RF decoupling.

REGULATED +5.5V

The RF enable signal applied on J201, pin 5 and to the base of Q110 turning the transistor on . This causes the collector to go low and applies a low to the control line of U110, pin 1. C904 decouples RF and R131 is a pull up resistor. The 13.3V from J201, pin 2 is on U110, pin 6 to produce a +5.5V regulated output on U110, pin 4. C119 stabilizes the voltage and C115 provides is a bypass capacitor for U110.

2.4 SYNTHESIZER

The synthesizer output signal is produced by the VCO (voltage controlled oscillator). The VCO frequency is controlled by a DC voltage produced by the phase detector in U800. The phase detector senses the phase and frequency of the two input signals and causes the VCO control voltage to increase or decrease if they are not the same. The VCO is then "locked" on frequency.

Programming of the synthesizer provides the data necessary for the internal prescaler and counters. One input signal is the reference frequency. This frequency is produced by the 17.5 MHz reference oscillator (TCXO). The other input signal is the VCO frequency. a block diagram of synthesizer IC is shown at the end of this section.

VOLTAGE-CONTROLLED OSCILLATOR

Oscillator (Q820)

Q820, several capacitors and varactor diodes, and ceramic resonator L826 form the VCO. It oscillates at the transmit frequency in transmit mode and first injection frequency in the receive mode Biasing of Q820 is provided by R823, R824 and R825. An AC voltage divider formed by C844, C845 initiates and maintains oscillation and also matches Q820 to the tank circuit ceramic resonator. L826 is grounded at one end to provide shunt inductance to the tank circuit.

Frequency control

The VCO frequency is controlled by DC voltage across varactor diode CR824. As voltage across a reverse-biased varactor diode increases, its capacitance decreases, Therefore, the VCO frequency increases as the control voltage increases. The control line is isolated from tank circuit RF by choke L825. The amount of frequency change produced by CR824 is controlled by series capacitor C836. The VCO frequency is modulated using a similar method. The transmit audio/data signal from J201, pin 6 is applied across varactor diode CR823 which varies the VCO frequency at an audio rate. Series capacitors C824/C825 set the amount of deviation produced. R821 provides a DC ground on the anodes of CR8222/CR823, and isolation is provided by R820 and C826.The DC voltage across CR823 provides compensation to keep modulation relatively flat over the entire bandwidth of the VCO. This compensation is required because modulation increases as the VCO frequency increases. CR823 also balances the modulation signals applied to the VCO and TCXO.

FREQUENCY MODULATION

Both the VCO and reference oscillator (TCXO) are modulated in order to achieve the required frequency response. If only the VCO was modulated, the phase detector in U800 would sense the frequency change and increase or decrease the VCO control voltage to counteract the change (especially at the lower audio frequencies). If only the reference oscillator frequency is modulated, the VCO frequency would not change fast enough (especially at the higher audio frequencies). Modulating both VCO and reference oscillators produces a flat audio response. Potentiometer R827 sets the VCO modulation sensitivity so that it is equal to the reference oscillator modulation sensitivity.

CASCADE AMPLIFIERS (Q821/Q822)

The output signal on the collector of Q820 is coupled by L861/C864 to buffer amplifier Q821/Q822. This is a shared-bias amplifier which provides amplification and also isolation between the VCO and the stages which follow. The signal is direct coupled from the collector of Q822 to the base of Q821. The resistors in this circuit provide biasing and stabilization.

AMPLIFIER (Q823)

Amplifier Q823 provides amplification and isolation between the VCO and receiver, and transmitter. C851/C861/L832 provides matching between the amplifiers. Bias for Q823 is provided by R840/R842/R843. Inductor L833 and capacitor C863 provide impedance matching on the output.

SUPPLY FILTER (Q845)

Q845 on the RF board is a capacitance multiplier to provide filtering of the 9.6V supply to the VCO. R945 provides transistor bias and C842 provides the capacitance that is multiplied. If a noise pulse or other voltage change appears on the collector, the base voltage does not change significantly because of C845.

VCO BAND SELECT AND T/R FREQUENCY SHIFT (U840)

The VCO must be capable of producing frequencies from 840 to 960 MHz to produce the required receive injection and transmit frequencies. If this large of a shift was achieved by varying the VCO control voltage, the VCO gain would be undesirably high. Therefore, capacitance is switched in and out of the tank circuit to provide a coarse shift in frequency.

The 928 to 960 MHz band is divided into two segments , 928 to 944 MHz and 944 to 960 MHz. The band selection controlled by the shift register U840 and digital transistors Q843, and Q844 and pin diode CR820 on the VCO board.

A frequency shift of 87.85 MHz is required to go from transmit to receive mode and visa versa. Transmit-to-Receive frequency shift is accomplished by programming the shift register U840 which drives the digital transistors Q841 and Q842. In transmit mode, Q841and Q842 forward bias pin diode CR821 which switches in an inductive transmission line in parallel with the VCO resonator causing the VCO frequency to increase. In receive mode, Q841, Q842 reverse bias CR821 which switches out the inductive transmission line and lowers the VCO frequency for the mixer injection.

SYNTHESIZER INTEGRATED CIRCUIT (U800)

Synthesizer chip U800 is shown in Figure 4-2. This device contains the following circuits: R (reference), Fractional-N, NM1 and NM2; phase and lock detectors, prescaler and counter programming circuitry.
Frequencies are selected by programming the R, Fractional-N, NM1 and NM2 in U800 to divide by a certain number. These counters are programmed by Modem board or a user supplied programming circuit. The counter divide numbers are chosen so that when the VCO is oscillating on the correct frequency, the VCO-derived input to the phase detector is the same frequency as the reference oscillator-derived frequency. The VCO frequency is divided by the internal prescaler and the main divider to produce the input to the phase detector.

LOCK DETECT

When the synthesizer is locked on frequency, the SYNTH LOCK output of U800, pin 18 (J201, pin 7) is a high voltage. Then when the synthesizer is unlocked, the output is a low voltage. Lock is defined as a phase difference of less than 1 cycle of the TCXO.

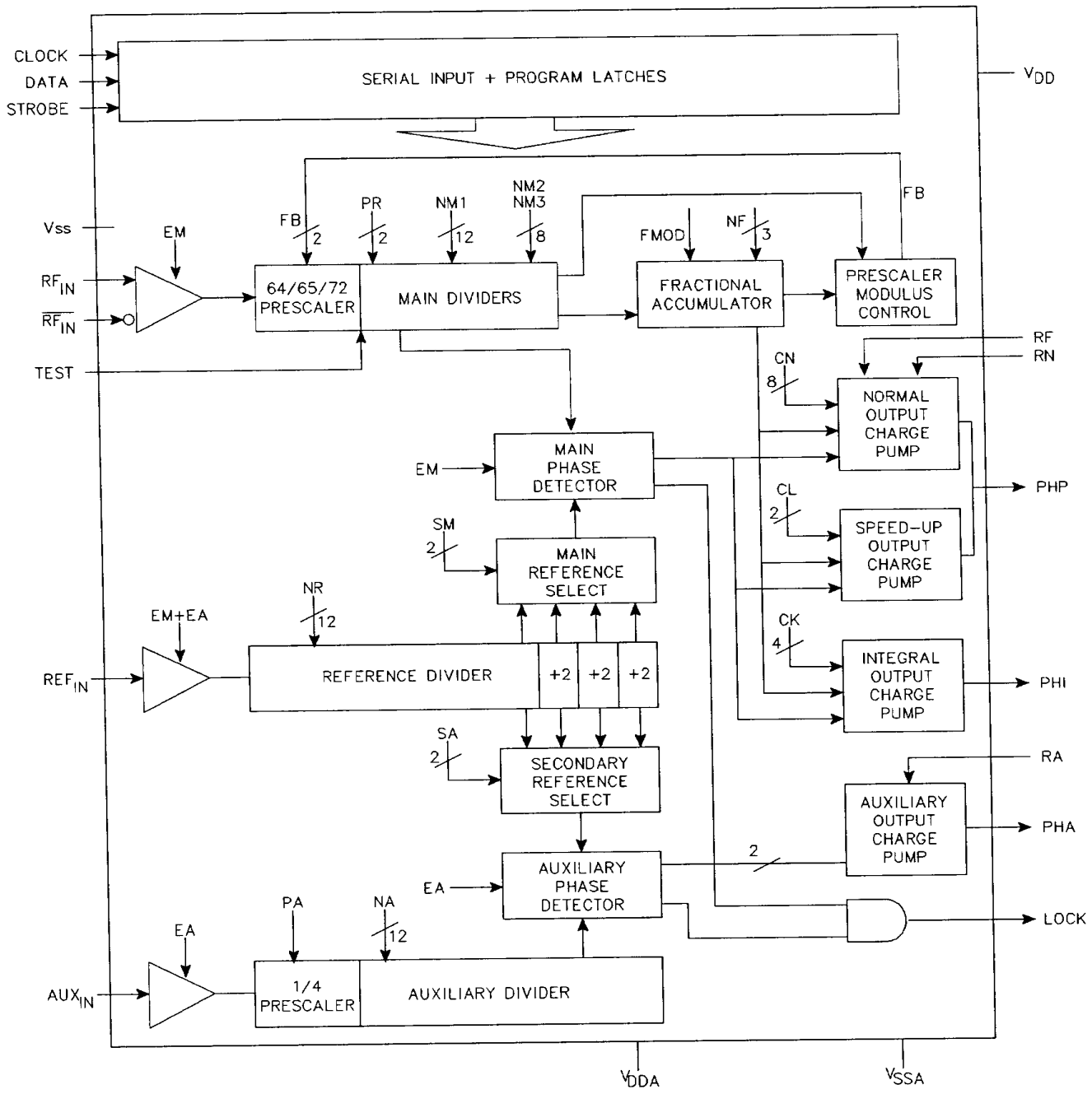

Figure 1: DL-3492 SYNTHESIZER INTEGRATED CIRCUIT (U800)

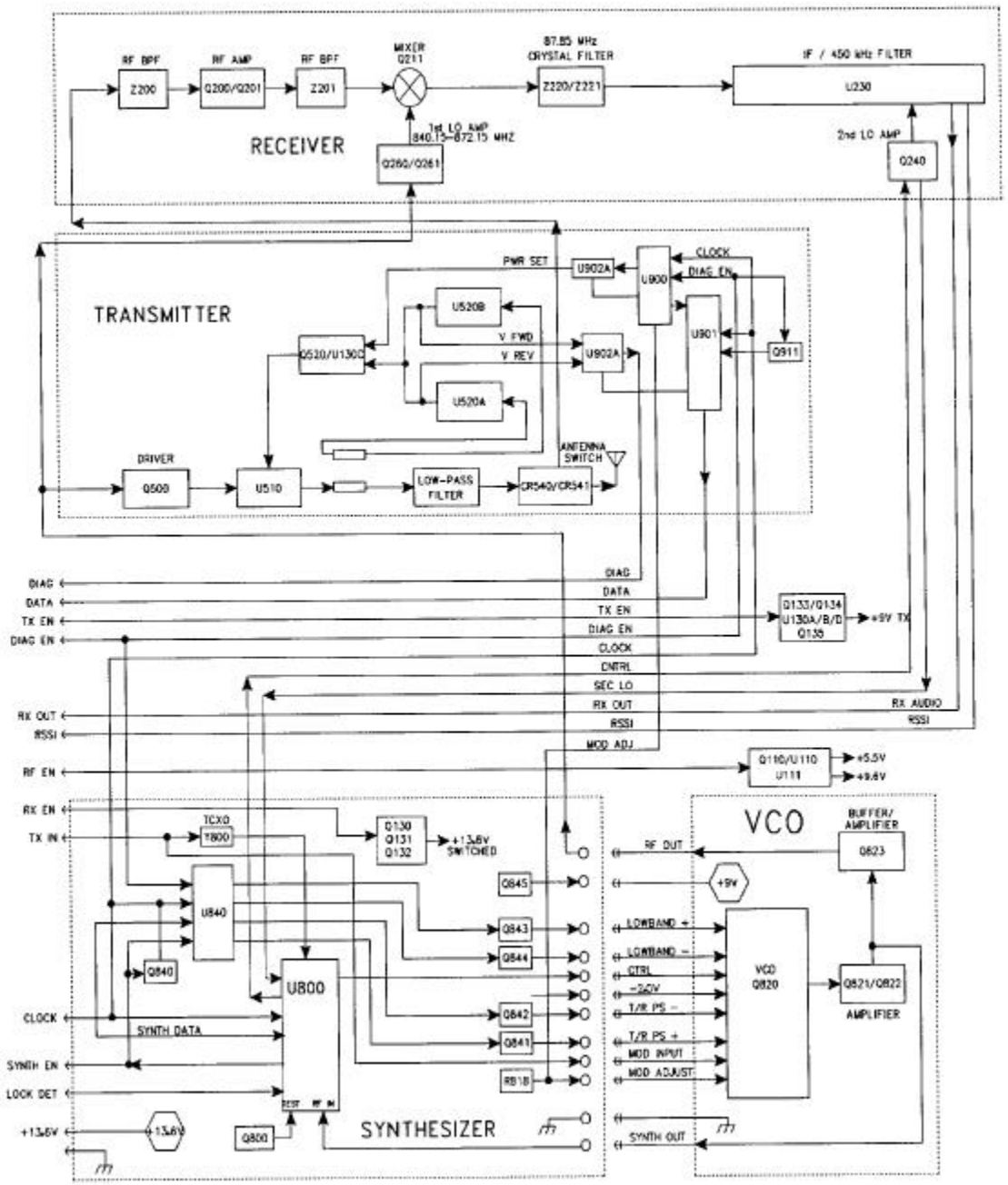

Figure 2: DL-3492 TRANSCEIVER BLOCK DIAGRAM

3.0 HNET MODEM Board Circuit Description

3.1 GENERAL

The Loader/Modem board, Part No. xxx-03280-001, is a plug-in circuit board. The four main functions of the Loader/Modem board include, loading the radio synthesizer, providing the baseband modulating signal for the transmitter and demodulating receive audio signals. The Loader/Modem board is programmed by a personal computer and software. The Loader/Modem board connects to the radio through 14-pin connector P1/J201. User data, programming channels and other operating parameters are provided through a DE-15 connector. A block diagram of the modem is shown at the end of this section.

3.2 TRANSMIT DATA

Transmit Data from the RS-232 port is level-shifted to TTL by U1, then gated through U6 and converted from asynchronous to synchronous format by U2. The CPLD modem, U6 takes the digital data stream and synthesizes to the constant-amplitude analog baseband signal, which is filtered by U12, buffered by U10B then applied to radio module TXA at P1-6.

The modem IC is a CPLD based on a Philips extended Programmable Logic Array (XPLA, PZ5128) which, with a programmable Raise–Cosine filter (U12), operates in DRCMSK[1] mode at 4800, 9600 and 19200 bits/sec. It incorporates a 7-bit hardware scrambler and uses Differential (NRZI) encoding in DRCMSK mode to minimize data pattern-sensitivity. Electronic potentiometer U9B (E-Pot), controlled by CPU U5, is used to set the transmitter deviation by amplitude adjustment of the baseband signal.

3.3 RECEIVE DATA

Received signals are applied to the RXA pin on P1-13 and amplified by U7A, whose gain is set by the electronic potentiometer U9A, then filtered by U12. The same filter circuit is used for transmission and reception: two analog multiplexer/demultiplexer gates (U11 A and B) controlled by TX_EN line are used for sharing. The filter U12 cut-off frequency is programmable by the CPU, based on the data rate. The analog signal is then fed to Peak Detectors U7C and U7D, to the slicer circuit U8C via U7B and U8B. The resulting synchronous bit stream is converted to asynchronous at U2 and shifted to RS-232 levels by U1.

3.4 SYNTHESIZER PROGRAMMING

The CPU programs the RF module synthesizer serially on each Tx/Rx transition. Logic of U1 and U11A/B switch the receive and transmit data path from the modem to the radio and/or the external serial port, under CPU control. The CPU also controls the sync/async converter U2, the filter cut-off frequency, the serial port handshake lines, and the LED indicators via Q1-3.

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[1] DRCMSK = Differential Raise Cosine Minimum Shift Keying

Three channel select inputs, ESD protected by D1, 2,3, in parallel with the on-board DIP switches, are read by the CPU to select the active channel. The fourth DIP switch puts the unit in TEST mode, which sends a test, tone (data rate/4).

3.5 POWER SUPPLIES

The main DC power (13.3V nom.) coming from J1.5, 10 is filtered out for transient and then sent directly to power-up the radio module at P1.2. Voltage Regulator U14 (AVCC) provides 5 V for the receiver RX_5V and analog modem circuitry, while U13 (DVCC) provides 5V for the CPU and other digital logic.

3.6 MISCELLANEOUS FUNCTIONS

U4 generates a power-on reset for the CPU and U3 is a temperature sensor used by the firmware to compensate for variations in RSSI.

The RF module's RSSI output, P1-12, is read by an analog input on the CPU, which implements a squelch threshold in software. Other analog inputs are used to read ambient temperature (used to correct RSSI variations) and various internal voltages (B+_LVL, AVCC, etc.).

The DTR_PGM input, J2-10, puts the CPU in programming mode in which the CPU accepts commands and setup data from the Radio Service Software.

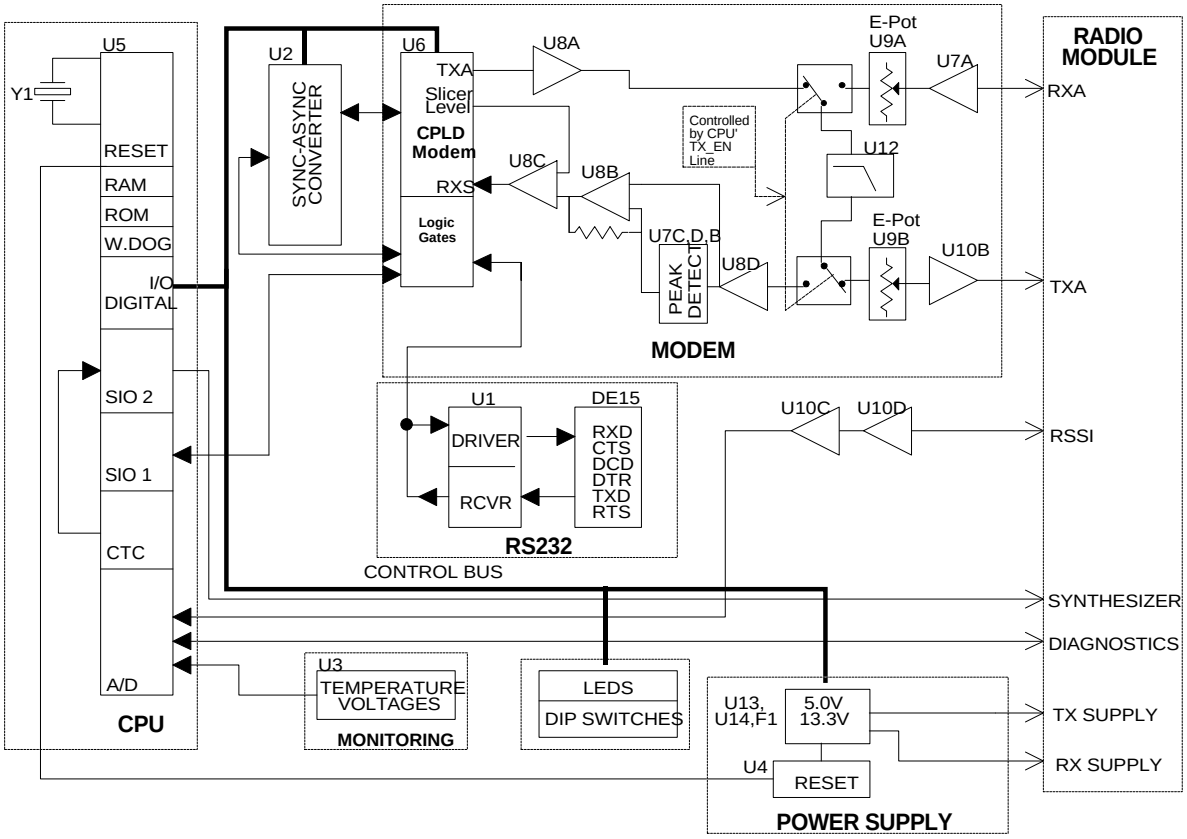

Figure 3: HNET MODEM BLOCK DIAGRAM