Acer NeWeb Corp.

WarpLink 2411 Theory of Operation

Version 1.1

06 March 2001

This document is only applied for Model WARPLINK 2411
of Acer NeWeb Corporation.
Total pages, including this page, of this document are 114 pages.

WarpLink 2411 PC Card Operation Theorem

Introduction:

The Acer NeWeb Corp.(ANC) WarpLink 2411, Wireless LAN PC card, is a complete wireless high speed Network Interface Card (NIC) utilizing the Intersil PRISM II Direct Sequence Spread Spectrum Wireless Transceiver chip set. The chip set is comprised of 5 major ICs:

- 1. HFA3841 Wireless LAN Medium Access Controller utilizes a processor optimized for control of the WLAN protocol.
- 2. HFA3861 Direct Sequence Spread Spectrum Baseband Processor.
- 3. HFA3683 2.4GHz RF/IF Converter and Synthesizer.
- 4. HFA3783 I/Q Modulator/Demodulator and Synthesizer.
- 5. HFA3983 2.4GHz Power Amplifier and Detector.

The detail information refers to attachment-1 to 5 for the datasheet of each devices.

The WarpLink 2411 operates in 2.4GHz ISM Band. The center frequency of transmitted RF signal range in 2412-2462MHz depending on the channel of operation. It is implemented from the IEEE 802.11b standard specification. It uses the CSMA/CA base protocol for media access control and physical layer with direct sequence radio transceiver. Following the IEEE 802.11b standard, it supports 11, 5.5, 2 and 1 Megabit Per Second (Mbps) Data Rates. The PC card is packaged in a PCMCIA Type II extended cover set. For different wireless LAN architectures such as direct communication between PC card and PC card or PC Card's communication via Access Point(AP), there are two network topologies are defined:

-**Infrastructure** is a network architecture for providing communication between wireless clients and wired network resources. The transition of data from the wireless to the wired medium is via an Access Point. The coverage area is defined by an Access Point (AP) and its associated wireless clients, and together all the devices from a Basic Service Set. When an AP is present within a Basic Service Set (BSS), STAs do not communicate on a peer-to-peer basis. Instead, all communications between STAs or between an STA and a wired network client go through the AP.

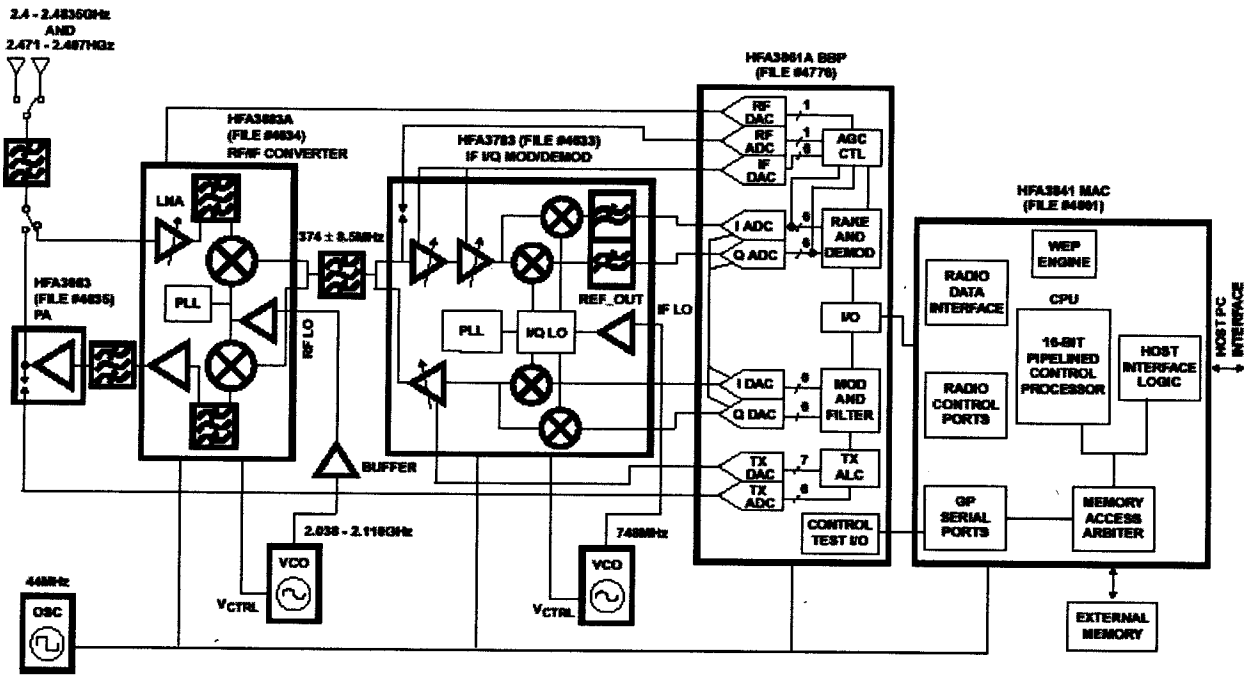
-**Ad-Hoc** network is an architecture that is used to support mutual communication among wireless clients. Typically created spontaneously, an Ad-Hoc network does not support access to wired networks, and an AP is not must to be a part of the network. For the reason, all STAs communicate with each other directly (peer to peer) in an Ad-Hoc network.

In order to compatible with different upper layers, the IEEE 802.11 specification is like the IEEE 802.3 Ethernet and 802.5 Token Ring standards addresses both the Physical (PHY) and Media

Access Control (MAC) layers.

Physical Layer:

The WarpLink 2411 is implemented with the block diagram below.



The spread spectrum transmitter is performed by the function of HFA3861A from Intersil Corp. (formerly Harris Semiconductor) The chip HFA3861A is a Direct Sequence Spread Spectrum Baseband Processor, with datasheet shown in the attachment-2.

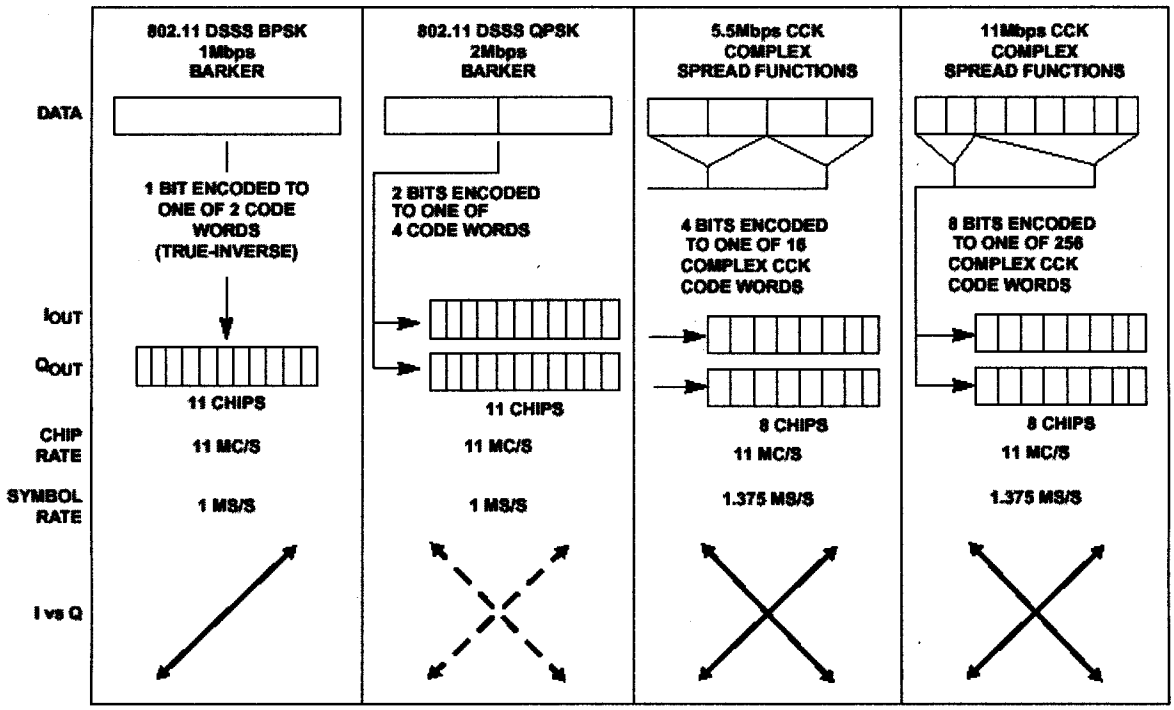


FIGURE 7. MODULATION MODES

In the Figure7 of Attachment-2, and as detail described in Attachment-2, the bit rates are 1Mbps, 2Mbps, 5.5Mbps, and 11Mbps. The corresponding symbol rates are 1MSps, 1MSps, 1.375MSps, and 1.375MSps. The chip rate is always 11MCps, so the ratio of chip rate to symbol rate is 11:1 for the 1Mbps and 2Mbps and 8:1 for the 5.5Mbps and 11Mbps rates. The reason, that symbol rate to bit rate is less than 10 for the 5.5Mbps and 11Mbps, is due to both spread spectrum processing gain and coding gain are utilized. This is reasonable in that they cannot be separated in the demodulation process. For detail of processing gain calculation and test, see the attachment-6.

For transmitter of WarpLink 2411, the data stream is modulated DBPSK and DQPSK along with Complementary Code Keying (CCK) in HFA3861A to provide a variety of data rates. Followed by this IC, the spread spectrum signal is I/Q modulated into IF by HFA3783, IF I/Q Modulator. Then it up-convert into 2.4GHz range by HFA3683, RF/IF Converter, and amplify to a certain limited power level for transmitting.

For receiver, the RF signal travels in the reverse path. The incoming 2.4GHz spread spectrum signal, received by antenna, is down-converted into IF with HFA3683. Then I/Q demodulated into baseband I/Q signals by the function of HFA3783. The receiver portion of the baseband processor, HFA3861A, performs A/D conversion and demodulation of the spread spectrum signal. It correlates the PN spread symbols, then demodulates the DBPSK, DQPSK, or CCK symbols.

Media Access Control Layer:

The IEEE 802.11 MAC layer, supported by an underlying PHY layers, is concerned primarily with rules for accessing the wireless medium. The primarily services provided by the MAC layer are as follow:

-Association

When a client enter the range of a wireless LAN initially, this service enables the establishment of wireless links between wireless clients and APs in Infrastructure Networks.

-Reassociation

This takes place in addition to association when a wireless client moves from one Basic Service Set (BSS) to another. Two adjoining Basic Service Sets form an Extended Service Set (ESS) if they are defined by a common ESSID. If a common ESSID is defined, a wireless client to roam from one area to another. Although reassociation is specified in 802.11, the mechanism that allows AP-to-AP coordination to handle roaming is not specified.

-Authentication

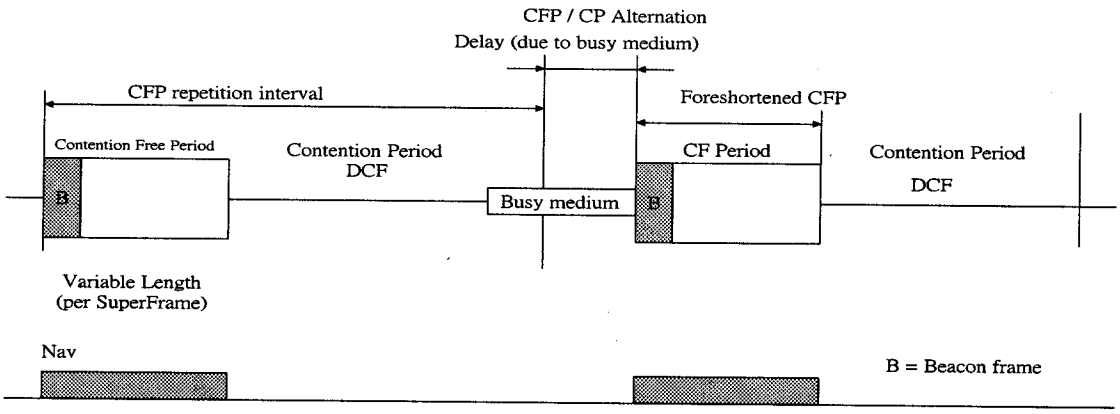
Authentication is the process of proving a client identity, and in IEEE 802.11 this process takes place prior to a wireless client associating with an AP. By default, IEEE 802.11 devices operate in an Open System, where essentially any wireless client can associate with an AP without the checking of credentials. True authentication is possible with the use of the IEEE 802.11 option known as Wired Equivalent Privacy or WEP, where a Shared Key is configured into the AP and its wireless clients. Only those devices with a valid Shared Key will be allowed to be associated to the AP.

-Data transfer

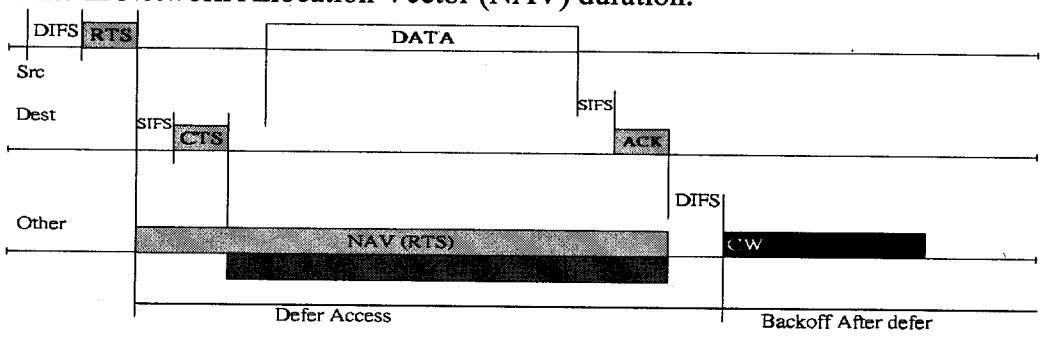
Wireless clients use Distributed Coordination Function (DCF) mode for asynchronous data service and optional Point Coordination Function (PCF) mode for time bounded services. Under DCF mode, each client should follow a Collision Sense Multiple Access with Collision Avoidance (CSMA/CA) algorithm as the media access scheme. AP also have to follow this method under DCF mode. Optional RTS / CTS pair of control frames exchange between transmitter and receiver will reserve the medium for subsequent data access and reduce "Hidden Node" problem. When a wireless LAN operates at PCF mode, the medium is controlled by Point Coordinator (PC, usually is AP) and each pollable client which received a poll frame from PC could use the medium. Hence, Ad-Hoc Network doesn't support PCF Mode.

-Operation Scheme

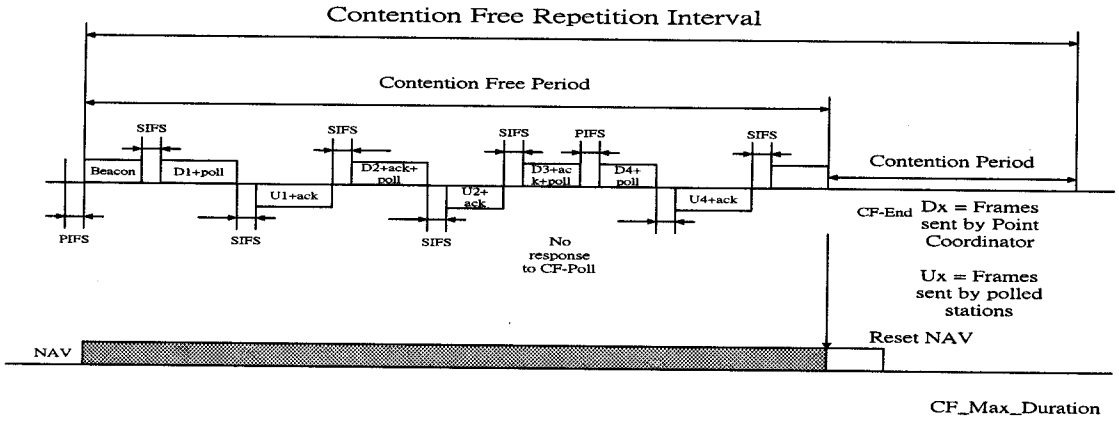
Contention Free Period (CFP) repetition interval consists of DCF and PCF durations and begins at PCF duration if PCF mode was used. The beacon which polls all clients enter PCF mode will be delayed due to the busy medium of last DCF duration.



In a wireless LAN under DCF mode, a client which wins the medium and uses RTS/CTS mechanism, the LAN has the time schedule as follow. Except Src and Dest, all the other clients stay at idle state in Network Allocation Vector (NAV) duration.

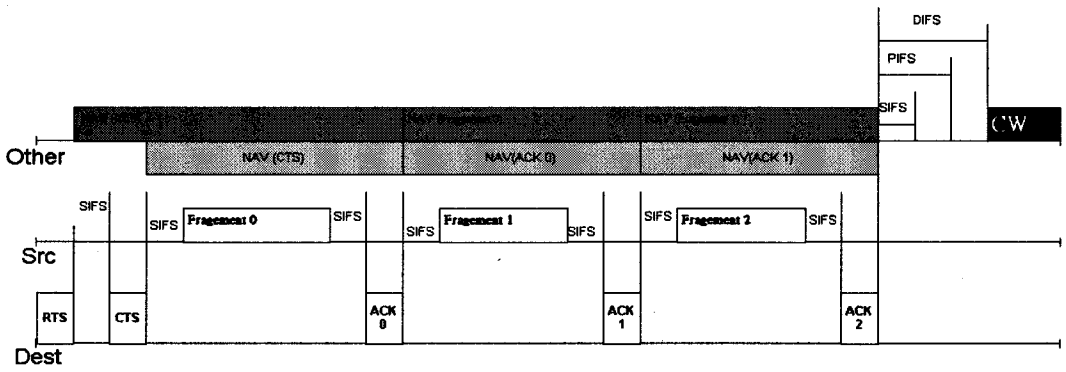


In PCF mode, PC (AP) sends polls to pollable clients according to polling scheme. Some of the poll frames include data inside and a pollable client then transmits a data frame include acknowledge. If PC sends a poll but and doesn't get a ACK frame, it will sends next poll while medium is free over a PIFS duration.



MSDU ordering

A data stream which is from LLC layer and serviced by MAC layer is called MAC Service Data Unit (MSDU). If the data frame is too long, it will be fragmented into several smaller frames. Then these smaller frames will be ordering and packaged as many MAC Package Data Unit (MPDU) individually. MSDU is assembled by these ordering MPDUs. According to the ordering MPDUs, it provide LLC to exchange MAC Service Data Units.



-Security Services by WEP

By default, data is transferred "in the clear" ; any 802.11-compliant device can potentially eavesdrop like-PHY 802.11 traffic that is within range. The WEP option encryption algorithm known as RC4 . The same Shared Key used in authentication is used to encrypt or decrypt the data; thus only wireless clients with the exact Shared Key can correctly decipher the data.

-Power management

IEEE 802.11 defines two power modes, an Active (awake) Mode, where a wireless client is powered to transmit and receive, and Power Save (doze) Mode, where a client is not able to transmit or receive, but consumes less power. Actual power consumption is not defined and is dependent upon the implementation.

Three circumstances arise in which a clients transforms its state from doze to awake: (a) a STA must be in active state for a specific time interval to receive the beacon from AP; (b) AP polls a STA to prepare receiving packets from AP through the TIM/DTIM in a beacon. In addition, the STA must remain in an active state until it receives the packets from AP; and (c) a STA itself wants to transmit packets. In an active state, transmission and reception consume the more power than in an idle state. An idle state occurs while waiting to transmit or receive packets. Transmission generally consumes the most power among all states. In addition, sleepy state consumes the least power of all states.

Attachement-1

Datasheet of HFA3841.

PRELIMINARY | Data Sheet | January 2000 | File Number 4661.2

Wireless LAN Medium Access Controller

The Intersil HFA3841 Wireless LAN Medium Access Controller is part of the PRISM® Enterprise 2.4GHz WLAN chip set. The HFA3841 directly interfaces with the Intersil HFA386x family of Baseband Processors, offering a complete end-to-end chip set solution for wireless LAN products. Protocol and PHY support are implemented in firmware to allow custom protocol and different PHY transceivers.

The HFA3841 is designed to provide maximum performance with minimum power consumption. External pin layout is organized to provide optimal PC board layout to all user interfaces.

Firmware implements the full IEEE 802.11 Wireless LAN MAC protocol. It supports BSS and IBSS operation under DCF, and operation under the optional Point Coordination Function (PCF). Low level protocol functions such as RTS/CTS generation and acknowledgement, fragmentation and de-fragmentation, and automatic beacon monitoring are handed without host intervention. Active scanning is performed autonomously once initiated by host command. Host interface command and status handshakes allow concurrent operations from multi-threaded I/O drivers. Additional firmware functions specific to access point applications are also available.

Designing wireless protocol systems using the HFA3841 is made easier with the availability of evaluation board, firmware, software device drivers, and complete documentation.

Features

- IEEE802.11 Standard Data Rates: 1, 2, 5.5 and 11Mbps
- Part of the Intersil PRISM Wireless LAN Chip Set
- Full Implementation of the MAC Protocol Specified in IEEE Std. 802.11-1999 and the 802.11b Draft Standard
- Host Interface Supports Full 16-Bit Implementation of PC Card 95, also ISA PnP with Additional Chip
- Host Interface Provides Dual Buffer Access Paths
- External Memory Interface Supports up to 4M bytes RAM
- Internal Encryption Engine Executes IEEE802.11 WEP
- Low Power Operation; 25mA Active, 8mA Doze, <1mA Sleep
- Operation at 2.7V to 3.6V Supply
- 3V to 5V Tolerant Input/Outputs
- 128 Pin LQFP Package Targeted for Type II PC Cards
- IEEE802.11 Wireless LAN MAC Protocol Firmware and Microsoft® Windows® Software Drivers

Applications

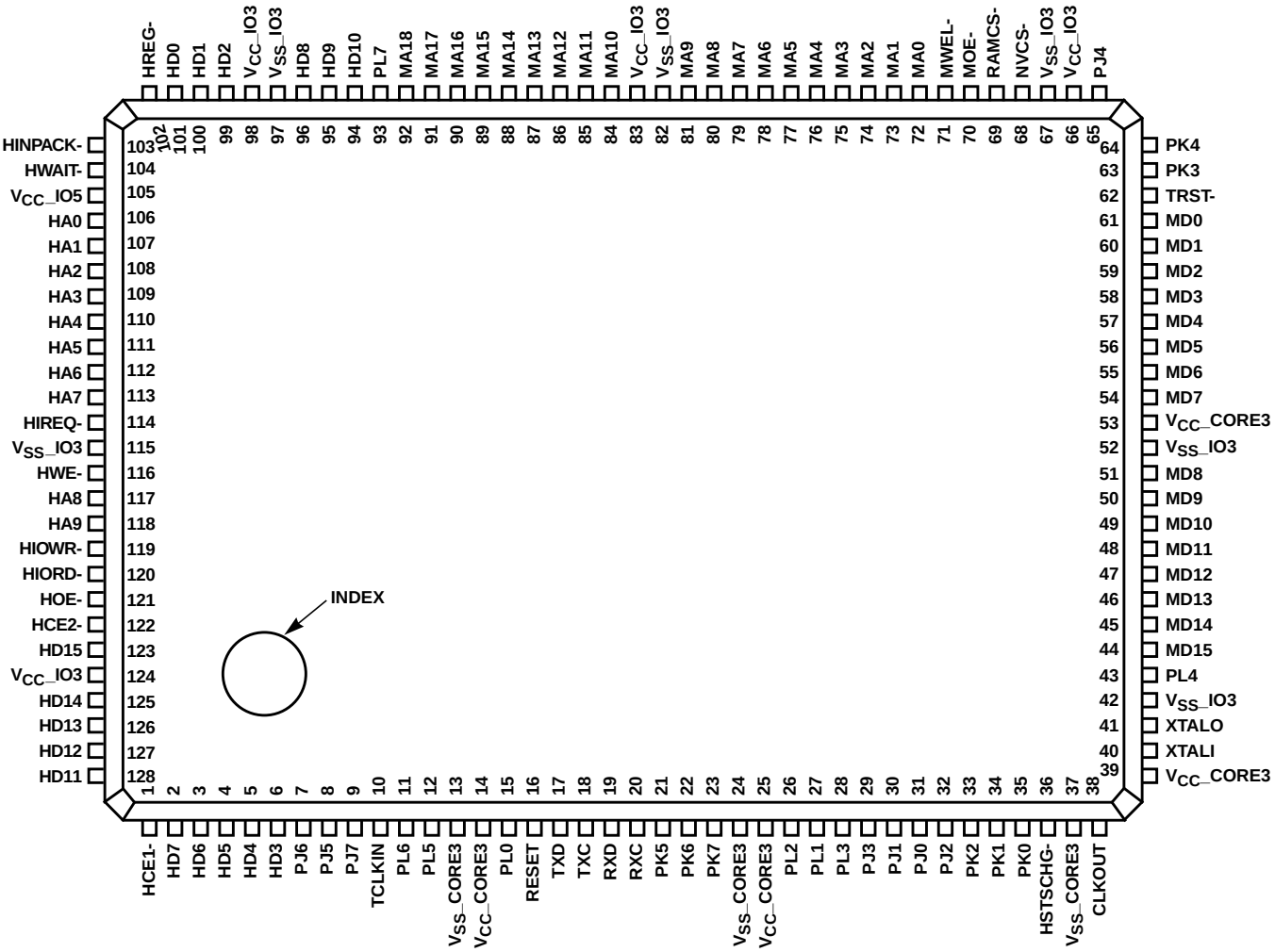
- High Data Rate Wireless LAN
- PC Card Wireless LAN Adapters
- ISA, ISA PnP WLAN Cards
- PCI Wireless LAN Cards (Using Ext. Bridge Chip)
- Wireless LAN Modules
- Wireless LAN Access Points
- Wireless Bridge Products
- Wireless Point-to-Multipoint Systems

Ordering Information

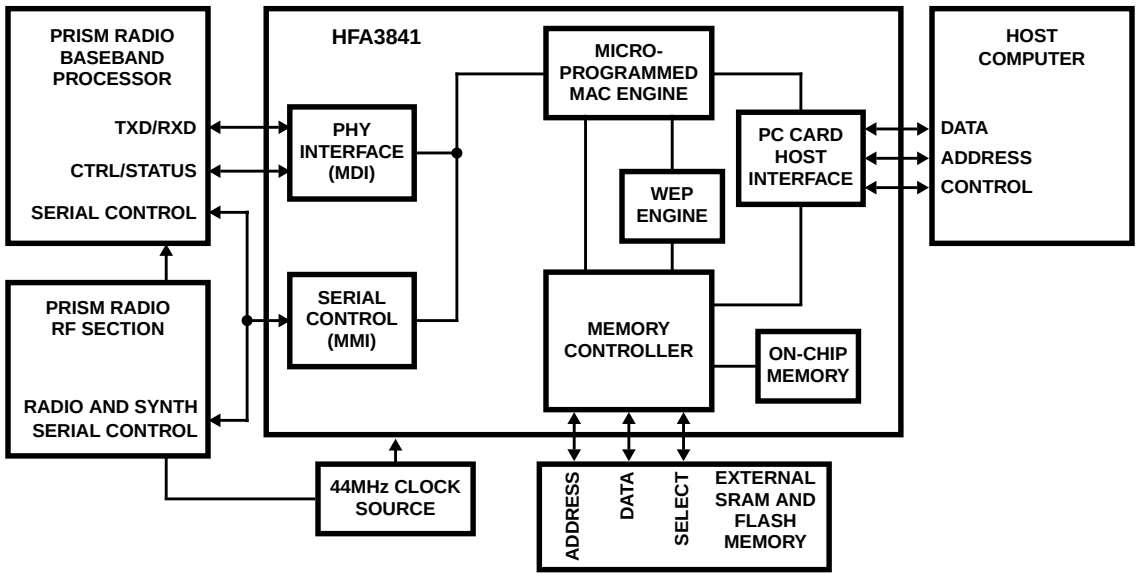
PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE	PKG. NO.
HFA3841CN	0 to 70	128 Ld LQFP	Q128.14x20
HFA3841CN96	0 to 70	Tape and Reel	

CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.

Pinout



Simplified Block Diagram



HFA3841 Pin Descriptions

Host Interface Pins

PIN NAME	PIN NUMBER	PIN I/O TYPE	DESCRIPTION
HA0-9	106-113, 117, 118	5V tol, CMOS, Input, 50K Pull Down	PC Card address input, bits 0 to 9
HCE1-	1	5V tol, CMOS, Input, 50K Pull Up	PC Card card select, low byte
HCE2-	122	5V tol, CMOS, Input, 50K Pull Up	PC Card card select, high byte
HD0-15	101-99, 6-2, 96-94, 128-125, 123	5V tol, BiDir, 2mA, 50K Pull Down	PC Card data bus, bit 0 to 15
HINPACK-	103	CMOS Output, 2mA	PC Card I/O decode confirmation
HIORD-	120	5V tol, CMOS, Input, 50K Pull Up	PC Card I/O space read
HIOWR-	119	5V tol, CMOS, Input, 50K Pull Up	PC Card I/O space write
HRDY/HIREQ-	114	CMOS Output, 4mA	PC Card interrupt request (I/O mode) Card ready (memory mode)
HOE-	121	5V tol, CMOS, Input, 50K Pull Up	PC Card memory attribute space output enable
HREG-	102	5V tol, CMOS, Input, 50K Pull Up	PC Card attribute space select
HRESET	16	5V tol, CMOS, ST Input, 50K Pull Up Hardware Reset	
HSTSCHG-	36	CMOS Output, 4mA	PC Card status change
HWAIT-	104	CMOS Output, 4mA	PC Card not ready (force host wait state)
HWE-	116	5V tol, CMOS Input, 50K Pull Up	PC Card memory attribute space write enable

Memory Interface Pins

PIN NAME	PIN NUMBER	PIN I/O TYPE	DESCRIPTION
MA0 MWEH-	72	CMOS TS Output, 2mA	MBUS address bit 0 (byte) for x8 memory High byte write enable for x16 memory
MA1-18	73-81, 84-92	CMOS TS Output, 2mA	MBUS address bits 1 to 18
PL4	43	CMOS BiDir, 2mA	MBUS address bit 19
PL5	12	CMOS BiDir, 2mA, 50K Pull Up	MBUS address bit 20
PL6	11	CMOS BiDir, 2mA	MBUS address bit 21
MOE-	70	CMOS TS Output, 2mA	Memory output enable
MWEL-	71	CMOS TS Output, 2mA	Low (or only) byte memory write enable
RAMCS-	69	CMOS TS Output, 2mA	RAM select
NVCS-	68	CMOS TS Output, 2mA	NV memory select
MD0-7	61-54	5V tol, CMOS, BiDir, 2mA, 100K Pull Up	MBUS low data byte, bits 0 to 7
MD8-15	51-44	5V tol, CMOS, BiDir, 2mA 50K Pull Down	MBUS high data byte, bits 8 to 15

Radio Interface and General Purpose Port Pins

PIN NAME	PIN NUMBER	PIN I/O TYPE	DESCRIPTION OF FUNCTION (IF OTHER THAN IO PORT)
TXD	17	CMOS Output, 2mA, 50K Pull Down	Transmit data out
TXC	18	5V tol, CMOS, BiDir 2mA, ST	Transmit clock in/out
RXD	19	CMOS Input	Receive data in
RXC	20	CMOS Input, ST	Receive clock in
PJ0	31	CMOS BiDir, 2mA, ST, 50K Pull Down	MMI serial clock in/out
PJ1	30	CMOS BiDir, 2mA, 50K Pull Down	MMI serial data in/out
PJ2	32	CMOS BiDir, 2mA, 50K Pull Down	MMI serial data read/write control, or data output
PJ3	29	CMOS BiDir, 2mA	MMI device enable
PJ4	65	CMOS BiDir, 2mA	
PJ5	8	CMOS BiDir, 2mA, 50K Pull Up	
PJ6	7	CMOS BiDir, 2mA	
PJ7	9	CMOS BiDir, 2mA, 50K Pull Up	
PK0	35	CMOS BiDir, 2mA, ST, 50K Pull Down	
PK1	34	CMOS BiDir, 2mA, 50K Pull Down	
PK2	33	CMOS BiDir, 2mA, 50K Pull Down	
PK3	63	CMOS BiDir, 2mA	
PK4	64	CMOS BiDir, 2mA	
PK5	21	CMOS BiDir, 2mA	MDREADY - PHY or MAC data available (in)
PK6	22	CMOS BiDir, 2mA	Medium busy (CCA from PHY)
PK7	23	CMOS BiDir, 2mA	
PL0	15	CMOS BiDir, 2mA	Transmitter enable
PL1	27	CMOS BiDir, 2mA	Receiver enable (or PHY sleep control)
PL2	26	CMOS BiDir, 2mA	
PL3	28	CMOS BiDir, 2mA	
PL4	43	CMOS BiDir, 2mA	MBUS address bit 19
PL5	12	CMOS BiDir, 2mA, 50K Pull Up MBUS address bit 20	
PL6	11	CMOS BiDir, 2mA	MBUS address bit 21 or PHY control I/O
PL7	93	CMOS BiDir, 2mA	Transmitter ready

Clocks

PIN NAME	PIN NUMBER	PIN I/O TYPE	DESCRIPTION
XTALI	40	CMOS Input, ST	Crystal or external clock input (at >= 2X desired MCLK frequency)
XTALO	41	CMOS Output, 2mA	Crystal output
CLKOUT	38	CMOS, TS Output, 2mA	Clock output (selectable as OSC or MCLK)
TCLKIN	10	CMOS Input, ST, 50K Pull Down	Timebase Reference Clock Input

Power

PIN NAME	PIN NUMBER	PIN I/O TYPE	DESCRIPTION
VCC_CORE3	14, 25, 39, 53	3.3V Core Supply	
VCC_IO3	66, 83, 98. 124	3.3V I/O Supply	
VCC_IO5	105	5V Tolerance Supply	
VSS_CORE3	13, 24, 37	Core V_{SS}	
VSS_IO3	42, 52, 67, 82, 97, 115	I/O V_{SS}	
TRST-	62	CMOS Input	Reserved - Must be tied low through 1K

ST = Schmitt Trigger (Hysteresis), TS = Three-State. Signals ending with “-” are active low.

NOTE: Output pins typically drive to positive voltage rail less 0.1V. Hence with a supply of 2.7V the output will just meet 5V TTL signal levels at rated loads.

Port Pin Uses for PRISM Application

PIN	NAME	PRISM I USE	PRISM II™ USE
20	RXC	RXC - Receive clock	RXC - Receive clock
19	RXD	RXD - Receive data	RXD - Receive data
18	TXC	TXC - Transmit clock	TXC - Transmit clock
17	TXD	TXD - Transmit data	TXD - Transmit data
31	PJ0	SCLK - Clock for the SD serial bus.	SCLK - Clock for the SD serial bus.
30	PJ1	SD - Serial bi-directional data bus	SD - Serial bi-directional data bus
32	PJ2	R/W - An input to the HFA3860A used to change the direction of the SD bus when reading or writing data on the SD bus.	Not Used
29	PJ3	CS - A Chip select for the device to activate the serial control port. (active low)	CS_BAR - Chip select for HFA3861 baseband (active low)
65	PJ4	Not Used	PE1 - Power Enable 1
8	PJ5	SYNTH_LE - Latches a frame of 22 bits after it has been shifted by the SCLK into the synthesizer registers.	LE_IF - Load enable for HFA3783 Quad IF
7	PJ6	LED - Activity indicator	LED - Activity indicator
9	PJ7	Not Used	RADIO_PE - RF power enable
35	PK0	Not Used	LE_RF - Load enable for HFA3983 RF chip
34	PK1	Not Used	SYNTHCLK - Serial clock to front end chips
33	PK2	Not Used	SYNTHDATA - Serial data to front end chips
63	PK3	TX_PE_RF - Power Enable	PA_PE - Transmit PA power enable
64	PK4	RX_PE_RF - Power Enable	PE2 - Power Enable 2
21	PK5	MD_RDY - Header data and data packet are ready to be transferred from Baseband on RXD	MDREADY - Header data and data packet are ready to be transferred from Baseband on RXD
22	PK6	CCA - Signal that the channel is clear to transmit.	CCA - Signal that the channel is clear to transmit.
23	PK7	RADIO_PE - Master power control for the RF section	CAL_EN - Calibration mode enable
15	PL0	TX_PE and PA_PE - Transmit Enable to Baseband	TX_PE - Transmit Enable to Baseband
27	PL1	RX_PE - Receive Enable to Baseband	RX_PE - Receive Enable to Baseband
26	PL2	RESET - Reset to Baseband	RESET_BB - Reset Baseband
28	PL3	Not Used	T/R-SW_BAR - Transient/Receive Control (Inverted)
43	PL4	MA19 (if required)	MA19 (if required)
12	PL5	MA20 (if required)	MA20 (if required)
11	PL6	MA21 (if required)	Reserved
93	PL7	TX_RDY - Baseband ready to receive data on TXD (not used by firmware)	T/R_SW - Transmit/Receive Control

Special Hardware Functions for Port Pins

PJ0	SCK	MMI serial clock in or out	
PJ1	SDO/SDIO	MMI serial data out or I/O	
	MOSI	SPI Master Out/Slave In	Also for MicroWire
PJ2	SDI/MISO	MMI serial data in	Or SPI Master In/Slave Out
	SDDIR	MMI (SDIO) data direction	Low while SDIO is driven as an output
PJ3	SDE0	MMI serial device enable 0	Generally selects PHY controller
	PCS-	SPI/MMI transfer qualifier	Asserted by hardware during transfer
	PHYCS-	PHY chip select (3-3.5MB)	For memory-mapped PHY controllers
PJ4	SDE1	MMI serial device enable 1	For serial EPROM, synthesizer, etc.
	SDDQ	MMI data delivery qualifier	Low for data on SDIO, high for address
	SS-	SPI slave select	In slave mode SCK is serial clock input
PJ5	MREQ-	MBUS request	
PJ6	MGNT-	MBUS grant	
	LED2	LED 2 driver	(Directly from I/O port)
PJ7	LED1	LED 1 driver	(Directly from I/O port)
PK0	GPCK	GP serial port clock in or out	
	UHSIn	Async handshake in	Indicates external async Rx ready
PK1	GPDO	GP serial port data output	
	UTXD	Async transmit data	
PK2	GPDI	GP serial port data input	
	URXD	Async receive data	
PK3	GPDS0	GP device select 0	
	UHSOut	Async handshake out	Indicates GP port async Rx ready
PK4	GPDS1	GP device select 1	
PK5	PDA	PHY (or MAC) data available	Qualifies RXD input to MAC controller
	UWDET	Unique word detected	Output from MAC controller
PK6	MBUSY	Medium busy	CCA status (PHY-dependent source)
	RATE0	Data Rate select 0	
PK7	EDET	Energy (or modulation) detect	
	RATE1	Data Rate select 1	
PL0	TXE	Transmitter enable	
PL1	RXE	Receiver enable	Can drive “awake” LED
	PHYSLP	PHY sleep	(Directly from I/O port)
PL2	PHYRES	PHY reset	(Directly from I/O port)
PL3	SLOT	Slot time reference (in or out)	
	ANTSEL	Antenna select	(Directly from I/O port)
PL4	MA19	MBUS address bit 19	For 1M byte SRAM
	LED0	LED 0 driver	(Directly from I/O port)
PL5	MA20	MBUS address bit 20	For 2M byte SRAM
PL6	MA21	MBUS address bit 21	For 4M byte SRAM
PL7	TXR	Transmitter ready	

Absolute Maximum Ratings

Supply Voltage 4V
Input, Output or I/O Voltage . . . . . .GND -0.5V to V_{CC} +0.5V
ESD Classification . . . . . .Class 2

Operating Conditions

Voltage Range . . . . . .+2.70V to +3.60V
Ambient Temperature Range . . . . . .0^oC to 70^oC

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} ($^oC/W$)
LQFP Package	56

Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Junction Temperature . . . . . .100^oC
Maximum Lead Temperature (Soldering 10s) . . . . . .300^oC
(Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

Maximum test temperature = 100^oC, V_{CC} = 3.0V to 3.3V ±10%, T_A = -40^oC to 85^oC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current	I_{CCOP}	V_{CC} = 3.6V, CLK Frequency 44MHz	-	35	45	mA
Standby Power Supply Current	I_{CCSB}	V_{CC} = Max, Outputs not Loaded	-	0.5	1	mA
Input Leakage Current	I_I	V_{CC} = Max, Input = 0V or V_{CC}	-10	1	10	mA
Output Leakage Current	I_O	V_{CC} = Max, Input = 0V or V_{CC}	-10	1	10	mA
Logical One Input Voltage	V_{IH}	V_{CC} = Max, Min	0.7V_{CC}	-	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = Min, Max	-	-	V_{CC}/3	V
Logical One Output Voltage	V_{OH}	I_{OH} = -1mA, V_{CC} = Min	V_{CC}-0.2	-	-	V
Logical Zero Output Voltage	V_{OL}	I_{OL} = 2mA, V_{CC} = Min	-	0.2	0.2	V
Input Capacitance	C_{IN}	CLK Frequency 1MHz. All measurements referenced to GND. T_A = 25^oC	-	5	10	pF
Output Capacitance	C_{OUT}	CLK Frequency 1MHz. All measurements referenced to GND. T_A = 25^oC	-	5	10	pF

NOTE: All values in this table have not been measured and are only estimates of the performance at this time.

AC Electrical Specifications

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
CLOCK SIGNAL TIMING					
OSC Clock Period (Typ. 44MHz)	t_{CYC}	22	22.7	200	
High Period	t_{H1}	15	11.36	-	
Low Period	t_{L1}	15	11.36	-	
Delay from OSC Edge to MCLK Edge	t_{D1}	-	10	-	
EXTERNAL MEMORY INTERFACE					
Rising Edge MCLK to EMA[15:0], EMCSxN, EMOEN, EMWRN	t_{D1}	0	-	10	ns
Width EMOEN	t_{D2}	2*t_{MCLK} - 10	-	9*t_{MCLK} + 10	ns
EMD[15:0] Read Data Setup	t_{S1}	10	-	-	ns
EMD[15:0] Read Data Hold	t_{H1}	-	-	0	ns
Minimum Width between Read and Write	t_{D3}	t_{MCLK} - 10	t_{MCLK}	t_{MCLK} + 10	ns
Width EMWRN	t_{D4}	2*t_{MCLK} - 10	-	9*t_{MCLK} + 10	ns
EMWRN Rising to EMCSxN Rising	t_{D5}	1*t_{MCLK} - 10	1*t_{MCLK}	1*t_{MCLK} + 10	ns
EMD[15:0] Write Data Hold Time to Rising Edge EMWRN	t_{D6}	1*t_{MCLK} - 10	1*t_{MCLK}	1*t_{MCLK} + 10	ns

AC Electrical Specifications (Continued)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SYNTHESIZER					
SPCLK Period	t_{CYC}	90	-	4,000	ns
SPCLK Width Hi	t_{H1}	$t_{CYC}/2$ - 10	-	$t_{CYC}/2$ + 10	ns
SPCLK Width Lo	t_{L1}	$t_{CYC}/2$ - 10	-	$t_{CYC}/2$ + 10	ns
SYNCLE to Rising Edge SPCLK	t_{D1}	35	-	-	ns
SPDATA Hold Time from Falling Edge of SPCLK	t_{D2}	0	-	-	ns
SPCLK Falling Edge to SYNLE Inactive	t_{D3}	35	-	-	ns
SERIAL PORT - HFA3824A/HFA3860B					
SPCLK Clock Period	t_{CYC}	90ns	-	4µs	
High Period	t_{H1}, t_{L1}	$t_{CYC}/2$ -10	-	$t_{CYC}/2$ + 10	
Delay from Clock Falling Edge to SPCSx, SPAS, SPREAD, SPDATA Outputs	t_{CD}	-	10	-	ns
Setup Time of SPDATA Read to SPCLK Falling Edge	t_{DRS}	15	-	-	ns
Hold Time of SPDATA Read from SPCLK Falling Edge	t_{DRH}	0	-	-	
Hold Time of SPDATA Write from SPCLK Falling Edge	t_{DWH}	0	-	-	
SYSTEM INTERFACE - PC CARD IO READ 16					
Data Delay After SIORDN	t_{DIORD}	-	-	100	ns
Data Hold Following SIORDN	t_{HIORD}	0	-	-	ns
SIORDN Width Time	t_{WIORD}	165	-	-	ns
Address Setup Before SIORDN	t_{SUA}	70	-	-	ns
SCE(1,2)N Setup Before SIORDN	t_{SUCE}	5	-	-	ns
SCE(1,2)N Hold After SIORDN	t_{HCE}	20	-	-	ns
SREGN Setup Before SIORDN	t_{SUREG}	5	-	-	ns
SREGN Hold Following SIORDN	t_{HREG}	0	-	-	ns
SINPACKN Delay Falling from SIORDN	$t_{DFINPACK}$	0	-	45	ns
SINPACKN Delay Rising from SIORDN	$d_{DRINPACK}$	-	-	45	ns
SIOIS16N Delay Falling from Address	$t_{DFIOIS16}$	-	-	35	ns
SIOIS16N Delay Rising from Address	$t_{DRIOIS16}$	-	-	35	ns
SWAITN	t_{DFWT}	-	-	35	ns
Data Delay from SWAITN Rising	t_{DRWT}	-	-	0	ns
SWAITN Width Time	t_{WWT}	-	-	12,000	ns
SYSTEM INTERFACE - PC CARD IO WRITE 16					
Data Setup Before SIOWRN	t_{SUIOWR}	60	-	-	ns
Data Hold Following SIOWRN	t_{HIOWR}	30	-	-	ns
SIOWRN Width Time	t_{WIOWR}	165	-	-	ns
Address Setup Before SIOWRN	t_{SUA}	70	-	-	ns
Address Hold Following SIOWRN	t_{HA}	20	-	-	ns
SCE(1,2)N Setup Before SIOWRN	t_{SUCE}	5	-	-	ns
SCE(1,2)N Hold Following SIOWRN	t_{HCE}	20	-	-	ns
SREGN Setup Before SIOWRN	t_{SUREG}	5	-	-	ns
SREGN Hold Following SIOWRN	t_{HREG}	0	-	-	ns

AC Electrical Specifications (Continued)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS
SIOIS16N Delay Falling from Address	$t_{DFIOIS16}$	-	-	35	ns
SIOIS16N Delay Rising from Address	$t_{DRIOIS16}$	-	-	35	ns
SWAITN Delay Falling from IOWRN	t_{DFWT}	-	-	35	ns
SWAITN Width Time	t_{WWT}	-	-	12,000	ns
SIOWRN High from SWAITN High	t_{DRIOWR}	0	-	-	ns
RADIO TX DATA - TX PATH					
TXC Rising to TXD	t_{DTXD}	-	-	10	ns
TXC Period	t_{TXC}	4* t_{TMCK}	-	-	ns
TXC Width Hi	t_{CHM}	31	-	-	ns
TXC Width Lo	t_{CLM}	31	-	-	ns
MCLK Period	t_{tMCK}	22.7	-	-	ns
TXC Rising to TX_PE2 Deassert (See Note 9)	t_{DTX_PE2}	-	TBD	TBD	ns
TX_RDY Assert Before TXC Rising	t_{TX_RDY}	10	-	-	ns
TX_RDY Hold After TXC Rising (See Note 2)	t_{TX_RDYH}	0	-	-	
RADIO RX DATA - RX PATH					
RX_RDY Setup Time to RXC Positive Edge (See Note 3)	t_{SURX_RDY}	10	-	-	ns
RX_RDY Hold Time from RXC Positive Edge (See Note 4)	t_{HRX_RDY}	45	-	-	ns
RX_PE2 Delay from RX_RDY deAssert (See Note 8)	t_{DRX_PE2}	-	3 * t_{MCLK}	-	ns
RX_PE2 Low Pulse Width (See Note 7)	t_{WRX_PE2}	-	4 * t_{MCLK}	-	ns
RXD Setup Time to RXC Positive Edge (See Note 5)	t_{SURXD}	10	-	-	ns
RXD Hold Time from RXC Positive Edge (See Note 5)	t_{HRXD}	0	-	-	ns
RXC Period (See Note 9)	t_{RXC}	-	3 * t_{MCLK}	-	ns
MCLK Period	t_{MCLK}	22.7	-	-	ns
RXC Width Hi	t_{RCHM}	31	-	-	ns
RXC Width Lo	t_{RCLM}	31	-	-	ns

NOTES:

2. TX_RDY is and'd with TXC_ONE_SHOT to shift data in shift register. However, once the last data bit is put on TXD output pin no further shifting of bits is required. In addition, TX_RDY remains asserted until TX_PE2 is de-asserted which occurs several MAC MCLK's after the last data bit is shifted into the BBP TX_PORT. Therefore, 0ns hold time is required for this signal.
   TX_RDY is used by the BBP to signal that the PLCP header and preamble have been generated and the MAC must provide the MPDU data. TX_RDY will remain asserted until TX_PE2 is deasserted by the MAC.
   TX_PE2 is async to the TX_PORT.
3. MD_RDY is and'd with RXC_ONE_SHOT (RXDAV) to shift data in shift register. RX_RDY is not required to be valid until 1 MCLK after RXC is sampled high. Therefore, a negative setup time could be used. Since this is an unlikely scenario, we will leave it at a nominal 10ns setup time.
4. MD_RDY is and'd with RXC_ONE_SHOT (RXDAV) to shift data in shift register. Therefore, for the last data bit, the MD_RDY must be held active until RXC_ONE_SHOT is sampled high by MAC's MCLK. However, it is assumed that BBP will be used in a mode that keeps RX_RDY (MD_RDY) and RXC running until RX_PE2 is de-asserted. The MAC will stop processing data after the number of bits retrieved from the PLCP header length field are received. THEREFORE, the RX_RDY hold time with respect to RXC does not matter. However, should the RX_RDY signal be cleared when the last RXD bit is received the hold time w/r RXC must be honored.
5. RXC positive edge clocks a flop which stores the RXD for internal usage.
6. RXC period (and Hi/Lo times) must be long enough for flops clocked by MAC MCLK to see 1 RXC high and 1 RXC low. Since RXC can be async to MAC MCLK it is assumed that 3 MCLK periods will suffice.
7. RX_PE inactive width at BBP is 3 BBP MCLK's. Since BBP MCLK and MAC MCLK can be async minimum should be 4 MAC MCLK's.
8. Not yet verified, but seems reasonable. When RX_RDY drops before expected number of RXD bits is received, then Tx/Rx FSM in mpctl.v signals timers which clear rx_pe2_int. More of a functional spec than a timing spec.
9. Need to sample 1 RXC high and 1 RXC low with MAC MCLK.

Waveforms

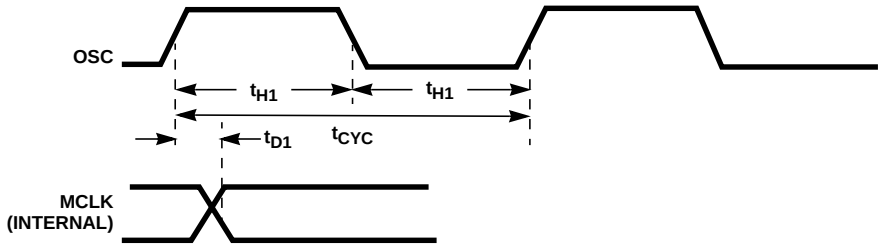
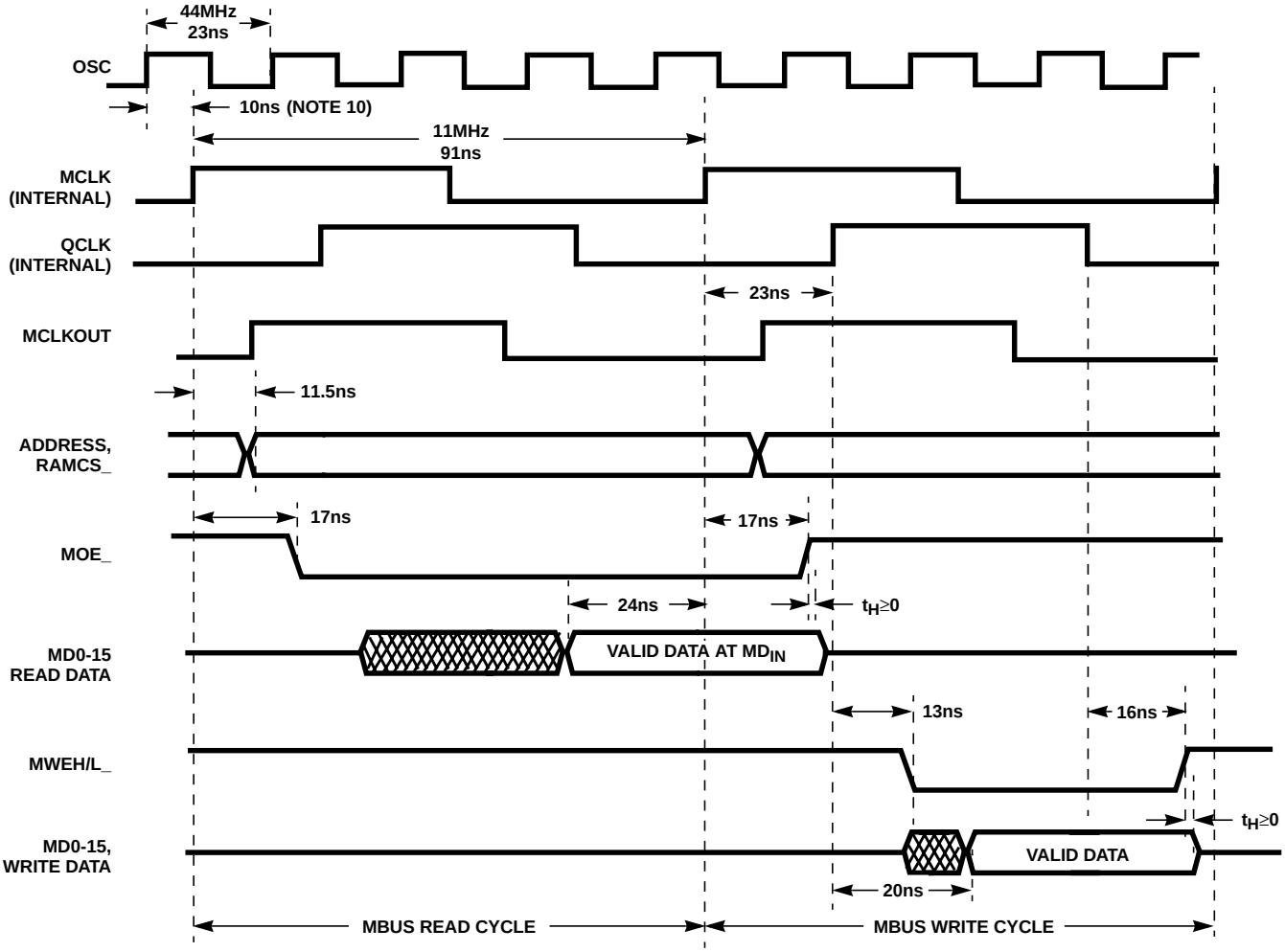


FIGURE 1. CLOCK SIGNAL TIMING

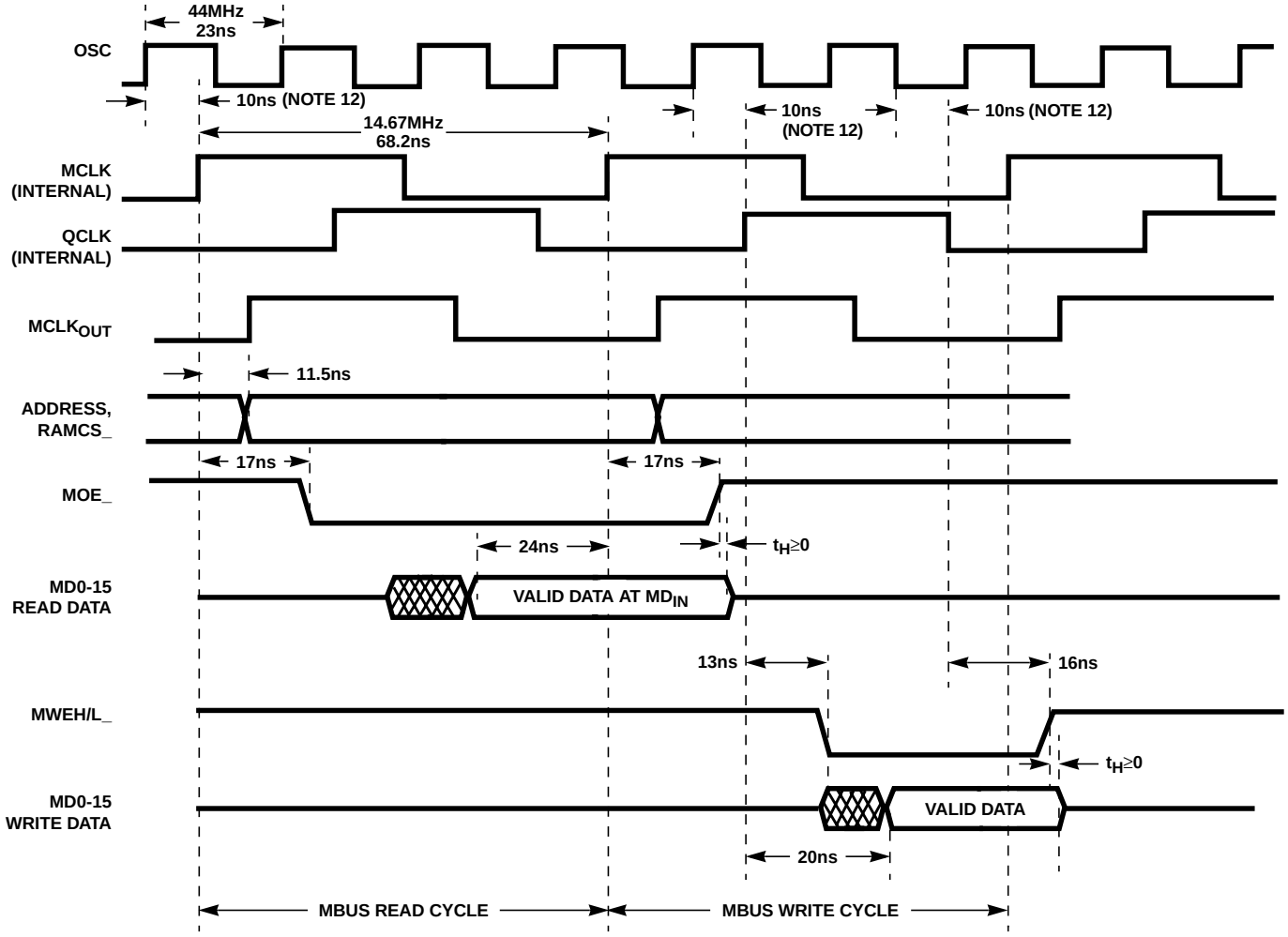


NOTE:

10. Timing delays between OSC and internal clocks are shown for information purposes only.

FIGURE 2. MBUS MEMORY TIMING - 11MHz MCLK

Waveforms (Continued)



NOTES:

11. 14.67MHz requires an odd divisor in the prescaler. Note that both edges of OSC are used to create MCLK and QCLK, thus a deviation from 50% duty cycle in OSC will result in corresponding changes in MBUS timing.

12. Timing delays between OSC and internal clocks are shown for information purposes only.

FIGURE 3. MBUS MEMORY TIMING - 14.67MHz MCLK

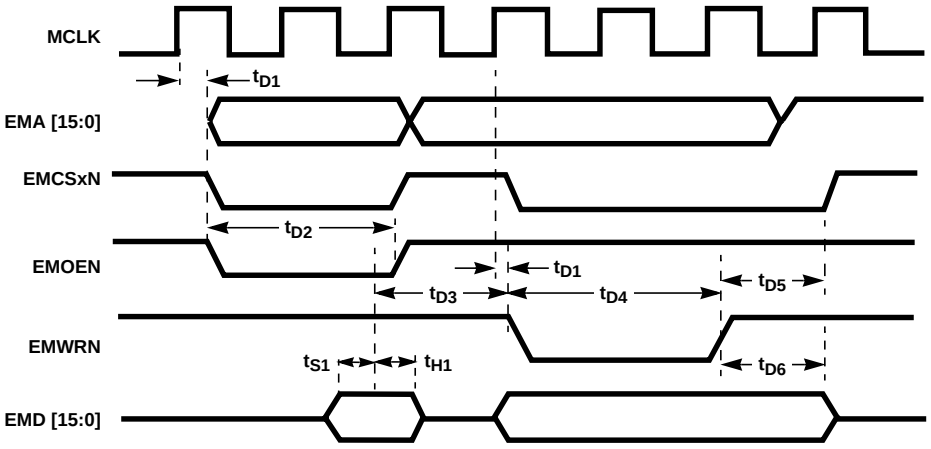


FIGURE 4.

Waveforms (Continued)

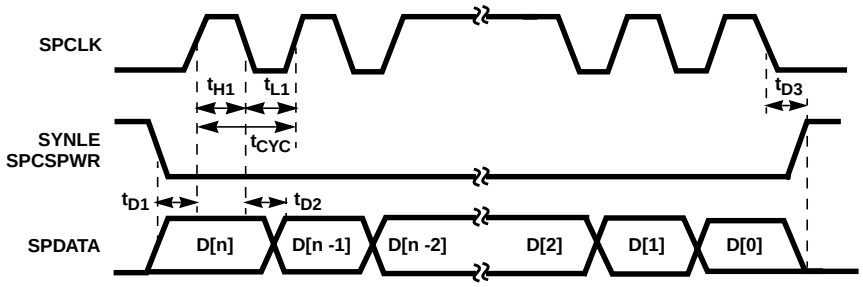


FIGURE 5. SYNTHESIZER

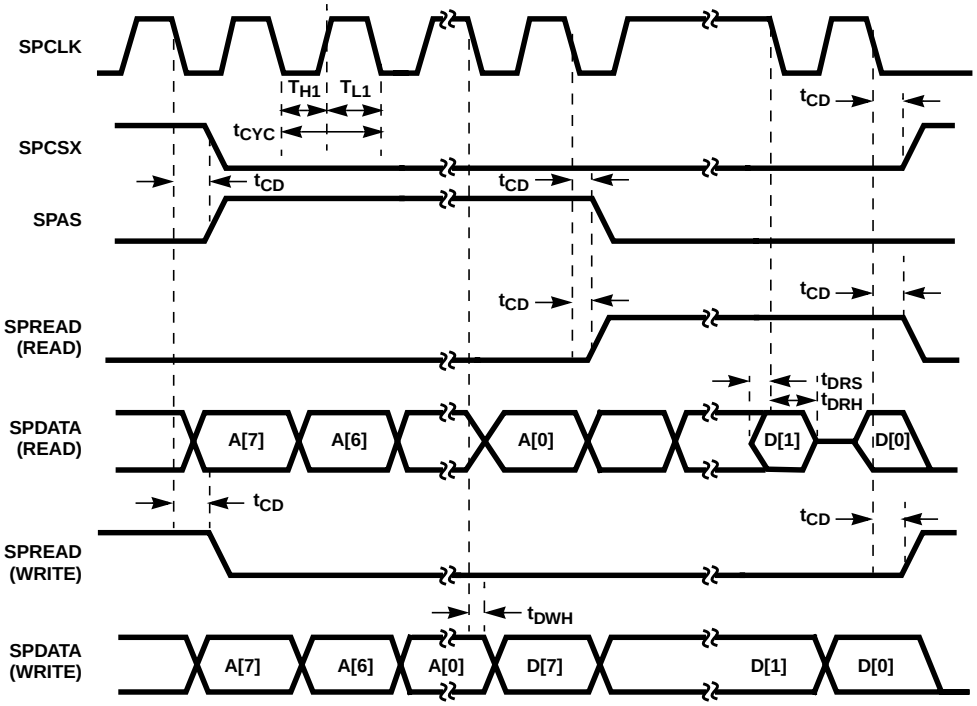


FIGURE 6. SERIAL PORT - HFA3824A/HFA3860B

Waveforms (Continued)

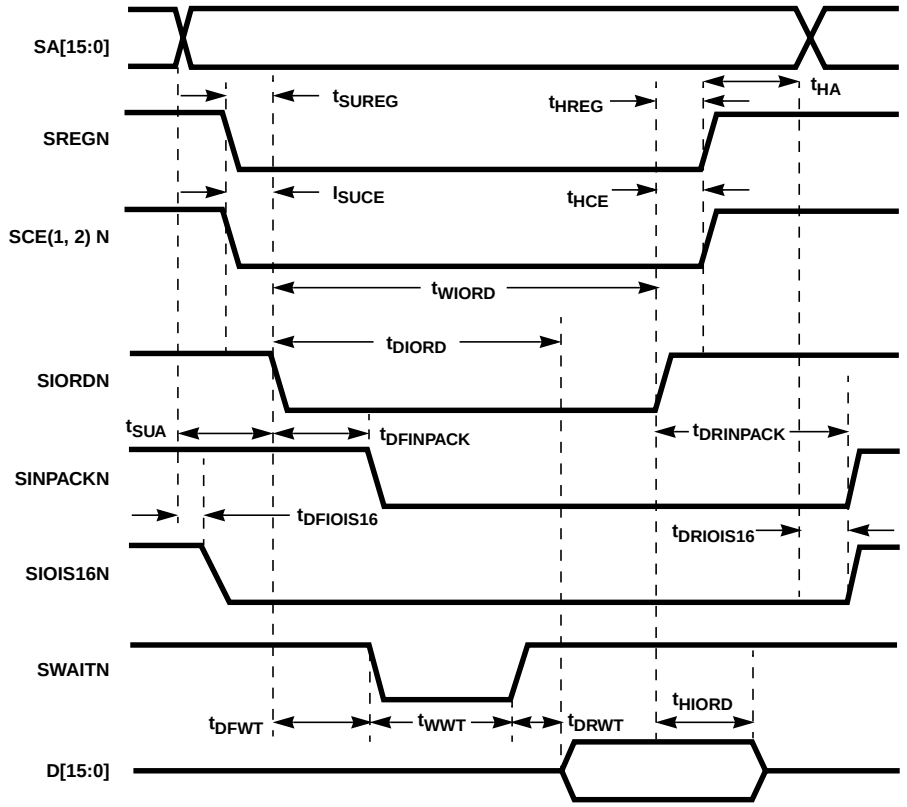


FIGURE 7. PC CARD IO READ 16

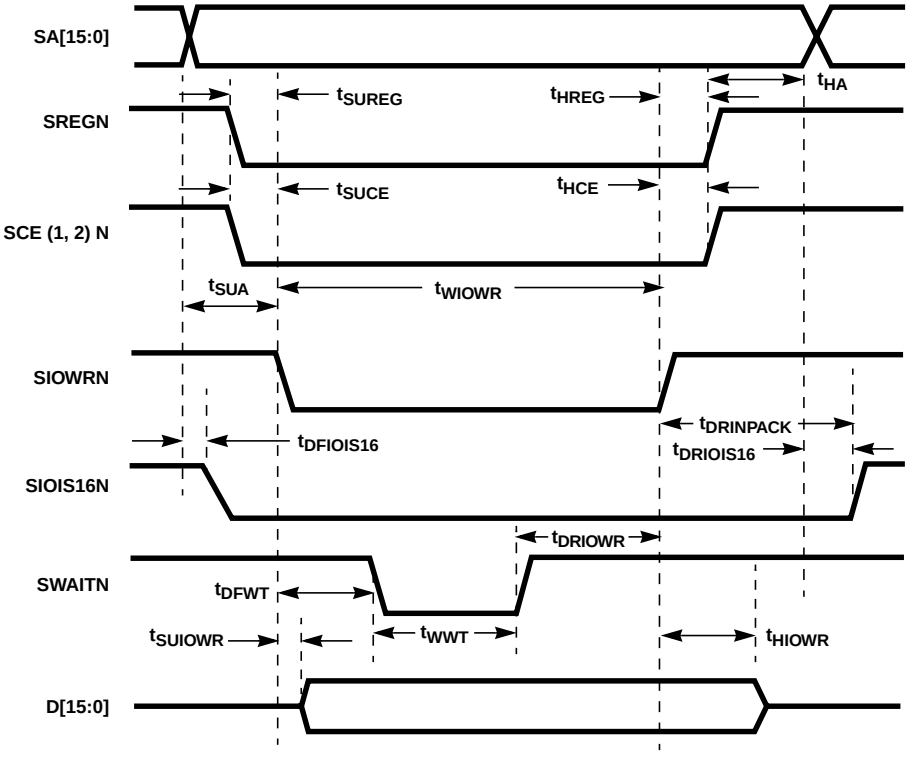


FIGURE 8. PC CARD IO WRITE 16

Waveforms (Continued)

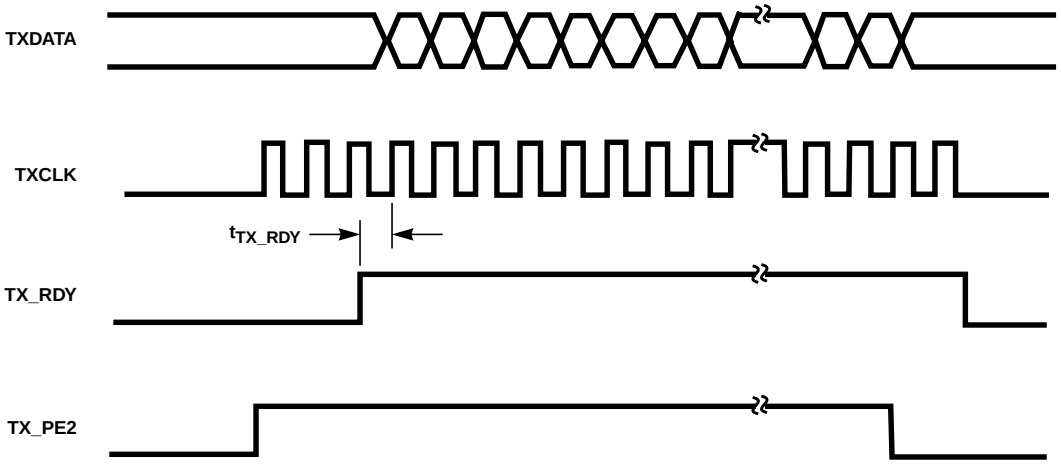


FIGURE 9. TX PATH

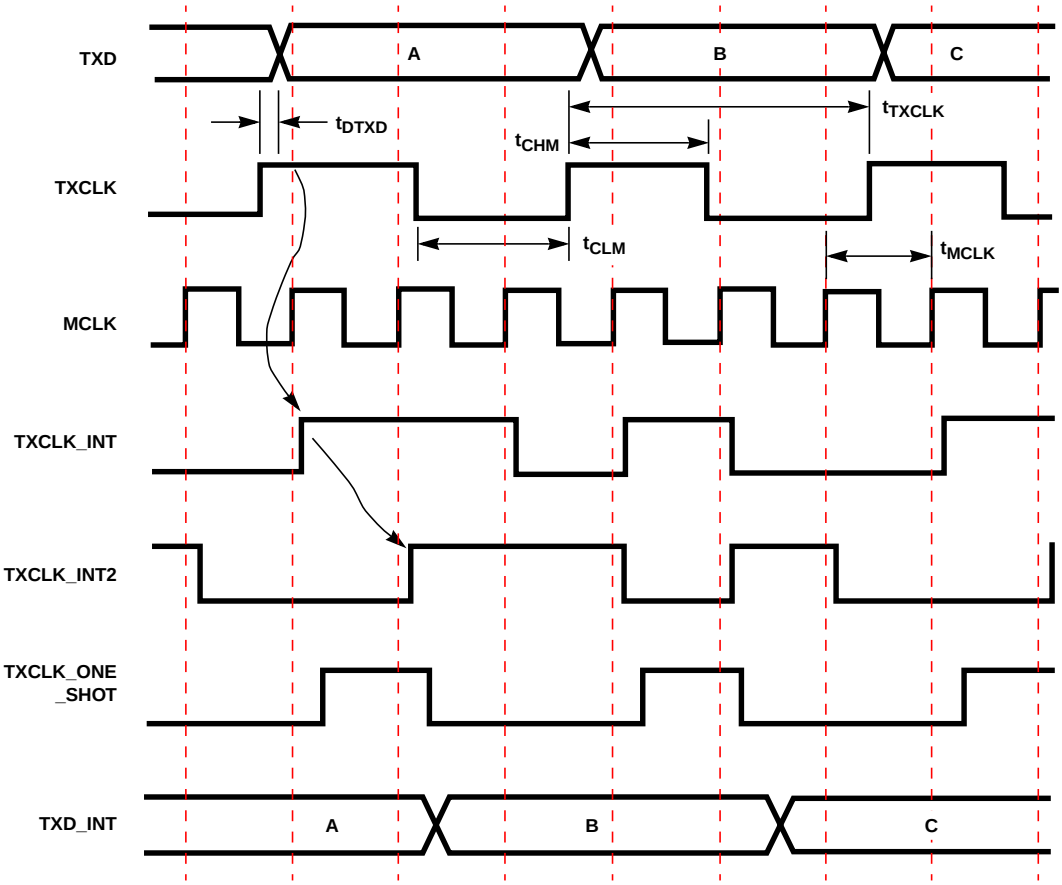


FIGURE 10.

Waveforms (Continued)

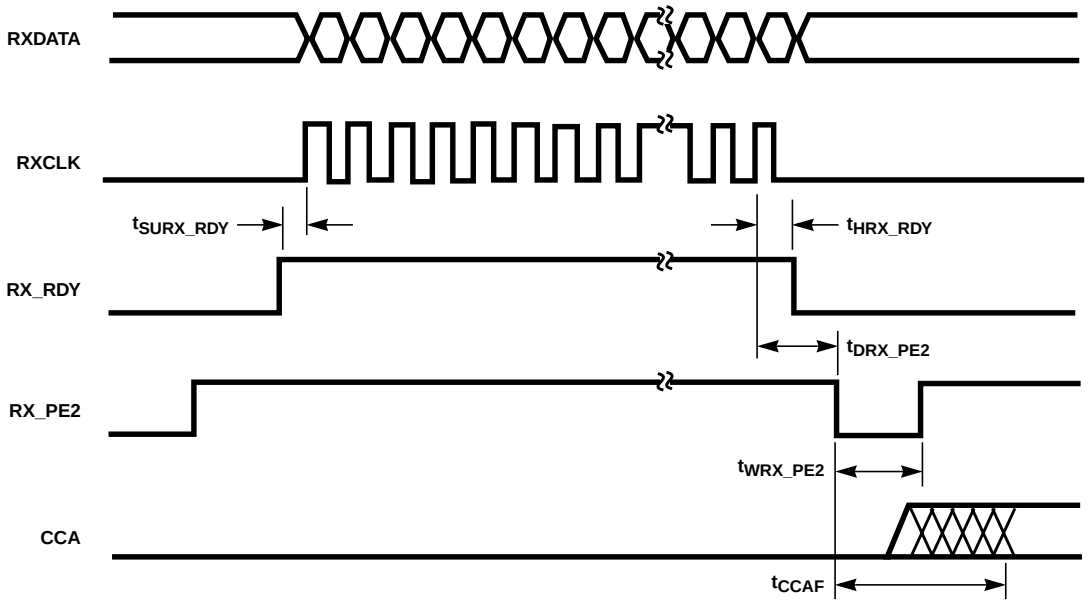


FIGURE 11. RX PATH

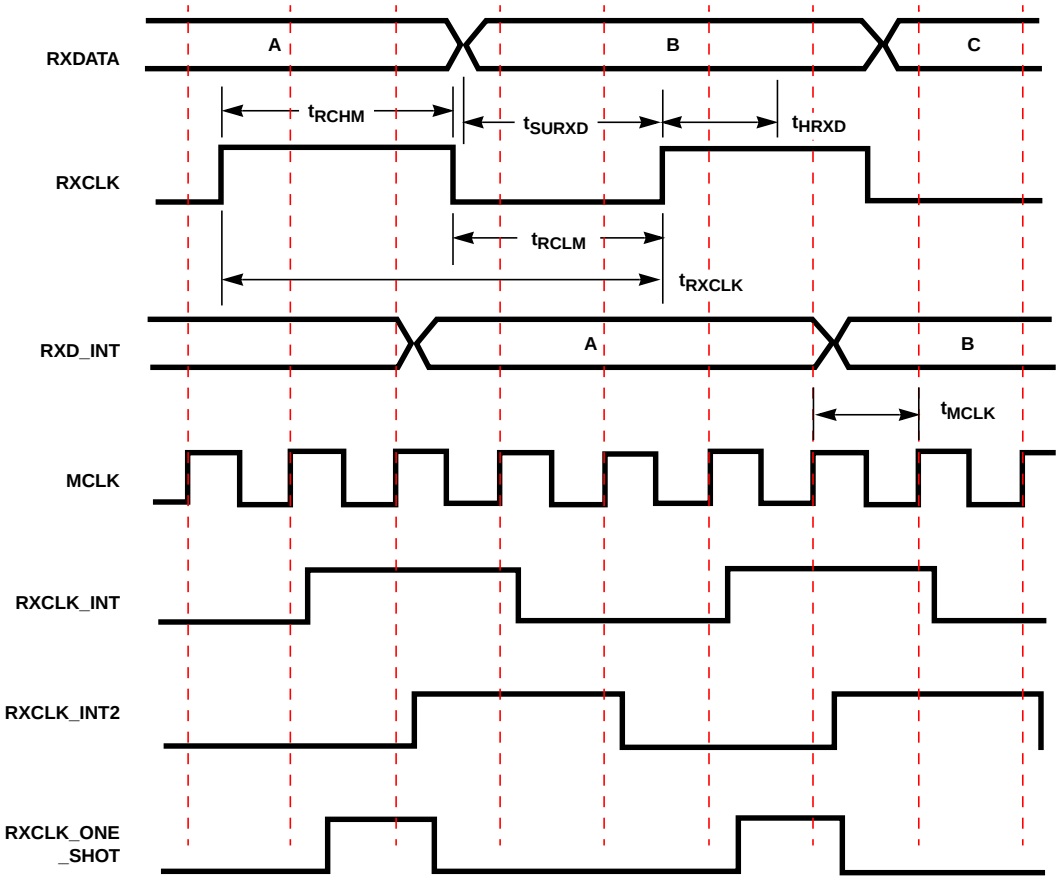


FIGURE 12.

HFA3841 System Overview

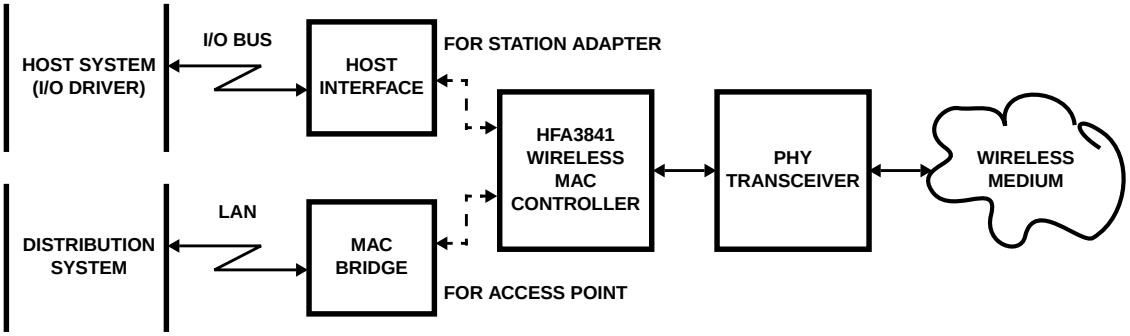


FIGURE 13. TYPICAL APPLICATION

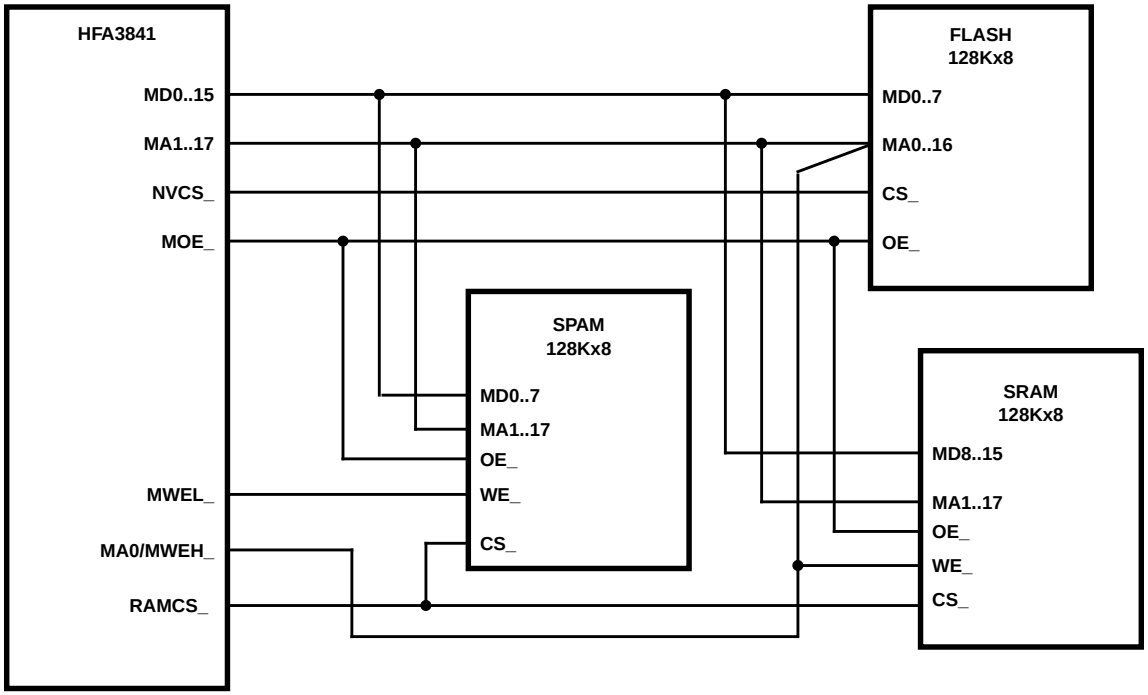


FIGURE 14.

External Memory Interface

An external memory space is provided for firmware and for buffers that are used for temporary storage of received and transmitted frames.

The total memory space is 4M bytes. 64K words are used for control store, where firmware is located. The high data bus has weak pull-up resistors so that external pull-down resistors can set the configuration of the HFA3841 during reset.

NVCS- is the enable to the Flash memory device. Typically the contents of the Flash are copied entirely into SRAM at initialization, and then rarely if ever accessed during normal operation. For this reason, it is acceptable to use low cost, slow Flash devices. During initialization, the clock prescaler is set to produce a longer cycle time while the Flash is accessed. Once all the data has been copied, execution jumps into SRAM and the clock is raised to the normal operating frequency.

It is possible to operate without a Flash device. In such a system, the firmware must be downloaded through the host interface before operation can commence.

The external SRAM memory must be organized in a 16-bit width to provide adequate performance to implement the 802.11 protocol at 11Mb/s rates. Systems designed for lower performance applications may be able to use 8-bit wide memory.

The minimum implementation of external memory consists of 128K bytes of SRAM organized as 64K x 16. Typical applications will use 256K bytes organized as 128K x 16. An access point application could make use of the full address space of the device with 4M bytes organized as 2M x 16.

The HFA3841 was designed to implement 16-bit wide memory by using two 8-bit RAM chips. The HFA3841 provides high and low write enable signals (MWEH_ and MWEL_), and a single output enable (MOE_). This allows a direct connection, enabling a pair of 8-bit SRAMs to function as a 16-bit device. MA0 functions as Address 0 for 8-bit access (such as Flash), and as MWEH (High Byte Write Enable) for 16-bit access (such as SRAM), since address bit 0 is not used for 16-bit accesses.

Some single chip 16-bit SRAMs use an alternate connection scheme with five pins: a Chip Select, an Output Enable, a single Write Enable, and Upper and Lower byte enables, which control both read and write cycles. Thus, external logic is required to generate the required signals.

See Application Note AN9844, "HFA3841 to PRISMII Connections" for important information regarding the connection of these types of 16-bit SRAM chips to the HFA3841.

Host Interface

PC Card Physical Interface

The Host interface is compatible to the PC Card 95 Standard (PCMCIA v2.1). The HFA3841 Host Interface pins connect directly to the correspondingly named pins on the PC Card connector with no external components (other than resistors) required. The HFA3841 operates as an I/O card using less than 64 octet locations. Reads and writes to internal registers and buffer memory are performed by I/O accesses. Attribute memory (256 octets) is provided for the CIS table which is located in external memory. Common memory is not used.

The following describes specific features of various pins:

HA[9:0]

Decoding of the system address space is performed by the HCEx-. During I/O accesses HA[5:0] decode the register. HA[9:6] are ignored when the internal HAMASK register is set to the defaults used by the standard firmware. During attribute memory accesses HA[9:1] are used.

HD[15:0]

The host interface is primarily designed for word accesses, although all byte access modes are fully supported. See HCE1-, HCE2- for a further description. Note that attribute memory is specified for and operates with even bytes accesses only.

HCE1-, HCE2-

The PC Card cycle type and width are controlled with the CE signals. Word and Byte wide accesses are supported, using the combinations of HCE1-, HCE2-, and HA0 as specified in the PC Card standard.

HWE-, HOE-

HOE- and HWE- are only used to access attribute memory. Common Memory, as specified in the PC Card standard, is not used in the HFA3841. HOE- is the strobe that enables an attribute memory read cycle. HWE- is the corresponding strobe for the attribute memory write cycle. The attribute space contains the Card Information Structure (CIS) as well as the Function Configuration Registers (FCR).

HIORD-, HIOWR-

HIORD- and HIOWR- are the enabling strobes for register access cycles to the HFA3841. These cycles can only be performed once the initialization procedure is complete and the HFA3841 has been put into IO mode.

HREG-

This signal must be asserted for I/O or attribute cycles. A cycle with HREG- unasserted will be ignored as the HFA3841 does not support common memory.

HINPACK-

This signal is asserted by the HFA3841 whenever a valid I/O read cycle takes place. A valid cycle is when HCE1-, HCE2-, HREG-, and HIORD- are asserted, once the initialization procedure is complete.

HWAIT-

Wait states are inserted in accesses using HWAIT-. The host interface synchronizes all PC Card cycles to the internal HFA3841 clock. The following wait states should be expected:

Direct Read or Write to Hardware Register

- 1/2 to 1 MCLK assertion of HWAIT- for internal synchronization.

Write to Memory Mapped Register, Buffer Access Path, or Attribute Space (Post-Write)

- The data required for the write cycle will be latched and therefore only the synchronizing wait state will occur.
- Until the queued cycle has actually written to the memory, any subsequent access by the Host will result in a WAIT.

Read to Attribute Space and Memory Mapped Registers

- WAIT will assert until the memory arbitration and access have completed.

Buffer Access Paths, BAP0 and BAP1

- An internal Pre-Read cycle to memory is initiated by a host Buffer Read cycle, after the internal address pointer has auto-incremented. If the next host cycle is a read to the same buffer, the data will be available without a memory arbitration delay.
- A single register holds the pre-read data. Thus, any read access to any other memory-mapped register (or the other

buffer access path) will result in the pre-read data becoming invalidated.

- If another read cycle has invalidated the pre-read, then a memory arbitration delay will occur on the next buffer access path read cycle.

HIREQ-

Immediately after reset, the HIREQ- signal serves as the RDY/BSY (per the PC Card standard). Once the HFA3841 firmware initialization procedure is complete, HIREQ- is configured to operate as the interrupt to the PC Card socket controller. Both Level Mode and Pulse Mode interrupts are supported. By default, Level mode interrupts are used, so the interrupt source must be specifically acknowledged or disabled before the interrupt will be removed.

HRESET

When reset is removed, the CIS table is initialized and, once complete, HIREQ- is set high (HIREQ- acts as RDY/BSY from reset and is set high to indicate the card is ready for use). The CIS table resides in Flash memory and is copied to RAM during firmware initialization. The host system can then initialize the card by reading the CIS information and writing to the configuration register.

ISA PnP

The HFA3841 can be connected to the ISA bus and operate in a Plug and Play environment with an additional chip such as the Fujitsu MB86703, Texas Instruments TL16PNP200A, or Fairchild Semiconductor NM95MS15. See the Application Note AN9874, "ISA Plug and Play with the HFA3841" for more details.

Register Interface

The logical view of the HFA3841 from the host is a block of 32 word wide registers. These appear in IO space starting at the base address determined by the socket controller. There are three types of registers.

HARDWARE REGISTERS (HW)

- 1 to 1 correspondence between addresses and registers.
- No memory arbitration delay, data transfer directly to/from registers.
- AUX base and offset are write-only, to set up access through AUX data port.
- Note: All register cycles, including hardware registers, incur a short wait state on the PC Card bus to insure the host cycle is synchronized with the HFA3841's internal MCLK.

MEMORY MAPPED REGISTERS IN DATA RAM (MM)

- 1 to 1 correspondence.
- Requires memory arbitration, since registers are actually locations in HFA3841 memory.
- Attribute memory access is mapped into RAM as Base-address + 0x400.
- AUX port provides host access to any location in HFA3841 RAM (reserved).

BUFFER ACCESS PATH (BAP)

- No 1 to 1 correspondence between register address and memory address (due to indirect access through buffer address pointer registers).
- Auto increment of pointer registers after each access.
- Require memory arbitration since buffers are located in HFA3841 memory.
- Buffer access may incur additional delay for Hardware Buffer Chaining.

I/O OFFSET	NAME	TYPE
00	Command	MM
02	Param0	MM
04	Param1	MM
06	Param2	MM
08	Status	MM
0A	Resp0	MM
0C	Resp1	MM
0E	Resp2	MM
10	InfoFID	MM
20	RxFID	MM
22	AllocFID	MM
24	TxComplFID	MM
18	BAP Select0	MM
1C	BAP Offset0	MM
36	BAP Data0	BAP
1A	BAP Select1	MM
1E	BAP Offset1	MM
38	BAP Data1	BAP
30	EvStat	HW
32	IntEn	HW
34	EvAck	HW
14	Control	MM
28	SwSupport0	MM
2A	SwSupport1	MM
2C	SwSupport2	MM
3A	AuxBase	HW
3C	AuxOffset	HW
3E	AuxData	(reserved)

Buffer Access Paths

The HFA3841 has two independent buffer access paths, which permits concurrent read and write transfers. The firmware provides dynamic memory allocation between Transmit and Receive, allowing efficient memory utilization. On-the-fly allocation of (128-byte) memory blocks as needed for reception wastes minimal space when receiving fragments. The HFA3841 hides management of free memory from the driver, and allows fast response and minimum data copying for low latency. The firmware provides direct access to TX and RX buffers based on Frame ID (FID). This facilitates Power Management queuing, and allows dynamic fragmentation and defragmentation by controller. Simple Allocate/Deallocate commands insure low host CPU overhead for memory management.

Hardware buffer chaining provides high performance while reading and writing buffers. Data is transferred between the host driver and the HFA3841 by writing or reading a single register location (The Buffer Access Path, or BAP). Each access increments the address in the buffer memory. Internally, the firmware allocates blocks of memory as needed to provide the requested buffer size. These blocks may not be contiguous, but the firmware builds a linked list of pointers between them. When the host driver is transferring data through a buffer access path and reaches the end of a physical memory block, hardware in the host interface follows the linked list so that the buffer access path points to the beginning of the next memory block. This process is completely transparent to the host driver, which simply writes or reads all buffer data to the same register. If the host driver attempts to access beyond the end of the allocated buffer, subsequent writes are ignored, and reads will be undefined.

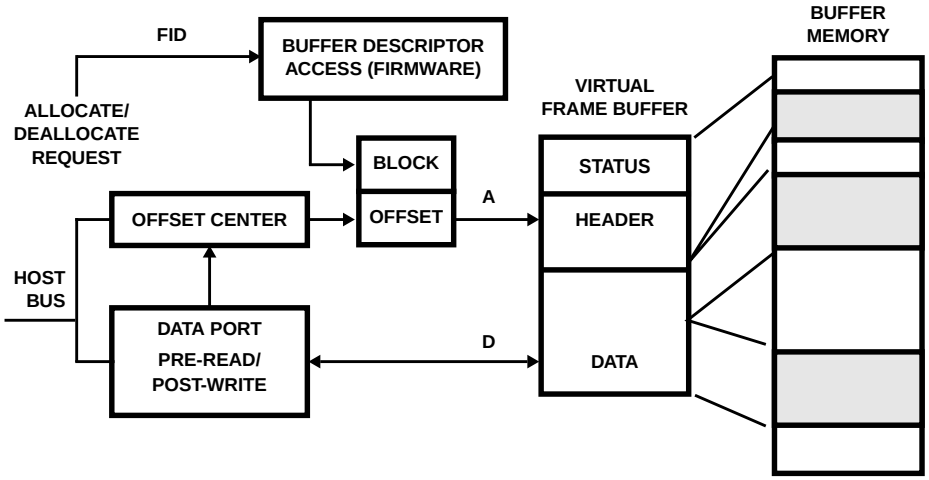


FIGURE 15. BLOCK DIAGRAM OF A BUFFER ACCESS PATH

PHY Interface

The HFA3841 is intended to support the PRISM family of Baseband processors with no additional components. This family currently includes the HFA3860B and HFA3861 DSSS baseband processors and the other ICs in the PRISM WLAN chip set. (Other baseband processors may be supported with custom firmware. See your sales representative for more information). The HFA3841 interfaces to the HFA386X baseband processors through two serial interfaces. The Modem Management Interface (MMI) is used to read and write internal registers in the baseband processor and access per-packet PLCP information. The Modem Data Interface (MDI) provides the receive and transmit data paths which transfer the actual MPDU data.

Serial Control Port (MMI)

The HFA3841 has a serial port that is used to program the baseband processor. There are individual chip selects and shared clock and data lines.

The MMI is used to program the registers and functionality of the PHY baseband processor.

PHY BASEBAND PROCESSOR

The PHY baseband processor is programmed by HFA3841 firmware.

The PRISM II baseband processor mode works as follows:

The Control Port consists of 4 signals: SD (serial data), SCLK (serial clock), R/W (read/write) and CS_BAR (active-low chip select).

Control Port signaling for read and write operations is illustrated in Figures 16 and 17 respectively. Detailed timing relationships appear in Figure 18 and timing specifications are contained in Table 1.

The BBP always uses the rising edge when clocking data on the Control Port. This means that when the BBP is receiving data it uses the rising edge of clock to sample; when driving data, transitions occur on the rising edge.

Address bits 6 through 1 are significant for selecting configuration registers. Address bits 7 and 0 are unused. See the BBP Programming section for register addresses and suggested values.

For read operations, the rising edge of R/W must occur after the 7th but prior to the 8th rising edge of SCLK. This ensures that the first data bit is clocked out of the BBP prior to the edge used to clock it into the MAC.

For more detailed information on the Control Port and BBP register programming see the HFA386x data sheets.

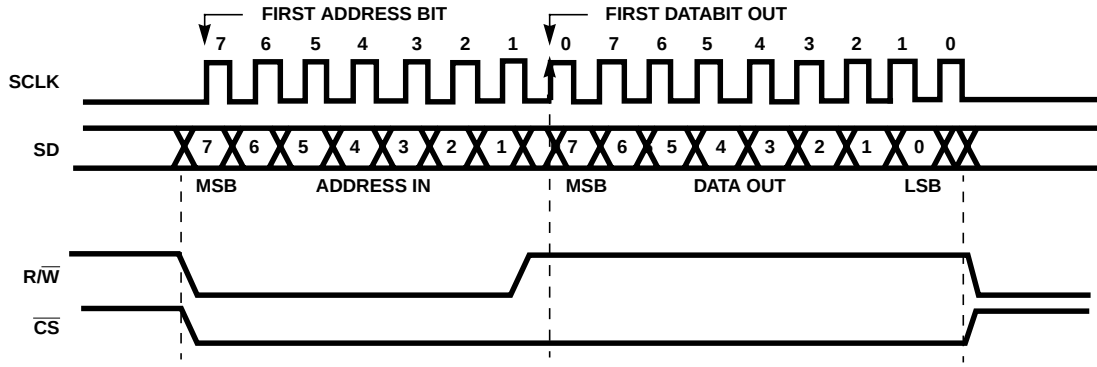


FIGURE 16. PRISM II BASEBAND PROCESSOR CONTROL PORT READ TIMING

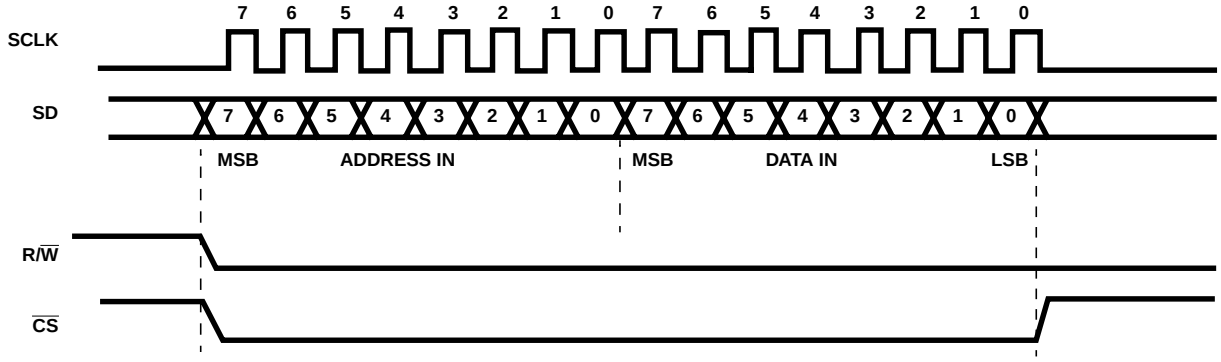


FIGURE 17. PRISM II BASEBAND PROCESSOR SERIAL CONTROL PORT WRITE TIMING

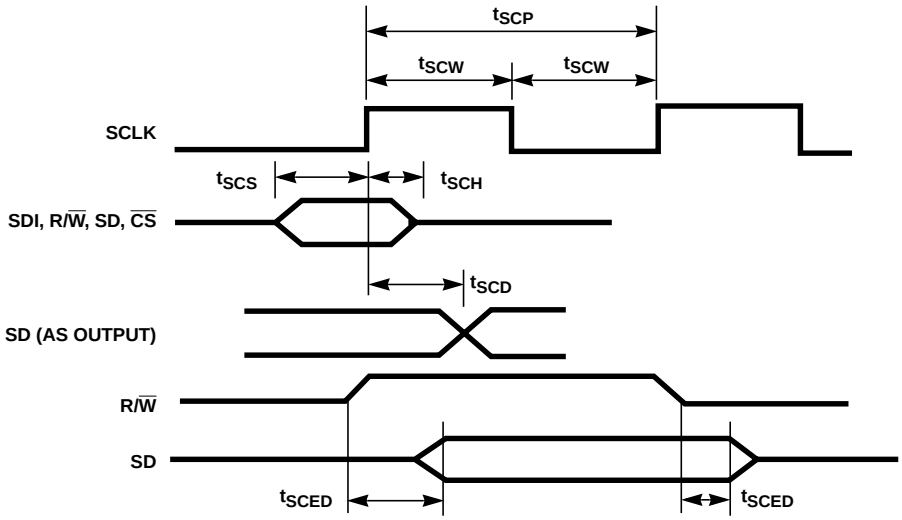


FIGURE 18. BBP CONTROL PORT SIGNAL TIMING

TABLE 1. BBP CONTROL PORT AC ELECTRICAL SPECIFICATIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
SCLK Clock Period	t_{SCP}	90	-	ns
SCLK Width Hi or Low	t_{SCW}	20	-	ns
Setup to SCLK + Edge (SD, SDI, R/W, CS)	t_{SCS}	30	-	ns
Hold Time from SCLK + Edge (SD, SDI, R/W, CS)	t_{SCH}	0	-	ns
SD Out Delay from SCLK + Edge	t_{SCD}	-	30	ns
SD Out Enable/Disable from R/W	t_{SCED}	-	15	ns

SYNTHESIZER

For the PRISM II, the synthesizer is programmed by firmware using different pins than the MMI. The HFA3841 will exchange data with the baseband during transmit and receive operations over the MMI interface. If the MMI interface was connected to the front end chips, the transitions on SCLK and SD could couple noise into them. The synthesizer serial bus consists of SYNTHDATA, SYNTHCLK, LE_IF and LE_RF. SYNTHDATA is on pin PK2, SYNTHCLK is on PK1, LE_IF is the enable for the HFA3783 Quad IF chip, and LE_RF is the enable for the HFA3683 synthesizer.

Data is provided on SYNTHDATA and clock on SYNTHCLK. The data is updated the falling edge of SYNTHCLK and expected to be latched into the synthesizer on the rising edge. The enable signal LE_RF is asserted while data is clocked out.

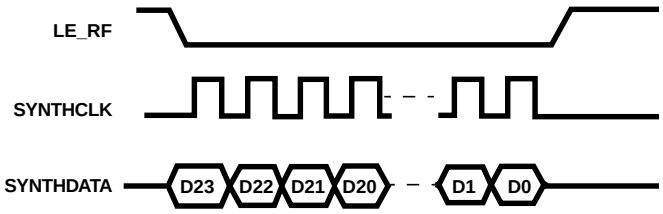


FIGURE 19. SYNTHESIZER DATA FORMAT

PHY Data Interface (MDI)

The HFA3841 has a dedicated serial port to provide the data interface to the baseband processor. This is referred to as the Modem Data Interface (MDI). The MDI operates on the data being transferred to and from the baseband on a word by word basis. There are no FIFOs needed, since the firmware is able to control the protocol in real time.

The MDI performs the following functions:

- Serial to parallel conversion of received data from the baseband, with synchronization between the incoming RX clock to the internal HFA3841 clock.
- Generating CRCs (HEC and FCS) from the received data stream to verify correct reception.
- Decrypt the received data when WEP is enabled.
- Parallel to serial conversion of transmit data, with the serial timing synchronized with the TX clock.
- Insertion of the CRCs (HEC and FCS) at the appropriate point during transmission.
- Encrypt the transmitted data when WEP is enabled.

The receive data path uses RX_RDY, RXC, RXD. The transmit data path uses TX_RDY, TXC, TXD and the CCA input to determine (under the IEEE802.11 protocol) whether to transmit.

In transmit mode, the HFA386X is used in the mode where it generates the PLCP header internally and only the MPDU is passed from HFA3841. In receive, the HFA386X is used in the mode where it passes the PLCP header and the MPDU to the HFA3841.

BBP Packet Reception

There are 4 signals associated with the BBP Receive Port: RX_PE (receive enable), MDRDY (receive ready), RXD (receive data), and RXCLK (receive clock). These connect to the HFA3841 on pins PL1, PK5, RXD, and RXC, respectively.

The receive demodulator in the BBP is activated via RX_PE. When RX_PE goes active the demodulator scrutinizes I and Q for packet activity. When a packet arrives at a valid signal level the demodulator acquires and tracks the incoming signal. It then sifts through the demodulator data for the Start Frame Delimiter (SFD). Normally, MDRDY is programmed to go active after SFD is detected. This signals the HFA3841, allowing it to pick off the needed header fields from the real-time demodulated bitstream rather than having to read these fields through the BBP Control Port.

Assuming all is well with the header, the BBP decodes the signal field in the header and switches to the appropriate data rate. If the signal field is not recognized, or the CRC16 is in error, then MDRDY will go inactive shortly after CRC16 and the demodulator will return to acquisition mode looking for another packet. If all is well with the header, and after the demodulator has switched to the appropriate data rate, then the demodulator will continue to provide data to the HFA3841 indefinitely.

Receive Port exchange details are depicted in Figure 20. Detailed timing is related in Figure 21 and Table 2.

For more detailed information concerning BBP packet reception see the HFA386x data sheets.

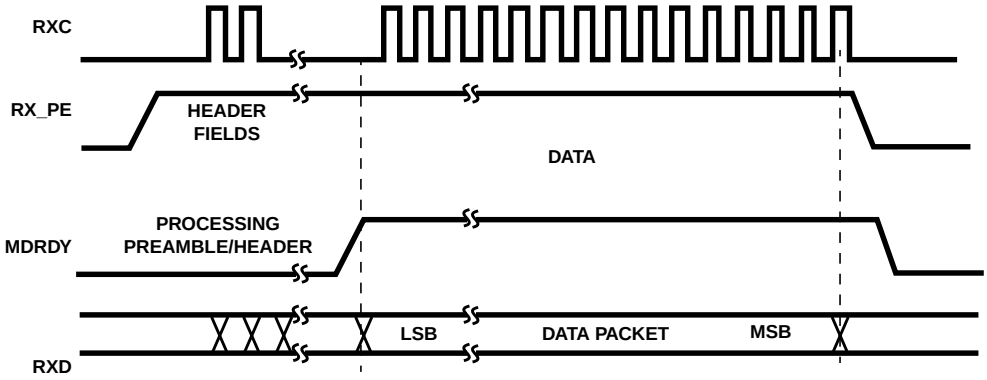


FIGURE 20. BBP RECEIVE PORT TIMING

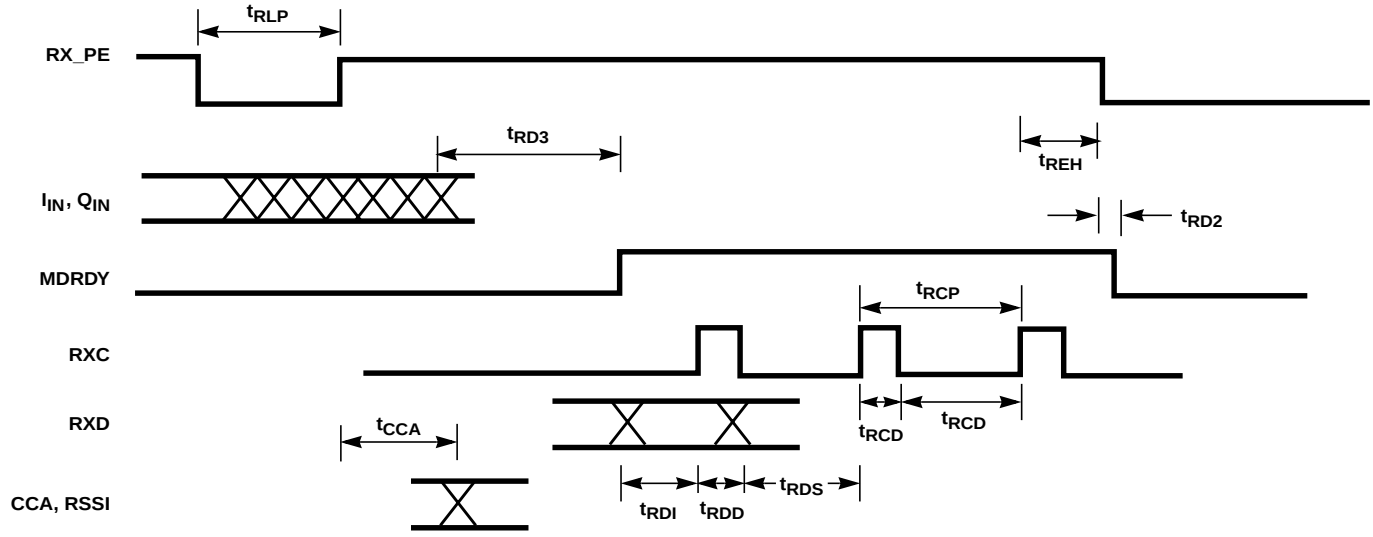


FIGURE 21. BBP RECEIVE PORT SIGNAL TIMING

NOTE: RXD, MDRDY is output two MCLK after RXC rising to provide hold time. RSSI output on TEST (5:0).

TABLE 2. BBP RECEIVE PORT AC ELECTRICAL SPECIFICATIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
RX_PE Inactive Width	t_{RLP}	70	-	ns (Note 13)
RXC Period (11MBps Mode)	t_{RCP}	77	-	ns
RXC Width Hi or Low (11MBps Mode)	t_{RCD}	31	-	ns
RXC to RXD	t_{RDD}	20	60	ns
MD_RDY to 1st RXC	t_{RD1}	940	-	ns (Note 14)
RXD to 1st RXC	$t_{RD!}$	940	-	ns
Setup RXD to RXC	t_{RDS}	31	-	ns
RXC to RX_PE Inactive (1MBps)	t_{REH}	0	925	ns (Note 15)
RXC to RX_PE Inactive (2MBps)	t_{REH}	0	380	ns (Note 15)
RXC to RX_PE Inactive (5.5MBps)	t_{REH}	0	140	ns (Note 15)
RXC to RX_PE Inactive (11MBps)	t_{REH}	0	50	ns (Note 15)
RX_PE inactive to MD_RDY Inactive	t_{RD2}	5	30	ns (Note 16)
Last Chip of SFD in to MD_RDY Active	t_{RD3}	2.77	2.86	µs (Note 14)
RX Delay		2.77	2.86	µs (Note 17)
RX_PE to CCA Valid	t_{CCA}	-	10	µs (Note 18)
RX_PE to RSSI Valid	t_{CCA}	-	10	µs (Note 18)

NOTES:

13. RX_PE must be inactive at least 3 MCLKs before going active to start a new CCA or acquisition.
14. MD_RDY programmed to go active after SFD detect (measured from I_{IN}, Q_{IN}).
15. RX_PE active to inactive delay to prevent next RXC.
16. Assumes RX_PE inactive after last RXC.
17. MD_RDY programmed to go active at MPDU start. Measured from first chip of first MPDU symbol at I_{IN}, Q_{IN} to MD_RDY active.
18. CCA and RSSI are measured once during the first 10µs interval following RX_PE going active. RX_PE must be pulsed to initiate a new measurement. RSSI may be read via serial port or from Test Bus.

BBP Packet Transmission

There are 4 signals associated with the BBP Transmit Port: TX_PE (transmit enable), TXRDY (transmit ready), TXD (transmit data), and TXCLK (transmit clock). These connect to the HFA3841 on PL0, PL7, TXD, and TXC, respectively.

State machines within the BBP control packet transmission and reception. In the case of a transmission, the MAC signals the BBP with the signal TX_PE. The BBP forms the preamble and header and then signals the MAC to begin transferring data with the signal TXRDY. This sequence is illustrated in Figure 22 with detailed signal timing shown in Figure 23 and specified delays contained in Table 3. Note that if the MAC deactivates TX_PE too early it may cut off modulation of the final symbol. For this reason, when TX_PE is de-asserted the BBP will hold TXRDY active until the last symbol containing data is modulated. This is important for power sequencing and is discussed in more detail in that section.

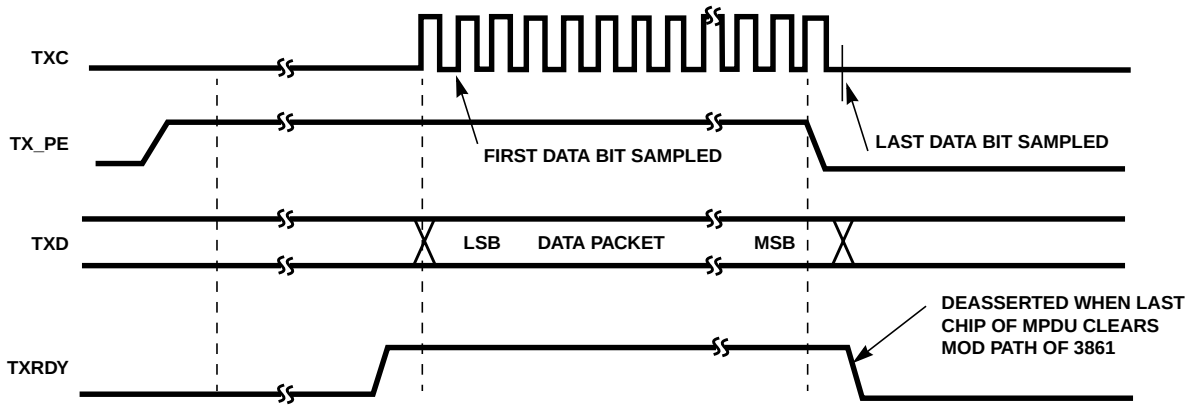
For more detailed information concerning BBP packet transmission see the HFA3861 data sheet.

TABLE 3. BBP TRANSMIT PORT AC ELECTRICAL SPECIFICATIONS

PARAMETER	SYMBOL	MIN	MAX	UNITS
TX_PE to I_{OUT}/Q_{OUT} (1st Valid Chip)	t_{D1}	2.18	2.3	µs (Note 19)
TX_PE Inactive Width	t_{TLP}	2.22	-	µs (Note 20)
TXC Width Hi or Low	t_{TCD}	40	-	ns
TXRDY Active to 1st TX_CLK Hi	t_{RC}	260	-	ns
Setup TXD to TXC Hi	t_{TDS}	30	-	ns
Hold TXD to TXC Hi	t_{TDH}	0	-	ns
TXC to TX_PE Inactive (1MBps)	t_{PEH}	0	965	ns (Note 22)
TXC to TX_PE Inactive (2MBps)	t_{PEH}	0	420	ns (Note 22)
TXC to TX_PE Inactive (5.5MBps)	t_{PEH}	0	160	ns (Note 22)
TXC to TX_PE Inactive (11MBps)	t_{PEH}	0	65	ns (Note 22)
TXRDY Inactive To Last Chip of MPDU Out	t_{RI}	-20	20	ns
TXD Modulation Extension	t_{ME}	2	-	µs (Note 21)

NOTES:

19. I_{OUT}/Q_{OUT} are modulated before first valid chip of preamble is output to provide ramp up time for RF/IF circuits.
20. TX_PE must be inactive before going active to generate a new packet.
21. I_{OUT}/Q_{OUT} are modulated after last chip of valid data to provide ramp down time for RF/IF circuits.
22. Delay from TXC to inactive edge of TXPE to prevent next TXC. Because TXPE asynchronously stops TXC, TXPE going inactive within 40ns of TXC will cause TXC minimum hi time to be less than 40ns.



NOTE: Preamble/Header and Data is transmitted LSB first. TXD shown generated from rising edge of TXC.

FIGURE 22. BBP TRANSMIT PORT TIMING

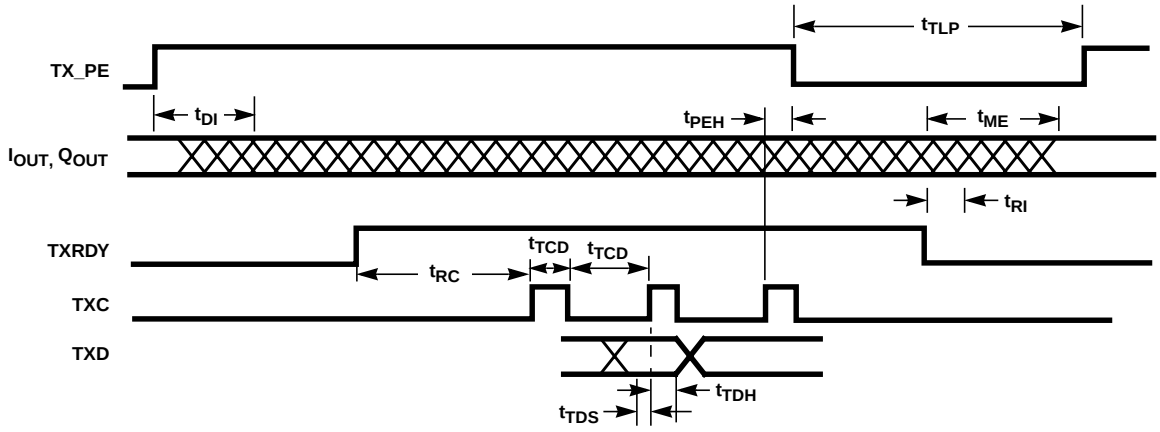


FIGURE 23. BBP TRANSMIT PORT SIGNAL TIMING

Power Sequencing

The HFA3841 provides a number of firmware controlled port pins that are used for controlling the power sequencing and other functions in the front end components of the PHY.

Packet transmission requires precise control of the radio. Ideally, energy at the antenna ceases after the last symbol of information has been transmitted. Additionally, the transmit/receive switch must be controlled properly to protect the receiver. It's also important to apply appropriate modulation to the PA while it's active.

Signaling sequences for the beginning and end of normal transmissions are illustrated in Figure 24. Table 4 lists applicable delays.

A transmission begins with PE2 as shown in Figure 24. Next, the transmit/receive switch is configured for transmission via the differential pair TR_SW and TR_SW_BAR. This is followed by TX_PE which activates the transmit state machine in the BBP. Lastly, PA_PE activates the PA. Delays for these signals related to the initiation of transmission are referenced to PE2.

Immediately after the final data bit has been clocked out of the HFA3841, TX_PE is de-asserted. The HFA3841 then waits for TXRDY to go inactive, signaling that the BBP has modulated the final information-rich symbol. It then immediately de-asserts PA_PE followed by placing the transmit/receive switch in the receive position and ending with PE2 going high. Delays for these signals related to the termination of transmission are referenced to the rising edge of PE2.

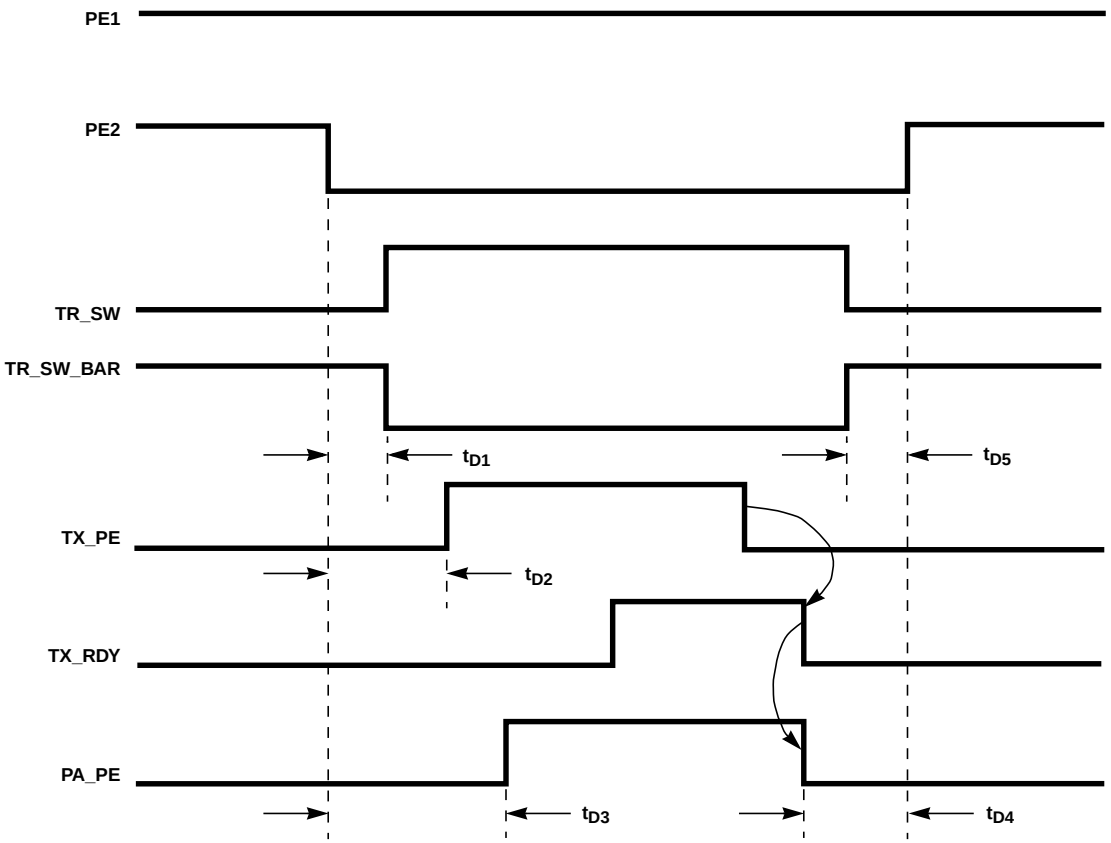


FIGURE 24. TRANSMIT CONTROL SIGNAL SEQUENCING

TABLE 4. TRANSMIT CONTROL TIMING SPECIFICATIONS

PARAMETER	SYMBOL	DELAY	TOLERANCE	UNITS
PE2 to TR Switch	t_{D1}	2	±0.1	µs
PE2 to BBP TX_PE	t_{D2}	TBD	±0.1	µs
PE2 to PA_PE	t_{D3}	3	±0.1	µs
PA_PE to PE2	t_{D4}	3	±0.1	µs
TR Switch to PE2	t_{D5}	2	±0.1	µs

PE1 and PE2 encoding details are found in Table 5.

Note that during normal receive and transmit operation that PE1 is static and PE2 toggles for receive and transmit states.

TABLE 5. POWER ENABLE STATES

	PE1	PE2	PLL_PE
Power Down State	0	0	1
Receive State	1	1	1
Transmit State	1	0	1
PLL Active State	0	1	1
PLL Disable State	X	X	0

NOTE: PLL_PE is controlled via the serial interface, and can be used to disable the internal synthesizer, the actual synthesizer control is an AND function of PLL_PE, and a result of the OR function of PE1 and PE2. PE1 and PE2 will directly control the power enable functionality of the LO buffer(s)/phase shifter.

Master Clock

Prescaler

The HFA3841 contains a clock prescaler to provide flexibility in the choice of clock input frequencies. For 11Mb/s operation, the internal master clock, MCLK, must be between 11MHz and 16MHz. The clock generator itself requires an input from the prescaler that is twice the desired MCLK frequency. Thus the lowest oscillator frequency that can be used for an 11MHz MCLK is 22MHz. The prescaler can divide by integers and 1/2 steps (IE 1, 1.5, 2, 2.5). Another way to look at it is that the divisor ratio between the external clock source and the internal MCLK may be integers between 2 and 14.

Typically, the 44MHz baseband clock is used as the input, and the prescaler is set to divide by 2. Another useful configuration is to set the prescaler to divide by 1.5 (resulting in 44MHz ÷3) for an MCLK of 14.67MHz.

Off Chip

If an off chip oscillator source is used, it should be connected to the XTALI pin. Insure that the signal amplitude meets CMOS levels at the XTALI pin.

Oscillator

The XTALI and XTALO pins provide an on-chip oscillator function to generate the master clock. For a standard pierce oscillator, the crystal is connected between XTALI and XTALO. Two capacitors, typically 15pF each, are connected from each pin to ground. The crystal should be a fundamental mode, specified under parallel resonance conditions. The load capacitance seen by the crystal will be approximately 2pF more than the series combination of C_1 and C_2 plus stray capacitance. After power on, the crystal will require time to stabilize before normal operation can commence. Insure that reset remains asserted for enough time for the crystal oscillator to stabilize.

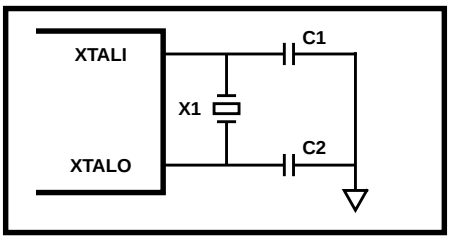


FIGURE 25. POWER ON RESET CONFIGURATION

Power On Reset Configuration

Power On Reset is issued to the HFA3841 with the HRESET pin or via the soft reset bit, SRESET, in the Configuration Option Register (COR, bit 7). HRESET originates from the HOST system which applies HRESET for at least 0.01ms after V_{CC} has reached 90% of its end value (see PC-Card standard, Vol. 2, Ch. 4.12.1).

The MD[15:8] pin values are sampled on the falling edge of HRESET or SRESET. These pins have internal 50K pull-down resistors. External pull-up resistors (typically 10kΩ) are used for bits that should be read as high at reset.

The table below summarizes the effect per pin.

TABLE 6. POR PINS AND FUNCTIONALITY

PIN	LATCH OUTPUT	FUNCTIONALITY
MD[8]	Reserved	
MD[9]	Nvdis	Disable mapping of CS to NV (Flash)
MD[10]	MEM16	External memory (RAM and Flash) is 16 bits wide
MD[11]	IDLE	See below
MD[12]	Reserved	
MD[15:13]	MD15/14/13	FW purposes

MD[11], IDLE, has no equivalent functionality in any control register. When asserted at reset, it will inhibit firmware execution. This is used to allow the initial download of firmware in “Genesis Mode”. See the Hardware Reference Manual for more details. The latch is cleared when the Software Reset, SRESET, COR(7) is active.

References

For Intersil documents available on the internet, see web site http://www.intersil.com/
Intersil AnswerFAX (321) 724-7800.

[1] IEEE Std 802.11-1999 Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specification.

[2] *HFA3860B Data Sheet*, Direct Sequence Spread Spectrum Baseband Processor, Intersil Corporation, AnswerFAX Doc. No. 4594.

[3] *HFA3861 Data Sheet*, Direct Sequence Spread Spectrum Baseband Processor, Intersil Corporation, AnswerFAX Doc. No. 4699.

[4] *HFA3783 Data Sheet*, Quad IF, Intersil Corporation, AnswerFAX Doc. No. 4633.

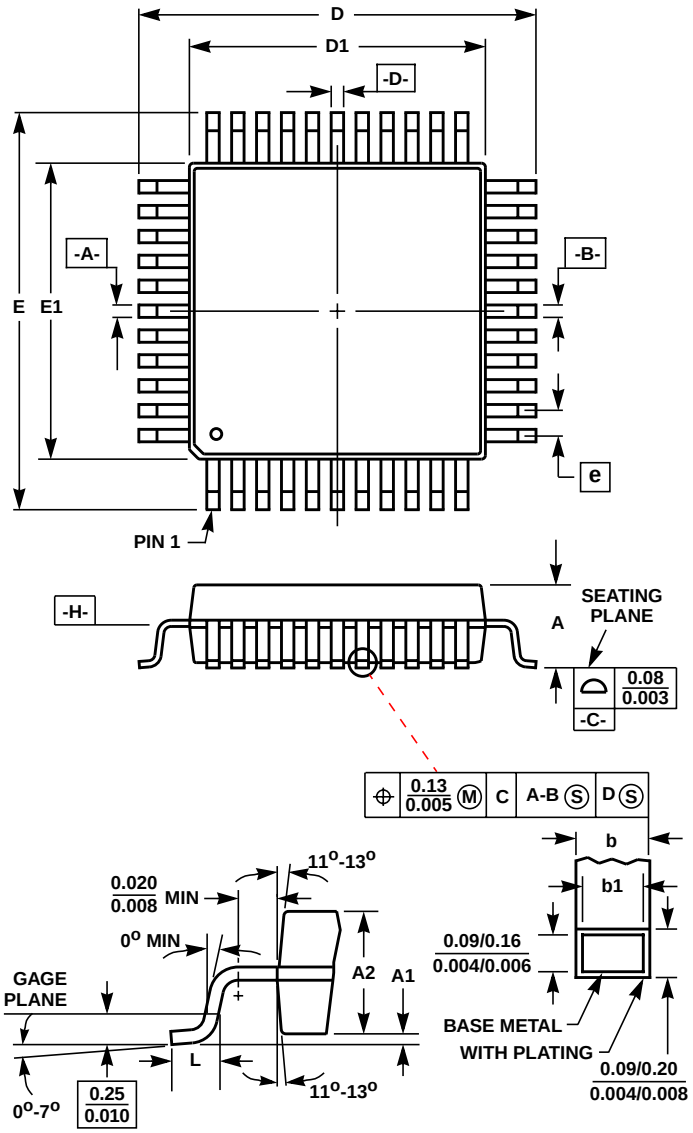
[5] *HFA3683 Data Sheet*, Direct Sequence Spread Spectrum Baseband Processor, Intersil Corporation, AnswerFAX Doc. No. 4634.

[6] PC Card Standard 1996, PCMCIA/JEIDA.

[7] A*N9874 Application Note*, Intersil Corporation, “ISA Plug and Play with the HFA3841”.

[8] A*N9844 Application Note*, Intersil Corporation, “HFA3841 to PRISMII Connections”, AnswerFAX Doc. No. 99844

Thin Plastic Quad Flatpack Packages (LQFP)



Q128.14x20 (JEDEC MS-026BHB ISSUE C)
128 LEAD THIN PLASTIC QUAD FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.062	-	1.60	-
A1	0.002	0.005	0.05	0.15	-
A2	0.054	0.057	1.35	1.45	-
b	0.007	0.010	0.17	0.27	6
b1	0.007	0.009	0.17	0.23	-
D	0.862	0.870	21.90	22.10	3
D1	0.783	0.791	19.90	20.10	4, 5
E	0.626	0.634	15.90	16.10	3
E1	0.547	0.555	13.90	14.10	4, 5
L	0.018	0.029	0.45	0.75	-
N	128		128		7
e	0.0197 BSC		0.50 BSC		-

Rev. 0 7/99

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm (0.003 inch).
7. “N” is the number of terminal positions.

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (321) 724-7000
FAX: (321) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029

Attachement-2

Datasheet of HFA3861.

ADVANCE INFORMATION | Data Sheet | November 1999 | File Number 4776.1

Direct Sequence Spread Spectrum Baseband Processor

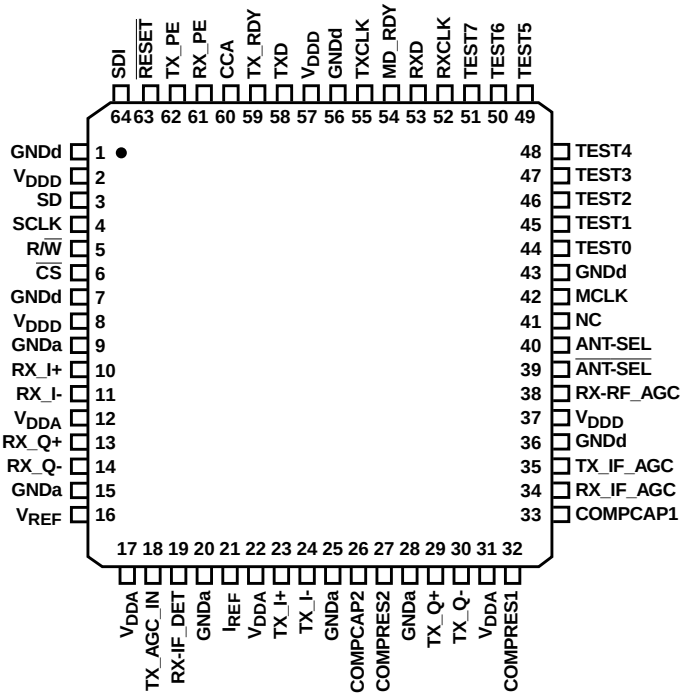
The Intersil HFA3861A Direct Sequence Spread Spectrum (DSSS) baseband processor is part of the PRISM® 2.4GHz radio chipset, and contains all the functions necessary for a full or half duplex packet baseband transceiver.

The HFA3861A has on-board A/D's for analog I and Q inputs and outputs, for which the HFA3783 IF QMODEM is recommended. Differential phase shift keying modulation schemes DBPSK and DQPSK, with data scrambling capability, are available along with Complementary Code Keying to provide a variety of data rates. Built-in flexibility allows the HFA3861A to be configured through a general purpose control bus, for a range of applications. Both Receive and Transmit AGC functions with 7-bit AGC control obtain maximum performance in the analog portions of the transceiver. The HFA3861A is housed in a thin plastic quad flat package (TQFP) suitable for PCMCIA board applications.

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HFA3861AIN	-40 to 85	64 Ld TQFP	Q64.10x10
HFA3861AIN96	-40 to 85	Tape and Reel	

Pinout



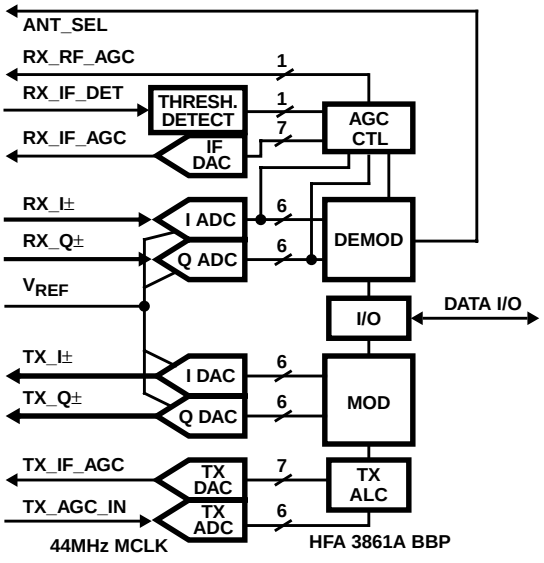
Features

- Complete DSSS Baseband Processor
- Processing Gain . . . . . FCC Compliant
- Programmable Data Rate . . . . . 1, 2, 5.5, and 11Mbps
- Ultra Small Package . . . . . 10 x 10mm
- Single Supply Operation (44MHz Max) . . . . . 2.7V to 3.6V
- Modulation Methods . . . . . DBPSK, DQPSK, and CCK
- Supports Full or Half Duplex Operations
- On-Chip A/D and D/A Converters for I/Q Data (6-Bit, 22MSPS), AGC, and Adaptive Power Control (7-Bit)
- Targeted for Multipath Delay Spreads ~50ns
- Supports Short Preamble Acquisition
- Supports Antenna Diversity

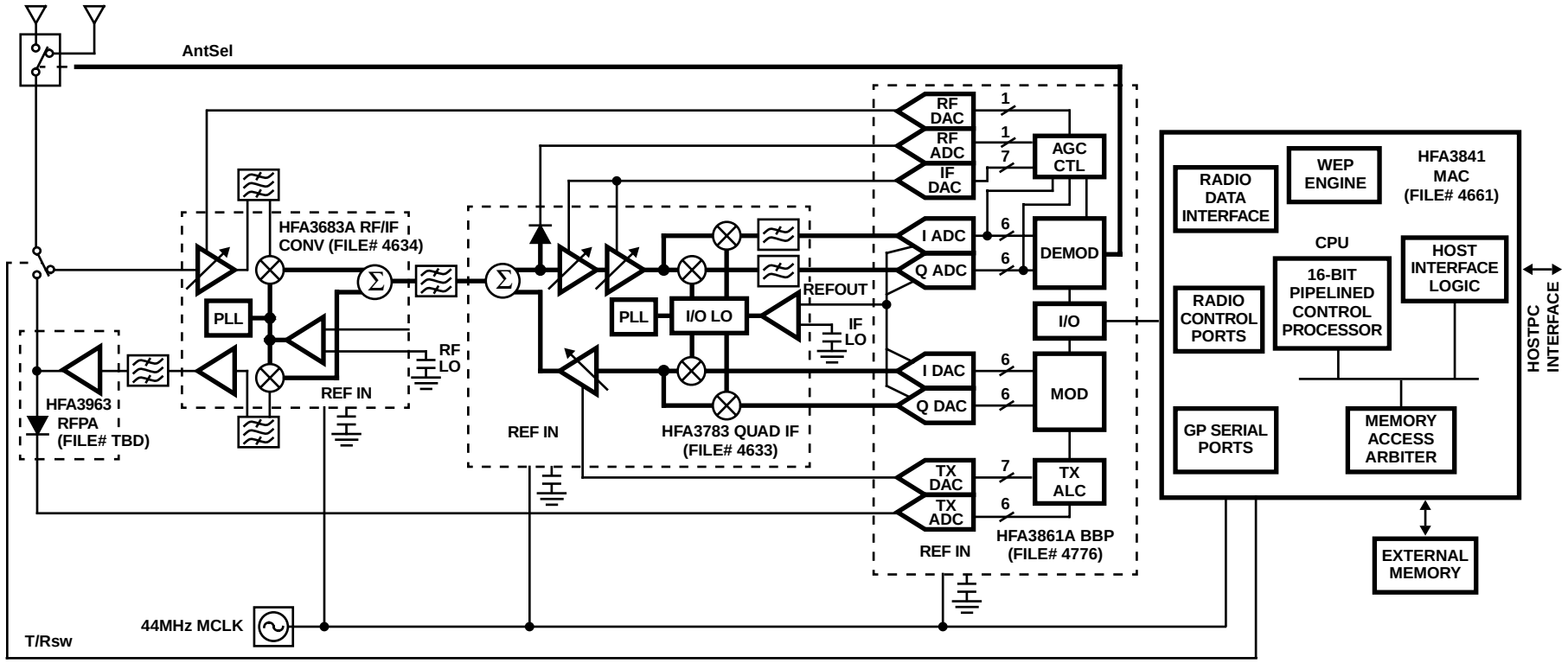
Applications

- Enterprise WLAN Systems
- Systems Targeting IEEE 802.11 Standard
- DSSS PCMCIA Wireless Transceiver
- Spread Spectrum WLAN RF Modems
- TDMA Packet Protocol Radios
- Part 15 Compliant Radio Links
- Portable PDA/Notebook Computer
- Wireless Digital Audio, Video, Multimedia
- PCN/Wireless PBX
- Wireless Bridges
- Antenna Diversity Supported

Simplified Block Diagram



Typical Application Diagram



TYPICAL TRANSCEIVER APPLICATION CIRCUIT USING THE HFA3861A

For additional information on the PRISM® chip set, call (407) 724-7800 to access Intersil' AnswerFAX system. When prompted, key in the four-digit document number (File #) of the data sheets you wish to receive.

The four-digit file numbers are shown in the Typical Application Diagram, and correspond to the appropriate circuit.

Pin Descriptions

NAME	PIN	TYPE I/O	DESCRIPTION
V_{DDA} (Analog)	12, 17, 22, 31	Power	DC power supply 2.7V - 3.6V (Not Hard wired Together On Chip).
V_{DDD} (Digital)	2, 8, 37, 57	Power	DC power supply 2.7 - 3.6V.
GNDa (Analog)	9, 15, 20, 25, 28,	Ground	DC power supply 2.7 - 3.6V, ground (Not Hard wired Together On Chip).
GNDd (Digital)	1, 7, 36, 43, 56	Ground	DC power supply 2.7 - 3.6V, ground.
V_{REF}	16	I	Voltage reference for A/D's and D/A's.
I_{REF}	21	I	Current reference for internal ADC and DAC devices. Requires a 12kΩ resistor to ground.
$RXI_{, +/-}$	10/11	I	Analog input to the internal 6-bit A/D of the In-phase received data. Balanced differential 10+/11-.
$RXQ_{, +/-}$	13/14	I	Analog input to the internal 6-bit A/D of the Quadrature received data. Balanced differential 13+/14-.
$\overline{\text{ANTSEL}}$	39	O	The antenna select signal changes state as the receiver switches from antenna to antenna during the acquisition process in the antenna diversity mode. This is a complement for ANTSEL (pin 40) for differential drive of antenna switches.
ANTSEL	40	O	The antenna select signal changes state as the receiver switches from antenna to antenna during the acquisition process in the antenna diversity mode. This is a complement for $\overline{\text{ANTSEL}}$ (pin 39) for differential drive of antenna switches.
RX_IF_DET	19	I	Analog input to the receive power A/D converter for AGC control.
RX_IF_AGC	34	O	Analog drive to the IF AGC control.
RX_RF_AGC	38	O	Drive to the RF AGC stage attenuator. CMOS digital.
TX_AGC_IN	18	I	Input to the transmit power A/D converter for transmit AGC control.
TX_IF_AGC	35	O	Analog drive to the transmit IF power control.
TX_PE	62	I	When active, the transmitter is configured to be operational, otherwise the transmitter is in standby mode. TX_PE is an input from the external Media Access Controller (MAC) or network processor to the HFA3861A. The rising edge of TX_PE will start the internal transmit state machine and the falling edge will initiate shut down of the state machine. TX_PE envelopes the transmit data except for the last bit. The transmitter will continue to run for 4µs after TX_PE goes inactive to allow the PA to shut down gracefully.
TXD	58	I	TXD is an input, used to transfer MAC Payload Data Unit (MPDU) data from the MAC or network processor to the HFA3861A. The data is received serially with the LSB first. The data is clocked in the HFA3861A at the rising edge of TXCLK.
TXCLK	55	O	TXCLK is a clock output used to receive the data on the TXD from the MAC or network processor to the HFA3861A, synchronously. Transmit data on the TXD bus is clocked into the HFA3861A on the rising edge. The clocking edge is also programmable to be on either phase of the clock. The rate of the clock will be dependent upon the data rate that is programmed in the signalling field of the header.
TX_RDY	59	O	TX_RDY is an output to the external network processor indicating that Preamble and Header information has been generated and that the HFA3861A is ready to receive the data packet from the network processor over the TXD serial bus.
CCA	60	O	Clear Channel Assessment (CCA) is an output used to signal that the channel is clear to transmit. The CCA may be configured to one of four possible algorithms. The CCA algorithm and its features are described elsewhere in the data sheet. Logic 0 = Channel is clear to transmit. Logic 1 = Channel is NOT clear to transmit (busy). This polarity is programmable and can be inverted.
RXD	53	O	RXD is an output to the external network processor transferring demodulated Header information and data in a serial format. The data is sent serially with the LSB first. The data is frame aligned with MD_RDY.
RXCLK	52	O	RXCLK is the bit clock output. This clock is used to transfer Header information and payload data through the RXD serial bus to the network processor. This clock reflects the bit rate in use. RXCLK is held to a logic "0" state during the CRC16 reception. RXCLK becomes active after the SFD has been detected. Data should be sampled on the rising edge. This polarity is programmable and can be inverted.

Pin Descriptions (Continued)

NAME	PIN	TYPE I/O	DESCRIPTION
MD_RDY	54	O	MD_RDY is an output signal to the network processor, indicating header data and a data packet are ready to be transferred to the processor. MD_RDY is an active high signal that signals the start of data transfer over the RXD serial bus. MD_RDY goes active when the SFD (Note) is detected and returns to its inactive state when RX_PE goes inactive or an error is detected in the header.
RX_PE	61	I	When active, the receiver is configured to be operational, otherwise the receiver is in standby mode. This is an active high input signal. In standby, RX_PE inactive, all RX A/D converters are disabled.
SD	3	I/O	SD is a serial bidirectional data bus which is used to transfer address and data to/from the internal registers. The bit ordering of an 8-bit word is MSB first. The first 8 bits during transfers indicate the register address immediately followed by 8 more bits representing the data that needs to be written or read at that register. In the 4 wire interface mode, this pin is three-stated unless the R/$\overline{W}$ pin is high.
SCLK	4	I	SCLK is the clock for the SD serial bus. The data on SD is clocked at the rising edge. SCLK is an input clock and it is asynchronous to the internal master clock (MCLK). The maximum rate of this clock is 11MHz or one half the master clock frequency, whichever is lower.
SDI	64	I	Serial Data Input in 3 wire mode described in Tech Brief 383. This pin is not used in the 4 wire interface described in this data sheet. It should not be left floating.
R/$\overline{W}$	5	I	R/$\overline{W}$ is an input to the HFA3861A used to change the direction of the SD bus when reading or writing data on the SD bus. R/$\overline{W}$ must be set up prior to the rising edge of SCLK. A high level indicates read while a low level is a write.
$\overline{CS}$	6	I	$\overline{CS}$ is a Chip select for the device to activate the serial control port. The $\overline{CS}$ doesn't impact any of the other interface ports and signals, i.e., the TX or RX ports and interface signals. This is an active low signal. When inactive SD, SCLK, and R/$\overline{W}$ become "don't care" signals.
TEST 7:0	51, 50, 49, 48, 47, 46, 45, 44	I/O	This is a data port that can be programmed to bring out internal signals or data for monitoring. These bits are primarily reserved by the manufacturer for testing. A further description of the test port is given in the appropriate section of this data sheet.
$\overline{RESET}$	63	I	Master reset for device. When active TX and RX functions are disabled. If $\overline{RESET}$ is kept low the HFA3861A goes into the power standby mode. $\overline{RESET}$ does not alter any of the configuration register values nor does it preset any of the registers into default values. Device requires programming upon power-up. See CR11 bit 7 for important initialization information.
MCLK	42	I	Master Clock for device. The nominal frequency of this clock is 44MHz. This is used internally to generate all other internal necessary clocks and is divided by 2 or 4 for the transceiver clocks.
$TXI_{+/-}$	23/24	O	TX Spread baseband I digital output data. Data is output at the chip rate. Balanced differential 23+/24-.
$TXQ_{+/-}$	29/30	O	TX Spread baseband Q digital output data. Data is output at the chip rate. Balanced differential 29+/30-.
CompCap	33	I	Compensation capacitor.
CompCap2	26	I	Compensation capacitor.
CompRes1	32	I	Compensation Resistor.
CompRes2	27	I	Compensation Resistor.

NOTE: See CR10<3>.

External Interfaces

There are three primary digital interface ports for the HFA3861A that are used for configuration and during normal operation of the device as shown in Figure 1. These ports are:

- The **Control Port**, which is used to configure, write and/or read the status of the internal HFA3861A registers.
- The **TX Port**, which is used to accept the data that needs to be transmitted from the network processor.
- The **RX Port**, which is used to output the received demodulated data to the network processor.

In addition to these primary digital interfaces the device includes a byte wide parallel **Test Port** which can be configured to output various internal signals and/or data. The device can also be set into various power consumption modes by external control. The HFA3861A contains three Analog to Digital (A/D) converters and four Digital to Analog converters. The analog interfaces to the HFA3861A include, the In phase (I) and quadrature (Q) data component inputs/outputs, and the RF and IF receive automatic gain control and transmit output power control.

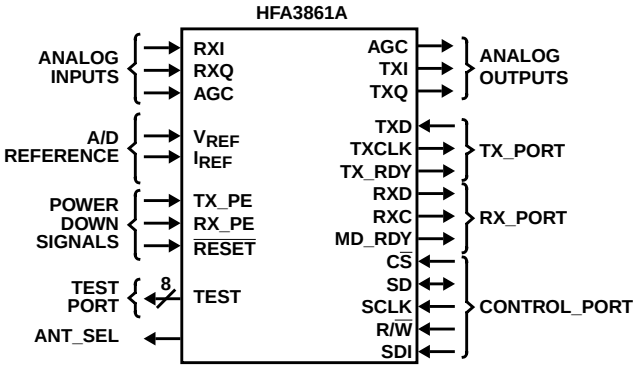
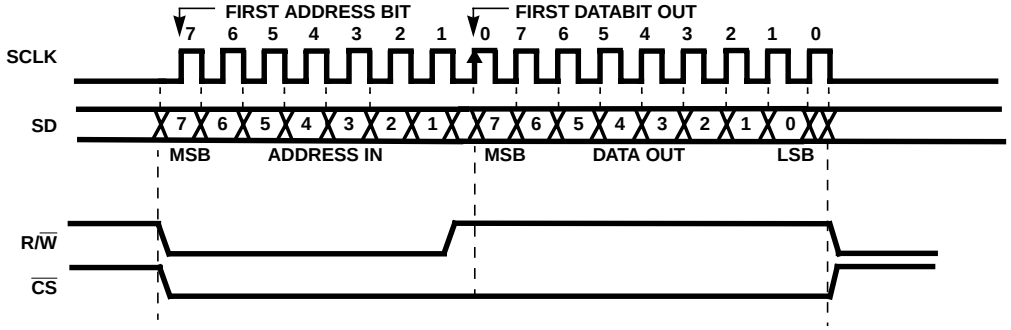


FIGURE 1. EXTERNAL INTERFACES

Control Port (4 Wire)

The serial control port is used to serially write and read data to/from the device. This serial port can operate up to a 11MHz rate or 1/2 the maximum master clock rate of the device, MCLK (whichever is lower). MCLK must be running and RESET must be inactive during programming. This port is used to program and to read all internal registers. The first 8 bits always represent the address followed immediately by the 8 data bits for that register. The LSB of the address is a don't care, but reserved for future expansion. The serial transfers are accomplished through the serial data pin (SD). SD is a bidirectional serial data bus. Chip Select ($\overline{CS}$), and Read/$\overline{Write}$ (R/$\overline{W}$) are also required as handshake signals for this port. The clock used in conjunction with the address and data on SD is SCLK. This clock is provided by the external source and it is an input to the HFA3861A. The timing relationships of these signals are illustrated in Figures 2 and 3. R/$\overline{W}$ is high when data is to be read, and low when it is to be written. $\overline{CS}$ is an asynchronous reset to the state machine. $\overline{CS}$ must be active (low) during the entire data transfer cycle. $\overline{CS}$ selects the serial control port device only. The serial control port operates asynchronously from the TX and RX ports and it can accomplish data transfers independent of the activity at the other digital or analog ports.

The HFA3861A has 96 internal registers that can be configured through the control port. These registers are listed in the Configuration and Control Internal Register table. Table 9 lists the configuration register number, a brief name describing the register, the HEX address to access each of the registers and typical values. The type indicates whether the corresponding register is Read only (R) or Read/Write (R/W). Some registers are two bytes wide as indicated on the table (high and low bytes).



NOTES:

1. The HFA3861A always uses the rising edge of SCLK to sample address and data and to generate read data.
2. These figures show the controller using the falling edge of SCLK to generate address and data and to sample read data.

FIGURE 2. CONTROL PORT READ TIMING

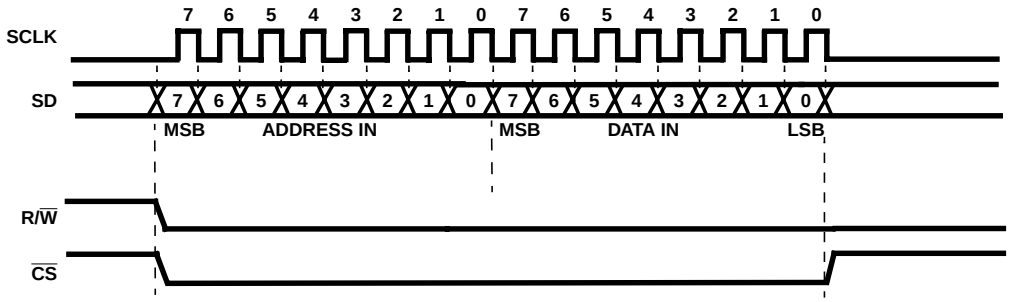


FIGURE 3. CONTROL PORT WRITE TIMING

TX Port

The transmit data port accepts the data that needs to be transmitted serially from an external data source. The data is modulated and transmitted as soon as it is received from the external data source. The serial data is input to the HFA3861A through TXD using the next rising edge of TXCLK to clock it in the HFA3861A. TXCLK is an output from the HFA3861A. A timing scenario of the transmit signal handshakes and sequence is shown on timing diagram Figure 4.

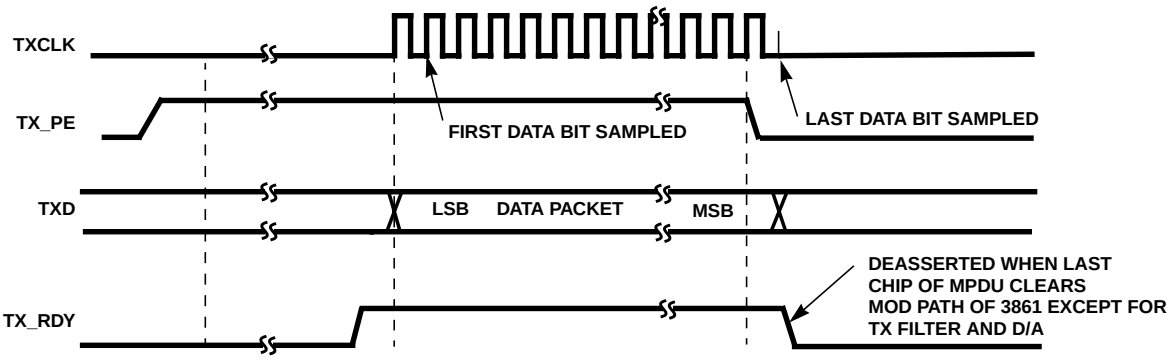
The external processor initiates the transmit sequence by asserting TX_PE. TX_PE envelopes the transmit data packet on TXD. The HFA3861A responds by generating a Preamble and Header. Before the last bit of the Header is sent, the HFA3861A begins generating TXCLK to input the serial data on TXD. TXCLK will run until TX_PE goes back to its inactive state indicating the end of the data packet. The user needs to hold TX_PE high for as many clocks as there bits to transmit. For the higher data rates, this will be in multiples of the number of bits per symbol. The HFA3861A will continue to output modulated signal for 4µs after the last data bit is output, to supply bits to flush the modulation path. TX_PE must be held until the last data bit is output from the MAC/FIFO. The minimum TX_PE inactive pulse required to restart the preamble and header generation is 2.22µs and to reset the modulator is 4.22µs.

The HFA3861A internally generates the preamble and header information from information supplied via the control registers. The external source needs to provide only the data portion of the packet and set the control registers. The timing diagram of this process is illustrated on Figure 4. Assertion of TX_PE will initialize the generation of the preamble and header. TX_RDY, which is an output from the HFA3861A, is used (if needed) to indicate to the external processor that the preamble has been generated and the device is ready to receive the data packet (MPDU) to be transmitted from the external processor. Signals TX_RDY, TX_PE and TXCLK can be set individually, by programming Configuration Register (CR) 1, as either active high or active low signals.

The transmit port is completely independent from the operation of the other interface ports including the RX port, therefore supporting a full duplex mode.

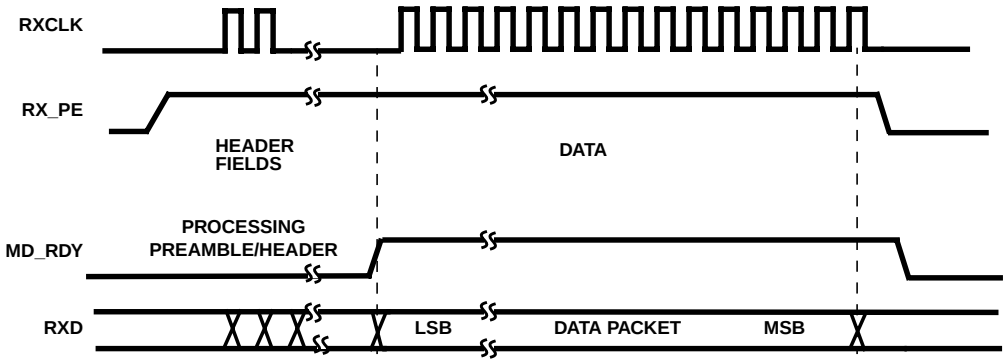
RX Port

The timing diagram Figure 5 illustrates the relationships between the various signals of the RX port. The receive data port serially outputs the demodulated data from RXD. The data is output as soon as it is demodulated by the HFA3861A. RX_PE must be at its active state throughout the receive operation. When RX_PE is inactive the device's receive functions, including acquisition, will be in a stand by mode.



NOTE: Preamble/Header and Data is transmitted LSB first. TXD shown generated from rising edge of TXCLK.

FIGURE 4. TX PORT TIMING



NOTE: MD_RDY active after CRC16. See detailed timing diagrams (Figures 18, 19, 20).

FIGURE 5. RX PORT TIMING

RXCLK is an output from the HFA3861A and is the clock for the serial demodulated data on RXD. MD_RDY is an output from the HFA3861A and it may be set to go active after the SFD or CRC fields. Note that RXCLK becomes active after the Start Frame Delimiter (SFD) to clock out the Signal, Service, and Length fields, then goes inactive during the header CRC field. RXCLK becomes active again for the data. MD_RDY returns to its inactive state after RX_PE is deactivated by the external controller, or if a header error is detected. A header error is either a failure of the CRC check, or the failure of the received signal field to match one of the 4 programmed signal fields. For either type of header error, the HFA3861A will reset itself after reception of the CRC field. If MD_RDY had been set to go active after CRC, it will remain low.

MD_RDY and RXCLK can be configured through CR 1, bits 1 and 0 to be active low, or active high. The receive port is completely independent from the operation of the other interface ports including the TX port, supporting therefore a full duplex mode.

RX I/Q A/D Interface

The PRISM baseband processor chip (HFA3861A) includes two 6-bit Analog to Digital converters (A/Ds) that sample the balanced differential analog input from the IF down converter. The I/Q A/D clock, samples at twice the chip rate. The nominal sampling rate is 22MHz.

The interface specifications for the I and Q A/Ds are listed in Table 1. The HFA3861A is designed to be DC coupled to the HFA3783.

TABLE 1. I, Q, A/D SPECIFICATIONS

PARAMETER	MIN	TYP	MAX
Full Scale Input Voltage (V_{P-P})	0.90	1.00	1.10
Input Bandwidth (-0.5dB)	-	11MHz	-
Input Capacitance (pF)	-	2	-
Input Impedance (DC)	5kΩ	-	-
f_S (Sampling Frequency)	-	22MHz	-

The voltages applied to pin 16, V_{REF} and pin 21, I_{REF} set the references for the internal I and Q A/D converters. In addition, For a nominal I/Q input of 250mV_{P-P}, the suggested V_{REF} voltage is 1.2V.

AGC Circuit

The AGC circuit is designed to optimize A/D performance for the I and Q inputs by maintaining the proper headroom on the 6-bit converters. There are two gain stages being controlled. At RF, the gain control is a 30dB step in gain from turning off the LNA. This RF gain control optimizes the receiver dynamic range when the signal level is high and maintains the noise figure of the receiver when it is needed most. At IF the gain control is linear and covers the bulk of the gain control range of the receiver.

The AGC sensing mechanism uses a combination of the I and Q A/D converters and the detected signal level in the IF to determine the gain settings. The A/D outputs are monitored in the HFA3861A for the desired nominal level. When it is reached, by adjusting the receiver gain, the gain control is locked for the remainder of the packet.

RX_AGC_IN Interface

The signal level in the IF stage is monitored to determine when to impose the up to 30dB gain reduction in the RF stage. This maximizes the dynamic range of the receiver by keeping the RF stages out of saturation at high signal levels. When the IF circuits' sensor output reaches 0.5V, the HFA3861A comparator switches in the 30dB pad and compensates the IF AGC and RSSI measures.

TX I/Q DAC Interface

The transmit section outputs balanced differential analog signals from the transmit DACs to the HFA3783. These are DC coupled and digitally filtered.

Test Port

The HFA3861A provides the capability to access a number of internal signals and/or data through the Test port, pins TEST 7:0. The test port is programmable through configuration register (CR 34). Any signal on the test port can also be read from configuration register (CR50) via the serial control port. Additionally, the transmit DACs can be configured to show signals in the receiver via CR 14. This allows visibility to analog like signals that would normally be very difficult to capture.

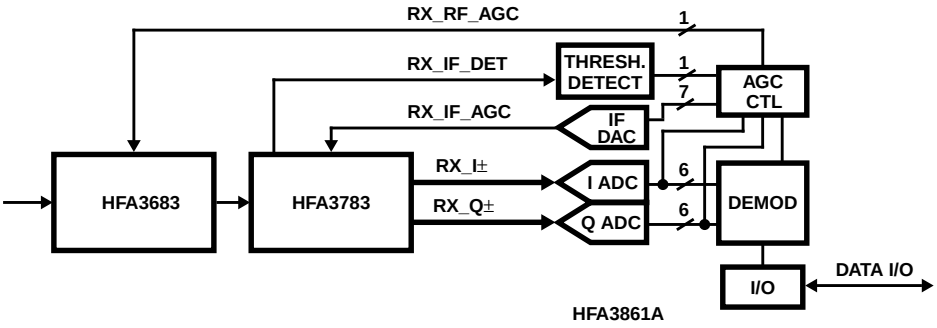


FIGURE 6. AGC CIRCUIT

Power Down Modes

The power consumption modes of the HFA3861A are controlled by the following control signals.

Receiver Power Enable (RX_PE, pin 61), which disables the receiver when inactive.

Transmitter Power Enable (TX_PE, pin 62), which disables the transmitter when inactive.

Reset ($\overline{\text{RESET}}$, pin 63), which puts the receiver in a sleep mode. The power down mode where, both $\overline{\text{RESET}}$ and RX_PE are used is the lowest possible power consumption mode for the receiver. Exiting this mode requires a maximum of 10µs before the device is operational.

The contents of the Configuration Registers are not effected by any of the power down modes. No reconfiguration is required when returning to operational modes. Activation of RESET does corrupt learned values of AGC settings and noise floor values. Optimum receiver operation may not be achieved until these values are reestablished (typically <50µs of operation in noise only needed). The power savings of activating RESET must be weighed against this.

Table 2 describes the power down modes available for the HFA3861A (V_{CC} = 3.3V). The table values assume that all other inputs to the part (MCLK, SCLK, etc.) continue to run except as noted.

Transmitter Description

The HFA3861A transmitter is designed as a Direct Sequence Spread Spectrum Phase Shift Keying (DSSS PSK) modulator. It can handle data rates of up to 11Mbps (refer to AC and DC specifications). The various modes of the modulator are Differential Binary Phase Shift Keying (DBPSK) for 1Mbps, Differential Quaternary Phase Shift Keying (DQPSK) for 2Mbps, and Complementary Code Keying (CCK) for 5.5Mbps and 11Mbps. These implement data rates as shown in Table 3. The major functional blocks of the transmitter include a network processor interface, DPSK modulator, high rate modulator, a data scrambler and a spreader, as shown in Figure 7. CCK is essentially a quadra-phase form of M-ARY Orthogonal Keying. A description of that modulation can be found in Chapter 5 of: “Telecommunications System Engineering”, by Lindsey and Simon, Prentis Hall publishing.

The preamble is always transmitted as the DBPSK waveform while the header can be configured to be either DBPSK, or DQPSK, and data packets can be configured for DBPSK, DQPSK, or CCK. The preamble is used by the receiver to achieve initial PN synchronization while the header includes the necessary data fields of the communications protocol to establish the physical layer link. The transmitter generates the synchronization preamble and header and knows when to make the DBPSK to DQPSK or CCK switchover, as required.

TABLE 2. POWER DOWN MODES

MODE	RX_PE	TX_PE	RESET	AT 44MHz	DEVICE STATE
SLEEP	Inactive	Inactive	Active	1mA	Both transmit and receive functions disabled. Device in sleep mode. Control Interface is still active. Register values are maintained. Device will return to its active state within 10µs.
STANDBY	Inactive	Inactive	Inactive	1.5mA	Both transmit and receive operations disabled. Device will resume its operational state within 1µs of RX_PE or TX_PE going active.
TX	Inactive	Active	Inactive	15mA	Receiver operations disabled. Receiver will return in its operational state within 1µs of RX_PE going active.
RX	Active	Inactive	Inactive	50mA	Transmitter operations disabled. Transmitter will return to its operational state within 2 MCLKs of TX_PE going active.
NO CLOCK	I_{CC} Standby		Active	300µA	All inputs at V_{CC} or GND.

TABLE 3. BIT RATE TABLE EXAMPLES FOR MCLK = 44MHz

DATA MODULATION	A/D SAMPLE CLOCK (MHz)	TX SETUP CR 5 BITS 1, 0	RX SIGNAL CR 63 BITS 7, 6	DATA RATE (Mbps)	SYMBOL RATE (MSPS)
DBPSK	22	00	00	1	1
DQPSK	22	01	01	2	1
CCK	22	10	10	5.5	1.375
CCK	22	11	11	11	1.375

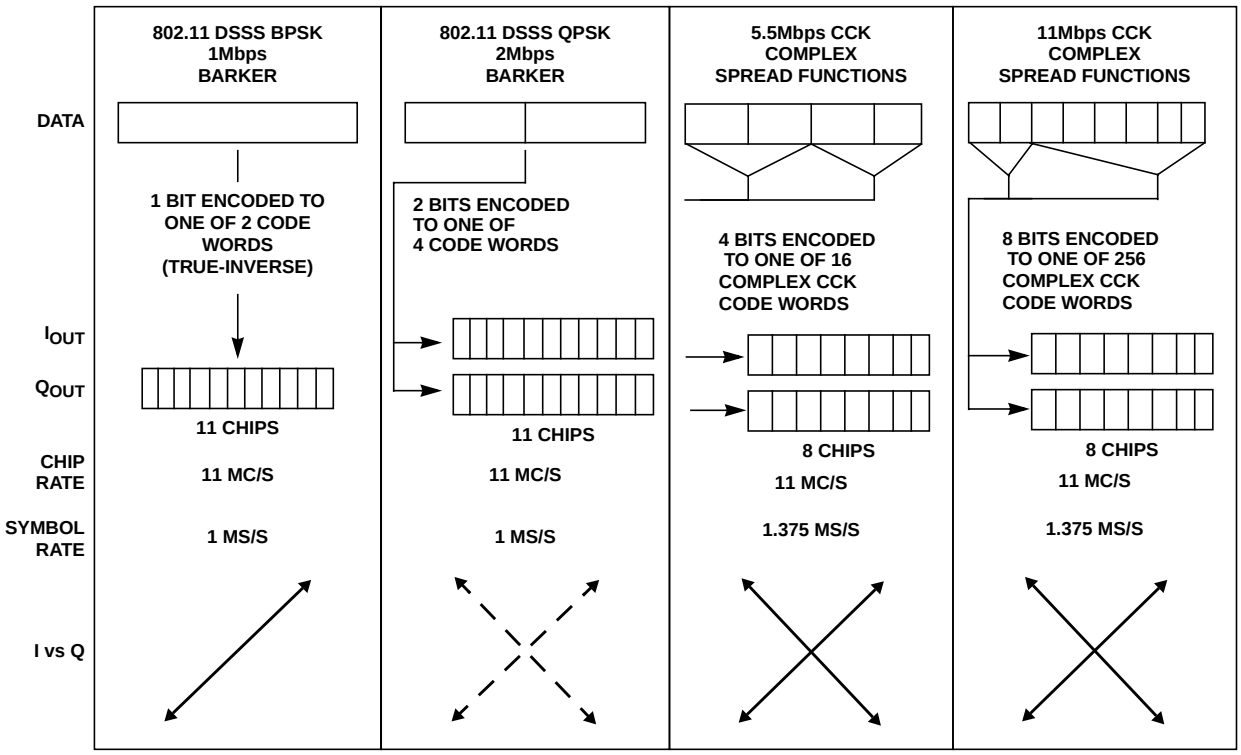


FIGURE 7. MODULATION MODES

For the 1 and 2Mbps modes, the transmitter accepts data from the external source, scrambles it, differentially encodes it as either DBPSK or DQPSK, and spreads it with the BPSK PN sequence. The baseband digital signals are then output to the external IF modulator.

For the CCK modes, the transmitter inputs the data and partitions it into nibbles (4 bits) or bytes (8 bits). At 5.5Mbps, it uses two of those bits to select one of 4 complex spread sequences from a table of CCK sequences and then QPSK modulates that symbol with the remaining 2 bits. Thus, there are 4 possible spread sequences to send at four possible carrier phases, but only one is sent. This sequence is then modulated on the I and Q outputs. The initial phase reference for the data portion of the packet is the phase of the last bit of the header. At 11Mbps, one byte is used as above where 6 bits are used to select one of 64 spread sequences for a symbol and the other 2 are used to QPSK modulate that symbol. Thus, the total possible number of combinations of sequence and carrier phases is 256. Of these only one is sent.

The bit rate Table 3 shows examples of the bit rates and the symbol rates and Figure 7 shows the modulation schemes. The modulator is completely independent from the demodulator, allowing the PRISM baseband processor to be used in full duplex operation.

Header/Packet Description

The HFA3861A is designed to handle packetized Direct Sequence Spread Spectrum (DSSS) data transmissions. The HFA3861A generates its own preamble and header information. It uses two packet preamble and header configurations. The first is backwards compatible with the existing IEEE 802.11-1997 1 and 2Mbps modes and the second is the optional shortened mode which maximizes throughput at the expense of compatibility with legacy equipment.

In the long preamble mode, the device uses a synchronization preamble of 128 symbols along with a header that includes four fields. The preamble is all 1's (before entering the scrambler) plus a start frame delimiter (SFD). The actual transmitted pattern of the preamble is randomized by the scrambler. The preamble is always transmitted as a DBPSK waveform (1Mbps). The duration of the long preamble and header is 192µs.

In the short preamble mode, the modem uses a synchronization field of 56 zero symbols along with an SFD transmitted at 1Mbps. The short header is transmitted at 2Mbps. The synchronization preamble is all 0's to distinguish it from the long header mode and the short preamble SFD is the time reverse of the long preamble SFD. The duration of the short preamble and header is 96µs.

Start Frame Delimiter (SFD) Field (16 Bits) - This field is used to establish the link frame timing. The HFA3861A will not declare a valid data packet, even if it PN acquires, unless it detects the SFD. The HFA3861A receiver is programmed to time out searching for the SFD via CR 10 BITS 4 and 5. The timer starts counting the moment that initial PN synchronization has been established on the preamble.

The four fields for the header shown in Figure 8 are:

Signal Field (8 Bits) - This field indicates what data rate the data packet that follows the header will be. The HFA3861A receiver looks at the signal field to determine whether it needs to switch from DBPSK demodulation into DQPSK, or CCK demodulation at the end of the preamble and header fields.

Service Field (8 Bits) - The MSB of this field is used to indicate the correct length when the length field value is ambiguous at 11Mbps. See IEEE STD 802.11 for definition of the other bits. These bits are not used by the HFA3861A.

Length Field (16 Bits) - This field indicates the number of microseconds it will take to transmit the payload data (PSDU). The external controller (MAC) will check the length field in determining when it needs to de-assert RX_PE.

CCITT - CRC 16 Field (16 Bits) - This field includes the 16-bit CCITT - CRC 16 calculation of the three header fields. This value is compared with the CCITT - CRC 16 code calculated at the receiver. The HFA3861A receiver will indicate a CCITT - CRC 16 error via CR24 bit 2 and will lower MD_RDY and reset the receiver to the acquisition mode if there is an error.

The CRC or cyclic Redundancy Check is a CCITT CRC-16 FCS (frame check sequence). It is the ones compliment of the remainder generated by the modulo 2 division of the protected bits by the polynomial:

$x^{16} + x^{12} + x^5 + 1$

The protected bits are processed in transmit order. All CRC calculations are made prior to data scrambling. A shift register with two taps is used for the calculation. It is preset to all ones and then the protected fields are shifted through the register. The output is then complemented and the residual shifted out MSB first.

The following Configuration Registers (CR) are used to program the preamble/header functions, more programming details about these registers can be found in the Control Registers section of this document:

CR 4 - Defines the preamble length minus the SFD in symbols. The 802.11 protocol requires a setting of 128d = 80h for the mandatory long preamble and 56d = 38h for the optional short preamble.

CR 10 Bits 4, 5 - Define the length of time that the demodulator searches for the SFD before returning to acquisition.

CR 5 Bits 0, 1 - These bits of the register set the Signal field to indicate what modulation is to be used for the data portion of the packet.

CR 6 - The value to be used in the Service field.

CR 7 and 8 - Defines the value of the transmit data length field. This value includes all symbols following the last header field symbol and is in microseconds required to transmit the data at the chosen data rate.

The packet consists of the preamble, header and MAC protocol data unit (MPDU). The data is transmitted exactly as received from the control processor. Some dummy bits will be appended to the end of the packet to insure an orderly shutdown of the transmitter. This prevents spectrum splatter. At the end of a packet, the external controller is expected to de-assert the TX_PE line to shut the transmitter down.

Scrambler and Data Encoder Description

The modulator has a data scrambler that implements the scrambling algorithm specified in the IEEE 802.11 standard. This scrambler is used for the preamble, header, and data in all modes. The data scrambler is a self synchronizing circuit. It consists of a 7-bit shift register with feedback from specified taps of the register. Both transmitter and receiver use the same scrambling algorithm. The scrambler can be disabled by setting CR32 bit 2 to 1.

NOTE: Be advised that the IEEE 802.11 compliant scrambler in the HFA3861A has the property that it can lock up (stop scrambling) on random data followed by repetitive bit patterns. The probability of this happening is 1/128. The patterns that have been identified are all zeros, all ones, repeated 10s, repeated 1100s, and repeated 111000s. Any break in the repetitive pattern will restart the scrambler. To insure that this does not cause any problem, the CCK waveform uses a ping pong differential coding scheme that breaks up repetitive 0s patterns.

FIGURE 8. 802.11 PREAMBLE/HEADER

Scrambling is done by a division using a prescribed polynomial as shown in Figure 9. A shift register holds the last quotient and the output is the exclusive-or of the data and the sum of taps in the shift register. The taps are programmable. The transmit scrambler seed is Hex 1B for the long preamble or 6C for the short preamble and can be set with CR36 or CR37.

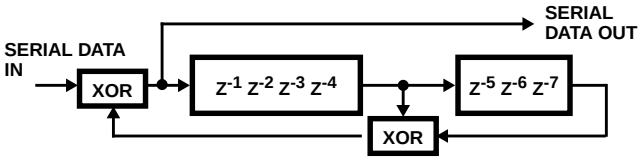


FIGURE 9. SCRAMBLING PROCESS

For the 1Mbps DBPSK data rates and for the header in all rates, the data coder implements the desired DBPSK coding by differential encoding the serial data from the scrambler and driving both the I and Q output channels together. For the 2Mbps DQPSK data rate, the data coder implements the desired coding as shown in the DQPSK Data Encoder table. This coding scheme results from differential coding of dibits (2 bits). Vector rotation is counterclockwise although bits 6 and 7 of configuration register **CR 1** can be used to reverse the rotation sense of the TX or RX signal if desired.

TABLE 4. DQPSK DATA ENCODER

PHASE SHIFT	DIBIT PATTERN (d0, d1) d0 IS FIRST IN TIME
0	00
+90	01
+180	11
-90	10

Spread Spectrum Modulator Description

The modulator is designed to generate DBPSK, DQPSK, and CCK spread spectrum signals. The modulator is capable of automatically switching its rate where the preamble is DBPSK modulated, and the data and/or header are modulated differently. The modulator can support date rates of 1, 2, 5.5 and 11Mbps. The programming details to set up the modulator are given at the introductory paragraph of this section. The HFA3861A utilizes Quadraphase (I/Q) modulation at baseband for all modulation modes.

In the 1Mbps DBPSK mode, the I and Q Channels are connected together and driven with the output of the scrambler and differential encoder. The I and Q Channels are then both multiplied with the 11-bit Barker word at the spread rate. The I and Q signals go to the Quadrature upconverter (HFA3724) to be modulated onto a carrier. Thus, the spreading and data modulation are BPSK modulated onto the carrier.

For the 2Mbps DQPSK mode, the serial data is formed into dibits or bit pairs in the differential encoder as detailed above. One of the bits from the differential encoder goes to the I Channel and the other to the Q Channel. The I and Q Channels are then both multiplied with the 11-bit Barker word at the spread rate. This forms QPSK modulation at the symbol rate with BPSK modulation at the spread rate.

CCK Modulation

The spreading code length is 8 and based on complementary codes. The chipping rate is 11Mchip/s and the symbol duration is exactly 8 complex chips long. The following formula is used to derive the CCK code words that are used for spreading both 5.5 and 11Mbps:

$$c = \left\{ e^{j(\varphi_1+\varphi_2+\varphi_3+\varphi_4)}, e^{j(\varphi_1+\varphi_3+\varphi_4)}, e^{j(\varphi_1+\varphi_2+\varphi_4)}, -e^{j(\varphi_1+\varphi_4)}, e^{j(\varphi_1+\varphi_2+\varphi_3)}, e^{j(\varphi_1+\varphi_3)}, -e^{j(\varphi_1+\varphi_2)}, e^{j\varphi_1} \right\}$$

(LSB to MSB), where c is the code word.

The terms: φ1, φ2, φ3, and φ4 are defined below for 5.5Mbps and 11Mbps.

This formula creates 8 complex chips (LSB to MSB) that are transmitted LSB first. The coding is a form of the generalized Hadamard transform encoding where φ1 is added to all code chips, φ2 is added to all odd code chips, φ3 is added to all odd pairs of code chips and φ4 is added to all odd quads of code chips.

The phases φ1 modify the phase of all code chips of the sequence and are DQPSK encoded for 5.5 and 11Mbps. This will take the form of rotating the whole symbol by the appropriate amount relative to the phase of the preceding symbol. Note that the last chip of the symbol defined above is the chip that indicates the symbol's phase.

For the 5.5Mbps CCK mode, the output of the scrambler is partitioned into nibbles. The first two bits are encoded as differential modulation in accordance with Table 5 . All odd numbered symbols of the short Header or MPDU are given an extra 180 degree (π) rotation in addition to the standard DQPSK modulation as shown in the table. The symbols of the MPDU shall be numbered starting with "0" for the first symbol for the purposes of determining odd and even symbols. That is, the MPDU starts on an even numbered symbol. The last data dibits d2, and d3 CCK encode the basic symbol as specified in Table 6. This table is derived from the formula above by setting φ2 = (d2*pi)+ pi/2, φ3 = 0, and φ4 = d3*pi. In the table d2 and d3 are in the order shown and the complex chips are shown LSB to MSB (left to right) with LSB transmitted first.

TABLE 5. DQPSK ENCODING TABLE

DIBIT PATTERN (d(0), d(1)) d(0) IS FIRST IN TIME	EVEN SYMBOLS PHASE CHANGE (+jω)	ODD SYMBOLS PHASE CHANGE (+jω)
00	0	π
01	π/2	3π/2 (-π/2)
11	π	0
10	3π/2 (-π/2)	π/2

TABLE 6. 5.5Mbps CCK ENCODING TABLE

d2, d3								
00 :	1*j*	1	1*j*	-1	1*j*	1	-1*j*	1
01 :	-1*j*	-1	-1*j*	1	1*j*	1	-1*j*	1
10 :	-1*j*	1	-1*j*	-1	-1*j*	1	1*j*	1
11 :	1*j*	-1	1*j*	1	-1*j*	1	1*j*	1

At 11Mbps, 8 bits (d0 to d7; d0 first in time) are transmitted per symbol.

The first dibit (d0, d1) encodes φ1 based on DQPSK. The DQPSK encoder is specified in Table 6 above. The phase change for φ1 is relative to the phase φ1 of the preceding symbol. In the case of rate change, the phase change for φ1 is relative to the phase φ1 of the preceding CCK symbol. All odd numbered symbols of the MPDU are given an extra 180 degree (π) rotation in accordance with the DQPSK modulation as shown in Table 7. Symbol numbering starts with “0” for the first symbol of the MPDU.

The data dibits: (d2, d3), (d4, d5), (d6, d7) encode φ2, φ3, and φ4 respectively based on QPSK as specified in Table 7. Note that this table is binary, not Grey, coded.

TABLE 7. QPSK ENCODING TABLE

DIBIT PATTERN (d(i), d(i+1)) d(i) IS FIRST IN TIME	PHASE
00	0
01	π/2
10	π
11	3π/2 (-π/2)

TX Power Control

The transmitter power can be controlled by the MAC via two registers. The first register, CR58, contains the results of power measurements digitized by the HFA3861A. By comparing this measurement to what the MAC needs for transmit power, the MAC can determine whether to raise or lower the transmit power. It does this by writing the power level desired to register CR31.

Clear Channel Assessment (CCA) and Energy Detect (ED) Description

The clear channel assessment (CCA) circuit implements the carrier sense portion of a carrier sense multiple access (CSMA) networking scheme. The Clear Channel Assessment (CCA) monitors the environment to determine when it is feasible to transmit. The CCA circuit in the HFA3861A can be programmed to be a function of RSSI (energy detected on the channel), CS1, SQ1, or both. The CCA output can be ignored, allowing transmissions independent of any channel conditions. The CCA in combination with the visibility of the various internal parameters (i.e., Energy Detection measurement results), can assist an external processor in executing algorithms that can adapt to the environment. These algorithms can increase network throughput by minimizing collisions and reducing transmissions liable to errors.

There are three measures that can be used in the CCA assessment. The receive signal strength indication (RSSI) which indicates the energy at the antenna, CS1 and carrier sense (SQ1). SQ1 becomes active only when a spread signal with the proper PN code has been detected, and the peak correlation amplitude to sidelobe ratio exceeds a set threshold, so it may not be adequate in itself.

CS1 becomes active anytime the AGC portion of the circuit becomes unlocked, which is likely at the onset of a signal that is strong enough to support 11Mbps, but may not occur with the onset of a signal that is only strong enough to support 1 or 2MBps. CS1 stays active until the AGC locks and a SQ1 assessment is done, if SQ1 is false, then CS1 is cleared, which deasserts CCA. If SQ1 is true, then tracking is begun, and CCA continues to show the channel busy. CS1 may occur at any time during acquisition as the AGC state machine runs asynchronously with respect to slot times.

A SQ1 evaluation occurs whenever the AGC has remained locked for the entire data ingest period, when this happens, SQ1 is updated between 8 and 9µs into the 10µs dwell. If CS1 is not active, two consecutive SQ1’s are required to advance the part to tracking.

The state of CCA is not guaranteed from the time RX_PE goes high until the first CCA assessment is made. At the end of a packet, after RXPE has been deasserted, the state of CCA is also not guaranteed.

The receive signal strength indication (RSSI) measurement is derived from the state of the AGC circuit. ED is the comparison result of RSSI against a threshold. The threshold may be set to an absolute power value, or it may be set to be N dB above the measured noise floor. See CR 38. The HFA3861A measures and stores the RSSI level when it detects no presence of BPSK or QPSK signals. The smallest value of a 256 value buffer is taken to be the noise floor. Thus, the value of the noise floor will adapt to the environment. A separate noise floor value is maintained for each antenna. An initial value of the noise floor is

established within 50µs of the chip being active and is refined as goes on. Deasserting RX_PE does not corrupt the learned values. If the absolute power metric is chosen, this threshold is normally set to between -70 and -80dBm.

If desired, ED may be used in the acquisition process as well as CCA. ED may be used to mask (squelch) weak signals and prevent radio reception of signals too weak to support the high data rates, signals from adjacent cells, networks, or buildings. See CR48.

The Configuration registers effecting the CCA algorithm operation are summarized below (more programming details on these registers can be found under the Control Registers section of this document).

The CCA output from pin 60 of the device can be defined as active high or active low through CR **1** (bit 2).

CR9(6:5) allow CCA to be programmed to be a function of ED only, the logical operation of (CS1 OR SQ1), the logical function of (ED AND (CS1 OR SQ1)), or (ED OR (CS1 OR SQ1)).

CR11(3) lets the user select from sampled CCA mode, which means CCA will not glitch, is updated once per symbol and is valid for reading at 15.8µs or 19.8µs. In non-sampled mode, CCA may change at anytime, potentially several times per slot, as ED and CS1 operate asynchronously to slot times.

In a typical system CCA will be monitored to determine when the channel is clear. Once the channel is detected busy, CCA should be checked periodically to determine if the channel becomes clear. CCA can be programmed to be stable to allow asynchronous sampling or even falling edge detection of CCA. Once MD_RDY goes active, CCA is then ignored for the remainder of the message. Failure to monitor CCA until MD_RDY goes active (or use of a time-out circuit) could result in a stalled system as it is possible for the channel to be busy and then become clear without an MD_RDY occurring.

AGC Description

The AGC system consists of the 3 chips handling the receive signal, the RF to IF downconverter, the IF to baseband converter, and the baseband processor. The AGC loop is digitally controlled by the BBP. Basically it operates as follows:

Initially, the radio is set for high gain. The percent of time that the A/D converters in the baseband processor are saturated is monitored along with signal amplitude and the gain is adjusted down until the amplitude is what will optimize the demodulator's performance. If the amount of saturation is great, the initial gain adjust steps are large. If the signal overload is small, they are less. If the signal level then varies more than a preset amount, the AGC is declared unlocked and the gain again allowed to readjust. When the gain is right and the A/Ds' outputs are within the lock window, the BBP declares AGC lock and stops adjusting for the duration of the packet.

We look for this locked state following an unlocked state as one indication that a received signal is on the antenna. This starts the receive process of looking for PN correlation. Once PN correlation and AGC lock are found, the processor begins acquisition.

For large signals, the power level in the RF stage output is also monitored and if it is large, the LNA stage is shut down. This removes 30dB of gain from the receive chain which is compensated for by replacing 30dB of gain in the IF AGC stage. There is some hysteresis in this operation. This improves the receiver dynamic range.

Demodulator Description

The receiver portion of the baseband processor, performs A/D conversion and demodulation of the spread spectrum signal. It correlates the PN spread symbols, then demodulates the DBPSK, DQPSK, or CCK symbols. The demodulator includes a frequency tracking loop that tracks and removes the carrier frequency offset. In addition it tracks the symbol timing, and differentially decodes (where appropriate) and descrambles the data. The data is output through the RX Port to the external processor.

The PRISM baseband processor, HFA3861A uses differential demodulation for the initial acquisition portion of the message processing and then switches to coherent demodulation for the MPDU demodulation. The HFA3861A is designed to achieve rapid settling of the carrier tracking loop during acquisition. Rapid phase fluctuations are handled with a relatively wide loop bandwidth which is then stepped down as the packet progresses. Coherent processing improves the BER performance margin as opposed to differentially coherent processing for the CCK data rates.

The baseband processor uses time invariant correlation to strip the PN spreading and phase processing to demodulate the resulting signals in the header and DBPSK/DQPSK demodulation modes. These operations are illustrated in Figure 13 which is an overall block diagram of the receiver processor.

In processing the DBPSK header, input samples from the I and Q A/D converters are correlated to remove the spreading sequence. The peak position of the correlation pulse is used to determine the symbol timing. The sample stream is decimated to the symbol rate and corrected for frequency offset prior to PSK demodulation. Phase errors from the demodulator are fed to the NCO through a lead/lag filter to maintain phase lock. The carrier is de-rotated by the carrier tracking loop. The demodulated data is differentially decoded and descrambled before being sent to the header detection section.

In the 1Mbps DBPSK mode, data demodulation is performed the same as in header processing. In the 2Mbps DQPSK mode, the demodulator demodulates two bits per symbol and differentially decodes these bit pairs. The bits are then serialized and descrambled prior to being sent to the output.

In the CCK modes, the receiver removes carrier frequency offsets and uses a bank of correlators to detect the modulation. A biggest picker finds the largest correlation in the I and Q Channels and determines the sign of those correlations. For this to happen, the demodulator must know the starting phase which is determined by referencing the data to the last bit of the header. Each symbol demodulated determines 1 or 2 nibbles of data. This is then serialized and descrambled before being passed to the output.

Chip tracking in the CCK modes is chip decision directed. Carrier tracking is via a lead/lag filter using a digital Costas phase detector.

Acquisition Description

A projected worst case time line for the acquisition of a signal with a short preamble and header is shown. The synchronization part of the preamble is 56 symbols long followed by a 16-bit SFD. The receiver must monitor the antenna to determine if a signal is present. The timeline is broken into 10µs blocks (dwells) for the scanning process.

This length of time is necessary to allow enough integration of the signal to make a good acquisition decision. This worst case time line example assumes that the signal arrives part way into the first dwell such as to just barely catch detection. The signal and the scanning process are asynchronous and the signal could start anywhere. In this timeline, it is assumed that the signal is present in the first 10µs dwell, but was missed due to power amplifier ramp up.

Meanwhile signal quality and signal frequency measurements are made simultaneous with symbol timing measurements. A CS1 followed by SQ1 active, or two consecutive SQ1's will cause the part to exit the acquisition phase and enter the tracking phase.

Prior to initial acquisition the NCO was inactive and DPSK demodulation processing was used. Carrier phase measurement are done on a symbol by symbol basis afterward and coherent DPSK demodulation is in effect. After a brief setup time as illustrated on the timeline of, the signal begins to emerge from the demodulator.

It takes 7 more symbols to seed the descrambler before valid data is available. This occurs in time for the SFD to be received. At this time the demodulator is tracking and in the coherent PSK demodulation mode it will no longer acquire signals.

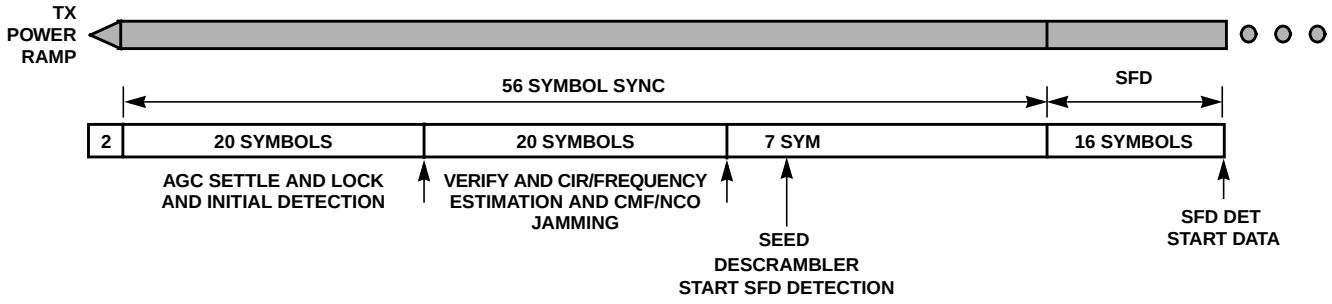


FIGURE 10. ACQUISITION TIMELINE

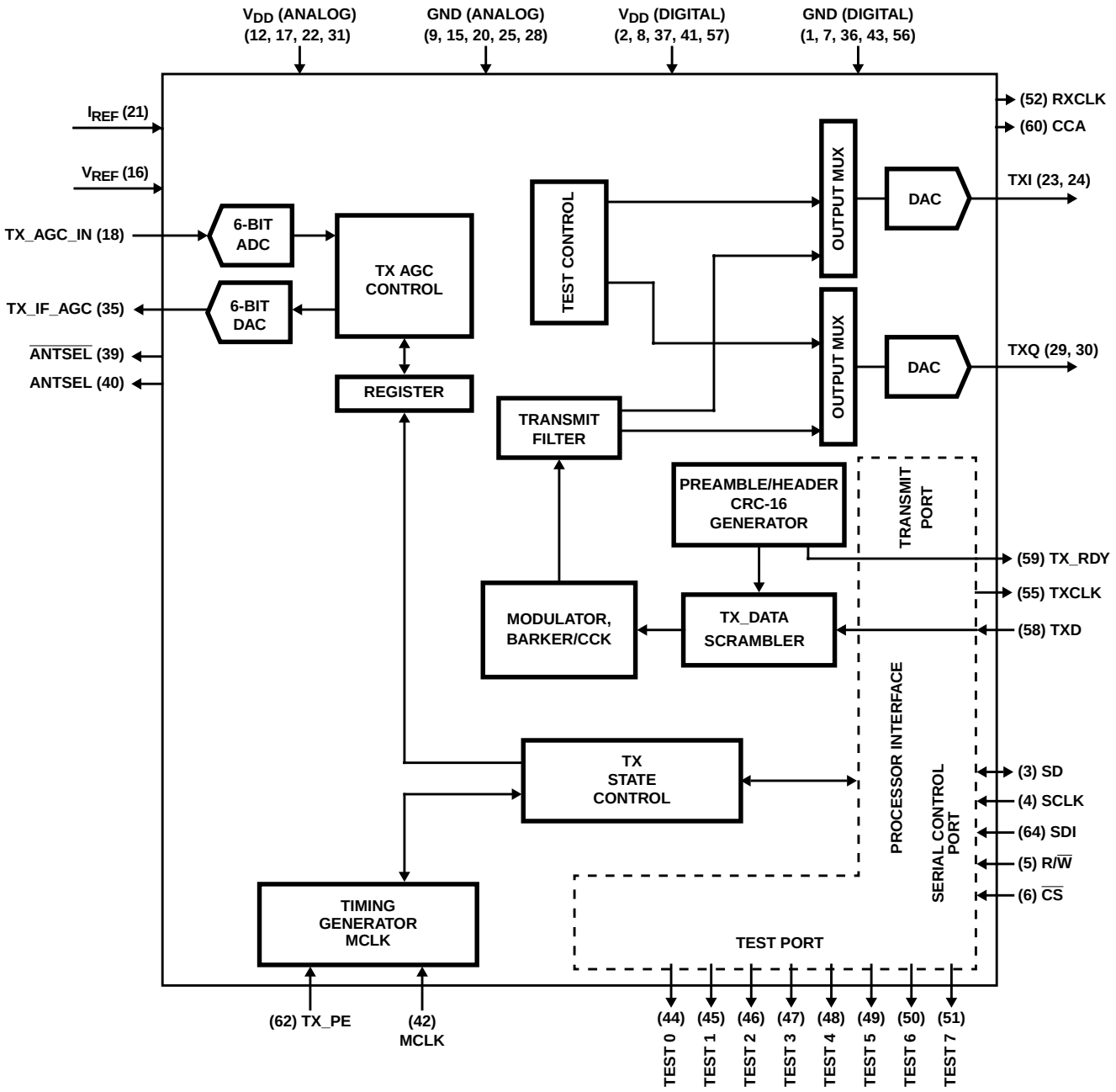


FIGURE 11. DSSS BASEBAND PROCESSOR, TRANSMIT SECTION

PN Correlators Description

There are two types of correlators in the HFA3861A baseband processor. The first is a parallel matched correlator that correlates for the Barker sequence used in preamble, header, and PSK data modes. This PN correlator is designed to handle BPSK spreading with carrier offsets up to ±50ppm and 11 chips per symbol. Since the spreading is BPSK, the correlator is implemented with two real correlators, one for the I and one for the Q Channel. The same Barker sequence is always used for both I and Q correlators.

These correlators are time invariant matched filters otherwise known as parallel correlators. They use one sample per chip for correlation although two samples per chip are processed. The correlator despreads the samples from the chip rate back to the original data rate giving 10.4dB processing gain for 11 chips per bit. While despreading the desired signal, the correlator spreads the energy of any non correlating interfering signal.

The second form of correlator is the correlator function used for detection of the CCK modulation. For the CCK modes, the correlation function uses a Fast Walsh Transform to

correlate the 4 or 64 code possibilities followed by a biggest picker. The biggest picker finds the biggest of 4 or 64 correlator outputs depending on the rate. This is translated into 2 or 6 bits. The detected output is then processed through the differential decoder to demodulate the last two bits of the symbol.

Data Demodulation and Tracking Description (DBPSK and DQPSK Modes)

The signal is demodulated from the correlation peaks tracked by the symbol timing loop (bit sync) as shown in Figure 12. The frequency and phase of the signal is corrected using the NCO that is driven by the phase locked loop. Demodulation of the DBPSK data in the early stages of acquisition is done by differential detection. Once phase locked loop tracking of the carrier is established, coherent demodulation is enabled for better performance. Averaging the phase errors over 10 symbols gives the necessary frequency information for proper NCO operation.

Configuration Register 10 sets the search timer for the SFD. This register sets this time-out length in symbols for the receiver. If the time out is reached, and no SFD is found, the receiver resets to the acquisition mode. The suggested value is the number of preamble symbols plus 16. If different transmit preamble lengths are used by various transmitters in a network, the longest value should be used for the receiver settings.

Data Decoder and Descrambler Description

The data decoder that implements the desired DQPSK coding/decoding as shown in Table 8. The data is formed into pairs of bits called dibits. The left bit of the pair is the first in time. This coding scheme results from differential coding of the dibits. Vector rotation is counterclockwise for a positive phase shift, but can be reversed with bit 7 or 6 of CR **1**.

For DBPSK, the decoding is simple differential decoding.

TABLE 8. DQPSK DATA DECODER

PHASE SHIFT	DIBIT PATTERN (D0, D1) D0 IS FIRST IN TIME
0	00
+90	01
+180	11
-90	10

The data scrambler and de-scrambler are self synchronizing circuits. They consist of a 7-bit shift register with feedback of some of the taps of the register. The scrambler is designed to insure smearing of the discrete spectrum lines produced by the PN code. One thing to keep in mind is that both the differential decoding and the descrambling cause error extension or burst errors. This is due to two properties of the processing. First, the differential decoding process causes errors to occur on pairs of symbols. When a symbol's phase is in error, the next symbol will also be decoded wrong since the data is encoded in the change in phase from one symbol to the next. Thus, two errors are made on two successive symbols. Therefore up to 4 bits may be wrong although on the average only 2 are. In QPSK mode, these may occur next to one another or separated by up to 2 bits. In the CCK mode, when a symbol decision error is made, up to 6 bits may be in error although on average only 3 bits will be in error. Secondly, when the bits are processed by the descrambler, these errors are further extended. The descrambler is a 7-bit shift register with two taps exclusive or'ed with the bit stream. Thus, each error is extended by a factor of three. Multiple errors can be spaced the same as the tap spacing, so they can be canceled in the descrambler. In this case, two wrongs do make a right. Given all that, if a single error is made the whole packet is discarded anyway, so the error extension property has no effect on the packet error rate.

Descrambling is self synchronizing and is done by a polynomial division using a prescribed polynomial. A shift register holds the last quotient and the output is the exclusive-or of the data and the sum of taps in the shift register.

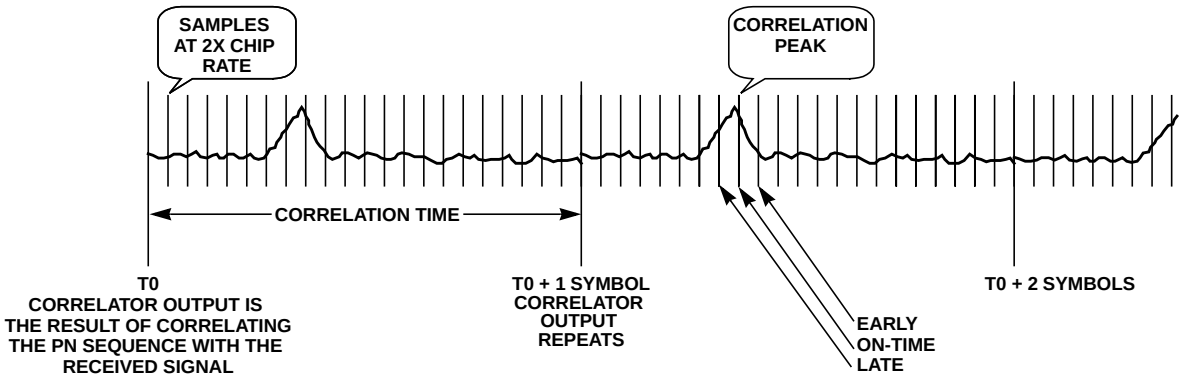


FIGURE 12. CORRELATION PROCESS

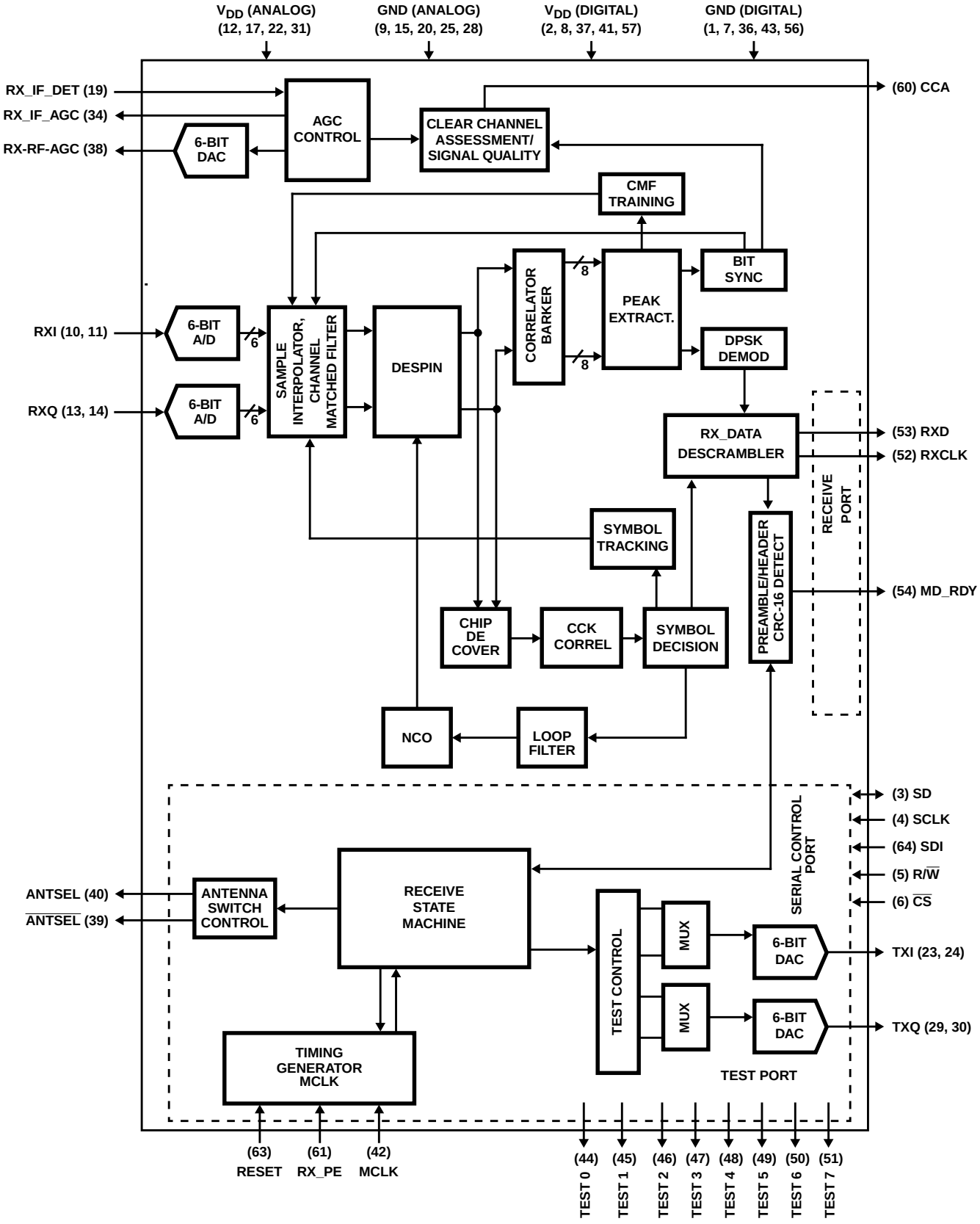


FIGURE 13. DSSS BASEBAND PROCESSOR, RECEIVE SECTION

Data Demodulation in the CCK Modes

In this mode, the demodulator uses Complementary Code Keying (CCK) modulation for the two highest data rates. It is slaved to the low rate processor which it depends on for acquisition of initial timing and phase tracking information. The low rate section acquires the signal, locks up symbol and carrier tracking loops, and determines the data rate to be used for the MPDU data.

The demodulator for the CCK modes takes over when the preamble and header have been acquired and processed. On the last bit of the header, the phase of the signal is captured and used as a phase reference for the high rate differential demodulator.

The signal from the A/D converters is carrier frequency and phase corrected by a DESPIN stage. This removes the frequency offset and aligns the I and Q Channels properly for the correlators. The sample rate is decimated to 11MSPS for the correlators after the DESPIN since the data is now synchronous in time.

The demodulator knows the symbol timing, so the correlation is batch processed over each symbol. The correlation outputs from the correlator are compared to each other in a biggest picker and the chosen one determines 6 bits of the symbol. The QPSK phase of the chosen one determines two more bits for a total of 8 bits per symbol. Six bits come from which of the 64 correlators had the largest output and the last two are determined from the QPSK differential demod of that output. In the 5.5Mbps mode, only 4 of the correlator outputs are monitored. This demodulates 2 bits for which of 4 correlators had the largest output and 2 more for the QPSK demodulation of that output for a total of 4 bits per symbol.

Tracking

Carrier tracking is performed on the de-rotated signal samples from the complex multiplier in a four phase Costas loop. This forms the error term that is integrated in the lead/lag filter for the NCO, closing the loop. Tracking is only measured when there is a chip transition. Note that this tracking is dependent on a positive SNR in the chip rate bandwidth.

The symbol clock is tracked by a sample interpolator that can adjust the sample timing forwards and backwards by 72 increments of 1/8th chip. This approach means that the HFA3861A can only track an offset in timing for a finite interval before the limits of the interpolator are reached. Thus, continuous demodulation is not possible.

Demodulator Performance

This section indicates the typical performance measures for a radio design. The performance data below should be used as a guide. In general, the actual performance depends on the application, interference environment, RF/IF implementation and radio component selection.

Overall Eb/N0 Versus BER Performance

The PRISM chip set has been designed to be robust and energy efficient in packet mode communications. The demodulator uses coherent processing for data demodulation. The figures below show the performance of the baseband processor when used in conjunction with the HFA3783 IF and the PRISM recommended IF filters. Off the shelf test equipment are used for the RF processing. The curves should be used as a guide to assess performance in a complete implementation.

Factors for carrier phase noise, multipath, and other degradations will need to be considered on an implementation by implementation basis in order to predict the overall performance of each individual system.

Figure 14 shows the curves for theoretical DBPSK/DQPSK demodulation with coherent demodulation and descrambling as well as the PRISM performance measured for DBPSK and DQPSK. The theoretical performance for DBPSK and DQPSK are the same as shown on the diagram. Figure 15 shows the theoretical and actual performance of the CCK modes. The losses in both figures include RF and IF radio losses; they do not reflect the HFA3861A losses alone. The HFA3861A baseband processing losses from theoretical are, by themselves, a small percentage of the overall loss.

The PRISM demodulator performs with an implementation loss of less than 3dB from theoretical in a AWGN environment with low phase noise local oscillators. For the 1 and 2Mbps modes, the observed errors occurred in groups of 4 and 6 errors. This is because of the error extension properties of differential decoding and descrambling. For the 5.5 and 11Mbps modes, the errors occur in symbols of 4 or 8 bits each and are further extended by the descrambling. Therefore the error patterns are less well defined.

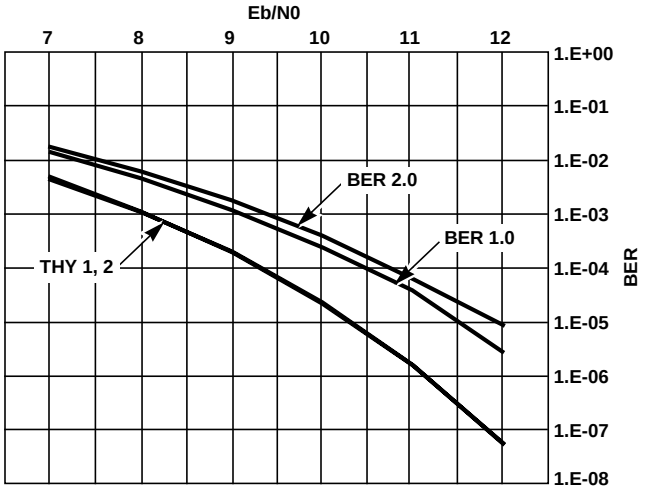


FIGURE 14. BER vs Eb/N0 PERFORMANCE FOR PSK MODES

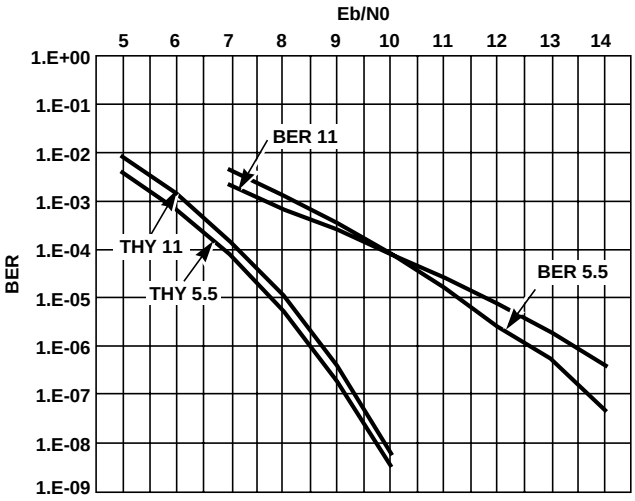


FIGURE 15. BER vs Eb/N0 PERFORMANCE FOR CCK MODES

Clock Offset Tracking Performance

The PRISM baseband processor is designed to accept data clock offsets of up to ±25ppm for each end of the link (TX and RX). This effects both the acquisition and the tracking performance of the demodulator. The budget for clock offset error is 0.75dB at ±50ppm. No appreciable degradation was seen for operation in AWGN at ±50ppm.

Carrier Offset Frequency Performance

The correlators used for acquisition for all modes and for demodulation in the 1 and 2Mbps modes are time invariant matched filter correlators otherwise known as parallel correlators. They use two samples per chip and are tapped at every other shift register stage. Their performance with carrier frequency offsets is determined by the phase roll rate due to the offset. For an offset of +50ppm (combined for both TX and RX) will cause the carrier to phase roll 22.5 degrees over the length of the correlator. This causes a loss of 0.22dB in correlation magnitude which translates directly to Eb/N0 performance loss. In the PRISM chip design, the carrier phase locked loop is inactive during acquisition. During tracking, the carrier tracking loop corrects for offset, so that no degradation is noted. In the presence of high multipath and high SNR, however, some degradation is expected.

A Default Register Configuration

The registers in the HFA3861A are addressed with 7-bit numbers where the lower 1 bit of an 8-bit hexadecimal address is left as unused. This results in the addresses being in increments of 2 as shown in the table below. Table 9 shows the register values for a default 802.11 configuration with various rate configurations. The data is transmitted as either DBPSK, DQPSK, or CCK depending on the configuration chosen. It is recommended that you start with the simplest configuration (DBPSK) for initial test and verification of the device and/or the radio design. The user can later modify the CR contents to reflect the system and the required performance of each specific application.

TABLE 9. CONTROL REGISTER VALUES FOR DUAL ANTENNA DIVERSITY

CONFIGURATION REGISTER	NAME	TYPE	REGISTER ADDRESS HEX	1/2/5.5/11Mbps
CR0	Part/Version Code	R	00	11
CR1	I/O Polarity	R/W	02	00
CR2	I Cover Code	R/W	04	48
CR3	Q Cover Code	R/W	06	48
CR4	TX Preamble Length	R/W	08	80
CR5	TX Signal Field	R/W	0A	03
CR6	TX Service Field	R/W	0C	As Required
CR7	TX Length Field, High	R/W	0E	As Required
CR8	TX Length Field, Low	R/W	10	As Required
CR9	RX/TX Configure	R/W	12	A0
CR10	RX Configure	R/W	14	B8
CR11	RX/TX Configure	R/W	16	1B
CR12	A/D Test Modes 1	R/W	18	00
CR13	A/D Test Modes 2	R/W	1A	00
CR14	A/D Test Modes 3	R/W	1C	00
CR15	AGC GainClip	R/W	1E	5C
CR16	AGC LowerSatCount	R/W	20	81
CR17	AGC TimerCount	R/W	22	20
CR18	AGC HiSat	R/W	24	C4
CR19	AGC LockinLevel/CW detect threshold	R/W	26	06
CR20	AGC LockWindow, pos side	R/W	28	0A
CR21	AGC Threshold	R/W	2A	16
CR22	AGC Lookup Table Addr and Control	R/W	2C	(Note 3)
CR23	AGC Lookup Table Data	R/W	2E	(Note 3)
CR24	AGC LoopGain	R/W	30	2D
CR25	AGC RX_IF	R/W	32	20
CR26	AGC Test Modes	R/W	34	98
CR27	AGC RX_RF Threshold	R/W	36	18
CR28	AGC Low SatAtten	R/W	38	7A
CR29	AGC LockWindow, negative side	R/W	3A	0A
CR30	Carrier Sense 2	R/W	3C	24
CR31	Manual TX Power Control	R/W	3E	BA
CR32	Test Modes 1	R/W	40	00
CR33	Test Modes 2	R/W	42	00
CR34	Test Bus Address	R/W	44	00
CR35	CMF Coefficient Control	R/W	46	0C
CR36	Scrambler Seed, Long Preamble Option	R/W	48	26
CR37	Scrambler Seed, Short Preamble Option	R/W	4A	5B
CR38	ED Threshold	R/W	4C	7F
CR39	CMF Gain Threshold	R/W	4E	29

TABLE 9. CONTROL REGISTER VALUES FOR DUAL ANTENNA DIVERSITY (Continued)

CONFIGURATION REGISTER	NAME	TYPE	REGISTER ADDRESS HEX	1/2/5.5/11Mbps
CR40	Threshold for antenna decision	R/W	50	0F
CR41	Preamble tracking loop lead coefficient	R/W	52	20
CR42	Preamble tracking loop lag coefficient	R/W	54	20
CR43	Header tracking loop lead coefficient	R/W	56	10
CR44	Header tracking loop lag coefficient	R/W	58	10
CR45	Data tracking loop lead coefficient	R/W	5A	10
CR46	Data tracking loop lag coefficient	R/W	5C	10
CR47	RF attenuator value	R/W	5E	1E
CR48	ED and SQ1 control and SQ1 scale factor	R/W	60	1A
CR49	Read only register mux control for registers 50 to 63	R/W	62	00
CR50	a&b: Test Bus Read	R	64	N/A
CR51	a: Noise floorAntA b: Signal Quality Measure Based on Carrier Tracking	R	66	N/A
CR52	a: Noise floorAntB b: Received Signal Field	R	68	N/A
CR53	a: AGC error b: Received Service Field	R	6A	N/A
CR54	b: Received Length Field, Low	R	6C	N/A
CR55	b: Received Length Field, High	R	6E	N/A
CR56	b: Calculated CRC on Received Header, Low	R	70	N/A
CR57	b: Calculated CRC on Received Header, High	R	72	N/A
CR58	b: TX Power Measurement	R	74	N/A
CR59	b: RX Mean Power	R	76	N/A
CR60	b: RX_IF AGC	R	78	N/A
CR61	b: RX Status Reg	R	7A	N/A
CR62	b: RSSI	R	7C	N/A
CR63	b: RX Status Reg	R	7E	N/A

NOTE:

3. This register is written, then the data is loaded into register 23 as per the following table.

AGC REGISTER SETTINGS

CR22 DECIMAL	CR23 HEX
00	0C
01	10
02	14
03	18
04	1C
05	20
06	24
07	28
08	2E
09	34
10	38
11	3C
12	3F
13	43
14	46
15	48

AGC REGISTER SETTINGS (Continued)

CR22 DECIMAL	CR23 HEX
16	46
17	50
18	55
19	5A
20	63
21	6D
22	76
23	7F
24	7F
25	7F
26	7F
27	7F
28	7F
29	7F
30	7F
31	7F

Control Registers

The following tables describe the function of each control register along with the associated bits in each control register.

CONFIGURATION REGISTER 0 ADDRESS (0h) R PART/VERSION CODE

Bit 7:4	Part Code 0001 = HFA3861A series
Bit 3:0	Version Code 0001 = 3861A Version

CONFIGURATION REGISTER 1 ADDRESS (02h) R/W I/O POLARITY

	This register is used to define the phase of clocks and other interface signals. 00h is normal setting.
Bit 7	This control bit selects the phase of the receive carrier rotation sense Logic 1 = Inverted rotation (CW), Invert Q in Logic 0 = normal rotation (CCW)
Bit 6	This control bit selects the phase of the transmit carrier rotation sense Logic 1 = Inverted rotation (CW), Invert Q out. Logic 0 = normal rotation (CCW)
Bit 5	This control bit selects the phase of the transmit output clock (TXCLK) pin Logic 1 = Inverted TXCLK Logic 0 = NON-Inverted TXCLK
Bit 4	This control bit selects the active level of the Transmit Ready (TX_RDY) output which is an output pin at the test port, pin Logic 1 = TX_RDY Active 0 Logic 0 = TX_RDY Active 1
Bit 3	This control bit selects the active level of the transmit enable (TX_PE) input pin Logic 1 = TX_PE Active 0 Logic 0 = TX_PE Active 1
Bit 2	This control bit selects the active level of the Clear Channel Assessment (CCA) output pin. Logic 1 = CCA Active 1 Logic 0 = CCA Active 0
Bit 1	This control bit selects the active level of the MD_RDY output pin. Logic 1 = MD_RDY is Active 0 Logic 0 = MD_RDY is Active 1
Bit 0	This controls the phase of the RX_CLK output Logic 1 = Invert Clk Logic 0 = Non-Inverted Clk

CONFIGURATION REGISTER 2 ADDRESS (04h) R/W I COVER CODE

Write to control, Read to verify control, setup while TX_PE and RX_PE are low

Bits 0 - 7	I cover code, nominally 48h

CONFIGURATION REGISTER 3 ADDRESS (06h) R/W Q COVER CODE

Bits 0 - 7	Q cover code, nominally 48h

CONFIGURATION REGISTER 4 ADDRESS (08h) R/W TX PREAMBLE LENGTH

Bits 0 - 7	This register contains the count for the Preamble length counter. Setup while TX_PE is low. For IEEE 802.11 use 80h. For other than IEEE 802.11 applications, in general increasing the preamble length will improve low signal to noise acquisition performance at the cost of greater link overhead. The minimum suggested value is 56d = 38h. These suggested values include a 2 symbol TX power amplifier ramp up. If you program 128 you get 130.

CONFIGURATION REGISTER 5 ADDRESS (0Ah) R/W TX SIGNAL FIELD

Bits 7:4	R/W but not currently used internally, should be set to zero to ensure compatibility with future revisions.
Bits 3	Select preamble mode 0 = Normal, long preamble interoperable with 1 and 2Mbps legacy equipment 1= short preamble and header mode (optional in 802.11)
Bit 2	Reserved, must be set to 0
Bits 1:0	TX data Rate. Must be set at least 2µs before needed in TX frame. This selects TX signal field code from the registers above. 00 = DBPSK - 11 chip sequence (1Mbps) 01 = DQPSK - 11 chip sequence (2Mbps) 10 = CCK - 8 chip sequence (5.5Mbps) 11 = CCK - 8 chip sequence (11Mbps)

CONFIGURATION REGISTER 6 ADDRESS (0Ch) R/W TX SERVICE FIELD

Bits 7:0	R/W but not currently used internally. Bit 7 may be employed by the MAC in 802.11 situations to resolve an ambiguity in the length field when in the 11Mbps mode. Bit 2 should be set to a 1 where the reference oscillator of the radio is common for both the carrier frequency and the data clock. All other bits should be set to 0 to insure compatibility.

CONFIGURATION REGISTER 7 ADDRESS (0Eh) R/W TX LENGTH FIELD (HIGH)

Bits 7:0	This 8-bit register contains the higher byte (bits 8-15) of the transmit Length Field described in the Header. This byte combined with the lower byte indicates the number of microseconds the data packet will take.

CONFIGURATION REGISTER 8 ADDRESS (10h) R/W TX LENGTH FIELD (LOW)

Bits 7:0	This 8-bit register contains the lower byte (bits 0-7) of the transmit Length Field described in the Header. This byte combined with the higher byte indicates the number of microseconds the data packet will take.

CONFIGURATION REGISTER 9 ADDRESS (12h) R/W TX CONFIGURE

Bit 7	CCA sample mode time 0 = 19.9 µs 1 = 15.8 µs
Bits 6:5	CCA mode 00 - CCA is based only on ED 01 - CCA is based on (CS1 OR SQ1/CS2) 10 - CCA is based on (ED AND (CS1 OR SQ1/CS2)) 11 - CCA is based on (ED OR (CS1 | SQ1/CS2))
Bit 4	TX test modes 0 = Alternating bits for carrier suppression test. (Needs scrambler off (CR32 <2> = 1)). 1 = all chips set to 1 for CW carrier. This allows frequency measurement
Bit 3	Enable TX test modes 0 = normal operation 1 = Invoke tests described by bit 4
Bit 2	Antenna choice for TX 0 = Set AntSel low 1 = Set AntSel high
Bit:1	TX Antenna Mode 0 = set AntSel pin to value in bit 2 1 = set AntSel pin to antenna for which last valid header CRC occurred
Bit 0	R/W but not currently used internally, should be set to zero to ensure compatibility with future revisions.

CONFIGURATION REGISTER 10 ADDRESS (14h) R/W RX CONFIGURE

Bit 7	Initial CS2 estimate 0 = Use dot product result 1 = Use SQ1 from Barker correlator peaks see CR30 and CR48 for related thresholds
Bit 6	CIR estimate/ Dot product clock control. 0 = on during acquisition 1 = only on after detect.

CONFIGURATION REGISTER 10 ADDRESS (14h) R/W RX CONFIGURE (Continued)

Bits 5:4	SFD Time-out values 00 = 56µs 01 = 64µs 10 = 128µs 11 = 144µs
Bit 3	MD_RDY control 0 = After CRC16 1 = After SFD
Bit 2	Force F. O. E. in all antenna diversity timelines.
Bit 1	Antenna choice for Receiver when single antenna acquisition is selected 0 = Antenna select pin low 1 = Antenna select pin high
Bit 0	Single or dual antenna acquire 0 = dual antenna for diversity acquisition 1 = single antenna

CONFIGURATION REGISTER 11 ADDRESS (16h) R/W RX-TX CONFIGURE

Bit 7	Continuous internal RX 22 and 44MHz clocks; (Only Reset active will stop) overrides CR10 bit 6. This bit should be loaded to a “1” then to a “0” during initial register loading to ensure receiver initialization.
Bit 6	A/D input coupling 0 = DC 1 = AC (external bias network required)
Bit 5	TX filter / CMF weight select 0 = US 1 = Japan
Bit 4	Ping Pong Differential Encode enable 0 = disabled Ping Pong Differential encoding 1 = normal Ping Pong Differential encoding
Bit 3	CCA mode 0 = normal CCA. CCA will immediately respond to changes in ED, CS1, and SQ1 as configured 1 = Sampled CCA. CCA will update once per slot (20µs), will be valid at 19.8µs or 15.8µs as determined by CR9 bit 7.
Bits 2:0	Precursor value in CIR estimate

CONFIGURATION REGISTER 12 ADDRESS (18h) R/W A/D TEST MODES 1

Bit 7	All DAC and A/D clock source control 0 = normal internal clocks 1 = clock via SDI pin
Bit 6	TX DAC clock 0 = enable 1 = disable
Bit 5	RX DAC clock 0 = enable 1 = disable
Bit 4	I DAC clock 0 = enable 1 = disable
Bit 3	Q DAC clock 0 = enable 1 = disable
Bit 2	RF A/D clock 0 = enable 1 = disable
Bit 1	I A/D clock 0 = enable 1 = disable

CONFIGURATION REGISTER 12 ADDRESS (18h) R/W A/D TEST MODES 1 (Continued)

bit 0	Q A/D clock 0 = enable 1 = disable

CONFIGURATION REGISTER 13 ADDRESS (1Ah) R/W A/D TEST MODES 2

Bit 7	Standby 1 = enable 0 = disable
Bit 6	SLEEPTX 1 = enable 0 = disable
Bit 5	SLEEP RX 1 = enable 0 = disable
Bit 4	SLEEP IQ 1 = enable 0 = disable
Bit 3	Analog TX Shut_down 1 = enable 0 = disable
Bit 2	Analog RX Shut_down 1 = enable 0 = disable
Bit 1	Analog Standby 1 = enable 0 = disable
Bit 0	Enable manual control of mixed signal power down signals using bits 1:7 1 = enable 0 = disable, normal operation (devices controlled by RESET, TX_PE, RX_PE)

CONFIGURATION REGISTER 14 ADDRESS (1Ch) R/W A/D TEST MODES 3

Bit 7	DFS - select straight binary output of I/Q and RF A/D converters
Bits 6:4	I/Q DAC input control. This DAC gives an analog look at various internal digital signals that are suitable for analog representation. 000 = normal (TX filter) 001 = down converter 010 = E/L integrator - upper 6 bits (Q) and AGC error (I) 011 = I/ Q A/D's 100 = Bigger picker output. Upper 6 bits of FWT_I winner and FWT_Q winner 101 = CMF weights - upper 6 bits of all 16 CMF weights are circularly shifted with full scale negative sync pulse interleaved between them 110 = TestBus pins (5:0) when configured as inputs, CR32(4), to both I and Q inputs 111 = Barker Correlator/ low rate samples - as selected by bit 7 CR32
Bit 3	Enable test bus into RX and TX DAC (if below bit is 0) 0 = normal 1 = enable
Bit 2	Enable RF A/D into RX DAC 0 = normal 1 = enable
Bit 1	VRbit1
Bit 0	VRbit0

CONFIGURATION REGISTER 15 ADDRESS (1Eh) R/W AGC CONTROL 1

Bit 7	R/W but not currently used internally, should be set to zero to ensure compatibility with future revisions.
Bits 6:0	AGC gain clip (7-bit value, 0-127) this is the attenuator accumulator upper limit. The lower limit is 0.

CONFIGURATION REGISTER 16 ADDRESS (20h) R/W AGC CONTROL 2

Bits 7:4	AGC mid Sat counts (0-15 range) these are the counts to kick in the attenuator steps (CR28).
Bits 3:0	AGC low Sat Count (0-15 range)

CONFIGURATION REGISTER 17 ADDRESS (22h) R/W AGC CONTROL 4

Bits 7:6	Unused, set to 0
Bit 5:0	AGC timer count (number of clocks in AGC cycle, 32-63 range). Note: Timer count must be > 31.

CONFIGURATION REGISTER 18 ADDRESS (24h) R/W AGC CONTROL 5

Bits 7:4	AGC high sat attenuation (0-30). Note: hi sat attenuation step is actual value programmed times 2. This attenuation step will occur if the # of I and Q saturations is greater than hi sat count.
Bits 3:0	AGC hi sat count (0-15 range)

CONFIGURATION REGISTER 19 ADDRESS (26h) R/W AGC CONTROL 6

Bits 7:5	CW detector scale multiplication factor. (xxxx.x). See CR35 for forcing default weights.
Bits 4:0	AGC Lock-in level (0-7.5 range)

CONFIGURATION REGISTER 20 ADDRESS (28h) R/W AGC CONTROL 7

Bits 7:5	R/W, But Not Used Internally
Bit 4:0	AGC Lock Window positive side (0-15.5 range). Note: outer lock window.

CONFIGURATION REGISTER 21 ADDRESS (2Ah) R/W AGC CONTROL 8

Bits 7,6	R/W but not currently used internally, should be set to zero to ensure compatibility with future revisions.
Bits 5:0	AGC Backoff (xxxxx.x, 0-31.5 range)

CONFIGURATION REGISTER 22 ADDRESS (2Ch) R/W AGC CONTROL 9

Bits 7,6	R/W but not currently used internally, should be set to zero to ensure compatibility with future revisions.
Bits 5	AGC Look up table read control bit 1 = Read AGC table at address given below 0 = Read contents of CR23
Bits 4:0	AGC lookup table address (32 address bits)

CONFIGURATION REGISTER 23 ADDRESS (2Eh) R/W AGC CONTROL 10

Bits 7	R/W but not currently used internally, should be set to zero to ensure compatibility with future revisions.
Bits 6:0	AGC look up table data unsigned

CONFIGURATION REGISTER 24 ADDRESS (30h) R/W AGC CONTROL 11

Bits 7	R/W but not currently used internally, should be set to zero to ensure compatibility with future revisions.
Bit 6:0	AGC loop gain (0.xxxx - x.00000, 0 - 1.0000 range)

CONFIGURATION REGISTER 25 ADDRESS (32h) R/W AGC CONTROL 12

Bits 7	AGC RX_RF, This input drives the RX-RF control if AGC override Enable is set to 1
Bits 6:0	AGC RX_IF, This reg is input to RF-IF DAC if AGC override Enable is set to 1. When polarity bit is zero, a “1” removes 30dB pad, a “0” inserts 30dB pad.

CONFIGURATION REGISTER 26 ADDRESS (34h) R/W AGC TEST MODES

Bits 7	AGC continuous update 0 = disable 1 = allow updates during freeze AGC and AGClock. CR26 bit 3 must be a ‘1’ for this mode to work.
Bit 6	rxRFAGC polarity control. 0 = normal 1 = invert
Bit 5	AGC extra update disable. Allows final update when AGClock is declared 0 = enable an extra update 1 = disable extra update
Bit 4	AGC lock verify 0 = lock verify 1 = disable lock verify
Bit 3	AGC run on freeze- AGC keeps running after acquisition is complete, only signal is updated, no changes to IF or RF gain occur 0 = normal 1 = enabled
Bit 2	AGC override Enable, if set, CR25 controls receiver gain in both RF and IF 0 = normal 1 = enabled
Bit 1	AGC random I/Q allows random data on AGC 6-bit I/Q inputs if PN is enabled 0 = normal 1 = enabled
Bit 0	AGC test math- always accumulates in gain adjust, always outputs mean power from log table. 0 = normal 1 = enabled

CONFIGURATION REGISTER ADDRESS 27 (36h) R/W AGC RF THRESHOLD

Bit 7	RXRF flag 0 = normal 1 = disables threshold
Bits 6:0	AGC threshold (0-64 range)

CONFIGURATION REGISTER ADDRESS 28 (38h) R/W AGC LOW SAT ATTENUATOR

Bits 7:4	Mid sat attenuation (0-30 range). Note: mid sat attenuation is programmed as value times 2. These attenuator steps will occur if the number of I and Q saturations are greater than the mid and low saturation counts set by CR16.
Bits 3:0	low sat attenuation (0-15 range)

CONFIGURATION REGISTER ADDRESS 29 (3Ah) R/W AGC MINIMUM SIGNAL ATTENUATION

Bits 7:5	R/W but not currently used internally, should be set to zero to ensure compatibility with future revisions.
Bits 4:0	AGC lock window negative side. (0-15 range) (outer lock window) Note: set as a positive number, logic will convert to negative.

CONFIGURATION REGISTER ADDRESS 30 (3Ch) R/W CARRIER SENSE 2 SCALE FACTOR

Bits 7:6	R/W but not currently used internally, should be set to zero to ensure compatibility with future revisions.
Bit 5:0	Carrier Sense 2 scale factor (0-7.875 range) (000000 - 100000). Used when DotProduct is source of CS2 calculation

CONFIGURATION REGISTER 31 ADDRESS (3Eh) MANUAL TX POWER CONTROL

Bits 7:1	7 bits to DAC input, -64 to 63 range
Bit 0	unused

CONFIGURATION REGISTER 32 ADDRESS (40h) R/W TEST MODES 1

Bit 7	Selection bit for DAC input test mode 7 0 = Barker 1 = Low rate I/Q samples
Bit 6	force high rate mode 0 = normal 1 = force high rate mode
Bit 5	TX 44 clock enable 0 = Normal 1 = enabled
Bit 4	Tristate test bus and enable inputs 0 = Normal 1 = enable inputs on test bus
Bit 3	Disable spread sequence for 1 and 2Mbps 0 = Normal 1 = disabled
Bit 2	Disable scrambler 0 = normal scrambler operation 1 = scrambler disabled (taps set to 0)
Bit 1	PN generator enable (RX 44MHz clock) 0 = not enabled 1 = enabled. Bit must first be written to a ‘0’ before a ‘1’ to initialize logic.
Bit 0	PN generator enable (RX 22MHz clock) 0 = not enabled 1 = enabled. Bit must first be written to a ‘0’ before a ‘1’ to initialize logic.

CONFIGURATION REGISTER ADDRESS 33 (42h) R/W TEST MODES 2

Bits 7:6	Unused, set to 0
Bit 5	DC offset control 0 = enable DC offset compensation 1 = disable DC offset compensation
Bit 4	Bypass I/Q A/Ds. 0 = disable bypass 1 = 4 MSBs of I/Q data are input on test bus. TESTin 3:0 is [5:2], TESTin 7:4 is Q[5:2], LSBs are zeroed.
Bit 3	disable time adjust 0 = normal 1 = disabled
Bit 2	Internal digital loop back mode (SDI pin becomes LOCK input to acquisition block) 0 = normal chip operation loop back disabled 1 = loop back enabled, A/D and D/A converters bypassed, chip will not respond to external signals
Bit 1	enable PN to lower test bus address (2-0) 0 = normal 1 = PN to test bus address
Bit 0	enable PN to upper test bus address (7-3) 0 = normal 1 = PN to test bus address

CONFIGURATION REGISTER ADDRESS 34 (44h) R/W TEST BUS ADDRESS

Bits 7:0	address bits for various tests. See Tech Brief #TBD for a description of the factory test modes

CONFIGURATION REGISTER ADDRESS 35 (46h) R/W CMF COEFFICIENT CONTROL THRESHOLD

Bit 7	Threshold control 0 = threshold is relative to noise floor 1 = threshold is absolute.
Bit 6:0	Threshold. For 100% calculated weights, set to 80h and set CR19[7:4] to 02h. For 100% default weights, set to 7fh and set CR19[7:4] to 00h.

CONFIGURATION REGISTER ADDRESS 36 (48h) R/W SCRAMBLER SEED LONG PREAMBLE

Bit 7	R/W but not currently used internally, should be set to zero to ensure compatibility with future revisions.
Bit 6:0	Scrambler seed for long preamble bit 3 of CR5 selects CR36 or CR 37

CONFIGURATION REGISTER ADDRESS 37 (4Ah) R/W SCRAMBLER SEED SHORT PREAMBLE

Bit 7	R/W but not currently used internally, should be set to zero to ensure compatibility with future revisions.
Bit 6:0	Scrambler seed for short preamble bit 3 of CR5 selects CR36 or CR 37

CONFIGURATION REGISTER ADDRESS 38 (4Ch) R/W ED THRESHOLD

Bit 7	CR_AGC_EDmode. 0 = noise floor + CR_AGC_EDthresh 1 = absolute threshold
Bit 7:0	CR_AGC_EDthresh. Energy detect threshold, (range 0-127)

CONFIGURATION REGISTER ADDRESS 39 (4Eh) R/W CMF GAIN THRESHOLD

Bit 7:0	Channel Matched filter scale threshold (range 0-255). After CMF is in operation, 8 correlation peaks are accumulated and compared to threshold to determine if there is headroom to scale gain up by a factor of 2. Set to 00h to disable scaling.

CONFIGURATION REGISTER ADDRESS 40 (50h) R/W RSSI ANTENNA THRESHOLD

Bit 7	Threshold. RSSI below this threshold will result in an antenna search. 0 = threshold is relative to noise floor 1 = threshold is absolute
Bits 6:0	Threshold for antenna decision (CR_AGC_AntSearchThresh), range 0-127

CONFIGURATION REGISTER ADDRESS 41 (52h) R/W PREAMBLE LEAD COEFFICIENT

Bit 7:6	R/W but not currently used internally, should be set to zero to ensure compatibility with future revisions.
Bit 5:0	Preamble Lead Coefficient (0-4 range) (000000 - 100000)

CONFIGURATION REGISTER ADDRESS 42 (54h) R/W PREAMBLE LAG COEFFICIENT

Bit 7:6	R/W but not currently used internally, should be set to zero to ensure compatibility with future revisions.
Bit 5:0	Preamble Lag Coefficient (0-4 range) (000000 - 100000)

CONFIGURATION REGISTER ADDRESS 43 (56h) R/W HEADER LEAD COEFFICIENT

Bit 7:6	R/W but not currently used internally, should be set to zero to ensure compatibility with future revisions.
Bit 5:0	Header Lead Coefficient (0-4 range) (000000 - 100000)

CONFIGURATION REGISTER ADDRESS 44 (58h) R/W HEADER LAG COEFFICIENT

Bit 7:6	R/W but not currently used internally, should be set to zero to ensure compatibility with future revisions.
Bit 5:0	Header Lag Coefficient (0-4 range) (000000 - 100000)

CONFIGURATION REGISTER ADDRESS 45 (5Ah) R/W DATA LEAD COEFFICIENT

Bit 7:6	R/W but not currently used internally, should be set to zero to ensure compatibility with future revisions.
Bit 5:0	Data Lead Coefficient (0-4 range) (000000 - 100000)

CONFIGURATION REGISTER ADDRESS 46 (5Ch) R/W DATA LAG COEFFICIENT

Bit 7:6	R/W but not currently used internally, should be set to zero to ensure compatibility with future revisions.
Bit 5:0	Data Lag Coefficient (0-4 range) (000000 - 100000)

CONFIGURATION REGISTER ADDRESS 47 (5Eh) R/W RF ATTENUATOR VALUE

Bit 7:6	R/W but not currently used internally, should be set to zero to ensure compatibility with future revisions.
Bit 5:0	CR_AGC_rxAGCpad value to use in the RSSI calculation. Range 0-63.

CONFIGURATION REGISTER ADDRESS 48 (60h) R/W ED AND SQ1 CONTROL

Bit 7	R/W but not currently used internally, should be set to zero to ensure compatibility with future revisions.
Bit 6	ED and SQ1 control 0 = SQ1 1 = ED and SQ1
Bits 5:0	SQ1 scale factor (0-7.875 range) (000.000-111.111)

CONFIGURATION REGISTER ADDRESS 49 (62h) R/W READ ONLY REGISTER MUX CONTROL

Bit 7	Read only register mux control 0 = READ ONLY registers read ‘b’ value 1 = READ ONLY registers read ‘a’ value
Bits 6:0	R/W but not currently used internally, should be set to zero to ensure compatibility with future revisions.

CONFIGURATION REGISTER ADDRESS 50 (64h) R TEST BUS READ

Bit 7:0	a&b: reads value on test bus

CONFIGURATION REGISTER ADDRESS 51 (66h) R SIGNAL QUALITY MEASURE

Bit 7:0	a: NOISEfloorAntA [7:0] unsigned, range 0-255 b: measures signal quality based on the SNR in the carrier tracking loop

CONFIGURATION REGISTER ADDRESS 52 (68h) R RECEIVED SIGNAL FIELD

Bit 7:0	a: NOISEfloorAntB [7:0] unsigned, range 0-255 b: 8-bit value of received signal field

CONFIGURATION REGISTER ADDRESS 53 (6Ah) R RECEIVED SERVICE FIELD

Bit 7:0	a: MSB unused, AGCerror [6:0] range -64 to 63, no fractional bits b: 8-bit value of received service field

CONFIGURATION REGISTER ADDRESS 54 (6Ch) R RECEIVED LENGTH FIELD, LOW

Bit 7:0	a: unassigned b: 8-bit value of received length field, low byte

CONFIGURATION REGISTER ADDRESS 55 (6Eh) R RECEIVED LENGTH FIELD, HIGH

Bit 7:0	a: unassigned b: 8-bit value of received length field, high byte

CONFIGURATION REGISTER ADDRESS 56 (70h) R CALCULATED CRC ON RECEIVED HEADER, LOW

Bit 7:0	a: unassigned b: 8-bit value of CRC calculated on header, low byte

CONFIGURATION REGISTER ADDRESS 57 (72h) R CALCULATED CRC ON RECEIVED HEADER, HIGH

Bit 7:0	a: unassigned b: 8-bit value of CRC calculated on header, high byte

CONFIGURATION REGISTER ADDRESS 58 (74h) R TX POWER MEASUREMENT

Bit 7:0	a&b: 8-bit value of transmit power measurement (-128 to 127 range)

CONFIGURATION REGISTER ADDRESS 59 (78h) R RX MEAN POWER

Bit 7:0	a&b: Average power of received signal after log table lookup (0-255 range)

CONFIGURATION REGISTER ADDRESS 60 (7Ah) R RX_IF_AGC

Bit 7	a&b: unused
Bits 6:0	a&b: AGC output to the DAC, MSB unused

CONFIGURATION REGISTER ADDRESS 61 (7Ch) R RECEIVE STATUS

Bit 7:5	a&b: unused
Bit 4	a&b: ED, energy detect past threshold
Bit 3	a&b: TX PWR det Reg semaphore - a 1 indicates CR58 has updated since last read
Bit 2	a&b: AGClock - a 1 indicates AGC is within limits of lock window CR20
Bit 1	a&b: hwStopBHit - a 1 indicates rails hit, AGC updates stopped
Bit 0	a&b: RX_RF_AGC - status of AGC output to RF chip

CONFIGURATION REGISTER ADDRESS 62 (7Eh) R RSSI

Bit 7:0	a&b: 8-bit value of RSSI

CONFIGURATION REGISTER ADDRESS 63 (80h) R CALCULATED CRC ON RECEIVED HEADER, HIGH

Bit 7:6	a&b: signal field value 00 = 1 10 = 2 01 = 5.5 or 11
Bit 5	a&b: SFD found
Bit 4	a&b: Short preamble detected
Bit 3	a&b: valid signal field found
Bit 2	a&b: valid CRC 16
Bit 1	a&b: Antenna used on last good packet NA
Bit 0	a&b: not used

Absolute Maximum Ratings

Supply Voltage 4.0V
Input, Output or I/O Voltage . . . . . GND -0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class 2

Operating Conditions

Voltage Range . . . . . +2.70V to +3.60V
Temperature Range . . . . . -40^oC to 85^oC

Thermal Information

Thermal Resistance (Typical, Note 4) θ_{JA} ($^oC/W$)
TQFP Package 60
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Junction Temperature . . . . . 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC
(Lead Tips Only)

Die Characteristics

Gate Count . . . . . 175,000 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

4. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

V_{CC} = 3.0V to 3.3V ±10%, T_A = -40^oC to 85^oC

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Power Supply Current	I_{CCOP}	V_{CC} = 3.6V, CLK Frequency 44MHz (Notes 5, 6, 7)	-	50	60	mA
Standby Power Supply Current	I_{CCSB}	V_{CC} = Max, Outputs Not Loaded	-	0.5	1	mA
Input Leakage Current	I_I	V_{CC} = Max, Input = 0V or V_{CC}	-10	1	10	µA
Output Leakage Current	I_O	V_{CC} = Max, Input = 0V or V_{CC}	-10	1	10	µA
Logical One Input Voltage	V_{IH}	V_{CC} = Max, Min	0.7 V_{CC}	-	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = Min, Max	-	-	$V_{CC}/3$	V
Logical One Output Voltage	V_{OH}	I_{OH} = -1mA, V_{CC} = Min	V_{CC}-0.2	-	-	V
Logical Zero Output Voltage	V_{OL}	I_{OL} = 2mA, V_{CC} = Min	-	0.1	0.2	V
Input Capacitance	C_{IN}	CLK Frequency 1MHz. All measurements referenced to GND. T_A = 25^oC, Note 6	-	5	10	pF
Output Capacitance	C_{OUT}		-	5	10	pF

NOTES:

5. Output load 40pF.
6. Not tested, but characterized at initial design and at major process/design changes.
7. User must allow for peak supply current of 100mA that lasts for 20µs when cir estimate is run, once per packet.

AC Electrical Specifications

V_{CC} = 3.0V to 3.3V ±10%, T_A = -40^oC to 85^oC (Note 8)

PARAMETER	SYMBOL	MCLK = 44MHz		UNITS
		MIN	MAX	
MCLK Period	t_{CP}	22.5	-	ns
MCLK Duty Cycle		40/60	60/40	%
Rise/Fall (All Outputs)		-	10	ns (Notes 9, 10)
TX_PE to I_{OUT}/Q_{OUT} (1st Valid Chip)	t_{D1}	2.18	2.3	µs (Notes 9, 11)
TX_PE Inactive Width	t_{TLP}	2.22	-	µs (Notes 9, 12)
TX_CLK Width Hi or Low	t_{TCD}	40	-	ns
TX_RDY Active to 1st TX_CLK Hi	t_{RC}	260	-	ns
Setup TXD to TX_CLK Hi	t_{TDS}	30	-	ns
Hold TXD to TX_CLK Hi	t_{TDH}	0	-	ns
TX_CLK to TX_PE Inactive (1Mbps)	t_{PEH}	0	965	ns (Notes 9, 20)
TX_CLK to TX_PE Inactive (2Mbps)	t_{PEH}	0	420	ns (Notes 9, 20)
TX_CLK to TX_PE Inactive (5.5Mbps)	t_{PEH}	0	160	ns (Notes 9, 20)

AC Electrical Specifications V_{CC} = 3.0V to 3.3V ±10%, T_A = -40°C to 85°C (Note 8) **(Continued)**

PARAMETER	SYMBOL	MCLK = 44MHz		UNITS
		MIN	MAX	
TX_CLK to TX_PE Inactive (11Mbps)	t_{PEH}	0	65	ns (Notes 9, 20)
TX_RDY Inactive to Last Chip of MPDU Out	t_{RI}	-20	800	ns
TXD Modulation Extension	t_{ME}	2	-	µs (Notes 9, 13)
RX_PE Inactive Width	t_{RLP}	70	-	ns (Notes 9, 14)
RX_CLK Period (11Mbps Mode)	t_{RCP}	90	-	ns
RX_CLK Width Hi or Low (11Mbps Mode)	t_{RCD}	44	-	ns
RX_CLK to RXD	t_{RDD}	25	60	ns
MD_RDY to 1st RX_CLK	t_{RD1}	940	-	ns (Notes 9, 17)
RXD to 1st RX_CLK	t_{RD1}	940	-	ns
Setup RXD to RX_CLK	t_{RDS}	31	-	ns
RX_CLK to RX_PE Inactive (1Mbps)	t_{REH}	0	925	ns (Notes 9, 15)
RX_CLK to RX_PE Inactive (2Mbps)	t_{REH}	0	380	ns (Notes 9, 15)
RX_CLK to RX_PE Inactive (5.5Mbps)	t_{REH}	0	140	ns (Notes 9, 15)
RX_CLK to RX_PE Inactive (11Mbps)	t_{REH}	0	50	ns (Notes 9, 15)
RX_PE inactive to MD_RDY Inactive	t_{RD2}	5	30	ns (Note 16)
Last Chip of SFD in to MD_RDY Active	t_{RD3}	2.77	2.86	µs (Notes 9, 17)
RX Delay		2.77	2.86	µs (Notes 9, 18)
RESET Width Active	t_{RPW}	50	-	ns (Notes 9, 19)
RX_PE to CCA Valid	t_{CCA}	-	16	µs (Note 9)
RX_PE to RSSI Valid	t_{CCA}	-	16	µs (Note 9)
SCLK Clock Period	t_{SCP}	90	-	ns
SCLK Width Hi or Low	t_{SCW}	20	-	ns
Setup to SCLK + Edge (SD, SDI, R/W, CS)	t_{SCS}	30	-	ns
Hold Time from SCLK + Edge (SD, SDI, R/W, CS)	t_{SCH}	0	-	ns
SD Out Delay from SCLK + Edge	t_{SCD}	-	30	ns
SD Out Enable/Disable from R/W	t_{SCED}	-	15	ns (Note 9)
TEST 0-7, CCA, ANTSEL, TEST_CK from MCLK	t_{D2}	-	40	ns

NOTES:

8. AC tests performed with C_L = 40pF, I_{OL} = 2mA, and I_{OH} = -1mA. Input reference level all inputs $V_{CC}/2$. Test $V_{IH} = V_{CC}$, V_{IL} = 0V; $V_{OH} = V_{OL} = V_{CC}/2$.
9. Not tested, but characterized at initial design and at major process/design changes.
10. Measured from V_{IL} to V_{IH}.
11. I_{OUT}/Q_{OUT} are modulated before first valid chip of preamble is output to provide ramp up time for RF/IF circuits.
12. TX_PE must be inactive before going active to generate a new packet.
13. I_{OUT}/Q_{OUT} are modulated after last chip of valid data to provide ramp down time for RF/IF circuits.
14. RX_PE must be inactive at least 3 MCLKs before going active to start a new CCA or acquisition.
15. RX_PE active to inactive delay to prevent next RX_CLK.
16. Assumes RX_PE inactive after last RX_CLK.
17. MD_RDY programmed to go active after SFD detect. (measured from I_{IN}, Q_{IN}).
18. MD_RDY programmed to go active at MPDU start. Measured from first chip of first MPDU symbol at I_{IN}, Q_{IN} to MD_RDY active.
19. Minimum time to insure Reset. RESET must be followed by an RX_PE pulse to insure proper operation. This pulse should not be used for first receive or acquisition.
20. Delay from TXCLK to inactive edge of TXPE to prevent next TXCLK. Because TXPE asynchronously stops TXCLK, TXPE going inactive within 40ns of TXCLK will cause TXCLK minimum hi time to be less than 40ns.

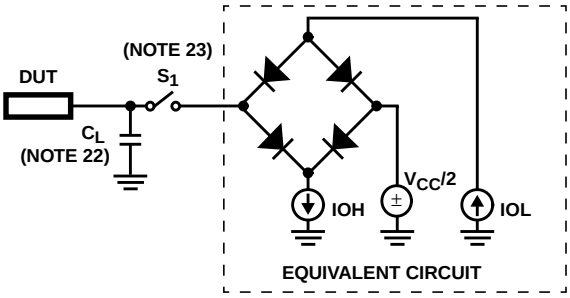
I and Q A/D AC Electrical Specifications (Note 21)

PARAMETER	MIN	TYP	MAX	UNITS
Full Scale Input Voltage (V_{P-P})	0.25	0.50	1.0	V
Input Bandwidth (-0.5dB)	-	20	-	MHz
Input Capacitance	-	5	-	pF
Input Impedance (DC)	5	-	-	kΩ
FS (Sampling Frequency)	-	-	22	MHz

NOTE:

21. Not tested, but characterized at initial design and at major process/design changes.

Test Circuit



NOTES:

22. Includes Stray and JIG Capacitance.

23. Switch S_1 Open for I_{CCSB} and I_{CCOP}.

FIGURE 16. TEST LOAD CIRCUIT

Waveforms

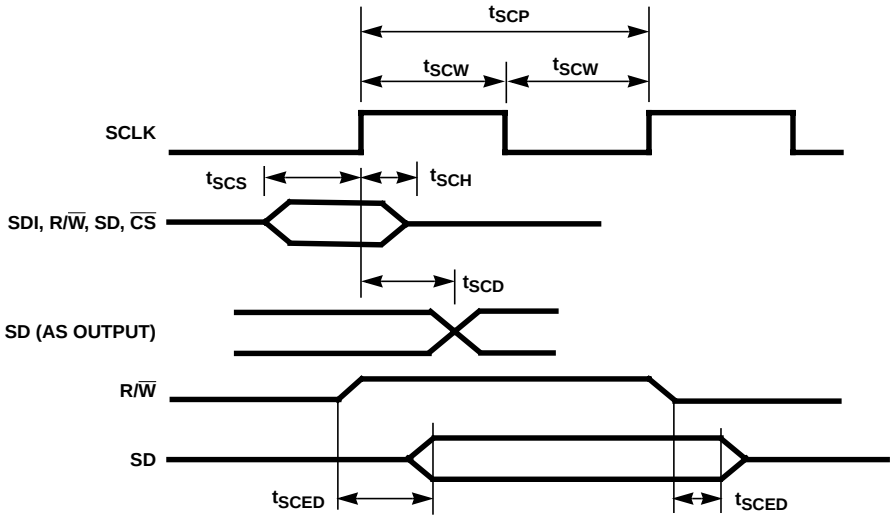


FIGURE 17. SERIAL CONTROL PORT SIGNAL TIMING

Waveforms (Continued)

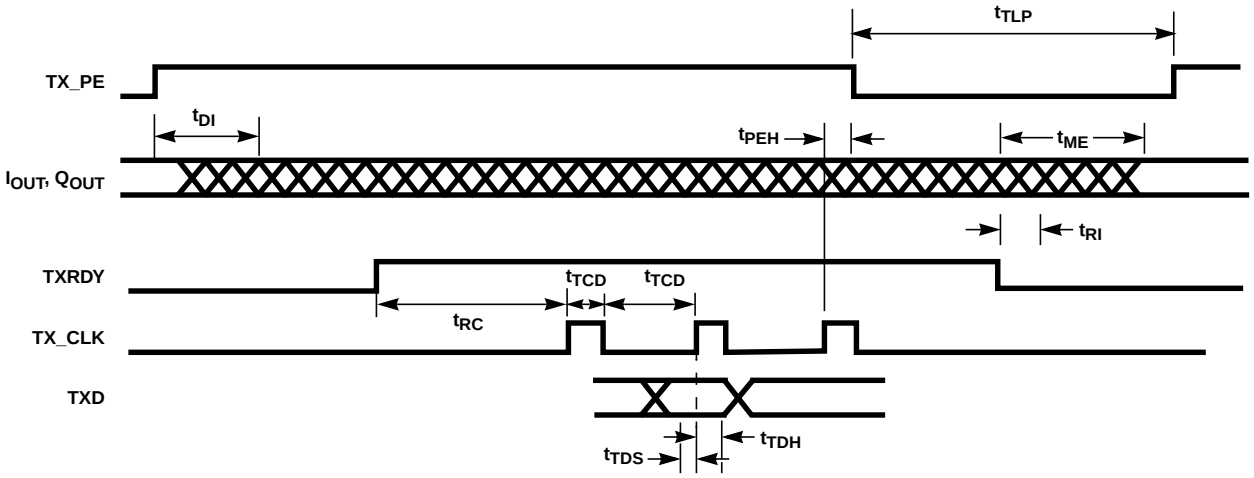
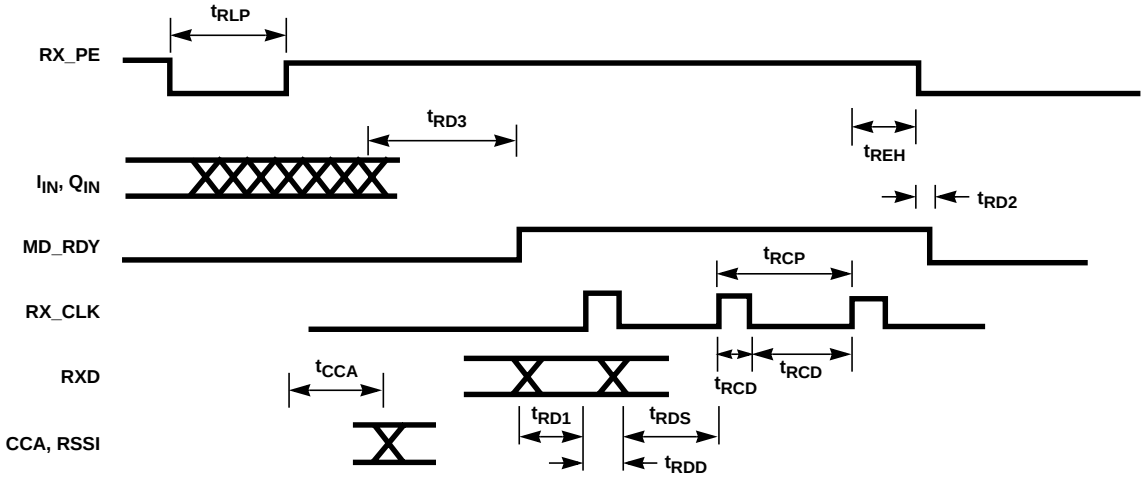


FIGURE 18. TX PORT SIGNAL TIMING



NOTE: RXD, MD_RDY is output two MCLK after RXCLK rising to provide hold time. RSSI Output on TEST (5:0).

FIGURE 19. RX PORT SIGNAL TIMING

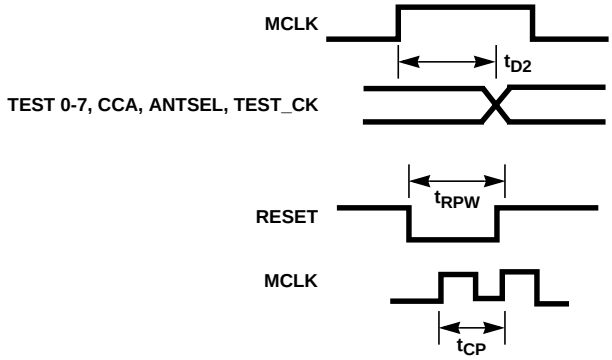
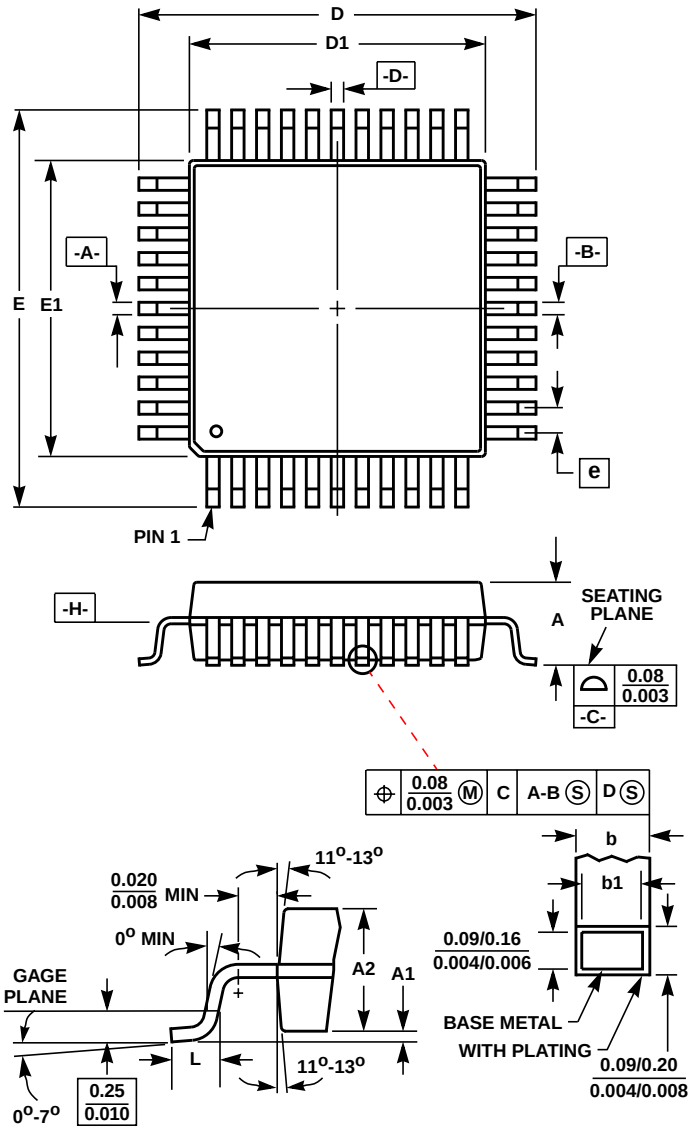


FIGURE 20. MISCELLANEOUS SIGNAL TIMING

Thin Plastic Quad Flatpack Packages (TQFP)



Q64.10x10 (JEDEC MS-026ACD ISSUE B)
64 LEAD THIN PLASTIC QUAD FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.005	0.05	0.15	-
A2	0.038	0.041	0.95	1.05	-
b	0.007	0.010	0.17	0.27	6
b1	0.007	0.009	0.17	0.23	-
D	0.468	0.476	11.90	12.10	3
D1	0.390	0.397	9.9	10.10	4, 5
E	0.468	0.476	11.9	12.10	3
E1	0.390	0.397	9.9	10.10	4, 5
L	0.018	0.029	0.45	0.75	-
N	64		64		7
e	0.020 BSC		0.50 BSC		-

Rev. 0 7/98

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm (0.003 inch).
7. “N” is the number of terminal positions.

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (321) 724-7000
FAX: (321) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029

Attachement-3

Datasheet of HFA3683.

Data Sheet | October 1999 | File Number 4634.3

2.4GHz RF/IF Converter and Synthesizer

The HFA3683A is a monolithic SiGe half duplex RF/IF transceiver designed to operate in the 2.4GHz ISM band. The receive chain features a low noise, gain selectable amplifier (LNA) followed by a down-converter mixer. An up-converter mixer and a high performance preamplifier compose the transmit chain. The remaining circuitry comprises a high frequency Phase Locked Loop (PLL) synthesizer with a three wire programmable interface for local oscillator applications.

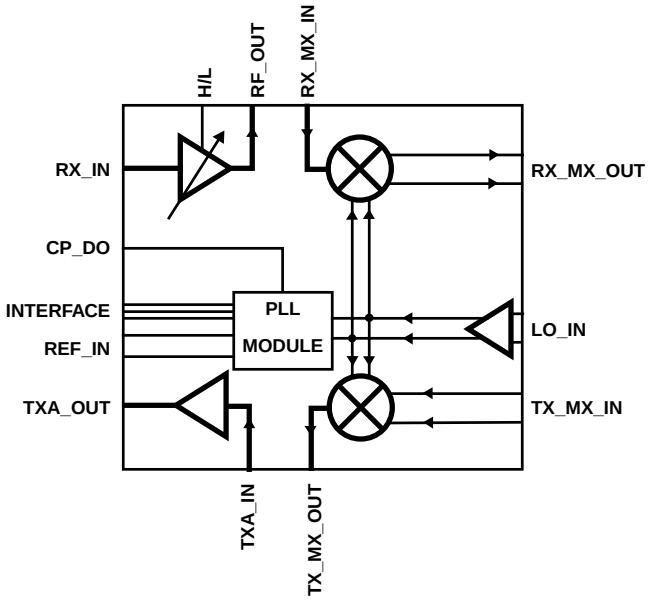
A reduced filter count is realized by multiplexing the receive and transmit IF paths and by sharing a common differential matching network. Furthermore, both transmit and receive RF amplifiers can be directly connected to mixers as image reject filters are integrated. The inherent image rejection of both the transmit and receive functions allow this economic advantage.

The HFA3683A is housed in a 64 lead TQFP package well suited for PCMCIA board applications.

Ordering Information

PART NUMBER	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HFA3683AIN	-40 to 85	64 Ld TQFP	Q64.10x10
HFA3683AIN96	-40 to 85	Tape and Reel	

Simplified Block Diagram



Features

- Highly Integrated
- Integrated Image Rejection Filters
- Multiplexed RX/TX IF Path Accords Single IF Filter
- Programmable Synthesizer
- Gain Selectable LNA
- Power Management/Standby Mode
- Single Supply 2.7V to 3.3V Operation

Cascaded LNA/Mixer (High Gain)

- Gain 25dB
- SSB Noise Figure. 3.7dB
- Input IP3. . . . . -13dBm
- IF Frequency . . . . . .280MHz to 600MHz

Cascaded LNA/Mixer (Low Gain)

- Gain . . . . . -5dB
- Input P1dB . . . . . +2.5dBm
- IF Frequency . . . . . .280MHz to 600MHz

Cascaded Mixer/Preamplifier

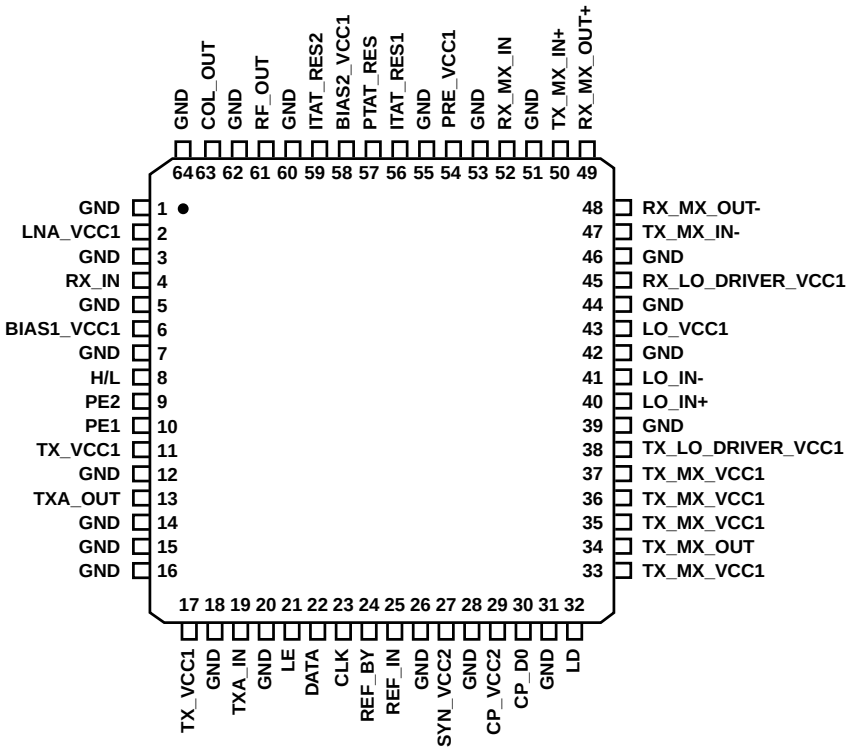
- Transmit Cascaded Mixer/Preamplifier Gain 25dB
- SSB Noise Figure. 10dB
- Output P1dB. 4dBm
- IF Frequency . . . . . .280MHz to 600MHz

Applications

- IEEE802.11 1Mbps and 2Mbps Standard
- Systems Targeting IEEE802.11, 11Mbps Standard
- Wireless Local Area Networks
- PCMCIA Wireless Transceivers
- ISM Systems
- TDMA Packet Protocol Radios
- Application Note AN9847

Pinout

HFA3683A
(TQFP)
TOP VIEW



Pin Description

PIN	NAME	DESCRIPTION
2	LNA_VCC1	Low Noise Amplifier Positive Power Supply.
4	RX_IN	Low Noise Amplifier RF Input, internally DC coupled and requires an external blocking capacitor. A shunt capacitor to ground matches the input for return loss and optimum NF.
6	BIAS1_VCC1	Bias Positive Power Supply for the LNA and Preamplifier.
8	H/L	High or Low Gain Select, controls the LNA high and low gain modes.
9	PE2	This pin along with pin PE1 and bit M(0) of PLL_PE determine which of various operational modes will be active. Please refer to the Power Enable Truth Table.
10	PE1	This pin along with pin PE2 and bit M(0) of PLL_PE determine which of various operational modes will be active. Please refer to the Power Enable Truth Table.
11	TX_VCC1	Transmit Amplifier Positive Power Supply, requires a high quality decoupling capacitor and a short return path.
13	TXA_OUT	Transmit Amplifier Output, internally matched to 50Ω, requires an external DC blocking capacitor.
17	TX_VCC1	Transmit Amplifier Positive Power Supply.
19	TXA_IN	Transmit Amplifier Input, internally AC coupled.
21	LE	Synthesizer Latch Enable, the serial interface is active when LE is low and the serial data is latched into defined registers on the rising edge of LE.
22	DATA	Synthesizer Serial Data Input, clocked in on the rising edge of the serial clock, MSB first.
23	CLK	Synthesizer Clock, DATA is clocked in on the rising edge of the serial clock, MSB first.
24	REF_BY	Synthesizer Reference Frequency Input Bypass, internally DC coupled and requires an external bypass to ground when REF_IN is used as a Single Ended input, requires an external AC coupling capacitor when used as a differential input.
25	REF_IN	Synthesizer Reference Frequency Input, internally DC coupled and requires an external AC coupling capacitor.

Pin Description (Continued)

PIN	NAME	DESCRIPTION
27	SYN_VCC2	Synthesizer Positive Power Supply.
29	CP_VCC2	Synthesizer Charge Pump Positive Power Supply.
30	CP_DO	Synthesizer Charge Pump Output, feeds the PLL loop filter.
32	LD	Synthesizer Lock Detect Output.
33	TX_MX_VCC1	Transmit Mixer Positive Power Supply.
34	TX_MX_OUT	Transmit Mixer RF output, internal AC coupled and internally matched to 50Ω.
35	TX_MX_VCC1	Transmit Mixer Positive Power Supply.
36	TX_MX_VCC1	Transmit Mixer Positive Power Supply.
37	TX_MX_VCC1	Transmit Mixer Positive Power Supply.
38	TX_LO_Driver_ VCC1	Transmit LO Driver Positive Power Supply.
40	LO_IN+	Local Oscillator Positive Input, internally AC coupled, internally matched to 50Ω when the LO is driven single ended and the LO_IN- is grounded.
41	LO_IN-	Local Oscillator Negative Input, internally AC coupled, differential or single ended capability, ground externally for single ended operation.
43	LO_VCC1	LO Buffer Positive Power Supply.
45	RX_LO_DRIVER _VCC1	Receiver LO Driver Positive Power Supply.
47	TX_MX_IN-	Transmit Mixer Negative Input, internally DC coupled, high impedance input. Designed to share a common IF matching network/IF SAW filter with the receive mixer. Care should be exercised regarding the PC board layout to avoid interference and noise pickup. Layout symmetry and management of PC board parasitics is also critical for maximizing the bandwidth of the IF matching network.
48	RX_MX_OUT-	Receive Mixer Negative Output, open collector, high impedance output. Designed to share a common IF matching network/IF SAW filter with the transmit mixer. Care should be exercised regarding the PC board layout to avoid interference and noise pickup. Layout symmetry and management of PC board parasitics is also critical for maximizing the bandwidth of the IF matching network.
49	RX_MX_OUT+	Receive Mixer Positive Output, open collector, high impedance output. Designed to share a common IF matching network/IF SAW filter with the transmit mixer. Care should be exercised regarding the PC board layout to avoid interference and noise pickup. Layout symmetry and management of PC board parasitics is also critical for maximizing the bandwidth of the IF matching network.
50	TX_MX_IN+	Transmit Mixer Positive Input, internally DC coupled, high impedance input. Designed to share a common IF matching network/IF SAW filter with the receive mixer. Care should be exercised regarding the PC board layout to avoid interference and noise pickup. Layout symmetry and management of PC board parasitics is also critical for maximizing the bandwidth of the IF matching network.
52	RX_MX_IN	Receive Mixer RF Input, internally DC coupled and requires external AC coupling as well as RF matching. The recommend network consists of a 3.3pF series capacitor followed by a small series inductance of 1.4nH and then a 1.2nH shunt inductor. The series inductance is best implemented on the PC board using a narrow transmission line inductor.
54	PRE_VCC1	PLL Prescaler Positive Power Supply.
56	ITAT_RES1	Connection to external resistor sets the receive and transmit mixers tail currents, independent of Absolute Temperature.
57	PTAT_RES	Connection to external resistor sets the receive and transmit mixers tail currents, proportional of Absolute Temperature.
58	BIAS2_VCC1	Bias Positive Power Supply for the receive and transmit mixers.
59	ITAT_RES2	Connection to external resistor sets the LNA and Preamplifier bias currents, independent of Absolute Temperature.
61	RF_OUT	Low Noise Amplifier RF Output, internally AC coupled and internally matched to 50Ω.
63	COL_OUT	LNA Collector Output, requires a bypass capacitance which is resonant with the PC board parasitics. A small resistance (20Ω) in series with the main PC board VCC buss is recommended to provide isolation from other VCC bypass capacitors. This ensures the image rejection performance of the LNA is maintained.
All Others	GND	Circuit Ground Pins (Quantity 23 each).

Absolute Maximum Ratings

Supply Voltage 3.6V
Voltage on Any Other Pin. . . . . -0.3 to V_{CC} +0.3V
V_{CC} to V_{CC} Decouple . . . . . -0.3 to +0.3V
Any GND to GND. . . . . -0.3 to +0.3V
Pins 4, 19, 52, 56, 57 and 59 . . . . . 0.3 to +0.6V

Operating Conditions

Temperature Range . . . . . -40 to 85^{o}C
Supply Voltage Range . . . . . 2.7V to 3.3V

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (^{o}C/W)
TQFP Package. 65
Maximum Junction Temperature (Plastic Package) . . . . . 150^{o}C
Maximum Storage Temperature Range . . . . . -65^{o}C to 150^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . . 300^{o}C
(TQFP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

General Electrical Specifications

PARAMETER	TEMP. (^{o}C)	MIN	TYP	MAX	UNITS
Supply Voltage	Full	2.7	-	3.3	V
Receive Total Supply Current (LNA in High Gain)	25	-	33	38	mA
Receive Total Supply Current (LNA in Low Gain)	25	-	27	32	mA
Transmit Total Supply Current	25	-	40	45	mA
Standby Total Supply Current (PLL and LO Buffers Active)	25	-	6	8	mA
TX/RX Power Down Supply Current	Full	-	10	100	µA
TX/RX/Power Down Time (Note 2)	Full	-	1	10	µs
RX/TX, TX/RX Switching Time (Note 2)	Full	-	0.2	1	µs
CMOS Low Level Input Voltage (CLK, DATA, LE) (Note 3)	Full	-	-	0.3*V_{DD}	V
CMOS High Level Input Voltage (CLK, DATA, LE) (Note 3)	Full	0.7*V_{DD}	-	3.6	V
CMOS High or Low Level Input Current (CLK, DATA, LE)	Full	-3.0	-	+3.0	µA
Control Logic Low Level Input Voltage (H/L, PE1, PE2) (Note 4)	Full	-0.3	-	0.5	V
Control Logic High Level Input Voltage (H/L, PE1, PE2) (Notes 3 and 4)	Full	$V_{DD-0.5}$	-	-	V

NOTES:

2. TX/RX/TX switching time and power Down/Up time are dependent on external components.
3. V_{DD} is the supply voltage of external Control sources.
4. These three pins H/L, PE1 and PE2 are not connected to CMOS circuitry and have different thresholds from all other control pins.

Cascaded LNA/Mixer AC Electrical Specifications

Assumes a direct connection between the LNA and Mixer, IF = 374MHz, LO = 2075MHz at -6dBm, V_{CC} = 2.7 Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (^{o}C)	MIN	TYP	MAX	UNITS
RF Frequency Range		Full	2400	-	2500	MHz
IF Frequency Range		Full	280	374	600	MHz
LO Frequency Range		Full	1800	-	2220	MHz
LO Input Drive Level	Single End or Differential	Full	-10	-6	0	dBm
Power/Voltage Gain	High Gain Mode	Full	21.5	25	29	dB
Noise Figure		Full	-	3.7	5.0	dB
Input IP3		Full	-17.5	-13	-	dBm
Input P1dB		Full	-27.5	-23	-	dBm

Cascaded LNA/Mixer AC Electrical Specifications

Assumes a direct connection between the LNA and Mixer, IF = 374MHz, LO = 2075MHz at -6dBm, V_{CC} = 2.7 Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (^{o}C)	MIN	TYP	MAX	UNITS
Power/Voltage Gain	Low Gain Mode	Full	-9	-5	-1	dB
Noise Figure		25	-	25	-	dB
Output IM3 at -4dBm Input Tones		Full	-	-45	-40	dBc
Input P1dB		Full	-1	+2.5	-	dBm
LNA Input 50Ω VSWR	High Gain Mode	25	-	1.65:1	2.0:1	-
	Low Gain Mode	25	-	1.3:1	2.0:1	-
LO 50Ω VSWR	LO = Single End	25	-	1.4:1	2.0:1	-
Differential IF Output Load	Shared with TX	25	-	200	-	Ω
IF Output Capacitance (Single Ended)		25	-	1.2	-	pF
IF Output Resistance (Single Ended)		25	-	5.5	-	kΩ
LO to Mixer RF Feedthrough (Uncascaded)		25	-	-50	-20	dBm
LO to LNA Input Feedthrough (Cascaded, no filter)		25	-	-60	-50	dBm
Gain Switching Speed at Full Scale - High to Low	±1dB settling	Full	-	0.03	0.1	µs
Gain Switching Speed at Full Scale - Low to High	±1dB settling	Full	-	0.25	0.3	µs

Cascaded Transmit Mixer AC Electrical Specifications

Assumes a direct connection between the Mixer and Preamplifier, F = 374MHz, LO = 2075MHz at -6dBm, VCC = 2.7 Unless Otherwise Specified.

PARAMETER	TEST CONDITIONS	TEMP. (^{o}C)	MIN	TYP	MAX	UNITS
RF Frequency Range		Full	2400	-	2500	MHz
IF Frequency Range		Full	280	374	600	MHz
LO Frequency Range		Full	1800	-	2220	MHz
Power Conversion Gain	200Ω In, 50Ω Out	Full	21	25	29	dB
SSB Noise Figure		Full	-	10	15	dB
Output IP3		Full	+12	+14	-	dBm
Output P1dB		Full	+2	+4	-	dBm
LO Input Drive Level	Same as RX	Full	-10	-6	0	dBm
LO to Transmit Mixer RF Feedthrough (Uncascaded)		25	-	-37	-20	dBm
LO to Transmit Amp. Output Feedthrough (Uncascaded)		25	-	-45	-30	dBm
LO to Transmit Amp. Output Feedthrough (Cascaded, no filter)		25	-	-15	-5	dBm
Preamplifier Output 50Ω VSWR		25	-	2.3:1	3.0:1	-
LO 50Ω VSWR	LO = Single End	25	-	1.4:1	2.0:1	-
Differential IF Input Load	Shared with RX	25	-	200	-	Ω
IF Input Capacitance (Single Ended)		25	-	1.1	-	pF
IF Input Resistance (Single Ended)		25	-	0.7	-	kΩ

Phase Lock Loop Electrical Specifications (See Notes 5 through 13)

PARAMETER	TEST CONDITIONS	TEMP. (^oC)	MIN	TYP	MAX	UNITS
Operating LO Frequency (32/33 Prescaler)		Full	1800	-	2220	MHz
Operating LO Frequency (64/65 Prescaler)		Full	1800	-	3500	MHz
Reference Oscillator Frequency		Full	-	-	50	MHz
Selectable Prescaler Ratios (P)		Full	32/33	-	64/65	-
Swallow Counter Divide Ratio (A Counter)		Full	0	-	127	-
Programmable Counter Divide Ratio (B Counter)		Full	3	-	2047	-
Reference Counter Divide Ratio (R Counter)		Full	3	-	32767	-
Reference Oscillator Sensitivity, Single or Differential Sine Inputs		Full	0.5	-	V_{CC}	V_{PP}
Reference Oscillator Sensitivity, CMOS Inputs, Single Ended or Complimentary		Full	-	CMOS	-	Note 7
Reference Oscillator Duty Cycle	CMOS Inputs	25	40	-	60	%
Charge Pump Sink/Source Current/Tolerance	250µA Selection ±25%	25	0.18	0.25	0.32	mA
Charge Pump Sink/Source Current/Tolerance	500µA Selection ±25%	25	0.375	0.50	0.625	mA
Charge Pump Sink/Source Current/Tolerance	750µA Selection ±25%	25	0.56	0.75	0.94	mA
Charge Pump Sink/Source Current/Tolerance	1mA Selection ±25%	25	0.75	1.0	1.25	mA
Charge Pump Sink/Source Mismatch		Full	-	-	15	%
Charge Pump Output Compliance		Full	0.5	-	V_{CC2}-0.5	V
Charge Pump Supply Voltage		Full	2.7	-	3.6	V
Serial Interface Clock Width	High Level t_{CWH}	Full	50	-	-	ns
	Low Level t_{CWL}	Full	50	-	-	ns
Serial Interface Data/Clk Set-Up Time t_{CS}		Full	50	-	-	ns
Serial Interface Data/Clk Hold Time t_{CH}		Full	10	-	-	ns
Serial Interface Clk/LE Set-Up Time t_{ES}		Full	50	-	-	ns
Serial Interface LE Pulse Width t_{EW}		Full	50	-	-	ns

NOTES:

5. The Serial data is clocked on the Rising Edge of the serial clock, MSB first. The serial Interface is active when LE is LOW. The serial Data is latched into defined registers on the rising edge of LE.
6. As long as power is applied, all register settings will remain stored, including the power down state. The system may then come in and out of the power down state without requiring the registers to be rewritten.
7. CMOS Reference Oscillator input levels are given in the General Electrical Specification section.

POWER ENABLE TRUTH TABLE

PE1	PE2	PLL_PE (SERIAL BUS)	STATUS
0	0	1	Power Down State
1	1	1	Receive State
1	0	1	Transmit State
0	1	1	PLL Active
X	X	0	PLL Disabled

NOTE:

8. PLL_PE is controlled via the serial interface, and can be used to disable the synthesizer. The actual synthesizer control is a logic AND function of PLL_PE and the result of the logic OR function of PE1 and PE2. PE1 and PE2 directly control the power enable functionality of the LO buffers.

PLL Synthesizer Table

	REGISTER DEFINITION																			
SERIAL BITS	**LSB 1**	**2**	**3**	**4**	**5**	**6**	**7**	**8**	**9**	**10**	**11**	**12**	**13**	**14**	**15**	**16**	**17**	**18**	**19**	**MSB**
R Counter	0	0	R(0)	R(1)	R(2)	R(3)	R(4)	R(5)	R(6)	R(7)	R(8)	R(9)	R(10)	R(11)	R(12)	R(13)	R(14)	X (Don't Care)		
A/B Counter	0	1	A(0)	A(1)	A(2)	A(3)	A(4)	A(5)	A(6)	B(0)	B(1)	B(2)	B(3)	B(4)	B(5)	B(6)	B(7)	B(8)	B(9)	B(10)
Operational Mode	1	0	M(0)	0	M(2)	M(3)	M(4)	M(5)	M(6)	M(7)	M(8)	0	0	0	0	M(13)	M(14)	M(15)	X	X

Reference Frequency Counter/Divider

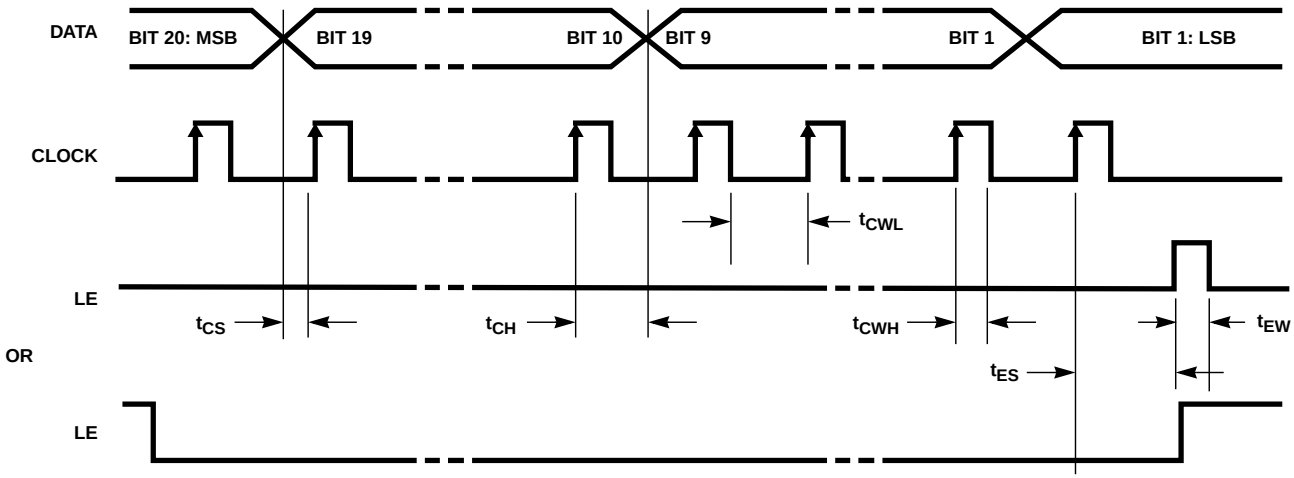
BIT	DESCRIPTION
R(0-14)	Least significant bit R(0) to most significant bit R(14) of the divide by R counter. The Reference signal frequency is divided down by this counter and is compared with a divided LO by a phase detector.

LO Frequency Counters/Dividers

BIT	DESCRIPTION
A(0-6)	Least significant bit A(0) to most significant bit A(6) of a 7-bit Swallow counter and LSB B(0) to MSB B(10) of the 11-bit divider. The LO frequency is divided down by [P*B+A], where P is the Prescaler divider set by bit M(2). This divided signal frequency is compared by a phase detector with the divided Reference signal.
B(0-11)	

Operational Modes

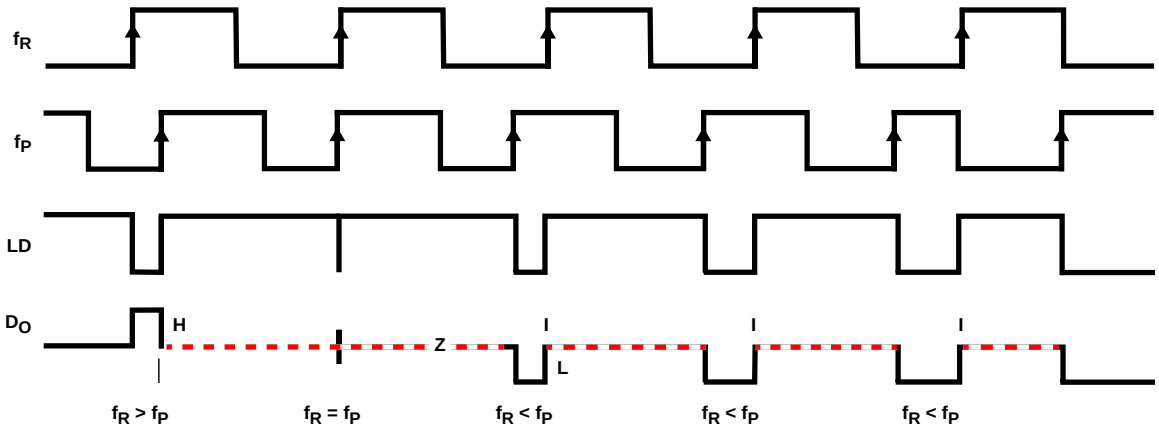
BIT	DESCRIPTION				
M(0)	(PLL_PE), Phase Lock Loop Power Enable. 1 = Enable, 0 = Power Down. Serial port always on.				
M(2)	Prescaler Select. 0 = 32/33, 1 = 64/65				
M(3) M(4)	Charge Pump Current Setting		**M(4)**	**M(3)**	**OUTPUT SINK/SOURCE**
			0	0	0.25mA
			0	1	0.50mA
			1	0	0.75mA
			1	1	1.00mA
M(5) M(6)	Charge Pump Sign	**M(6)**	**M(5)**		
		0	0	Source if LO/ [P*B+A] < Ref/R	
		0	1	Source if LO/ [P*B+A] > Ref/R	
M(7) M(8) M(13)	LD Pin Multiplex Operation	**M(13)**	**M(8)**	**M(7)**	**OUTPUT AT PIN LD**
		0	0	X	Lock Detect Operation
		0	1	X	Short to GND
		1	0	X	Serial Register Read Back
		1	1	0	Ref. Divided by R Waveform
		1	1	1	LO Divided by [P*B+A] Waveform
M(14) M(15)	Charge Pump Operation/Test	**M(15)**	**M(14)**	**OPERATION/TEST**	
		0	0	Normal Operation	
		0	1	Charge Pump Constant Current Source	
		1	0	Charge Pump Constant Current Sink	
		1	1	High Impedance State	



NOTES:

9. Parenthesis data indicates programmable reference divider data.
10. Data shifted into register on clock rising edge.
11. Data is shifted in MSB first.

FIGURE 1. SERIAL DATA INPUT TIMING

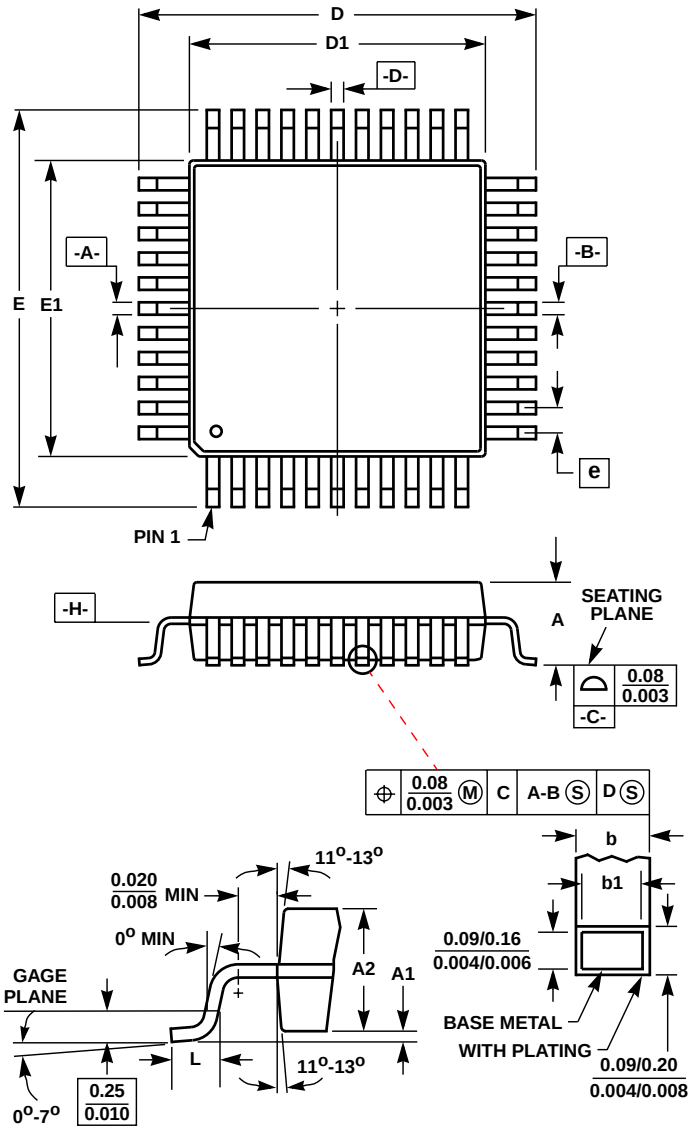


NOTES:

12. Phase difference detection range: -2π to $+2\pi$.
13. The minimum width pump up and pump down current pulses occur at the D_O pin when the loop is locked.

FIGURE 2. PHASE COMPARATOR AND INTERNAL CHARGE PUMP CHARACTERISTICS

Thin Plastic Quad Flatpack Packages (TQFP)



Q64.10x10 (JEDEC MS-026ACD ISSUE B)
64 LEAD THIN PLASTIC QUAD FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.005	0.05	0.15	-
A2	0.038	0.041	0.95	1.05	-
b	0.007	0.010	0.17	0.27	6
b1	0.007	0.009	0.17	0.23	-
D	0.468	0.476	11.90	12.10	3
D1	0.390	0.397	9.9	10.10	4, 5
E	0.468	0.476	11.9	12.10	3
E1	0.390	0.397	9.9	10.10	4, 5
L	0.018	0.029	0.45	0.75	-
N	64		64		7
e	0.020 BSC		0.50 BSC		-

Rev. 0 7/98

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm (0.003 inch).
7. “N” is the number of terminal positions.

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029

Attachement-4

Datasheet of HFA3783.

PRELIMINARY | Data Sheet | July 1999 | File Number 4633.1

I/Q Modulator/Demodulator and Synthesizer

The HFA3783 is a highly integrated and fully differential SiGe baseband converter for half duplex wireless applications. It features all the necessary blocks for quadrature modulation and demodulation of “I” and “Q” baseband signals.

It has an integrated AGC receive IF amplifier with frequency response to 600MHz. The AGC has 70dB of voltage gain and better than 70dB of gain control range. The transmit output also features gain control with 70dB of range.

The receive and transmit IF paths can share a common differential matching network to reduce the filter component count required for single IF half duplex transceivers. A pair of 2nd order antialiasing filters with an integrated DC offset cancellation architecture is included in the receive chain for baseband operation down to DC. In addition, an IF level detector is included in the AGC chain for threshold comparison. Up and down conversion are performed by doubly balanced mixers for “I” and “Q” IF processing. These converters are driven by a broadband quadrature LO generator with frequency of operation phase locked by an internal 3 wire interface synthesizer and PLL.

The device requires low LO levels from an external VCO and a PLL reference signal up to 44MHz. The HFA3783 is housed in a thin 48 lead LQFP package well suited for PCMCIA board applications.

Features

- Integrates All IF Transmit and Receive Functions
- Broad Quadrature Frequency Range . . . . . .70 to 600MHz
- 600MHz AGC IF Strip with Level Detector 69dB
- DC Coupled Baseband Interfaces
- Integrates a Receiver DC Offset Calibration Loop
- Integrated 3 Wire Interface PLL For LO Applications
- Low LO Drive Level . . . . . -15dBm
- Fast Transmit-Receive Switching 1µS
- Power Management/Standby Mode
- Single Supply 2.7 to 3.3V Operation

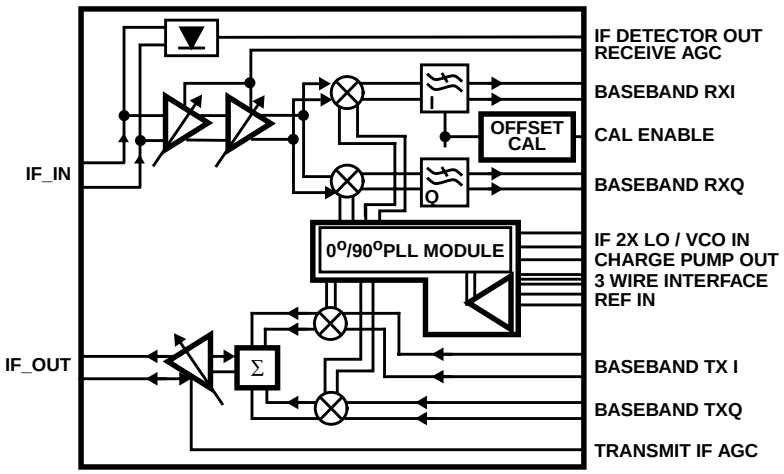
Applications

- IEEE802.11 1 and 2Mbps Standard
- Systems Targeting IEEE 802.11 11Mbps Standard
- Wireless Local Area Networks
- PCMCIA Wireless Transceivers
- ISM Systems
- TDMA Packet Protocol Radios

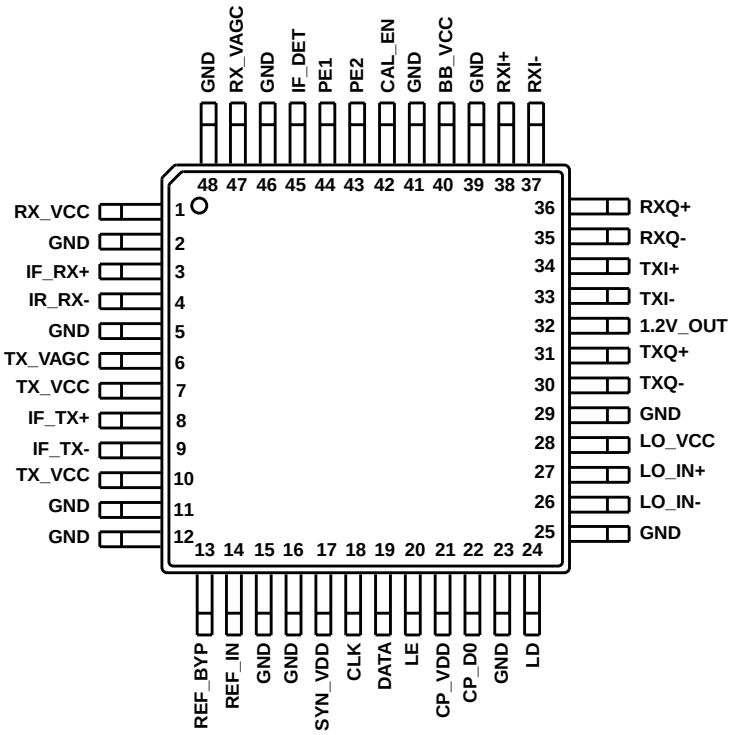
Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HFA3783IN	-40 to 85	48 Ld LQFP	Q48.7x7A
HFA3783IN96	-40 to 85	Tape and Reel	

Simplified Block Diagram



Pinout


GND
RX_VAGC
GND
IF_DET
PE1
PE2
CAL_EN
GND
BB_VCC
GND
RXI+
RXI-
48 47 46 45 44 43 42 41 40 39 38 37
RX_VCC 1
GND 2
IF_RX+ 3
IR_RX- 4
GND 5
TX_VAGC 6
TX_VCC 7
IF_TX+ 8
IF_TX- 9
TX_VCC 10
GND 11
GND 12
36 RXQ+
35 RXQ-
34 TXI+
33 TXI-
32 1.2V_OUT
31 TXQ+
30 TXQ-
29 GND
28 LO_VCC
27 LO_IN+
26 LO_IN-
25 GND
13 14 15 16 17 18 19 20 21 22 23 24
REF_BYP
REF_IN
GND
GND
SYN_VDD
CLK
DATA
LE
CP_VDD
CP_D0
GND
LD

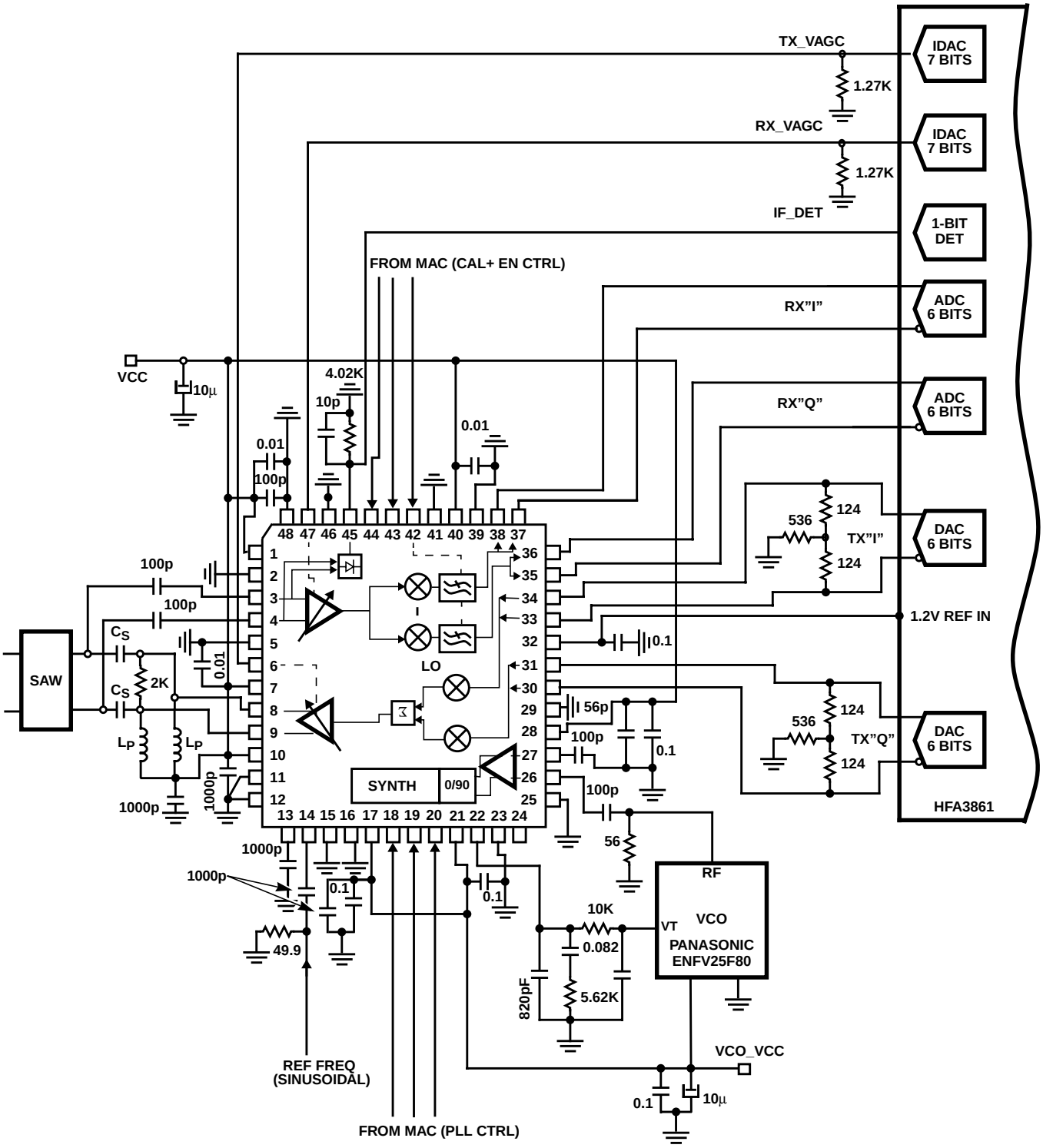
Pin Descriptions

PIN NUMBER	NAME	DESCRIPTION
1	RX_VCC	Receive AGC Amplifier Power Supply. Requires high quality capacitor decoupling.
3	IF_RX+	Receive AGC Differential Amplifier Non-Inverting IF Input. Requires a DC blocking capacitor.
4	IF_RX-	Receive AGC Differential Amplifier Inverting IF Input. Requires a DC blocking capacitor. Pins 3 and 4 are interchangeable and can be used single end with the other being bypassed to ground with a capacitor.
6	TX_VAGC	Transmit AGC amplifier DC gain control input.
7	TX_VCC	Transmit AGC Amplifier Power Supply. Requires high quality capacitor decoupling.
8	IF_TX+	Transmit AGC Differential Amplifier Positive Output. Open collector requiring DC bias from VCC via an inductor.
9	IF_TX-	Transmit AGC Differential Amplifier Negative Output. Open collector requiring DC bias from VCC via an inductor.
10	TX_VCC	Transmit AGC Amplifier Power Supply. Requires high quality capacitor decoupling.
13	REF_BYP	PLL Reference Buffer Signal Negative Differential Input. Pin has active bias and can be used in conjunction with pin14 either differential or single end. CMOS inputs must be DC coupled. Small sinusoidal inputs must be DC blocked with this pin bypassed to ground via a capacitor.
14	REF_IN	PLL Reference Buffer Signal Positive Differential Input. Pin has active bias and can be used in conjunction with pin13 either differential or single end. CMOS inputs must be DC coupled. Small sinusoidal inputs must be DC blocked with this pin used as an input for the reference signal. When used in single end CMOS inputs, pin 13 must be left floating. Pins 13 and 14 are interchangeable.
17	SYN_VDD	PLL Synthesizer Digital Power Supply. Requires high quality capacitor decoupling.
18	CLK	PLL Synthesizer Serial Interface Clock. CMOS input.
19	DATA	PLL Synthesizer Serial Interface Data. CMOS input.
20	LE	PLL Synthesizer Serial Interface Latch Enable Control. CMOS input.
21	CP_VDD	PLL Charge Pump Power Supply. Independent supply for the charge pump rails not to exceed 3.6V. Requires high quality capacitor decoupling.
22	CP_D0	PLL Charge Pump Current Output.
24	LD	PLL Lock Detect Output. Requires low capacitive loading not to exceed 5pF.
26	LO_IN-	Local Oscillator Differential Buffer Negative Input. Requires AC coupling. For single end applications its complementary input Pin 27 must be bypassed to ground via a capacitor.
27	LO_IN+	Local Oscillator Differential Buffer Positive Input. Requires AC coupling. For single end applications its complementary input Pin 26 must be bypassed to ground via a capacitor. Pins 26 and 27 are interchangeable. NOTE: High second harmonic content LO waveform may degrade I/Q phase accuracy.
28	LO_VCC	Local Oscillator Buffer Amplifier Power Supply. Requires high quality capacitor decoupling.
30	TXQ-	Baseband Quadrature Differential Inputs for IF Transmission. DC coupled requiring 1.2V common mode bias voltages.
31	TXQ+	
32	1.2V_OUT	Highly Regulated Band Gap 1.2V Buffered Output. Used in conjunction with ADCs and DACs for voltage /temperature tracking. Requires high quality capacitor decoupling to ground.
33	TXI-	Baseband In Phase Differential Inputs for IF Transmission. DC coupled requiring 1.2V common mode bias voltages.
34	TXI+	
35	RXQ-	Baseband Quadrature Differential Outputs From IF Demodulation. DC coupled output with 1.2V common mode DC outputs. AC coupling pins 35, 36, 37 and 38 requires programmable register activation for DC hold during TX to RX switching.
36	RXQ+	
37	RXI-	Baseband In Phase Differential Outputs From IF Demodulation. DC coupled output with 1.2V common mode DC outputs.
38	RXI+	

Pin Descriptions (Continued)

PIN NUMBER	NAME	DESCRIPTION
40	BB_VCC	Baseband Receive LPF Output and Offset Control Power Supply. Requires high quality capacitor decoupling.
42	CAL_EN	CMOS Input for Activation Of Internal DC Offset Adjust Circuit for the Receive Baseband Outputs. A rising edge activates the calibration cycle, which completes within Max 100µS and holds the calibration while this pin is held high.
43	PE2	Power Enable Control Pins: Please refer to the POWER ENABLE TRUTH TABLE in the electrical specifications section
44	PE1	
45	IF_DET	IF Detector Current Output. A current source of 174µA is generated at this pin when the IF AGC receive differential or single ended signal at pins 3 and 4 is between 100 and 200mV_{PP}.
47	RX_VAGC	Receive AGC amplifier DC gain control input.
2, 5, 11, 12, 15, 16, 23, 25, 29, 39, 41, 46, 48	GND	Grounds. Connect to a solid ground plane.

Application Circuit



Absolute Maximum Ratings

Voltage on Any Other Pin . . . . . -0.3 to V_{CC} +0.3V
V_{CC} to V_{CC} Decouple . . . . . -0.3 to +0.3V
Any Gnd to Gnd . . . . . -0.3 to +0.3V

Operating Conditions

Operating Temperature Range . . . . . -40 to +85^{o}C
Supply Voltage Range . . . . . TBD
Power Dissipation at 25^{o}C . . . . . TBD

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (^{o}C/W)	θ_{JC} (^{o}C/W)
TQFP Package	70	N/A

Maximum Junction Temperature (Plastic Package) 150
Maximum Storage Temperature Range . . . . . -65 to 150
Maximum Lead Temperature (Soldering 10s) 300

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

DC Electrical Specifications

PARAMETER	TEMP. (^{o}C)	MIN	TYP	MAX	UNITS
Supply Voltage	Full	2.7	-	3.3	V
Receive Total Supply Current	25	-	36	40	mA
Transmit Total Supply Current	25	-	32	40	mA
Voltage Reference Output at ±1mA, 0.1µF Load	Full	1.14	1.2	1.26	V
TX/RX Power Down Supply Current (PLL Serial Interf. Active)	Full	-	-	100	µA
TX/RX/Power Down Speed (Note 2)	Full	-	-	10	µs
RX/TX, TX/RX Switching Speed (Note 2)	Full	-	-	1	µs
CMOS Low Level Input Voltage	Full	-	-	0.3*V_{DD}	V
CMOS High Level Input Voltage (V_{DD} = 3.6V)	Full	0.7*V_{DD}	-	3.6	V
CMOS Threshold Voltage	Full	-	0.5*V_{DD}	-	V
CMOS High or Low Level Input Current	Full	-3.0	-	+3.0	µA

NOTE:

2. TX/RX/TX switching speed and power Down/Up speed are dependent on external components.

Receive Cascaded AC Electrical Specifications

IF = 375MHz, LO = 748MHz, V_{CC} = 2.7V,
Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (^{o}C)	MIN	TYP	MAX	UNITS
IF Frequency Range		Full	70	-	600	MHz
2XLO Frequency Range		Full	140	-	1200	MHz
Voltage Gain	Full Gain. Differential 250Ω in, 5kΩ output load. AGC Control voltage set to 69dB of voltage gain	Full	-	69	-	dB
Power Gain		Full	-	56	-	dB
Cascaded Noise Figure		Full	-	-	8	dB
Output IP3		Full	+2.2	-	-	dBm
Output P1dB		Full	-14.1	-	-	dBm
Voltage Gain	AGC Control Voltage set to 10dB attenuation. Differential 250Ω input, differential 5kΩ output load.	Full	-	59	-	dB
Power Gain		Full	-	46	-	dB
Cascaded Noise Figure		Full	-	-	11	dB
Output IP3		Full	+1.5	-	-	dBm
Output P1dB		Full	-14.3	-	-	dBm

Receive Cascaded AC Electrical Specifications

IF = 375MHz, LO = 748MHz, V_{CC} = 2.7V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (^{O}C)	MIN	TYP	MAX	UNITS
Voltage Gain	AGC Control Voltage set to 20dB attenuation. Differential 250Ω input, differential 5kΩ output load.	Full	-	49	-	dB
Power Gain		Full	-	36	-	dB
Cascaded Noise Figure		Full	-	14.1	-	dB
Output IP3		Full	+1.0	-	-	dBm
Output P1dB		Full	-14.4	-	-	dBm
Voltage Gain	AGC Control Voltage set to 30dB attenuation. Differential 250Ω input, differential 5kΩ output load.	Full	-	39	-	dB
Power Gain		Full	-	26	-	dB
Cascaded Noise Figure		Full	-	19.9	-	dB
Output IP3		Full	+0.3	-	-	dBm
Output P1dB		Full	-14.6	-	-	dBm
Voltage Gain	AGC Control Voltage set to 40dB attenuation. Differential 250Ω input, differential 5kΩ output load.	Full	-	29	-	dB
Power Gain		Full	-	16	-	dB
Cascaded Noise Figure		Full	-	27	-	dB
Output IP3		Full	+0.8	-	-	dBm
Output P1dB		Full	-15.0	-	-	dBm
Voltage Gain	AGC Control Voltage set to 50dB attenuation. Differential 250Ω input, differential 5kΩ output load.	Full	-	19	-	dB
Power Gain		Full	-	6	-	dB
Cascaded Noise Figure		Full	-	35.1	-	dB
Output IP3		Full	-2.0	-	-	dBm
Output P1dB		Full	-15.5	-	-	dBm
Voltage Gain	AGC Control Voltage set to 60dB attenuation. Differential 250Ω input, differential 5kΩ output load.	Full	-	9	-	dB
Power Gain		Full	-	-4	-	dB
Cascaded Noise Figure		Full	-	43.9	-	dB
Output IP3		Full	-3.3	-	-	dBm
Output P1dB		Full	-16.1	-	-	dBm
Voltage Gain	AGC Control Voltage set to 72dB attenuation. Differential 250Ω input, differential 5kΩ output load.	Full	-	-3	-	dB
Power Gain		Full	-	-16	-	dB
Cascaded Noise Figure		Full	-	60.0	-	dB
Output IP3		Full	-6.7	-	-	dBm
Output P1dB		Full	-18.2	-	-	dBm
Input Differential Impedance	Shared with TX	25	-	250	-	Ω
AGC Gain Control Voltage		Full	0.2	-	2.25	V
AGC Gain Control Supply Sensitivity	Over Supply Range	25	-	61	-	dB/V
AGC Gain Control Input Impedance		Full	20	23	-	kΩ
Gain Switching Speed to ±1dB Settling	Full AGC Scale	Full	-	0.2	1	µs
Insertion Phase vs AGC	Full AGC Range	25	-2	±0.3	+2	deg/dB
IF Detector Response Time	10pF, 2.9K External Load	Full	-	0.15	0.25	µs
IF Detector Input Voltage	0.5V, 174µA Out	Full	100	150	200	mV_{PP}
LO Internal Input Resistance	Single End. Across F. Range	25	950	-	1.1K	Ω
LO Internal Input Capacitance		25	-	0.26	-	pF

Receive Cascaded AC Electrical Specifications

IF = 375MHz, LO = 748MHz, V_{CC} = 2.7V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (^{O}C)	MIN	TYP	MAX	UNITS
LO Drive Level	External 50Ω Match Network	Full	-15	10	0	dBm
Upper Baseband 3dB Bandwidth (2nd Order)		Full	6.7	8.5	10.3	MHz
Lower Baseband 3dB Bandwidth	DC Coupled Load	Full	DC	-	-	-
I and Q 3dB BW Matching		Full	-2	-	+2	%
Cascaded Receive I or Q Baseband THD	1MHz, 1V_{PP} Diff. for First 50dB of Attenuation Range	Full	-	-	1	%
Cascaded Receive I/Q Crosstalk		Full	-	-	-40	dB
I/Q Amplitude Balance	100KHz CW	Full	-1	-	+1	dB
I/Q Phase Balance	100KHz CW	Full	-2	-	+2	deg
Cascaded I or Q Baseband Differential Offset Voltage	After Calibration Cycle	Full	-	-	10	mV
Cascaded I or Q Common Mode Voltage		Full	1.08	1.17	1.32	V
Offset Calibration Time	Ref = 44MHz, Offset Counter C = 25	Full	-	26	100	µs
Offset Counter Divide Ratio (C Counter)	Input Ref Clock is Divided by (C+1) * 2 for SAR Offset Correction	Full	1	-	127	-
Baseband Output Load Resistance	Differential	Full	-	5	-	kΩ
Baseband Output Load Capacitance	Single End, Each	Full	-	-	10	pF
	Differential	Full	-	-	10	pF

NOTE:

3. A positive frequency offset from the carrier produces I leading Q by 90 degrees.

Transmit Cascaded AC Electrical Specifications

LO = 748MHz, V_{CC} = 2.7V, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	TEMP. (^{O}C)	MIN	TYP	MAX	UNITS
IF Frequency Range		Full	70	-	600	MHz
2 X LO Frequency Range		Full	140	-	1200	MHz
Output Power at 250Ω Differential Load	AGC Voltage Set to -10dBm Output Power for 0.35V_{PP} Sine I and Q Inputs	Full	-	-10	-	dBm
Output Noise Floor		Full	-	-141	-	dBm/Hz
P1dB/Output Power Ratio		Full	10	-	-	dB
Output Power at 250Ω Differential Load	AGC Voltage Set to 10dB Attenuation. 0.35V_{PP} Sine I and Q Inputs	Full	-	-20	-	dBm
Output Noise Floor		Full	-	-149	-	dBm/Hz
P1dB/Output Power Ratio		Full	10	-	-	dB
Output Power at 250Ω Differential Load	AGC Voltage Set to 20dB Attenuation. 0.35V_{PP} Sine I and Q Inputs	Full	-	-30	-	dBm
Output Noise Floor		Full	-	-157	-	dBm/Hz
P1dB/Output Power Ratio		Full	10	-	-	dB
Output Power at 250Ω Differential Load	AGC Voltage Set to 30dB Attenuation. 0.35V_{PP} Sine I and Q Inputs	Full	-	-40	-	dBm
Output Noise Floor		Full	-	-161	-	dBm/Hz
P1dB/Output Power Ratio		Full	10	-	-	dB
Output Power at 250Ω Differential Load	AGC Voltage Set to 40dB Attenuation. 0.35V_{PP} Sine I and Q Inputs	Full	-	-50	-	dBm
Output Noise Floor		Full	-	-162	-	dBm/Hz
P1dB/Output Power Ratio		Full	10	-	-	dB

Transmit Cascaded AC Electrical Specifications LO = 748MHz, V_{CC} = 2.7V, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	TEMP. (^oC)	MIN	TYP	MAX	UNITS
Output Power at 250Ω Differential Load	AGC Voltage Set to 50dB Attenuation. 0.35V_{PP} Sine I and Q Inputs	Full	-	-60	-	dBm
Output Noise Floor		Full	-	-163	-	dBm/Hz
P1dB/Output Power Ratio		Full	10	-	-	dB
Output Power at 250Ω Differential Load	AGC Voltage Set to 60dB Attenuation. 0.35V_{PP} Sine I and Q Inputs	Full	-	-70	-	dBm
Output Noise Floor		Full	-	-164	-	dBm/Hz
P1dB/Output Power Ratio		Full	10	-	-	dB
Output Power at 250Ω Differential Load	AGC Voltage Set to 70dB Attenuation. 0.35V_{PP} Sine I and Q Inputs	Full	-	-80	-	dBm
Output Noise Floor		Full	-	-164	-	dBm/Hz
P1dB/Output Power Ratio		Full	10	-	-	dB
AGC Gain Control Voltage		Full	0.1	-	2.25	V
AGC Gain Control Supply Sensitivity	Supply Range	25	-	40	-	dB/V
AGC Control Input Impedance		Full	20	21	-	KΩ
Gain Switching Speed to ±1% Settling	Full Scale	25	-	1.6	4	µs
Insertion Phase vs AGC	50dB Range from Max	Full	-	-	4.0	deg
Output Power Temperature Coefficient		Full	-2	-	+2	dB
I/Q Baseband Bandwidth		Full	0	13	-	MHz
Cascaded Baseband to IF TX THD	1MHz, 0.5V_{PP}	Full	-	-	0.5	%
Amplitude Balance	DC Inputs	Full	-0.5	-	+0.5	dB
Phase Balance	DC Inputs	Full	-2	-	+2	deg
Carrier Suppression	Full AGC Range	Full	-	-	-30	dBc
SSB Sideband Suppression	100KHz Inputs	Full	-	-	-32	dBc
IF Output Differential Impedance	Shared with RX	25	-	250	-	Ω
IF Output 250Ω Differential VSWR	17MHz BW, Full AGC Range	Full	-	-	1.4:1	-
LO Internal Input Resistance	Single End Across F. Range	25	950	-	1.1K	Ω
LO Internal Input Capacitance		25	-	0.26	-	pF
LO Drive Level	External 50Ω Match Network	Full	-15	-10	0	dBm
Baseband Differential Input Impedance		Full	100	150	-	kΩ
Baseband Differential Input Voltage	Shaped Pulses	Full	-	0.5	-	V_{PP}
Common Mode Baseband Input Voltage	All Inputs	Full	1.2	1.30	1.40	V

NOTE:

4. I leading Q produces a+jw CCW rotation and a positive frequency offset from the carrier.

Phase Lock Loop Electrical Specifications

PARAMETER	TEST CONDITIONS	TEMP. (^oC)	MIN	TYP	MAX	UNITS
Operating 2X LO Frequency		Full	140	-	1200	MHz
Reference Oscillator Frequency		Full	-	44	50	MHz
Selectable Prescaler Ratios (2 Settings)		Full	16/17	N/A	32/33	-
Swallow Counter Divide Ratio (A Counter)		Full	0	-	127	-
Programmable Counter Divide Ratio (B Counter)		Full	3	-	2047	-
Reference Counter Divide Ratio (R Counter)		Full	3	-	32767	-

Phase Lock Loop Electrical Specifications (Continued)

PARAMETER	TEST CONDITIONS	TEMP. (^oC)	MIN	TYP	MAX	UNITS
Reference Oscillator Sensitivity	Single or Differential Sine Inputs	Full	0.5	-	-	V_{PP}
	CMOS Single or Complementary	Full	-	-	-	-
Reference Oscillator Duty Cycle	CMOS Inputs	Full	40	-	60	%
Charge Pump Sink/Source Current	250µA Selection	Full	0.2	-	0.3	mA
Charge Pump Sink/Source Current	500µA Selection	Full	0.4	-	0.6	mA
Charge Pump Sink/Source Current	750µA Selection	Full	0.6	-	0.9	mA
Charge Pump Sink/Source Current	1mA Selection	Full	0.8	-	12	mA
Charge Pump Sink/Source Mismatch		Full	-	-	15	%
Charge Pump Output Compliance		Full	0.5	-	V_{DD}-0.5	V
Charge Pump Supply Voltage		Full	2.7	-	3.6	V
Serial Interface Clock Width	High Level	Full	50	-	-	ns
	Low level	Full	50	-	-	ns
Serial Interface Data/Clk Set-Up Time		Full	50	-	-	ns
Serial Interface Data/Clk Hold Time		Full	10	-	-	ns
Serial Interface Clk/LE Set-Up Time		Full	50	-	-	ns
Serial Interface LE Pulse Width		Full	50	-	-	ns

NOTE:

5. A positive frequency offset from the carrier produces I leading Q by 90 degrees.

POWER ENABLE TRUTH TABLE

PE1	PE2	PLL_PE (SERIAL BUS)	STATUS
0	0	1	Power Down State
1	1	1	Receive State
1	0	1	Transmit State
0	1	1	PLL Active
X	X	0	PLL Disabled

PLL Synthesizer and DC Offset Clock Programming Table

SERIAL BITS	REGISTER DEFINITION																			
	LSB 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	MSB
R Counter	0	0	R(0)	R(1)	R(2)	R(3)	R(4)	R(5)	R(6)	R(7)	R(8)	R(9)	R(10)	R(11)	R(12)	R(13)	R(14)	X (Don't Care)		
A/B Counter	0	1	A(0)	A(1)	A(2)	A(3)	A(4)	A(5)	A(6)	B(0)	B(1)	B(2)	B(3)	B(4)	B(5)	B(6)	B(7)	B(8)	B(9)	B(10)
Operational Mode	1	0	M(0)	0	M(2)	M(3)	M(4)	M(5)	M(6)	M(7)	M(8)	0	0	0	0	M(13)	M(14)	M(15)	X	X
Offset Calibration	1	1	C(0)	C(1)	C(2)	C(3)	C(4)	C(5)	C(6)	0	0	0	0	0	X (Don't Care)					

NOTE:

6. The Serial data is clocked on the Rising Edge of the serial clock, MSB first. The serial Interface is active when LE is LOW. The serial Data is latched into defined registers on the rising edge of LE.

Reference Frequency Counter/Divider

BIT	DESCRIPTION
R(0-14)	Least significant bit R(0) to most significant bit R(14) of the divide by R counter. The Reference signal frequency is divided down by this counter and is compared with a divided LO by a phase detector.

LO Frequency Counters/Dividers

BIT	DESCRIPTION
A(0-6)	Least significant bit A(0) to most significant bit A(6) of a 7-bit Swallow counter and LSB B(0) to MSB B(10) of the 11 bits divider. The LO frequency is divided down by [P*B+A], where P is the prescaler divider set by bit M(2). This divided signal frequency is compared by a phase detector with the divided Reference signal.
B(0-10)	

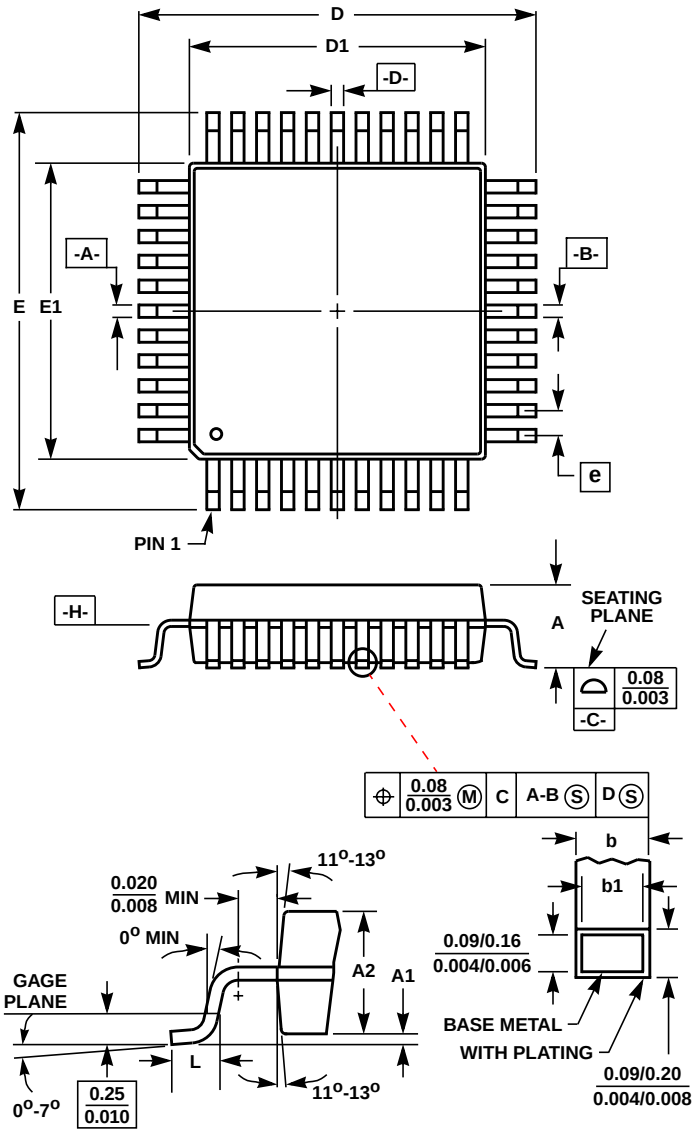
Operational Modes

BIT	DESCRIPTION				
M(0)	(PLL_PE), Phase Lock Loop Power Enable. 1 = Enable, 0 = Power Down. Serial port always on.				
M(2)	Prescaler Select. **0 = 16/17, 1 = 32/33**				
M(3) M(4)	Charge Pump Current Setting.		**M(4)**	**M(3)**	**OUTPUT SINK/SOURCE**
			0	0	0.25mA
			0	1	0.50mA
			1	0	0.75mA
			1	1	1.00mA
M(5) M(6)	Charge Pump Sign.	**M(6)**	**M(5)**		
		0	0	Source if LO/ [P*B+A] < Ref/R	
		0	1	Source if LO/ [P*B+A] > Ref/R	
M(7) M(8) M(13)	LD Pin Multiplex Operation.	**M(13)**	**M(8)**	**M(7)**	**OUTPUT AT PIN LD**
		0	0	X	Lock Detect Operation
		0	1	X	Short to GND
		1	0	X	Serial Register Read Back
		1	1	0	Ref. Divided by R Waveform
		1	1	1	LO Divided by [P*B+A] Waveform
M(14) M(15)	Charge Pump Operation/Test.	**M(15)**	**M(14)**	**OPERATION/TEST**	
		0	0	Normal Operation	
		0	1	Charge Pump Constant Current Source	
		1	0	Charge Pump Constant Current Sink	
		1	1	High Impedance State	

DC Offset Calibration Counter

BIT	DESCRIPTION
C(0-6)	Least Significant bit C(0) to Most significant bit C(6) of the offset calibration counter/divider. The calibration clock frequency and calibration time is defined by the Reference signal frequency divided down by this counter as follows: CAL TIME = $22 * \frac{\text{COUNT}}{\text{REFCLKFREQ}}$ where count = (C + 1) * 2 (SAR Clock)

Thin Plastic Quad Flatpack Packages (LQFP)



Q48.7x7A (JEDEC MS-026BBC ISSUE B)
48 LEAD THIN PLASTIC QUAD FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.062	-	1.60	-
A1	0.002	0.005	0.05	0.15	-
A2	0.054	0.057	1.35	1.45	-
b	0.007	0.010	0.17	0.27	6
b1	0.007	0.009	0.17	0.23	-
D	0.350	0.358	8.90	9.10	3
D1	0.272	0.280	6.90	7.10	4, 5
E	0.350	0.358	8.90	9.10	3
E1	0.272	0.280	6.90	7.10	4, 5
L	0.018	0.029	0.45	0.75	-
N	48		48		7
e	0.020 BSC		0.50 BSC		-

Rev. 2 1/99

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08mm (0.003 inch).
7. “N” is the number of terminal positions.

Sales Office Headquarters

NORTH AMERICA
Intersil Corporation
P. O. Box 883, Mail Stop 53-204
Melbourne, FL 32902
TEL: (407) 724-7000
FAX: (407) 724-7240

EUROPE
Intersil SA
Mercure Center
100, Rue de la Fusee
1130 Brussels, Belgium
TEL: (32) 2.724.2111
FAX: (32) 2.724.22.05

ASIA
Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029

Attachement-5

Datasheet of HFA3983.

ADVANCE INFORMATION | Data Sheet | September 1999 | File Number 4635.2

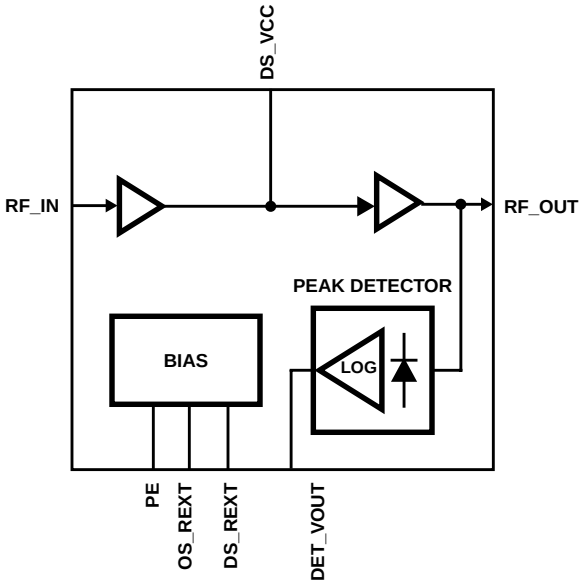
2.4GHz Power Amplifier and Detector

The HFA3983 is a 2.4GHz monolithic SiGe Power Amplifier designed to operate in the ISM Band. It features two low voltage single supply stages. Cascaded, they deliver a 18dBm (Typ) of an output power for the typical DSSS signal (ACPR, 1st Side Lobe < -30dBc, 2nd Side Lobe < -50dBc).

In addition, the device includes a 2.4GHz detector which is accurate over a 15dB of dynamic range with (±)1dB. Therefore, an accurate ALC function can be implemented.

The HFA3983 is housed in a 28 lead exposed paddle EPTSSOP package well suited for PCMCIA board applications.

Simplified Block Diagram



Features

- Single Supply . . . . . 2.7V to 3.6V
- Output Power . . . . . 18dBm (Typ) at ACPR, DSSS, 1st Side Lobe < -30dBc, 2nd Side Lobe < -50dBc
- Power Gain . . . . . 30dB (Typ)
- Detector Linear Input Power Range 15dB
- Detector Accuracy . . . . . ±1.0dB

Applications

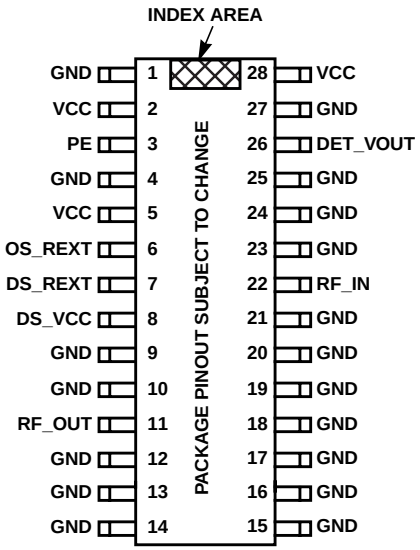
- EEE802.11 1 and 2Mbps Standard
- Systems Targeting IEEE802.11, 11Mbps Standard
- Wireless Local Area Networks
- PCMCIA Wireless Transceivers
- ISM Systems Including Automatic Level Control (ALC)
- TDMA Packet Protocol Radios

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HFA3983IV	-40 to 85	28 Ld EPTSSOP	M28.173A
HFA3983IV96	-40 to 85	Tape and Reel	

Pinout

HFA3983
(EPTSSOP)
TOP VIEW



Detailed Device Description

As part of the Prism II WLAN chip set, the HFA3983 works seamlessly with the chip set components to give you a highly integrated, cost effective 11Mb/sec WLAN solution in the 2.4 to 2.5GHz ISM band. The HFA3983 is fabricated in the fastest SiGe BiCMOS process available allowing superior RF performance, normally found only in GaAs IC's, and cost effective functions, normally requiring external components, to be integrated onto one IC. The HFA3983 integrates the following functions in one compact 28 pin EPTSSOP:

- Two Stage, 30dB Gain RFPA,
- Logarithmic power detect function (15dB Dynamic Range),
- CMOS level compatible Power Up/Down function,
- Single Supply, 2.7V to 3.6V Operation.

The HFA3983 contains a highly linear RFPA designed to deliver 17dBm or higher power levels and meet an ACPR specification of -30dBc in the 2.4 to 2.5GHz ISM band. The performance of this two stage RFPA can be optimized by adjusting the bias current in each stage with a dedicated resistor. No external positive or negative power supplies are required to set the bias currents. The on chip bias network provides the optimum bias current temperature compensation when low TC external resistors are used. To get the best performance from the HFA3983, the output stage matching network can be tailored using external components.

The HFA3983 power detect function provides a DC output voltage that is proportional to the logarithm of the output power. For an output power of 18dBm, the detector is accurate to within a dB. The slope of the detector output voltage is 100mV/dB over a 15dB dynamic range. A simple application of the detector is to provide in-line monitoring of the output power using a DC voltmeter. No longer is a power meter or spectrum analyzer required. A more value added application would use the HFA3861 Baseband Processor to dynamically monitor the HFA3983 output power and to control transmit power by adjusting the AGC of the HFA3783 IF Quadrature Modem to provide the best possible error free data transfer rate for any given environment. Closed loop power control is very important feature which compensates for variability in the transmit chain (radio to radio, channel to channel, over temperature...).

The HFA3983 power up/down feature integrates the power down capability onto the IC and requires no external components thus freeing up board space and reducing external component count and cost. When the CMOS compatible PE (power enable) pin is driven low, the total supply current drops to under 200uA in, typically 230nS. When the PE pin is driven high, the full HFA3983 output power is available in a few hundred nanoseconds.

In summary, the HFA3983 RFPA provides a highly cost effective solution for the PA function by integrating many features that would require significant development time, drive up the total bill of materials cost and consume precious board space. It mates seamlessly with the other Prism II IC's to provide a highly integrated, cost effective 11Mb/sec WLAN solution in the 2.4 to 2.5GHz ISM band.

Pin Descriptions

PIN NUMBER	NAME	DESCRIPTION
1	GND	DC and RF Ground.
2	VCC	Power supply.
3	PE	Digital input control pin to enable the operation of the Power Amplifier. Enable logic level is High.
4	GND	DC and RF Ground.
5	VCC	Power supply.
6	OS_REXT	Output stage bias resistor, biasing scheme independent of absolute temperature.
7	DS_REXT	Driver stage bias resistor, biasing scheme independent of absolute temperature.
8	DS_VCC	Driver stage power supply.
9, 10	GND	DC and RF Ground.
11	RF_OUT	RF Output of the Power Amplifier.
12, 13, 14, 15, 16, 17, 18, 19, 20, 21	GND	DC and RF Ground.
22	RF_IN	RF Input of the Power Amplifier.
23, 24, 25	GND	DC and RF Ground.
26	DET_VOUT	Detector output.
27	GND	DC and RF Ground.
28	VCC	Power supply.

Absolute Maximum Ratings

Supply Voltage . . . . . TBD
Voltage on Any Other Pin. . . . . -0.3 to V_{CC} +0.3V
V_{CC} to V_{CC} Decouple . . . . . -0.3 to +0.3V
Any GND to GND. . . . . -0.3 to +0.3V

Operating Conditions

Temperature Range . . . . . -40 to 85^{o}C
Supply Voltage Range . . . . . 2.7V to 3.6V
Power Dissipation at 25^{o}C. . . . . TBD

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JC} (^{o}C/W)
EPTSSOP Package	15

Maximum Junction Temperature (Plastic Package) . . . . . .150^{o}C
Maximum Storage Temperature Range. . . . . -65^{o}C to 150^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . . .300^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JC} is measured with the component mounted on an evaluation PC board in free air with the exposed paddle soldered to an infinite heatsink.

General DC Electrical Specifications

PARAMETER	TEMP. (^{o}C)	MIN	TYP	MAX	UNITS
Supply Voltage	Full	2.7	-	3.6	V
Total Power Amplifier Supply Current at 3.3V, 18dBm Output	25	-	180	-	mA
RF Detector Supply Current	25	-	-	5	mA
Power Down Supply Current	Full	-	200	-	µA
Power Up/ Down Speed	Full	-	230	-	ns
CMOS Low Level Input Voltage	Full	-	-	0.3*V_{DD}	V
CMOS High Level Input Voltage (V_{DD} = 3.6V)	Full	0.7*V_{DD}	-	4.0	V
CMOS Threshold Voltage	Full	-	0.5*V_{DD}	-	V
CMOS High or Low Level Input Current	Full	-1.0	-	+1.0	µA

Power Amplifier AC Electrical Specifications

V_{CC} = 3.3V, f = 2.45GHz, Unless Otherwise Specified. Typical Application Circuit (external input and output matching networks) has been used.

PARAMETER	TEST CONDITIONS	TEMP. (^{o}C)	MIN	TYP	MAX	UNITS
RF Frequency Range		Full	2400	-	2500	MHz
Power/Voltage Gain		Full	28	30	32	dB
Noise Figure		Full	-	-	7	dB
Input 50Ω VSWR		25	-	-	2.00:1	-
Output 50Ω VSWR		25	-	-	3.00:1	-
Output Power	ACPR, DSSS, 1st Side Lobe <-30dBc, 2nd Side Lobe <-50dBc	Full	17	18		dBm
Output Stability VSWR	Output Spurs Less than -60dBc	Full	-	-	10:1	-
Output Load Mismatch	(Note 2)	Full	-	-	10:1	-

NOTE:

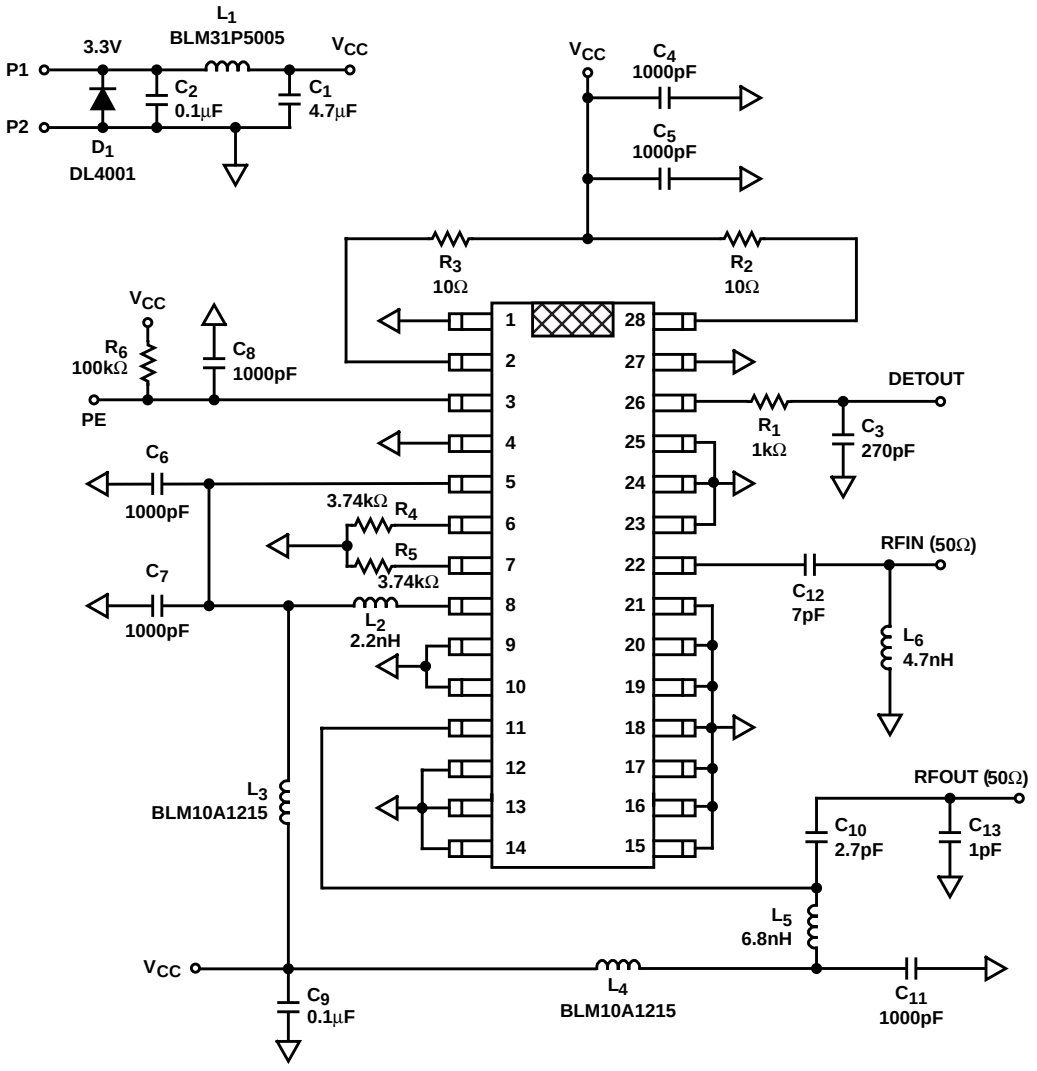
2. Devices sustain no damage when subjected to a mismatch of maximum 10:1.

Peak Detector AC Electrical Specifications

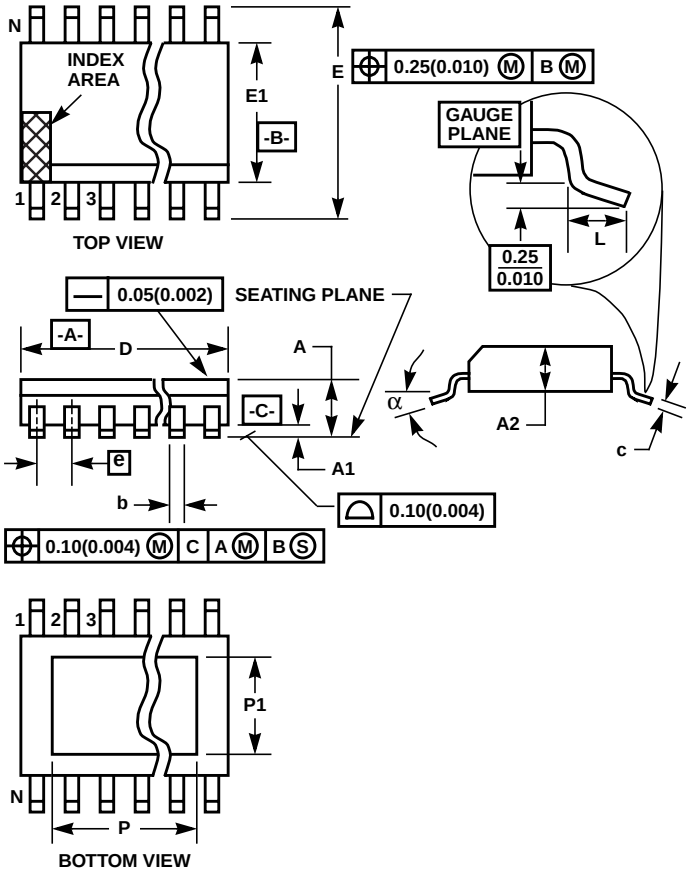
PARAMETER	TEST CONDITIONS	TEMP. (^{o}C)	MIN	TYP	MAX	UNITS
RF Output Detector Response Time	External Capacitor, C = 5pF	Full	-	0.1	1	µs
RF Output Detector Voltage Range	Load > 1M	Full	0	-	1.5	V
RF Output Detector Linearity	Over Linear Range	Full	-0.5	-	+0.5	dB/V
RF Output Detector Accuracy	600mVDC Output	Full	-1	-	+1	dB
RF Output Detector Slope	Over Linear Range	Full	-	10	-	dB/V

HFA3983EVAL Board Schematic

TYPICAL APPLICATION EXAMPLE



Thin Shrink Small Outline Exposed Pad Plastic Packages (EPTSSOP)



M28.173A

28 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.047	-	1.20	-
A1	0.002	0.006	0.05	0.15	-
A2	0.031	0.051	0.80	1.05	-
b	0.0075	0.0118	0.19	0.30	9
c	0.0035	0.0079	0.09	0.20	-
D	0.378	0.386	9.60	9.80	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.0177	0.0295	0.45	0.75	6
N	28		28		7
α	0^o	8^o	0^o	8^o	-
P	-	0.138	-	3.50	11
P1	-	0.118	-	3.0	11

NOTES: Rev. 1 6/99

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AET, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)
11. Dimensions “P” and “P1” are thermal and/or electrical enhanced variations. Values shown are maximum size of exposed pad within lead count and body size.

Attachement-6

Document on Processing Gain Calculation and Test.

Intersil Corporation Certification Report

Testing for Compliance with FCC Rules 15-247e

Theoretical BER Curves for the IEEE 1 and 2Mbps Modulations

11Mbps Channel 1 Processing Gain

11Mbps Channel 6 Processing Gain

11Mbps Channel 11 Processing Gain

2Mbps Channel 6 Processing Gain

Certification Report on Compliance with Respect to FCC CFR 47, Para. 15.247(e)
Measurement of Processing Gain of Direct Sequence Spread Spectrum

Product: Intersil HWB3163 Rev B WLAN PCMCIA

Tested by: Intersil Corp.
2401 Palm Bay Rd.
Palm Bay, FL 32905

Prepared by: Robert J. Rood, Staff Eng.
Ph (407)724-7108
Fax(407)724-7886
e-mail: rrood@intersil.com

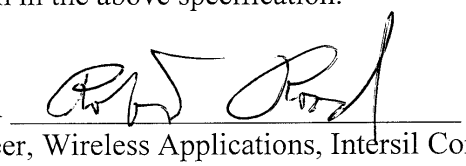
Date: October 14, 1999

ENGINEERING SUMMARY AND CERTIFICATION

This report contains the results of the engineering evaluation performed on an Intersil Wireless LAN PC Card, Model HWB3163 Rev B. The tests were carried out in accordance with FCC CFR 47, Para. 15.247(e).

Robert Rood is a Wireless Applications Staff Engineer at Intersil Corporation. Intersil is a new independent company as of August 13, 1999, previously known as Harris Semiconductor. Robert received a BSEE from the University of Florida in 1979 and his Masters of Science in Engineering Management from Florida Tech in 1988. He joined Harris Semiconductor in 1983 as a Test Engineer after 3 ½ years with Burr Brown Research Corp. He was promoted to Test Staff Engineer in 1989 and moved into Applications in 1991 where he has built on his experience with high speed linear and currently leads the wireless radio development team.

I certify that this data was taken by me or at my direction and to the best of my knowledge and belief, is true and accurate. Based on the test results, it is certified that the product meets the requirements as set forth in the above specification.

Submitted by: Robert Rood  Date: Nov 11, 1999
Staff Engineer, Wireless Applications, Intersil Corp.

Processing Gain of a Direct Sequence Spread Spectrum, FCC CFR 47, Para. 15.247(e)

Product Name: HWB3163 Rev B

FCC Requirements: The processing gain of a direct sequence system shall be at least 10dB. The processing gain shall be determined from the ratio in dB of the signal-to-noise ratio with the system spreading code turned off to the signal-to-noise ratio with the system spreading code turned on, as measured at the demodulated output of the receiver.

Environmental Conditions: Room Temperature and Humidity: 25°C and 50%.

Power Input: DC Power from a laptop computer.

Test Equipment:
Hewlett Packard Spectrum Analyzer, Model HP8593E 9kHz to 22GHz
Marconi Signal Generator, Model 2031, Freq. Range 10kHz to 2.7GHz
Hewlett Packard Power Meter, Model HP438A
Hewlett Packard Power Sensor, Model HP8481D, -20 to -70dBm
Hewlett Packard Attenuators, Model HP8493A, 6dB and 10dB
Hewlett Packard Step Attenuator, Model HP8494A, 1dB steps
Hewlett Packard Step Attenuator, Model HP8495D, 10dB steps
Hewlett Packard Power Splitter, Model HP11667B
Campaq Laptop Computers (Qty 2), Model Armada 1700

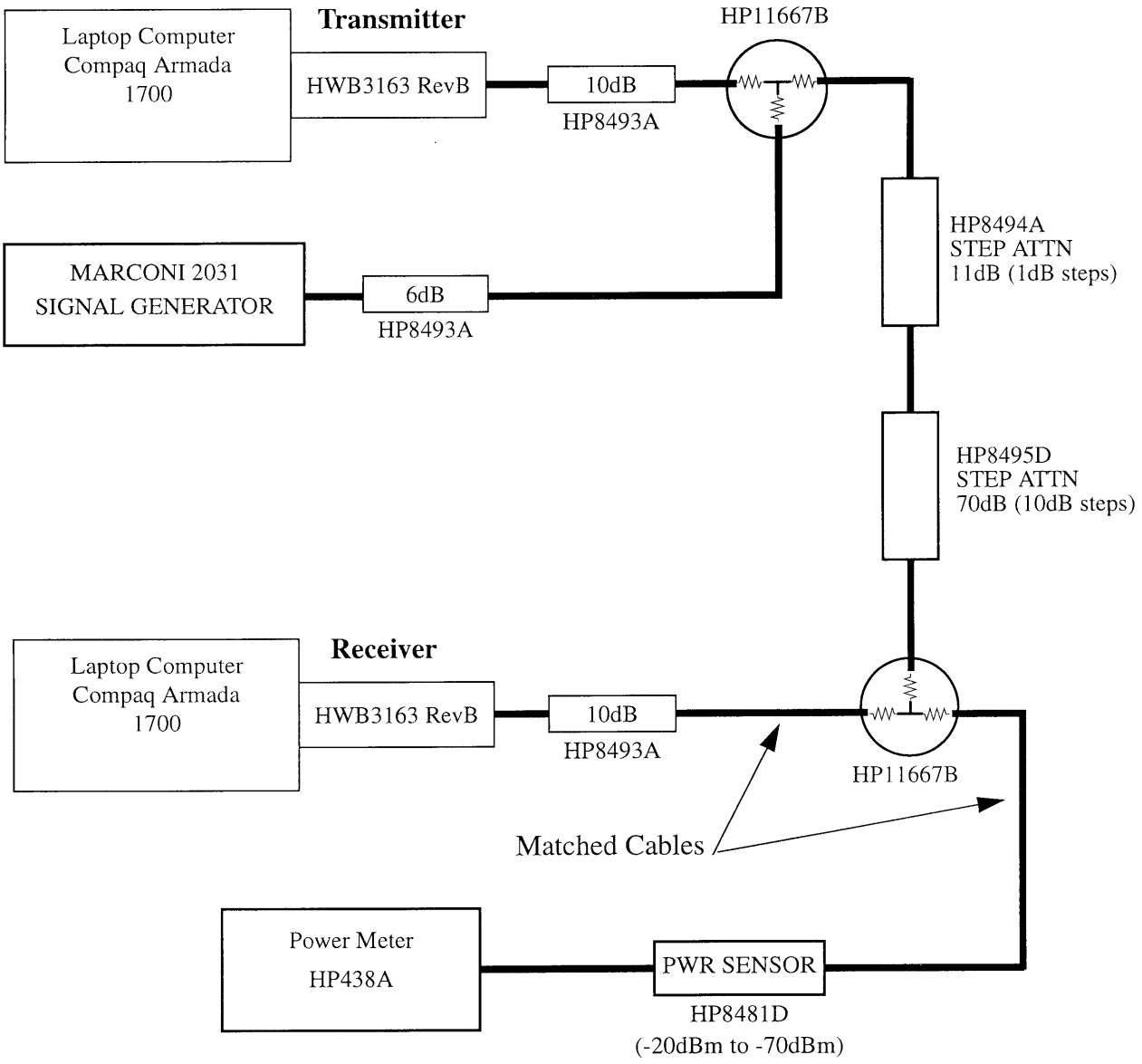
Method of Measurement: Jamming Margin Method. The processing gain may be measured using the CW jamming margin method. Figure 1 shows the test configuration. The test consists of stepping a signal generator in 50kHz increments across the passband of the system. At each point, the generator level required to produce the recommended Bit Error Rate (BER) is recorded. This level is the jammer level. The output power of the transmitting unit is measured at the same point. The Jammer to Signal (J/S) ratio is the calculated. Discard the worst 20% of the J/S data points. The lowest remaining J/S ratio is used when calculating the Process Gain.

Theoretical Calculation: The use of 8% FER frame error rate (or PER packet error rate) as a substitute for the recommended BER bit error rate and the ideal signal to noise ratio per symbol (Es/No) is derived in the attached documents; "Testing for compliance with FCC rules 15-247e", by Carl Andren and "Theoretical BER curves for the IEEE 1 and 2 Mbps modulations" by Carl Andren.

Engineering Summary: Processing Gain Results Summary

Frequency Channel	Data Rate(Mbps)	Gp (dB)
1	11	11.5
6	11	11.4
11	11	12
6	2	12.5

Processing Gain Test Set Up



Testing for compliance with FCC rules 15-247e

Carl Andren
intersil Corporation
October 7, 1999
candren@intersil.com
407-724-7535

Scope

This report presents the test procedure, test configuration and test data associated with a FCC Part 15.247 (e) Jamming Margin test for the indirect measurement of processing gain.

Applicable Reference Documents.

1. "Operation within the bands 902-928 MHz, 2400-2483.5, and 5725-5850 MHz" ***Title 47 Part 15 section 247 (e) Code of Federal Regulations***. **(47 CFR 15.247).**

2. "Report and Order: Amendment of Parts 2 and 15 of the Commission's Rules Regarding Spread Spectrum Transmitters. Appendix C: 'Guidance on Measurements for Direct Sequence Spread Spectrum Systems" ***FCC 97-114. ET Docket No. 96-8, RM-8435, RM-8608, RM-8609.***

3. "HFA3861A Direct Sequence Spread Spectrum Baseband Processor" ***Harris Corporation Semiconductor Sector Preliminary Data Sheet***, Melbourne FL, July 1999.

4. " M-ary Orthogonal Keying BER Curve",

Test Background and Procedure.

According to FCC regulations [1], a direct sequence spread spectrum system must have a processing gain, G_p of at least 10 dB. Compliance to this requirement can be shown by demonstrating a relative bit-error-ratio (BER) performance improvement (and corresponding signal to noise ratio per symbol improvement of at least 10 dB) between the case where spread spectrum processes (coding, modulation) are engaged relative to

the processes being bypassed. In some practical systems, the spread spectrum processing cannot simply be bypassed. In these cases, the processing gain can be indirectly measured by a jamming margin test [2]. In accordance with the new NPRM 99-231, if the vendor has a system with less than 10 chips per symbol, the CW jamming results must be supported by a theoretical explanation of the system processing gain.

Theoretical calculations

The processing gain is related to the jamming margin as follows [2]:

$$G_p = \left(\frac{S}{N}\right)_{output} + \left(\frac{J}{S}\right) + L_{system}$$

Where $BER_{REFERENCE}$ is the reference bit error ratio with its corresponding, theoretical output signal to noise ratio per symbol, $(S/N)_{output}$, (J/S) is the jamming margin (jamming signal power relative to desired signal power), and L_{system} are the system implementation losses.

The maximum allowed total system implementation loss is 2 dB.

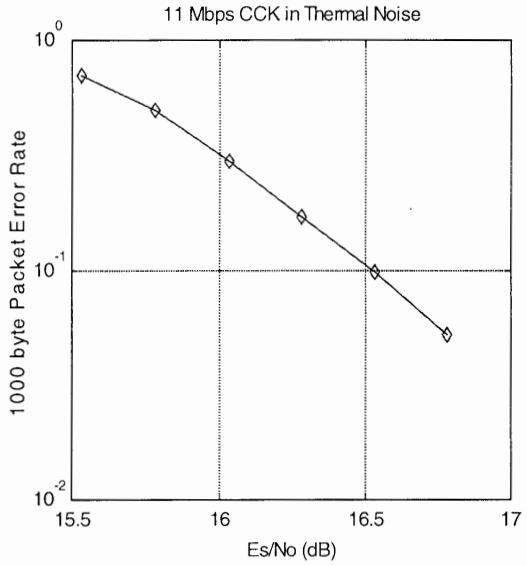
The HFA3861A direct sequence spread spectrum baseband processor uses CCK modulation which is a form of M-ary Orthogonal Keying. The BER performance curve is given by [5]:

" The probability of error for generalized M-ary Orthogonal signaling using coherent demodulation is given by:

$$P_e = 1 - P_{c1} = 1 - \frac{1}{\sqrt{2\pi}} \int_{-\frac{S_{01}}{N_0}}^{\infty} \left[2\left(1 - Q\left\{ z + \sqrt{2\frac{E_b}{\eta}} \right\}\right) \right]^{\frac{M}{2}-1} \exp\left\{ -\frac{z^2}{2} \right\} dz$$

This integral cannot be solved in closed form, and numerical integration must be used. This is done in a MATHCAD environment and is displayed in graphical format.

1.1 1000 byte PER vs. Es/No



The reference PER is specified as 8% . The corresponding Es/No (signal to noise ratio per symbol) is 16.4 dB. The Es/No required to achieve the desired BER with maximum system implementation losses is 18.4 dB. The minimum processing gain is again, 10 dB, therefore:

$$G_p = \left(\frac{E_s}{N_o}\right)_{output} + \left(\frac{J}{S}\right) + L_{system} = 16.4dB + 2.0dB + \left(\frac{J}{S}\right) \geq 10dB$$

$$G_p = 18.4\,dB + \left(\frac{J}{S}\right) \geq 10dB$$

The minimum jammer to signal ratio is as follows:

$$\left(\frac{J}{S}\right) \geq -8.4\,dB$$

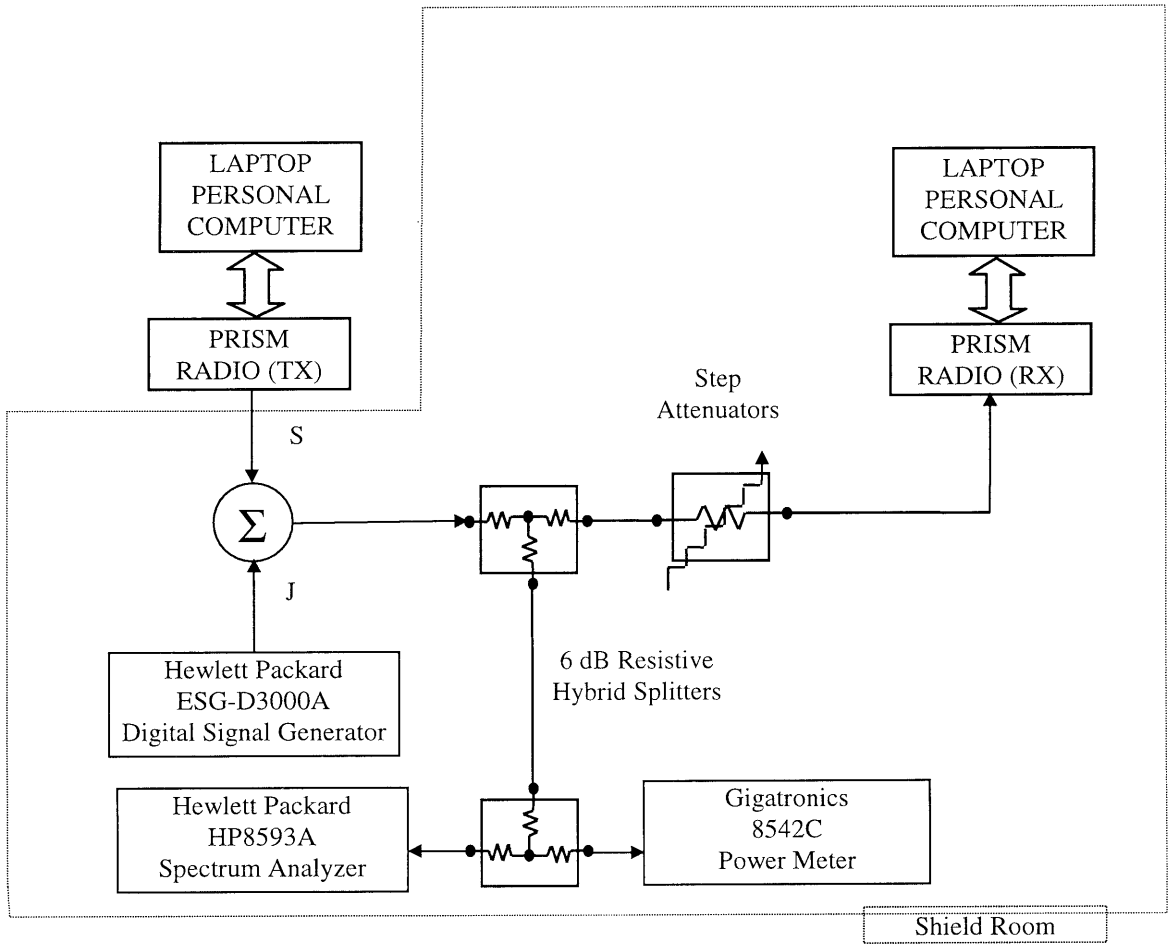
For the case of the HFA3861A, the bit rates are 1, 2, 5.5, and 11 Mbps. The corresponding symbol rates are 1, 1, 1.375, and 1.375 MSps. The chip rate

is always 11 MCps, so the ratio of chip rate to symbol rate is 11:1 for the 1 and 2 Mbps rates and 8:1 for the 5.5 and 11 Mbps rates. Since the symbol rate to bit rate is less than 10 for the higher rates, we supply the theoretical processing gain calculation for these cases where both spread spectrum processing gain and coding gain are utilized. This is reasonable in that they cannot be separated in the demodulation process. If a separable FEC coding scheme were used, we would not be comfortable making this assertion.
As can be seen from the curve of figure 1, the Es/N0 is 16.4 dB at the PER of 8%. This PER can be related to a BER of 1e-5 on 1000 byte packets. With 8 bits per symbol, the Eb/N0 is then 7.4 dB or 9 dB less than the Es/N0. It is well known that the Eb/N0 of BPSK is 9.6 dB for 1e-5 BER, so therefore the coding gain of CCK over BPSK is 2.2 dB. We add this to the processing gain of 9 dB to get 11.2 dB overall processing gain for the CW jammer test.

Taking the calculations above, if the $\left(\frac{J}{S}\right) \geq -8.4\,dB$ then the equipment passes the CW jamming test.

Test Configuration: CW Jamming Margin (15.247) (e)

Basic Test Block Diagram



Test Procedure

Obtain the simplex link shown. Perform all independent instrumentation calibrations prior to this procedure. Set operating power levels using fixed and variable attenuators in system to meet the following objectives:

1. Signal Power at receiver approximately -60 dBm (above thermal sensitivity such that thermal noise does not cause bit errors).

2. Signal Power at power meter between -20 and -30 dBm for optimal linearity.

3. Use spectrum analyzer to monitor test.

4. Ensure that CW Jammer generator RF output is disabled and measure the power at the power meter port using the power meter. This is the relative signal power, S_r.

5. Disable Transmitter, and set CW Jammer generator RF output frequency equal to the carrier frequency and enable generator output. Set reference CW Jammer power level at power meter port 8.4 dB below S_r (minimum J/S, or 10 dB processing gain reference level). Note the power level setting on the generator, this is the reference CW Jammer power setting, J_r.

6. Disable CW Jammer, re-establish link. PER test should be operating essentially error-free.

7. Enable CW Jammer at the reference power level and verify that the PER test indicates a PER of less than 8%.

8. Alternatively, adjust the CW Jammer level to that which causes 8% PER and verify that the S/J is less than 8.4 dB.

9. Repeat step 7 for uniform steps in frequency increments of 50 kHz across the receiver passband with the CW Jammer. In this case the receiver passband is $\pm$8.5 MHz.

The number of points where the PER fails to achieve 8% (is higher than 8%) is determined and if this is above 20% of the total, the test is failed otherwise it is passed.

The margin by which the radio passes the test (for informational purposes) can be determined from the average of the remaining points' PERs scaled on the PER curve above.

The numerical data associated with the following radio channels is tabulated and presented for:

Channel 1: 2412 MHz
Channel 6: 2437 MHz
Channel 11: 2462 MHz

Theoretical BER curves for the IEEE 1 and 2 Mbps modulations

Carl Andren Intersil Corp.

The expected BER versus Eb/N0 curves for these cases may be determined as follows.

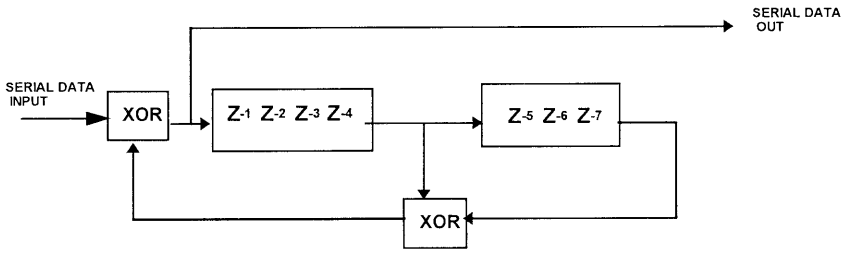
Differential error extension.

The modulation is either DBPSK or DQPSK for 1 and 2 Mbps. With differential coding, there is an error extension factor of 2 which comes from the fact that if one symbol is in error, then the next will be demodulated in error too since it's phase is dependent on the change of phase from symbol to symbol. In DBPSK, this results in a simple factor of two in BER. With QDQPSK, the picture is a little muddied in that a symbol error may cause one or two bit errors since two bits are carried per symbol. The IEEE 802.11 modulations use Grey coding of the phase so that usually only one bit error occurs with a symbol error. Sometimes, two bit errors occur, but this is infrequent at the BER considered. The bit error pattern can be adjacent, separated by one or separated by two for the two error case. This will be shown to be important in descrambling.

De-Scrambling Error Extension

The IEEE 802.11 modulation is scrambled with a self synchronizing scrambler. This scrambler implements a polynomial multiply operation using a feed back shift register configuration as shown in figure 1.

Scrambler Polynomial; $G(z)=Z^{-7}+Z^{-4}+1$



It mixes two taps out of a 7 bit shift register with the data stream. The shift register is fed the received data and any error will propagate through the register for the next 7 clocks. As the error bit passes each of the taps, it will contaminate the output data. Thus each input error can produce several errors on the output. The bit error rate has to be adjusted to account for this effect. For the IEEE 802.11 modulation, taps at registers 4 and 7 are used. In BPSK mode, this produces an error extension of 3. Thus, for an output rate of 10^{-5}, the input rate must be $0.33 * 10^{-6}$ which requires that the Eb/N0 be increased by 0.5 dB. In QPSK mode, the errors can be non adjacent since they are symbol errors and the bit in error can be either the first or second of the dibits. This makes it possible for some errors to cancel in the de-scrambler. Therefore the error extension can be either 2 or 3 in this case.

What we see when running the BER test is that the errors generally occur in groups of 6 with occasional 4s.

The overall effect is to move where we operate on the BER curve. The curve below shows the resulting BER versus Eb/N0 curve. It is well known that a simple BPSK link operates at 9.6 dB for 1e-5 BER. With the error extension effect, we see that at that Eb/N0, the error rate is 6 e-5. Or, conversely, we must operate at 10.3 dB to get 1e-5.

When operating DQPSK at 2 Mbps, the Eb/N0 remains essentially the same, but the Es/N0 goes up by 3 dB. For the purposes of the FCC testing for CW jamming, we add the allowed 2 dB for implementation loss to get a net Es/N0 of 15.3 dB.