SWA54, 5GHz Module Datasheet

High Resolution Wireless I2S Audio, based on the Skyworks SKY76303-21, with on board RF PA

General Description

The SWA54 module is a member of the VMX family of wireless module products. The VMX module product concept offers customers fast time to market for point-to-multipoint mono, stereo, or multichannel wireless audio connection. It incorporates Skyworks newest wireless audio chip, Sky76303-21.

As the successor to SKY76303-21, the SKY76303-21 adds high resolution audio to Skyworks world-class proprietary radio protocol as well as an improved RF interface, containing upgrades to 5 GHz band coverage and user flexibility as well as upgraded interference immunity. The radio retains the core features and functions of its predecessors including low and fixed latency audio, superior interference immunity, and inherent coexistence with WiFi.

The SWA54 module hardware integrates all components necessary to complete a 5 GHz wireless multi-client, multichannel link, including SKY76303-21 Wireless Audio Chip, printed diversity antennas, shield can, flash memory, interface connector and all passive components. Just provide power and an I2S interface and you are ready to create a wireless audio link.

The module measures 35 x 35 x 3.5 mm and is provided with a 24 pin FPC connector.

The module is designed to pass FCC, CE, and IC along with various other regional standards.

Applications

- ✓ Hi Resolution Wireless Subwoofer, Front / Rear Speaker
- ✓ Dolby ATMOS Soundbars
- ✓ Multi-channel Soundbar

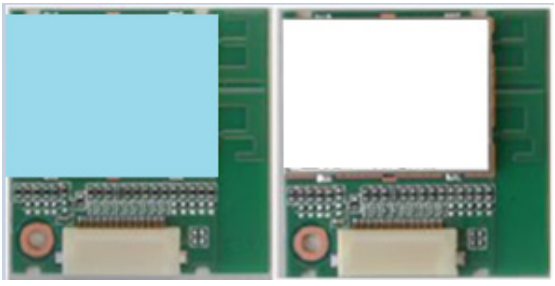
Ordering Options

SWA54-TX: Transmit module with digital audio input

SWA54-RX: Receive module with digital audio output

Features

- ✓ Dual-Band 5GHz (5.2 and 5.8 GHz Bands)
- ✓ FW defined TX or RX. Same Module Hardware serves both.
- ✓ High resolution over-the-air audio and Interfaces
  - ✓ 120 dB SNR end-to-end digital audio path
  - ✓ 2 x I2S Digital Input / Output interface support up to 24 bits.
- ✓ Wireless Range (Typ)
  - ✓ > 30m Non-Line of Sight (NLOS) range
  - ✓ > 100m Line of Sight (LOS) range
- ✓ Auto-search/synch, WIFI avoidance and dynamic channel selection
- ✓ Sample rate converter: Support for 32 - 96kHz input sample rates
- ✓ General purpose over-the-air (OTA) serial interface / data channel:
  - ✓ 11 kbps, bi-directional, full duplex
  - ✓ Support for amplifier control data, meta-data, and remote-control commands
- ✓ Low, fixed latency OTA audio (<16 ms typ)
- ✓ Inter-channel, Inter-client latency less than 5us (All clients at same sample rate)
- ✓ Dual printed PCB diversity antennas for multipath and fading mitigation
- ✓ 24 pin FPC or pin header connector
- ✓ RF parts can-shielded
- ✓ Module meets FCC part 15 / CE rules for emissions



Different label color and WNC P/Ns are used to distinguish between TX and RX.

Revision History

Revision	Description of Changes	Date
1.2	Initial Preliminary release	Aug. 18th, 2022

SWA54 Functional Description

The SWA54 module is available in 2 variations; digital input transmitter module or digital output receiver module.

There are three available I2S digital audio data inputs/outputs, each of these can be configured to operate as either a master or a slave - depending on the application, the I2S ports can operate simultaneously as either inputs or outputs. When configured as slaves, the I2S inputs/outputs can be independently clocked by up to two external masters. In addition, MCLK can be output from the module to provide a reference clock source to an external ADC or DAC. MCLK can also be input to the module to provide a reference clock from an external source.

Figure 1 shows the block diagram of the SWA54 module. The hardware for the audio input (transmit) and audio output (receive) versions of the module is identical and only the firmware loaded onto the module determines its function.

The highly integrated nature of the SKY76303-21 transceiver IC results in few external components being required for the SWA54 module design. 2 printed PCB antennas are used to achieve increased range, and to achieve antenna spatial diversity. The extended-range RF path consists of the antennas, associated tuning components, shield can, the RF switch, RF power amplifer (PA) and two baluns, one connected to each of the RF input/output ports on the SKY76303-21 IC.

A 16MHz crystal oscillator generates the SKY76303-21 fundamental system clock used as the basis for all RF and digital audio clocks.

A 2Mb flash memory chip is used to store the module's application firmware. The SKY76303-21 is able to boot from internal ROM upon first power up, which enables programming the flash chip with the application firmware through USB. In addition, Over-the-air Firmware upgrade capability can be enabled through the application firmware. The module can be controlled from an external host device via the I2C Slave or the SPI Slave data interfaces. The I2C master port allows the module to control other system audio devices such as a sub-woofer amplifier system without having to add another MCU to the product design. Up to 9 additional GPIOs are available on the SWA54 module (not including I2C and I2S signals) for implementing different UI features on the target application. The resources mentioned above can be leveraged to implement low cost sub-woofer designs as outlined below.

Typical Sub-Woofer Implementation

A basic SKY76303-21 Wireless Subwoofer system block Diagram is shown in Fig. 2.

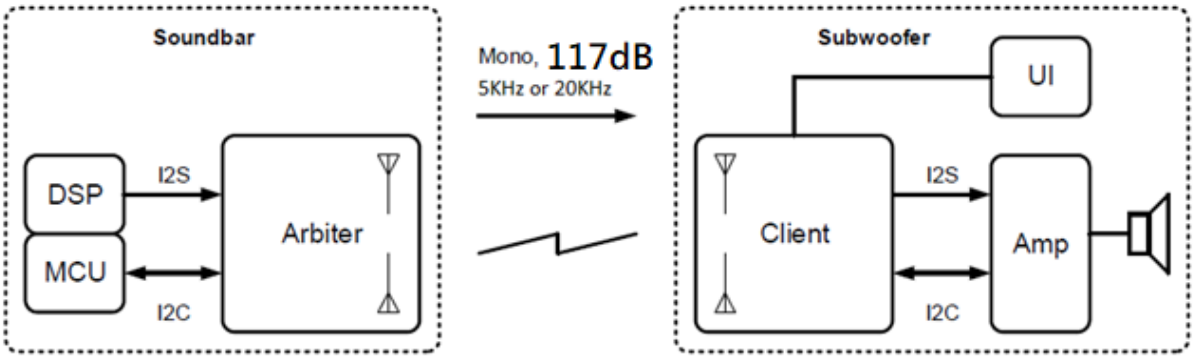


Figure 1: SKY76303-21 Wireless Subwoofer Solution Block Diagram

A simple low cost implementation of sub-woofer design is shown in Figure 3. The sub amplifier consists of a PWM chip plus an output stage device, but no external MCU is required as the SWA54-RX module performs the control function using the I2C master communication port in conjunction with multiple GPIOs. The SWA54 module is configured to accept nominal 5V power from the main application board. An optional reset signal can be supplied to the SWA54-RX module and I2C or SPI slave communication can be used to control the module if required.

Several GPIOs can be used to drive LEDs, or to connect to UI buttons. Typically 2 LEDs may be used and 1 button for pairing purposes. Another button could be used, for example, to implement a “bass enhance” feature. Another GPIO can be used to control the power supply to external system blocks such as the PWM IC and the output stage. The SWA54-RX module can remain powered up during a standby or low power operating mode; however, a true power-down mode can be implemented by configuring pin 17 (GPIO15/ADAT2/CEN) to be used as a chip-enable pin that can be used to power down the SKY76303-21. The SWA54 can also be completely powered down by turning off the main 5V supply.

If the wireless link is lost (ex. when the sound bar is powered down), the SWA54_RX module can, after a timeout period, power down the amplifier and output stage sections to conserve power and to help meet Energy Star requirements.

The I2C master port from the SWA54_RX module (pins 5 and 6 on the connector) can communicate, control, and initialize external audio ICs such as the PWM chip in this example. Other GPIOs can be used to detect fault conditions (over temperature etc) and notify the module. The audio is routed from the SWA54-RX module to the amplifier circuit with the I2S output port which can be configured as either a master or a slave as required. MCLK can also be generated from the SWA54-RX module as a 12.00 MHz clock if required.

SWA54 Module Connections and Interfaces

Signal Type	Description
+5.0V Supply	The SWA54 hardware is configured to accept a nominal +5.0V supply.
Reset	Active low reset input. This pin is driven from an open collector/drain device such that it can be pulled to ground for the active reset state but, when released, must go to a high impedance state. This pin should not be actively driven high, as the SKY76303-21 internal reset circuit will not operate correctly.
I2S In Port	The I2S input port can be configured as a master or slave. Consequently BCLK and LRCK can be either inputs or outputs. In addition, MCLK can be sourced by the module on pin 16. Since the SKY76303-21 IC contains a sample rate converter, MCLK is not required to be supplied to the module when it is an I2S slave. CMOS 3.3V logic levels are used for all I2S signals.
I2S Out Port	The I2S output port can be configured as a master or slave. Consequently BCLK and LRCK can be either inputs or outputs. In addition, MCLK can be sourced by the module on pin 16. Since the SKY76303-21 IC contains a sample rate converter, MCLK is not required to be supplied to the module when it is an I2S slave. CMOS 3.3V logic levels are used for all I2S signals.
I2C Slave Port	The I2C slave port can be used for external host communication and for module testing. It is assumed that external pull up resistors are connected at the I2C master communicating with the module.

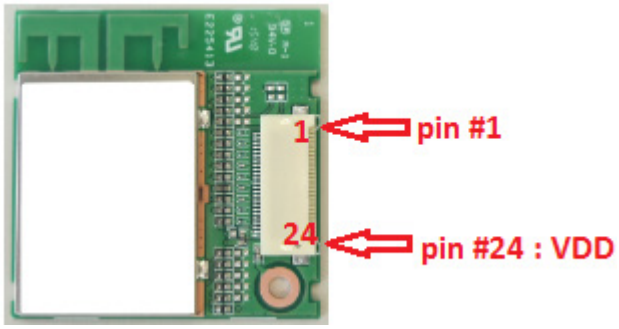
I2C Master Port	The I2C master port is used to communicate with external audio devices such as a sub-woofer amplifier. It is assumed that external pull up resistors are included on the application board.
GPIOs	3.3V CMOS logic level GPIOs available to connect to other devices, or to use as UI supporting GPIOs for LED and button support. All supported GPIOs can be configured as outputs or inputs with configurable pull-ups/pull-downs.

SWA54 Connector Information

Table 1: SWA54 Connector Information

No	Pin Name	Pin Type	AV65100 Pin	SWA54-TX Pin Description	SWA54-RX Pin Description
1	GPIO2/S_SSB	Digital I/O	12	GPIO or SPI Slave Chip Select	GPIO or SPI Slave Chip Select
2	GPIO3/S_SCLK	Digital I/O	11	GPIO or SPI Slave Serial Clock	GPIO or SPI Slave Serial Clock
3	GPIO4/S_SDA/S_MOSI	Digital I/O	10	GPIO, I2C Slave Serial Data or SPI Slave Data In	GPIO, I2C Slave Serial Data or SPI Slave Data In
4	GPIO5/S_SCL/S_MISO	Digital I/O	9	GPIO, I2C Slave Serial Clock or SPI Slave Data Out	GPIO, I2C Slave Serial Clock or SPI Slave Data Out
5	GPIO16/M_SDA	Digital I/O	4	GPIO, I2C Master Serial Data	GPIO, I2C Master Serial Data
6	GPIO17/M_SCL	Digital I/O	3	GPIO, I2C Master Serial Clock	GPIO, I2C Master Serial Clock
7	GPIO20/LINK_LED	Digital I/O	56	GPIO, or LINK_LED Output	GPIO, or LINK_LED Output
8	GPIO21/PAIR	Digital I/O	55	GPIO, or input from PAIR Button	GPIO, or input from PAIR Button
9	GPIO18/BCLK1	Digital I/O	2	GPIO or I2S Port 1 Bit Clock	GPIO or I2S Port 1 Bit Clock
10	GPIO19/WCLK1	Digital I/O	1	GPIO or I2S Port 1 Word Clock	GPIO or I2S Port 1 Word Clock
11	GPIO10/MCLK	Digital I/O	53	GPIO or Master Clock	GPIO or Master Clock
12	GND	GND	Paddle (57)	GND	GND
13	GPIO11/BCLK0	Digital I/O	52	GPIO or I2S Port 0 Bit Clock	GPIO or I2S Port 0 Bit Clock
14	GPIO12/WCLK0	Digital I/O	51	GPIO or I2S Port 0 Word Clock	GPIO or I2S Port 0 Word Clock
15	GPIO13/ADAT0	Digital I/O	50	GPIO or I2S Port 0 Audio Data	GPIO or I2S Port 0 Audio Data
16	GPIO14/ADAT1	Digital I/O	49	GPIO or I2S Port 1 Audio Data	GPIO or I2S Port 1 Audio Data
17	GPIO15/ADAT2/CEN	Digital I/O or Digital Input	48 or 38	GPIO, I2S Port 2 Audio Data or chip enable (1)	GPIO, I2S Port 2 Audio Data or chip enable (1)

18	GPIO22/D+	Digital I/O	47 or 43	GPIO or USB Data Plus (2)	GPIO or USB Data Plus (2)
19	GPIO23/D-	Digital I/O	46 or 42	GPIO or USB Data Minus (2)	GPIO or USB Data Minus (2)
20	GPIO24	Digital I/O	41	GPIO (3)	GPIO (3)
21	RESETN_EXT	Digital Input	37	RESET signal active low (4)	RESET signal active low (4)
22	GND	GND	Paddle (57)	GND	GND
23	VDD	Supply Input	31, 45, 54	+5.0V input supply voltage	+5.0V input supply voltage
24	VDD	Supply Input	31, 45, 54	+5.0V input supply voltage	+5.0V input supply voltage



Notes:

(1) Pin 17 is hardware configured as GPIO15/ADAT2 by default; utilizing this pin as a CEN requires a different stuffing option.

(2) Utilizing pins 18 and 19 as USB D+ and D- requires the firmware to Tri-state GPIOs 22 and 23.

(3) Pin 20 (GPIO24) can be utilized to implement a “Data Waiting” interrupt signal for I2C and SPI Slave data communication.

(4) Pin 21 (RESET_EXT) can be pulled to GND with a switch or an open drain/collector type device to provide a hard reset signal to the SKY76303-21. This pin is pulled up to VDDIO (3.3V) internally in the SKY76303-21 and should not be actively driven high.

1 Electrical, Audio and Timing Specifications

1.1 Module ESD spec.

CONDITION	MIN	MAX
ESD Contact HBM	4kV	----

Notes:

1) HBM = ESD Human Body Model; C = 150pF, R = 330Ω ; non-operational mode.

1.2 Recommended Operating Range

PARAMETER	MIN	TYP	MAX	UNIT
VDD, +5V Supply pin voltage	4.5	5.0	5.5	V
Ambient Temperature (T_A)	0		55	ºC
RESET pin hold time	10			msec
Power Supply Rise Time (to 4.5V)	0		10	msec

1.3 Electrical Characteristics – DC Characteristics

Operating Conditions: VDD = 4.5 to 5.5V, T_A = 0°C to +55 °C, RF Freq = 5150-5250;5725-5875MHz, measured relative to the RF balun single-ended I/O. Typical specifications at T_A = 25°C, VDD = 5.0V

5V.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supply Current (IVDDA)					
	RX mode (continuous RX)		89		mA
	Link mode (for SWA54 TX)		270*a		mA
	Link mode (for SWA54 RX)		130*a		
	TX mode (continuous TX); Pout=+14dBm		350*a		mA
CMOS I/O Logic Levels – 3.3V I/O					
Input Voltage Logic Low, VIL				0.6	V
Input Voltage Logic High, VIH		VDDIO -0.6			V
Output Voltage Logic Low, VOL				0.3	V
Output Voltage Logic High, VOH		VDDIO -0.3			V

*a : This is DCRMS current consumption value. If customer want to implement OCP(over current protection) for SWA54, please consult with WNC for proper setting and design.

1.4 Electrical Characteristics – RF PLL Characteristics

Operating Conditions: VDD =4.5 to 5.5V, T_A = 0°C to +55 °C, RF Freq = 5150-5250;5725-5875MHz, measured relative to the RF balun single-ended I/O. Typical specifications at T_A = 25°C, VDD = 5.0V

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
RF Channel Frequency Range	Band1(lower band)	5150		5250	MHz
	Band4(Upper band)	5725		5875	MHz
RF Channel spacing			2		MHz
RF I/O Impedance	ANT0,ANT1		50		ohm
Crystal Oscillator Frequency	External crystal		16		MHz

1.5 Electrical Characteristics – RF RX Characteristics

Operating Conditions: VDD = 4.5 to 5.5V, T_A = 0°C to +55 °C, RF Freq = 5150-5250;5725-5875MHz, measured relative to the RF balun single-ended I/O. Typical specifications at T_A = 25°C, VDD = 5.0V

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
RF Channel Frequency Range	Band1(lower band)	5150		5250	MHz
	Band4(Upper band)	5725		5875	MHz
RF I/O Impedance	ANT0,ANT1		50		ohm
RX Sensitivity	SSC (single sub-carrier)		-89 *b		dBm
	DSC (double sub-carrier)		-86 *b		dBm
Max input signal	LNA = low gain mode, min IF gain		-5		dBm
Out-of-band blocker level	<5150 MHz, >5850 MHz 2400-2483.5 MHz		-45 -20		dBm dBm
Conductive 2nd harmonic	Main freq. : 5150-5250;5725-5875MHz		-61		dBm

*b : The sensitivity been defined with BER <= 0.002.

1.6 Electrical Characteristics – RF TX Characteristics

Operating Conditions: VDD = 4.5 to 5.5V, T_A = 0°C to +55 °C, RF Freq = 5150-5250;5725-5875MHz, measured relative to the RF balun single-ended I/O. Typical specifications at T_A = 25°C, VDD = 5.0V

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
RF Channel Frequency Range	Band1(lower band)	5150		5250	MHz
	Band4(Upper band)	5725		5875	MHz
RF I/O Impedance	ANT0,ANT1		50		ohm
TX Output power*1	SSC (single sub-carrier) : 2MHZ OBW		14		dBm
	DSC (double sub-carrier) : 4MHZ OBW		13		dBm

***1 : Skyworks has an application note "ATN-126 5 GHz bands for MAC 2.0" mentioned about band setting for worldwide certification.**

1.7 Electrical Characteristics – Audio C/CS

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Frequency Response (-3dB)	24 bit audio, 11KSps over-the-air sample rate	20		5K	Hz
	24 bit audio, 14.8KSps over-the-air sample rate	20		6.5K	Hz
	24 bit audio, 22KSps over-the-air sample rate	20		10K	Hz
	24 bit audio, 29.6KSps over-the-air sample rate	20		13K	Hz
	24 bit audio, 44KSps over-the-air sample rate	20		20K	Hz
Gain Flatness[1]	0dB Input / Output Gain		±0.2		dB
SNR	I2S Input / Output	93		117	dB

1.8 I²S Communication Interface Timing

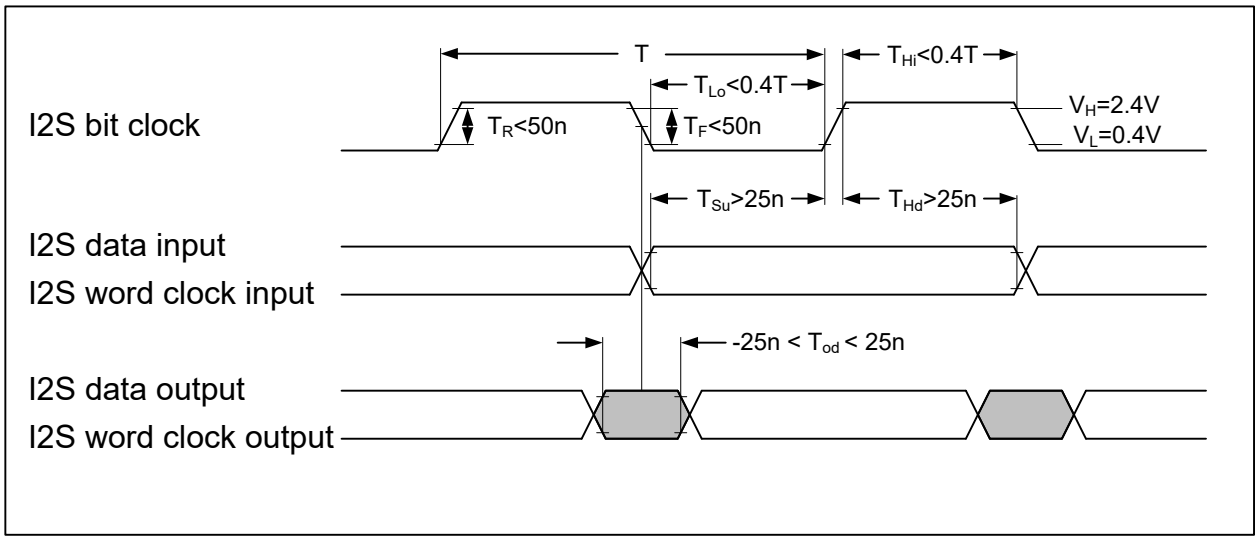
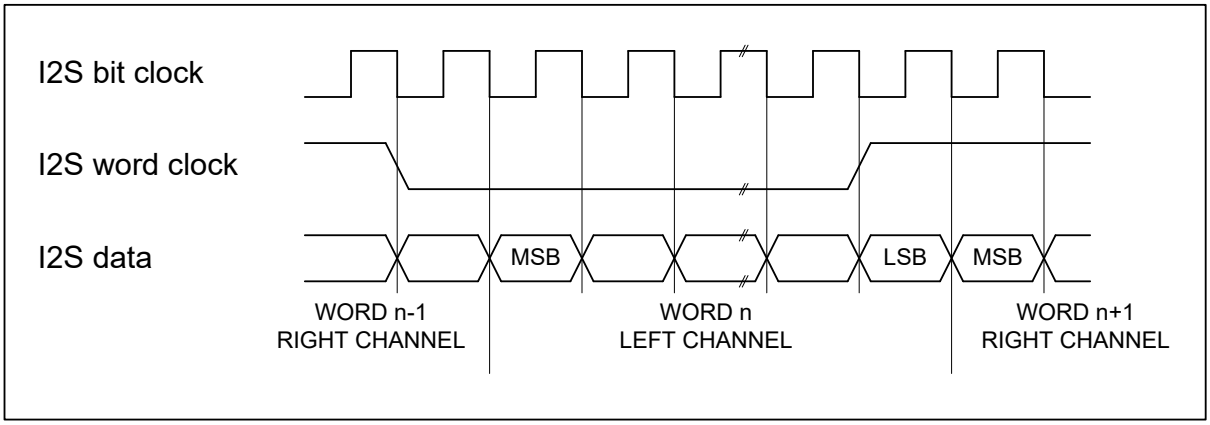


Table 2: SWA54 I2S Timing

		MIN	TYP	MAX	UNIT	NOTES
V_L	low voltage level	-0.3V	0.0V	0.4V	V	
V_H	high voltage level	2.4V	3.3V	3.6V	V	
T	clock period		325.5n		s	1/3.072MHz
T_{Lo}	clock low period	0.4T		0.6T		
T_{Hi}	clock high period	0.4T		0.6T		
T_R	rise time			50n	s	Note 1
T_F	fall time			50n	s	Note 1
T_{Su}	setup time	25n			s	
T_{Hd}	hold time	25n			s	
T_{Od}	output delay	-25n		25n	s	
	bit clocks/word clock		64			

I2S protocol is “I2S Justified” as shown below.



Note 1: The timing specified for the rise and fall times represents the edge rates on the module itself. The rise and fall times of the I2S signals are determined by ESD/EMI mitigation components on the modules, as well as external loading, and will be higher than the specified numbers

1.9 I2C Master/Slave Communication Interface Timing (S_SCL, S_SDA)

The SWA54 has both I2C slave and master interfaces available with their respective pins S_SCL, S_SDA and M_SCL, M_SDA. The interfaces operate in I2C fast-mode and can receive and transmit at up to 400 kbit/s.

Bytes are 8 bits long and are transferred with the most significant bit (MSB) first. Each byte has to be followed by an acknowledge bit. The SWA54 will apply clock-stopping (by holding the clock line S_SCL LOW to force the master into a wait state) if necessary due to internal high-priority tasks.

The slave/master interface can be used both for writing (e.g. sending commands) or reading (e.g. requesting status). An additional GPIO pin on the SWA54 (Ex. GPIO24), can be used to notify the I2C master when a pending message is ready to be sent.

The SWA54 slave interface responds to the 7-bit slave address 1000000 (0x40) as shown in Figure 1 below.

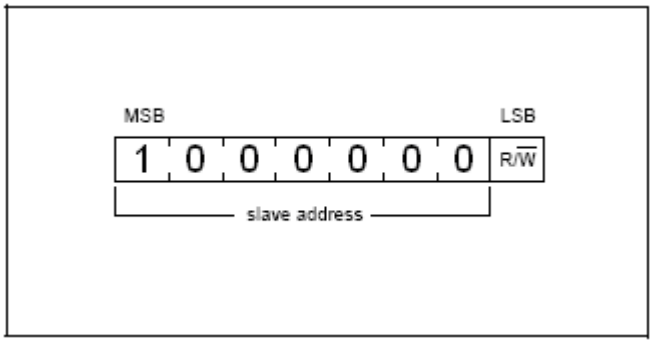


Figure 5: First Byte after the START Procedure

ELECTRICAL SPECIFICATIONS AND TIMING

Table 3: Characteristics of the S_SDA and S_SCL I/Os

PARAMETER	SYMBOL	FAST-MODE		UNIT
		MIN.	MAX.	
LOW level input voltage	V_{IL}	–0.3	0.8	V
HIGH level input voltage	V_{IH}	2.0	3.6	V
LOW level output voltage (open drain or open collector) at 1 mA sink current:	V_{OL}	0	0.4	V
Output fall time from V_{IHmin} to V_{ILmax} with a bus capacitance from 10 pF to 400 pF	t_{of}	0	250	ns
Pulse width of spikes which must be suppressed by the input filter	t_{SP}	0	50	ns
S_SCL clock frequency	f_{SCL}	0	400	kHz
LOW period of the S_SCL clock	t_{LOW}	1.3	–	µs
HIGH period of the S_SCL clock	t_{HIGH}	0.6	–	µs
Data hold time	$t_{HD;DAT}$	100	–	ns
Data set-up time	$t_{SU;DAT}$	100	–	ns

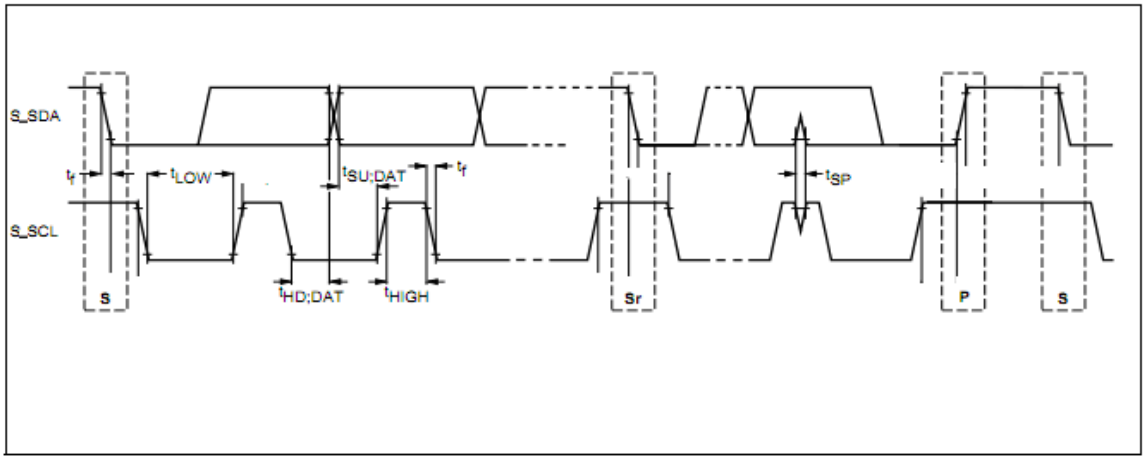


Figure 6: Definition of Timing for F/S-Mode Devices on the I^2C-Bus

Ordering Information

Table 4: SWA54 Module Ordering Information

Module Part Number	Option Code	Description
SWA54	TX	Digital Input , FPC Connector, integrated printed PCB antennas
SWA54	RX	Digital Output, FPC Connector, integrated printed PCB antennas
SWA54	UFL RX	Digital Output, FPC Connector, integrated printed PCB + UFL conn @ bottom side for external ant.

FCC Statement:
Federal Communication Commission Interference Statement
This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

FCC Caution: Any changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate this equipment.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

This device and its antenna(s) must not be co-located with any other transmitters except in accordance with FCC multi-transmitter product procedures.
Refering to the multi-transmitter policy, multiple-transmitter(s) and module(s) can be operated simultaneously without C2P.

IMPORTANT NOTE:
FCC Radiation Exposure Statement:
This equipment complies with FCC radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

IMPORTANT NOTE:
This module is intended for OEM integrator. The OEM integrator is responsible for the compliance to all the rules that apply to the product into which this certified RF module is integrated.
Additional testing and certification may be necessary when multiple modules are used.

20 cm minimum distance has to be able to be maintained between the antenna and the users for the host this module is integrated into. Under such configuration, the FCC radiation exposure limits set forth for an population/uncontrolled environment can be satisfied.

Any changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment.

USERS MANUAL OF THE END PRODUCT:
In the users manual of the end product, the end user has to be informed to keep at least 20 cm separation with the antenna while this end product is installed and operated. The end user has to be informed that the FCC radio-frequency exposure guidelines for an uncontrolled environment can be satisfied. The end user has to also be informed that any changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment. If the size of the end product is smaller than 8x10cm, then additional FCC part 15.19 statement is required to be available in the users manual: This device complies with Part 15 of FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference and (2) this device must accept any interference received, including interference that may cause undesired operation.

LABEL OF THE END PRODUCT:
The final end product must be labeled in a visible area with the following " Contains TX FCC ID: NKR-SWA54 ". If the size of the end product is larger than 8x10cm, then the following FCC part 15.19 statement has to also be available on the label: This device complies with Part 15 of FCC rules. Operation is subject to the following two conditions: (1) this device may not cause harmful interference and (2) this device must accept any interference received, including interference that may cause undesired operation.

IC Statement:

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes : (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

This device and its antenna(s) must not be co-located with any other transmitters except in accordance with IC multi-transmitter product procedures.

Refering to the multi-transmitter policy, multiple-transmitter(s) and module(s) can be operated simultaneously without reassessment permissive change.

Cet appareil et son antenne (s) ne doit pas être co-localisés ou fonctionnement en association avec une autre

antenne ou transmetteur.

IMPORTANT NOTE:

IC Radiation Exposure Statement:

This equipment complies with IC RSS-102 radiation exposure limits set forth for an uncontrolled environment. This equipment should be installed and operated with minimum distance 20 cm between the radiator & your body.

Cet équipement est conforme aux limites d'exposition aux rayonnements IC établies pour un environnement non contrôlé. Cet équipement doit être installé et utilisé avec un minimum de 20cm de distance entre la source de rayonnement et votre corps.

IMPORTANT NOTE:
This module is intended for OEM integrator. The OEM integrator is responsible for the compliance to all the rules that apply to the product into which this certified RF module is integrated.
Additional testing and certification may be necessary when multiple modules are used.

20 cm minimum distance has to be able to be maintained between the antenna and the users for the host this module is integrated into. Under such configuration, the IC RSS-102 radiation exposure limits set forth for an population/uncontrolled environment can be satisfied.

Any changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment.

USERS MANUAL OF THE END PRODUCT:
In the users manual of the end product, the end user has to be informed to keep at least 20 cm separation with the antenna while this end product is installed and operated. The end user has to be informed that the IC radio-frequency exposure guidelines for an uncontrolled environment can be satisfied. The end user has to also be informed that any changes or modifications not expressly approved by the manufacturer could void the user's authority to operate this equipment. Operation is subject to the following two conditions: (1) this device may not cause harmful interference and (2) this device must accept any interference received, including interference that may cause undesired operation.

LABEL OF THE END PRODUCT:
The final end product must be labeled in a visible area with the following " Contains IC: 4441A-SWA54 ".
The Host Model Number (HMN) must be indicated at any location on the exterior of the end product or product packaging or product literature which shall be available with the end product or online.

Professional installation is required

This radio transmitter [4441A-SWA54] has been approved by Innovation, Science and Economic Development Canada to operate with the antenna types listed below, with the maximum permissible gain indicated. Antenna types not included in this list that have a gain greater than the maximum gain indicated for any type listed are strictly prohibited for use with this device.

Le présent émetteur radio (4441A-SWA54) a été approuvé par Innovation, Sciences et Développement économique Canada pour fonctionner avec les types d'antenne énumérés ci-dessous et ayant un gain admissible maximal d'antenne. Les types d'antennes non inclus dans cette liste qui ont un gain supérieur au gain maximal indiqué pour tout type listé sont strictement interdits pour une utilisation avec cet appareil.

The device for operation in the band 5150–5250 MHz is only for indoor use to reduce the potential for harmful interference to co-channel mobile satellite systems.

les dispositifs fonctionnant dans la bande 5150-5250 MHz sont réservés uniquement pour une utilisation à l'intérieur afin de réduire les risques de brouillage préjudiciable aux systèmes de satellites mobiles utilisant les mêmes canaux.

The maximum antenna gain permitted for devices in the band 5725-5850 MHz shall be such that the equipment still complies with the e.i.r.p. limits specified for point-to-point and non-point-to-point operation as appropriate.

le gain maximal d'antenne permis (pour les dispositifs utilisant la bande 5725-5850 MHz) doit se conformer à la limite de p.i.r.e. spécifiée pour l'exploitation point à point et non point à point, selon le cas.

Table of Antenna

Ant.	Port	Brand	Model Name	Antenna Type	Connector	Gain (dBi)			Remark
						UNII 1	UNII 3	UNII 4	
1	1	WNC	**SWA54**	Printed Antenna	N/A	4.32	4.90	4.50	Internal
2	2	WNC	**SWA54**	Printed Antenna	N/A	2.40	3.50	2.96	
3	1	KINGRF	IA.0355.LA.2FI	PCB Antenna	I-PEX	3.03	4.23	3.01	External

FCC: UNII-1 + UNII-3 + UNII-4

IC：UNII-1 + UNII-3

Notice : IC do Not support UNII-4

Client device (EUT) are prohibited from connecting directly to another client device and must be under control of an indoor AP.

Client, Access Point (AP) and Subordinate are restricted to indoor operation only.

Client devices cannot be used to provide connections between separate buildings or structures.

Client device (EUT) has no direct connection to internet

Devices are prohibited for control of or communications with unmanned aircraft systems including drones.

SWA54 integration manual :

SWA54 integration/comm. is through I2C interface, below contains are register settings for customer to integrate SWA54 module into their platform.

Below host means SWA54 TX module. SWA54 TX and SWA54 RX are the same module HW, only diff. FW configuration to distinguish as SWA54 TX(host) or SWA54 RX(client). For regulation catalog, SWA54 is client only device which NO external host AP neededFinal page app. diagram tell all.

3.1. Command Interface Registers

For the SWA54 product, a block of I^2C registers is reserved for command interface and data passing. The registers are allocated as follows:

Table 3-1; I2C Command Registers

Register Addresses	Names	Description
0x41..0x58	TXData	Buffer to hold message for host-to-SWA54 communication. 24 bytes long.
0x59	TXLen	Host-to-SWA54 message indicator. 0 means no message present; nonzero indicates the length of the message. Set by the host after filling in TXData, cleared by SWA54 after the message has been read.
0x5a	RXLen	SWA54-to-host message indicator. 0 means no message present; nonzero indicates the length of the message. Set by the SWA54 after filling in RXData, cleared by the host after the message has been read.
0x5b..0x72	RXData	Buffer to hold message for SWA54-to-host communication. 24 bytes long.

3.2. MCU-to-SWA54 Message Passing

When the host needs to send a message (for example to provide data to write to flash), the following steps must be followed:

1. First the host insures that all previous messages have been received. This is done by reading the TXLen register (0x59) of the SWA54 Module. If the register is zero, then it is safe to proceed; otherwise, the host must wait and read TXLen again until it is zero.
2. After TXLen has been seen as zero or low, the message data is written to the TXData registers. If the message is shorter than 24 bytes, then the unused registers may be cleared to 0 or may be left unchanged. Message longer than 24 bytes are not allowed.
3. After the message has been written to the TXData registers, the length of the message must be written to TXLen. This may be done in the same I^2C transaction that wrote to TXData, or it may be a separate transaction.
4. As soon as TXLen has been written to nonzero, the firmware will start to read and process the message, then it will write a 0 to TXLen when it is ready for the next message. There is an internal queue of messages where they are stored, so clearing TXLen does not indicate that processing the message is complete, it only indicates that firmware is ready for another message. If the internal queue of messages is full, the firmware will delay clearing TXLen until there is room in the queue for the next message. In this way TXLen will provide flow control, indicating to the host the rate at which messages can be accepted.

3.3. SWA54-to-MCU Message Passing

When the host expects a message from the SWA54, it can use the Data Waiting pin, RXLen and RXData to wait for the message and read it in when it is ready. These registers operate in the same way as the TXData and TXLen registers, but the roles of the host and the SWA54 are reversed. The host must follow these steps:

1: The host must check the Data Waiting GPIO pin (pin 5 on SWA54 modules) to see if there are data ready to be read. Once the Data Waiting pin is pulled low, the RXLen and RXData registers are filled and ready for the host

2: After the host see that the Data Waiting GPIO pin is pulled to LOW, the host must read RXLen (0x5a) of the SWA54 module. The RXLen contains the length of the message that is ready, and the host may proceed to read the message.

3: Once RXLen is nonzero, the host may read the message from the RXData registers. If the message is fewer than 24 bytes, then the unused RXData registers are meaningless and their value cannot be predicted. The RXData registers may be read in the same I^2C transaction as the one that read the RXLen register, or a new transaction may be used.

4: After reading the message from RXData, the host must write a 0 to RXLen to indicate that it is ready for another message. Failing to write a 0 to RXLen will leave the SWA54 unable to pass more messages and the INT flag will stay high. Under no circumstance may the host write to any of the RXData registers; doing so may result in erroneous messages.

4. Extended Commands

Extended commands contain routing information and an encapsulated Command OpCode. Each device in the link has a node number assigned to it. Each peripheral interface in a device has a module identifier number assigned to it. This allows for routing data from any interface on any device in the link, to any interface on any device in the link. This is the mechanism that an outside device must use to perform end to end data communications.

4.1. Extended Command Architecture

The command maximum size per transaction is 24 bytes, allowing for 19 bytes of payload data. The payload can be partially filled, indicated by the Length byte. The format of a command is as follows:

Byte 0 = Extended Command OpCode (Extended Query / Extended Command)

Byte 1 = Source Module ID

Byte 2 = Destination Module ID

Byte 3 = Node ID (upper 4 bits = source, lower 4 bits = destination)

Byte 4 = Length

Bytes 5 through 24 carry the payload (command and / or raw data) to transfer.

Table 4-1; Extended Command Architecture

Byte	Name	Description
0	Message Type	There are three types used: 0xfd Queries that need a response message 0xfe Responses to queries 0xff Commands that need no response
1	Source Module	Always 0x19 for messages sent via I^2C
2	Destination Module	0x00 = Local Command Loop (not OTA) 0x12 for messages sent to the SWA54 application (upgrade or RF application) 0x19 for messages sent to the slave I2C port of the receiving module
3	Destination Node	0xf1 for the TX module to linked RX module 0x1f for the RX module to linked TX module
4	Payload Length	The byte count of the message, excluding the first 4 byte header. For example, a 10 byte message (including the 4 byte header) would need a value of 0x06 here.
5	Embedded Opcode (See Section 0)	This byte specifies exactly what operation the message requires. i.e 0x02 to start upgrade through I2C

Byte	Name	Description
	Or 1st byte of data	
6..23	Data	Varies depending on the command.

4.2. Extended Command OpCodes

For the purpose of this interface, there are three extended commands of interest:

0xFD – Extended Query

0xFE – Extended Response

0xFF – Extended Command

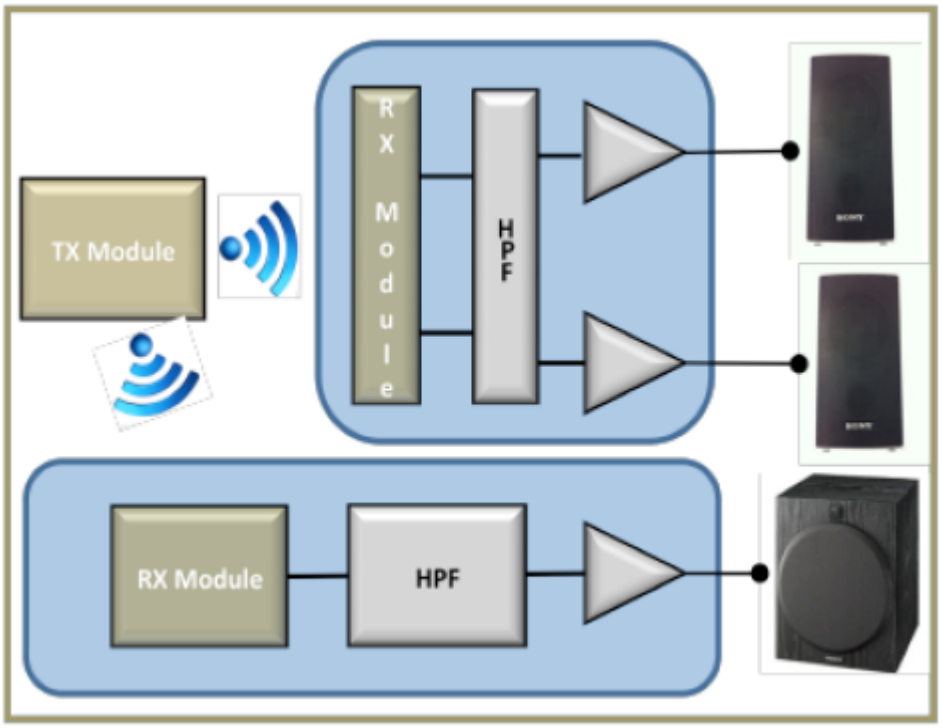


Figure 1-2; 2 Clients Application

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