PCI3610

IS-136 Integrated Baseband Processor

Specifications

The PCI3610 is PrairieComm's next generation of an IS-136A TDMA solution. It's a single chip design that is the product of a refined integration of systems knowledge and product innovation.

The PCI3610 Integrated Baseband Processor provides a fully integrated digital CMOS solution for both dual-mode IS-136A/AMPS Cellular and upbanded IS-136A PCS subscriber products. The list of standards this integrated circuit is compatible with includes, but is not limited to IS-130, IS-136A, IS-137A, IS-641, IS-684, TIA/EIA627, TIA/EIA628, and TIA/EIA635.

Leveraging our experience in bringing to market a two chip solution in the IS-136A TDMA technology, **PrairieComm delivers a single chip design by integrating the Mixed Signal D/A and A/D converters to the Baseband Processor for a powerful solution** in the next generation in mobile terminals. The PCI3610 TDMA single chip solution offers several advantages in power consumption, size, flexibility, and extensibility.

By combining the functions of the digital baseband processor and the mixed signal device onto a single chip, **the PCI3610 is more power efficient and has less pin count (reducing the chip size) than other multiple chip solutions available today**. This not only helps to reduce power consumption, but also allows for smaller terminal designs.

Utilizing PrairieComm's unique open architecture and the ARM/OAK platform, the PCI3610 device provides flexibility and extensibility for customization and future add-ons.

Delivering an optimal IS-136A solution in terms of performance, flexibility, and power consumption, the PCI3610 IS-136A Baseband Processor Series is the best solution for the next generation of IS-136A TDMA terminals.

A number of packaging options exists for the device. A 257-pin PGA is available for development with the OAK DSP bus bonded out. A 180-ball FPBGA is available for production silicon.

General Features:

- Complete IS-136A baseband solution, exceeding all IS-137A specifications
- Low 2.5 V DC power consumption during operation for Digital Core and Mixed Signal blocks
- Low 3.0 V DC power consumption for I/O pads allowing for compatibility with 3.0 V devices
- Supports Cellular, PCS and WiLL applications
- Supports RLP-1 and RLP-2 data services
- Software-controlled power management
- Full calibration for analog signal impairments and manufacturing tolerances
- State-of-the-art submicron CMOS design with built-in testability functions
- A 180-ball FPBGA is available for volume production
- ANSI/IEEE 1149.1 (JTAG) test compliant
- Uses the industry standard ARM microprocessor core running at up to 20 MHz and the industry standard OAK DSP core capable of 80 MIPS

Voice Coding Features

- Internal VSELP and EFR(IS-641) Vocoders

IS-136 Processing Features

- Supports VSELP, EFR(IS-641), RLP-1, RLP-2 channel coding
- Viterbi decoding designed to deliver the maximum coding gain allowed by theory
- Hardware co-processors work with the DSP core to maximize throughput and to minimize power consumption
- Multiple low-power and sleep modes, including complete system shut-down in Paging Modes
- Support for public and private encryption/decryption

AMPS Processing Features

- Internal digital Manchester decoder for AMPS operation
- Wideband data and SAT detection and transponding

Acoustic Signal Processing Features

- Internal DTMF generation/detection
- Internal acoustic echo cancellation

- Programmable digital filters for audio signal path compensation in both IS-136A and AMPS mode
- Voice activity detection
- Support for hands-free operation and audio record/playback

Microprocessor Subsystem Features

- Powerful and efficient 32-bit RISC ARM microprocessor core
- Internal watchdog and sleep timers
- Internal interrupt controllers with support for both internal and external interrupt driven devices
- Internal DMA controller supports efficient and fast serial port operation
- External chip selects with direct connections for devices such as ROM and EEPROM
- Two on-board UARTs, one with fully compliant IS-707 hardware flow control
- On-board synchronous serial interface (SSI) enables three-wire serial control of devices such as EEPROM, CODEC, LCD, and RF and mixed-signal chips
- Flexible External Memory Interface supports 2 MByte 8 and 16-bit devices with programmable wait states
- External Memory Interface allows patching of DSP ROM code
- Complete control of the DSP subsystem via an internal host interface
- Multiple low-power and sleep modes
- Source-level debugging via the JTAG interface
- Support for ROM ICE debugging tools
- 50 programmable general purpose input/outputs
- Flexible keypad interface
- Multiple low-power modes including a selectable microprocessor clock input (32 KHz) for ultra low power operation
- Programmable synthesizer interface
- Real Time Clock module

Mixed Signal Features

- Internal Audio Codec meeting IS-137A and ITUG7.14 standards
- Baseband DACs and ADCs convert for both IS-136A and AMPS modes eliminating need for Mixed Signal IC

- Direct interface to Mitel Scorpio and Moon ICs as RF interface
- Eight input ADC for Auxiliary measurements of Analog signals
- Eight output Pulse Width Modulated Digital-to-Analog converters for user-defined analog control

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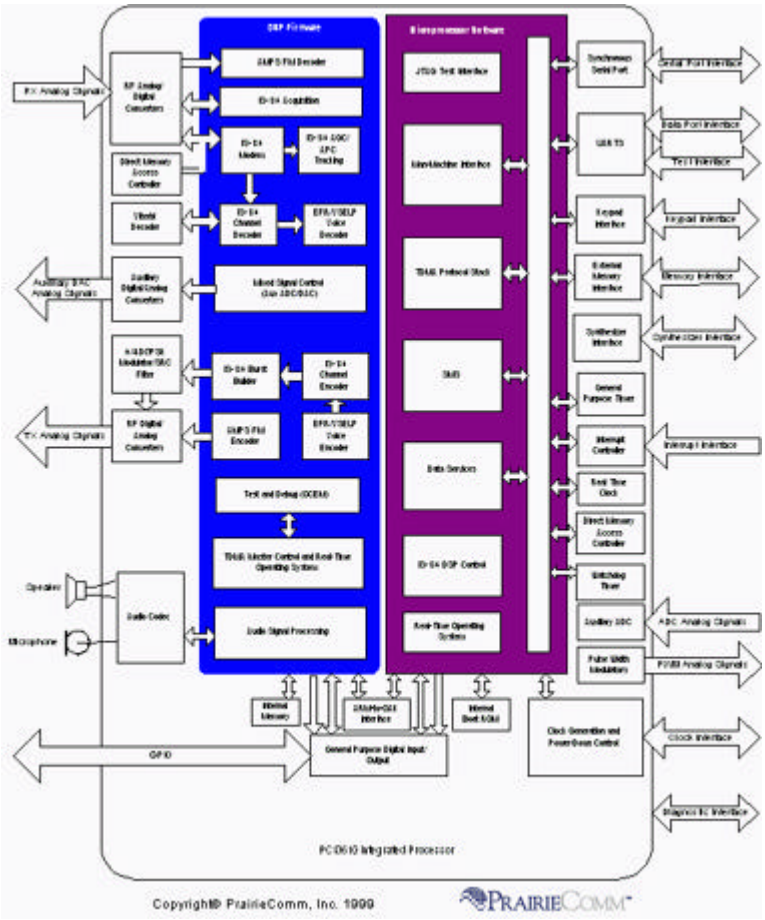

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