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# TDMA/AMPS Analog Baseband Interface

# Target Specification

# 'Scorpio'

## Revision 0.8

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This document details the design description and target IC specification of the 'Scorpio' TDMA/AMPS Analog Baseband Interface.

This ASIC component combines a monolithic active filter circuit incorporating circuits for receiving both TDMA and AMPS signals with equivalent transmit filters and two fully programmable if synthesizers. None of the integrated filters will require external tuning.

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| Characteristic | Value | | | Units | Comments |
|---|---|---|---|---|---|
| | Min | Typ | Max | | |
| **Operating Conditions** | | | | | |
| Supply Voltage | 2.7 | 3.0 | 3.3 | Volts | |
| Temperature | -30 | | 85 | ° C | |
| **Supply Current** | | | | | |
| Sleep | | | 25 | µA | |
| Receive Section (I/Q) | | 5.5 | 6.5 | mA | |
| Receive Section (FM) | | 4 | 5 | mA | |
| Receive Section (RSSI) | | 1 | 1.5 | mA | |
| Receive PLL | | 1.5 | 2 | mA | |
| Transmit Section | | | | mA | |
| Transmit PLL | | 1.5 | 2 | mA | |
| **Receive - General** | | | | | |
| Frequency Range | | | 10 | MHz | |
| Input Impedance | | 10 | | kΩ | Differential |
| Output Impedance | | 2 | | kΩ | Differential |
| **Receive (IQ Mode)** | | | | | |
| Input Signal | | 0.53 | | mV | Differential |
| Gain | | 56 | | dB | |
| I/Q Gain Matching | -0.5 | | 0.5 | dB | |
| Noise | | | 17 | µV | 10 Hz to 100kHz referred to input |
| Output 1dB Compression | 3 | | | V p-p | Differential |
| **Receive (FM Mode)** | | | | | |
| Input Signal | 30 | | | µV | Output SINAD = 12dB |
| Audio Output | | | 500 | mV | Defined by external components |
| **RSSI** | | | | | |
| Dynamic Range | 70 | 73 | | dB | |
| Accuracy | -3 | | +3 | dB | |
| Input Signal | 0.024 | | 110 | mV | Internal Attenuator enabled |
| Input Signal | 0.024 | | 20 | mV | Internal Attenuator disabled |
| Input Noise | | 0.024 | | mV | |
| RSSI Output Level | Vdd/2 - 1.2 | | Vdd/2 + 1.2 | V | |
| Attenuator gain | -31.5 | -32 | -32.5 | dB | |
| Attenuator switch-in level | | 4.5 | | mV | Input referred |
| Attenuator switch-out level | | 2.25 | | mV | Input referred |
| RSSI Output Impedance | | 1 | | kΩ | |
| **Receive Filter** | | | | | I/Q and FM Mode |
| Centre Frequency | | 60 | | kHz | |
| 3dB Bandwidth | +/- 16 | | +/- 18 | kHz | |

## Contents

# INTRODUCTION

This details a target specification for the 'Scorpio' IC development. The document is subdivided into 8 sections, section 1 is a general description of the ASIC and sections 2 to 6 cover each of the functional blocks in turn and section 7 & 8 cover package/pinning.

## 1. General Description

This ASIC component combines a monolithic active filter circuit incorporating circuits for receiving both AMPS and TDMA signals with equivalent transmit filters and two fully programmable IF synthesizers. None of the integrated filters will require external tuning.

### 1.1 Receive Path

In the RX path there are two distinct operating modes; The first, baseband I & Q mode, will employ a 60kHz switched capacitor bandpass filter whose output will be down converted and low-pass filtered to remove mixer harmonics, giving a 0-15kHz passband response characteristic for a I and Q baseband channel. This path will be for TDMA.

The second operational mode assumes that FM demodulation is being done in a more traditional fashion and therefore a 60kHz bandpass filter is required. This filter will provide a nominal 49.5dB of in-band gain and 31dB of image rejection, which will be achieved by a 5th order switched capacitor filter with a 3dB bandwidth of +/-15kHz. This FM channel is also supported by an integrated FM analog discriminator and RSSI circuitry, allowing direct Audio/Data and signal strength information at the device boundary.

### 1.2 Transmit Path

The transmit path will provide a variable 0 to 12dB voltage gain in-band, programmable in 3dB steps via a Serial Interface. A lowpass filter will also be provided to reduced data noise from the baseband DAC's. This will allow Scorpio a generic interface to various differing baseband solutions.

### 1.3 IF Synthesis

Two fully programmable IF synthesizers, including two high frequency pre-scalers, two separate reference dividers will be included in order to minimize cross talk between the two synthesizers. The output charge-pump current will be programmable and the supply to the charge pump is supplied via an external device pin, allowing a higher VCO control range.

### 1.4 Power Control

A single dedicated device pin will be assigned to incorporate a "power save" mode within the device. The power save function will be programmable through the Serial Interface path and activated by a multifunction dedicated pin, Power Control Assert (PCA). This will allow the device to be placed in various "sleep" modes and timings defined at a system level.

A dedicated power mode will exist for TDMA which will be dependent upon the state of the PCA pin i.e. PCA high receive path off/transmit path on, PCA low receive path on/transmit path off.

Typical current figures for differing modes are shown below:

RX Channel TDMA mode, Bandpass Filter, Mixers and Post Filters, RX PLL, RSSI on, typical current 8mA
RX Channel AMPS mode, Bandpass Filter, FM Discriminator, RX PLL, RSSI on, typical current 7.2mA
TX Channel TDMA mode, I/Q Filters, TX PLL, typical current 4mA
TX Channel AMPS mode, FM Filter, TX PLL, typical current 3mA
Misc. circuits, Power-On-Reset, Serial Interface, Clock Comparator, Clock Generator, Bandgap, typical current 550uA.

### 1.5 Serial Control

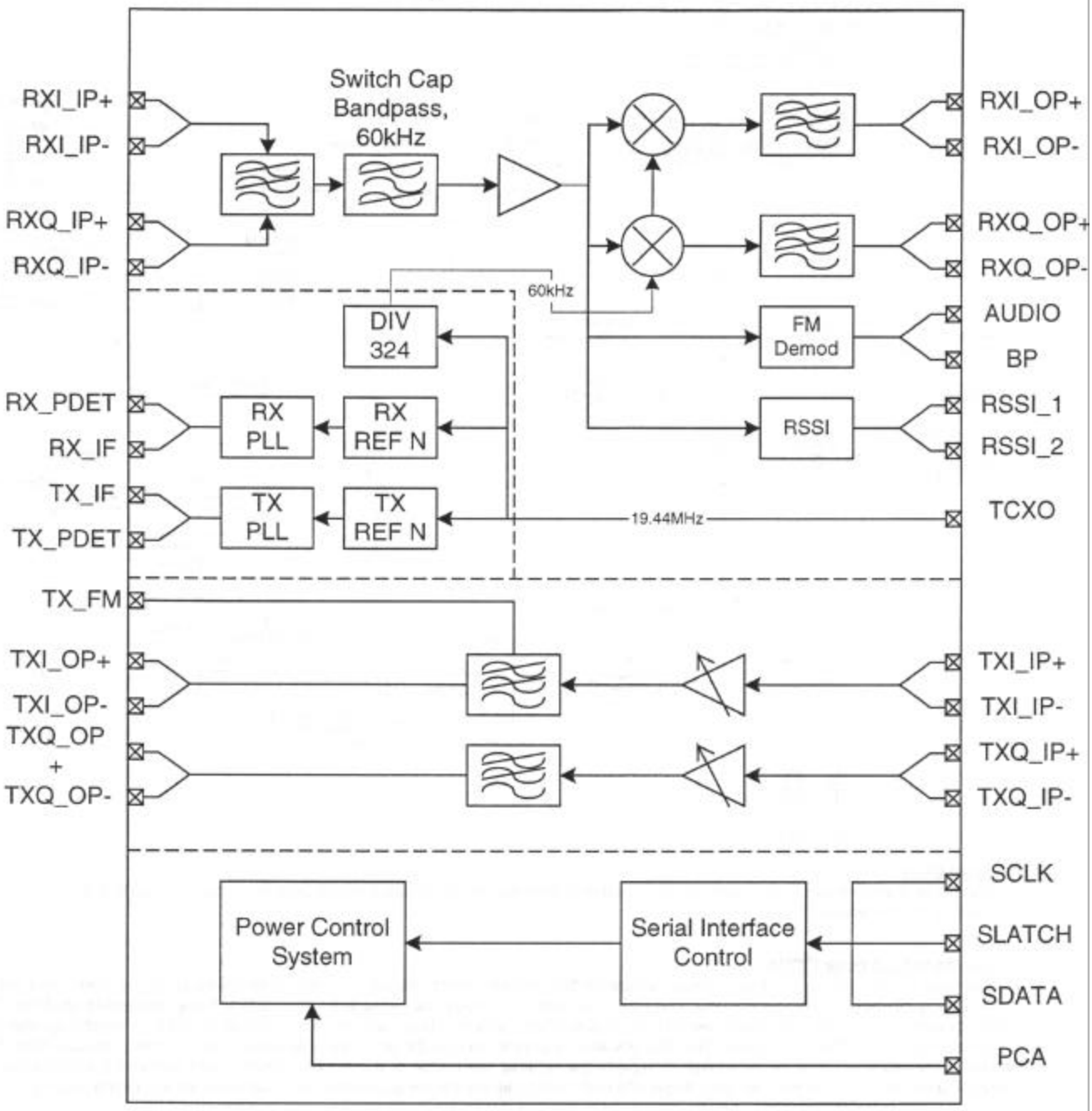
A three-wire control bus (clock, data and latch) will allow programming of the synthesizers and also allow selection of the various operating/power saving-modes. In addition a reset pin will facilitate testing of the device.

### 1.6 Absolute Specification Limits

| | | Limits | | |
|---|---|---|---|---|
| | | Max. | Units | Comments |
| 1. | Power Supply VDD to GND | - 0.3 to + 3.9 | V | |
| 2. | GND or SUB to GND | -0.3 to 0.3 | V | |
| 3. | Digital I/O Pin to DGND | - 0.3 to DVDD+ 0.3 | V | |
| 4. | Analog I/O Pin to AGND | - 0.3 to AVDD+ 0.3 | V | |
| 5. | Storage Temperature Range | - 55 to 150 | °C | |

# SCORPIO

## Mixed Signal Interface Circuit

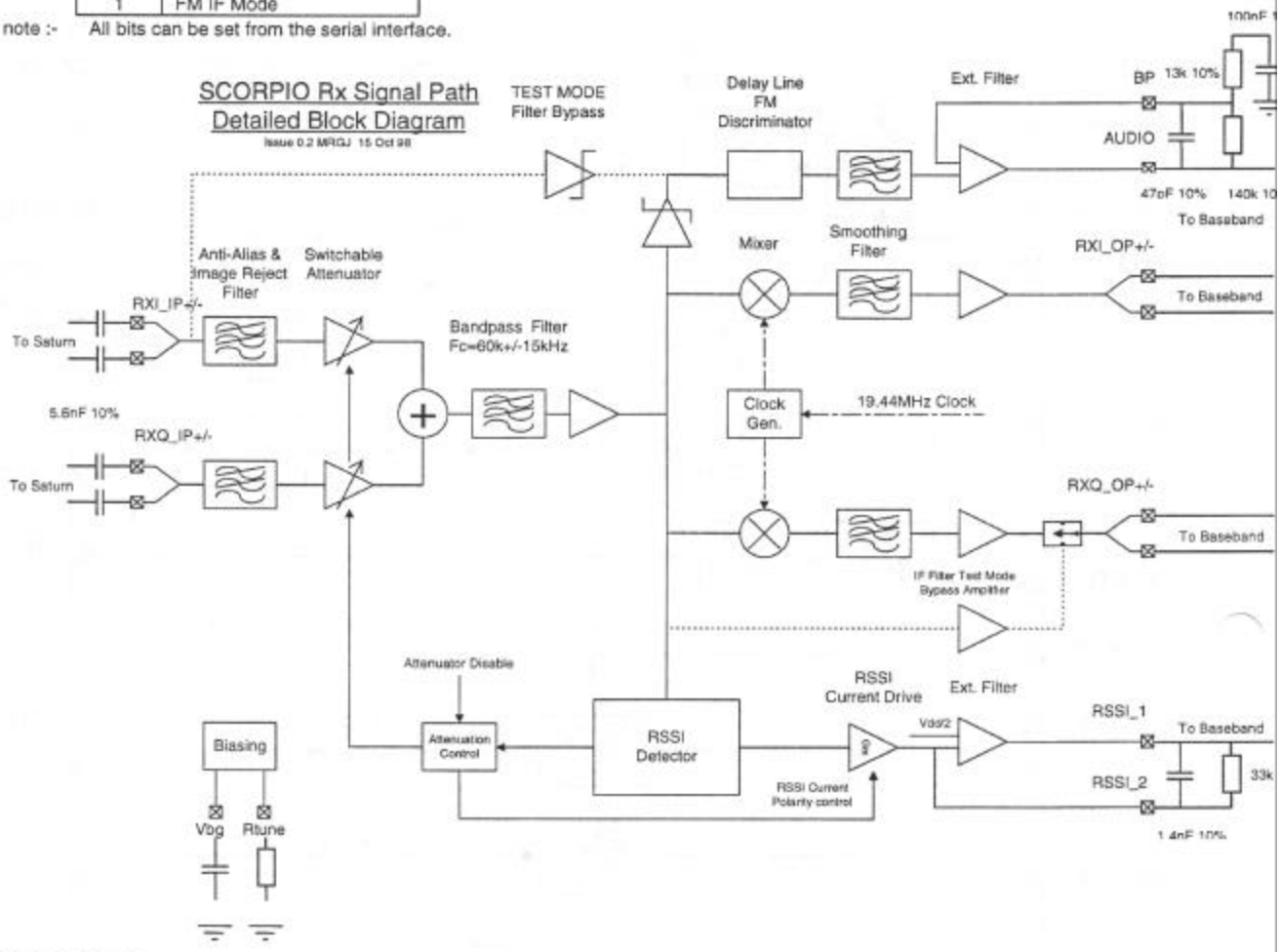


## 2. Receive Path

The receive circuit has several modes of operation, these are defined by control bits in the serial interface registers and the internal initialization circuits as follows:

| RX1 | Mode |
|---|---|
| 0 | Baseband I & Q Mode |
| 1 | FM IF Mode |

note :- All bits can be set from the serial interface.




### 2.1 Sleep Mode

In sleep mode all receive circuits are powered down in order to save current, this includes any clocked logic and bias circuits and results in a total current (for the receive circuits) of <25uA.

### 2.2 Baseband I & Q mode (TDMA)

In Baseband I & Q mode a switched capacitor bandpass filter implementation will be used with a center frequency at 60kHz and will be achieved by a 10th order switch capacitor filter with a 3dB bandwidth of +/-15kHz cascaded with appropriate anti-alias and anti-image filters. The bandpass filter output will then be mixed down to I and Q (0 to 15kHz) by a switching mixer which will then be filtered by a switch capacitor filter to minimize the 2*IF – 15kHz component. This filter will also be used to improve the group delay deviation caused by the bandpass filter. Post filtering of the signal will then be undertaken to provide the required attenuation of the sample spectrum and to partially equalize the RX channels group delay. One of the main advantages of a main switch capacitor/mixer approach is that it will eliminate any tuning circuitry.

### 2.3 IF FM mode (AMPS)

IF FM mode assumes that the FM demodulation is done using a discriminator acting on the 60kHz IF signal. The channel filtering is done by reusing the switched capacitor bandpass filter and this reuse for both Baseband I & Q and IF FM allows a more compact signal-path, hence reduced noise, die-size and thus cost. The IF FM channel will also be supported by an integrated FM analog discriminator and RSSI circuitry, providing direct Audio/Data and signal strength information at the device boundary.

### 2.4 FM Discriminator function

The FM Discriminator will be based on a internal limiter followed by a digital delay line whose input and output are EXOR'd together to implement the demodulation scheme. Tuning will be implemented internally to maximize the S/N by controlling the signal propagation through the digital delay line. The demodulated signal is then regenerated, lowpass filtered and finally bandpass filtered. This signal is then passed off chip as a single ended voltage to the baseband device. A feature of the FM Discriminator is that it will have a gain function defined by a small group of discrete passive components and a device pin BP (defines the internal bandpass filter characteristics.), thus allowing good definition of the AUDIO/Data output signal. A bypass mode will also exist such that the IF FM can be accessed at the output pin, AUDIO.

### 2.5 RSSI function

The RSSI circuit is a fast response input signal power indicator with a dynamic range of over 70dB. It has two modes of operation; one mode with the standard RX path gain and a second mode in which the RX signal path gain is reduced by switching in a 20dB attenuator. This 20dB attenuator is automatically switched in when the input signal is greater than about 4.5mV. The drop in RX gain stops the internal circuits saturating and extends the upper range of the RSSI. The output characteristic of the RSSI will reflect whether the 20dB attenuator has been switched in by toggling the sign bit (MSB) of the external ADC. The RSSI circuit will be calibrated using a two-point calibration scheme with standard gain within the RX path. This calibration information, together with the MSB of the ADC will allow reconstruction of a monotonic RSSI response within the digital domain.

The gain of the RSSI circuitry is directly proportional to an external resistor, which is connected between the pins RSSI_1 and RSSI_2.

### 2.6 Receive Path Electrical Specification

| 2.6.1 DC specification | | Limits | | | | |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Units | Comments/Conditions |
| 6. | Supply Voltage | 2.7 | 3.0 | 3.3 | V | |
| 7. | Operating temperature | -30 | 27 | +85 | °C | |
| | **Current Consumption** | | | | | |
| 8. | IDD, Sleep Mode | | | 0.025 | mA | |
| 9. | IDD, I & Q Mode | | 5.5 | 6.5 | mA | |
| 10. | IDD, IF FM Mode | | 4 | 5 | mA | |
| 11. | Turn on time Sleep mode to I & Q / IF FM mode, PCA asserted | | | 1.0 | ms | Bandgap and misc. circuits to be already powered up and stable |
| 12. | Turn off time I & Q / IF mode to Sleep mode, PCA asserted | | | 1.0 | ms | IDD to be <10% of value in RX channel operating modes |
| | **I/O DC Voltages** | | | | | |
| 13. | Common-mode i/p DC Voltages RXI_IP± & RXQ_IP± | | Vdd/2 | | V | |
| 14. | Common-mode o/p DC Voltages RXI_OP± & RXQ_OP± | Vdd-1.6V | Vdd-1.4V | Vdd-1.2V | V | |

| 2.6.2 Cascaded Bandpass Filter and Anti Alias Filter Specification<br><br>This specification applies to both IF FM (AMPS) and Baseband I/Q (TDMA) Modes<br><br>**MEASURED AT RXQ_OP± IN 'IF FILTER TEST MODE'** | | Limits | | | | |
|---|---|---|---|---|---|---|
| | | **Min.** | **Typ.** | **Max.** | | **Comments/Conditions** |
| | **Frequency Range** | | | | | |
| 15. | Maximum specified input frequency | | | 10 | MHz | |
| | **Voltage gain**[1] | | | | | ZloadExt=40kΩ min, parallel 5pFmax |
| 16. | Output amplitude balance | -0.25 | | 0.25 | dB | RXQ_OP+ to RXQ_OP- |
| 17. | Typical Input Signal Level | | 0.53 | | mVrms diff | Typical signal level gives approx. 334mVrms at output |
| | **Power Supply Rejection Ratio** | | | | | Defined as (Vgain_test(dB) - 'Gain' from Vdd to differential output (dB)) |
| 18. | Out of band (Fc+60kHz) | | 40 | | dB | Supply ripple = 10mVrms |
| 19. | In-band (Fc+/- <12.5kHz) | | 30 | | dB | Supply ripple = 10mVrms |
| | **Noise** | | | | | |
| 20. | Input referred maximum integrated noise. (Integrated 10Hz to 100kHz) | 17 | | | uVrms. | Source impedance 4kΩ differential. Gain is measured with input signal at Fc=62kHz. |
| | **Inband Compression** | | | | | Items 17 to 20 all i/o voltages are defined as being measured differentially across i/o |
| 21. | Output 1dB Compression | 3.0 | | | Vpk-pk. differential | Input In-band tone at 62kHz. External load is differential: 40kΩ min, parallel 5pF max,<br>each end to ground is 60kΩ min parallel 10pF max |
| | **Out of band Compression**<br>Out of band signal at input causing 1dB of in-band compression. | | | | | Input in-band tone @62kHz<br>V1dB = max. blocker level |
| 22. | Fc +/-60kHz Blocker<br>All Conditions | 125 | | | mVrms. | Input Signal Fc=62kHz in-band tone at 0.53mVrms<br>Blocking signal at Fc +/- 60kHz out of band tone. |
| 23. | Fc+/- 120kHz to 25 MHz Blocker<br>All Conditions | 13 | | | mVrms. | Input Signal Fc=62kHz in-band tone and Fc +/- >120kHz out of band tone. |
| | **Intermodulation**<br>Input referred intermodulation product | | | | | Input Signals<br>Fc=62kHz in-band tone : 0.53mvrms<br>Out of band unmodulated interferers:<br>Fc+/-60kHz : 20mVrms<br>(-wanted+19dB) + 31.5dB<br>Fc+/-120kHz : 20mVrms<br>(- wanted +19dB) + 31.5dB |
| 24. | All Conditions<br>Input referred intermodulation product<br><br>Input referred IP3 | 19<br><br>0.65 | <br><br>1.0 | | uVrms.<br><br>Vrms | <br><br>Extrapolate IIP3 assumes a 3rd order response |
| | **Filter Characteristics** | | | | | |
| | **Anti-Alias & Bandpass Filter Cascaded Response** | **AA & Bandpass Filter Only In Test Mode** | | | | **Measured in test mode where bandpass filter outputs are directed directly to RXQ_IP± outputs in "IF Filter Test Mode"** |

[1] Gain is measured from the differential Q inputs to the differential Q output when a signal of equal amplitude and in quadrature is applied to the I channel input.

| | | Limits | | | | |
|---|---|---|---|---|---|---|
| **2.6.2 Cascaded Bandpass Filter and Anti Alias Filter Specification**<br><br>This specification applies to both IF FM (AMPS) and Baseband I/Q (TDMA) Modes<br><br>**MEASURED AT RXQ_OP± IN 'IF FILTER TEST MODE'** | | **Min.** | **Typ.** | **Max.** | | **Comments/Conditions** |
| | Filter Types:<br>Anti Alias Filter<br>Bandpass Filter | | 3rd Order Butterworth, Fc=230kHz<br>10th Order, 0.5dB bandpass Switched Capacitor Chebeyshev Response | | | |
| 25. | Bandpass Filter Centre Frequency, Fo | | 60 | | KHz | |
| 26. | Bandpass 3dB Passband Edge | Fo ± 16 | Fo ± 17 | Fo ± 18 | kHz | Measured relative to gain With Input signal at Fc=60kHz |
| 27. | Stop band attenuation<br>Input Signal Frequency: | | | | | Measured relative to gain With Input signal at Fc=60kHz |
| | 0 to 3kHz | 67 | 69 | | dB | |
| | 3kHz to 10kHz | 61 | 63 | | dB | |
| | 10kHz to 22kHz | 49 | 51 | | dB | |
| | 22kHz | 50 | 51 | | dB | Extrapolate linearly between 22kHz |
| | 38kHz | 21 | 22 | | dB | & 38kHz. |
| | 82kHz | 20 | 21 | | dB | Extrapolate linearly between 82kHz |
| | 98kHz | 49 | 50 | | dB | & 98kHz. |
| | 98kHz to 110kHz | 48 | 50 | | dB | |
| | 110kHz to 117kHz | 61 | 63 | | dB | |
| | 117kHz to 123kHz | 68 | 70 | | dB | |
| | 123kHz to 1.36Hz | 71 | 73 | | dB | |
| | 1.36MHz to 1.52MHz | 36 | 48 | | dB | (due to aliased response within filter) |
| | 1.52MHz to 10MHz | 71 | 73 | | dB | |
| 28. | Image Rejection<br>( i.e. stop band attenuation for negative frequencies)<br>Input Signal Frequency: | | | | | |
| | 0Hz to 10kHz | 61 | | | dB | This performance assumes that |
| | -10kHz to –45kHz | 40 | | | dB | RXI_IP± / RXQ_IP± input signals |
| | -45kHz to –57kHz | 30 | 37 | | dB | have a worst case relative gain |
| | -57kHz to –63kHz | 31.5 | 39 | | dB | accuracy of 0.5dB |
| | -63kHz to –70kHz | 30 | 37 | | dB | and a worst case |
| | -70kHz to –105kHz | 40 | | | dB | Quadrature phase accuracy of 2deg |
| | -70kHz to –1.36MHz | 61 | | | dB | |
| | -1.36MHz to –1.52MHz | 36 | 48 | | dB | (due to aliased response within filter) |
| | -1.52MHz to –10MHz | 61 | | | dB | |
| 29. | Attenuation of Aliased responses | 36 | 48 | | dB | Alias in 30kHz BW around Fclk+/- 60kHz<br>Fclk=1.44MHz |
| 30. | Group delay Deviation | | 16 | 18[2] | µs pk-pk. | Frequency range Fo±12.5kHz<br>ie 47.5kHz to 72.5kHz<br>Measured at RXI_OP± & RXQ_OP± |
| 31. | In-band Gain Ripple (Max. sig-min. sig) | | 1.0 | 1.5 | dB pk-pk | Frequency range Fo±12.5kHz i.e. 47.5kHz to 72.5kHz,<br>Measured at RXI_OP± & RXQ_OP± |
| | **Input Impedance** | | | | | |
| 32. | Differential IP impedance<br>RXI_IP± and RXQ_IP± | | 10.0 | | kΩ | Balanced @ 60kHz |
| 33. | SE ip impedance to ground<br>RXI_IP± and RXQ_IP± | | 5 | | kΩ | Low impedance is desired to minimize the DC transient at power-up. |

[2] In TDMA mode the I & Q smoothing filters improve the group delay deviation by approximately 2us over that of the stand-alone bandpass filter.

| 2.6.2 Cascaded Bandpass Filter and Anti Alias Filter Specification<br><br>This specification applies to both IF FM (AMPS) and Baseband I/Q (TDMA) Modes<br><br>**MEASURED AT RXQ_OP± IN 'IF FILTER TEST MODE'** | | Limits | | | | |
|---|---|---|---|---|---|---|
| | | **Min.** | **Typ.** | **Max.** | | **Comments/Conditions** |
| | **Output Impedance** | | | | | |
| 34. | RXI_OP± | | 1.0<br>2.0 | | kΩ<br>kΩ | Single ended.<br>Differential |

| | 2.6.3 Baseband I & Q (TDMA) & IQ FM Mode AC Specification | Limits | | | | |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Units | Comments/Conditions |
| | **Frequency Range** | | | | | |
| 35. | Maximum specified input frequency | | | 10 | MHz | |
| | **Voltage gain**[3] | | | | | ZloadExt=40kΩ min, parallel 5pFmax |
| 36. | I and Q Voltage gain[4] | 54 | 56 | 58 | dB | Vgain |
| 37. | I and Q Gain imbalance | -0.5 | | 0.5 | dB | Defined as Gain I - Gain Q |
| 38. | Output amplitude balance | -0.25 | | 0.25 | dB | RXQ_OP+ to RXQ_OP- (Also I) |
| 39. | Typical Input Signal Level<br>At sensitivity + 3dB, TDMA<br>At sensitivity + 3dB, IQ FM<br>At large signal, TDMA<br>At large signal, IQ FM | | <br>0.53<br>0.12<br>0.53<br>0.53 | | <br>mVrms diff<br>mVrms diff<br>mVrms diff<br>mVrms diff | <br>AGC active<br>AGC fixed value<br>AGC active<br>AGC active |
| 40. | Average Phase balance (I and Q) | | 3 | 5 | Deg | Average taken from 0Hz to 12.5kHz. Measured at RXI_OP± & RXQ_OP± 0.5 dB ampl and 3 degree phase produce 28dBc residual sideband |
| | **Power Supply Rejection Ratio** | | | | | Defined as ( Vgain(dB) (taking into account mixing action) - 'Gain' from Vdd to differential output (dB)) |
| 41. | Out of band<br>0 to 30kHz<br>90kHz to 1MHz | | 40 | | dB | Supply ripple = 10mVrms |
| 42. | In-band (Fc+/- <12.5kHz) | | 30 | | dB | Supply ripple = 10mVrms |
| | **Noise** | | | | | |
| 43. | I & Q channel input referred maximum integrated noise. (10Hz to 5MHz) | 17 | | | uVrms. | Source impedance 4kΩ differential. Gain is measured with input signal at Fc=61kHz. Output signal at 1kHz. |
| | **Inband Compression** | | | | | Items 39-41 all i/o voltages are defined as being measured differentially across i/o |
| 44. | Output 1dB Compression | 3.0 | | | Vpk-pk. differential | Input In-band tone at 61kHz giving an output signal at 1kHz. External load is differential: 40kΩ min, parallel 5pF max, each end to ground is 60kΩ min parallel 10pF max |
| 45. | **Out of band Compression**<br>Out of band signal at input causing 1dB of in-band compression. | As Bandpass Filter & AA Filter Specification | | | | |
| 46. | **Intermodulation**<br>Input referred intermodulation product | As Bandpass Filter & AA Filter Specification | | | | |
| | **Filter Characteristics** | | | | | |
| | **Combined bandpass SC filter & IQ smoothing and image filters** | **Combined Response of AA, SC Bandpass Filter, Mixer and I/Q smoothing filters** | | | | **Characteristic measured from RXI_IP± / RXQ_IP± to RXI_OP± and RXQ_OP±** |
| 47. | I/Q bandwidth matching | | 0.5 | 2 | % | The same filter determines both 3dB BWs. I and Q differences are just due to the smoothing filters |
| 48. | Group delay Deviation | | 14<br>(10.5) | 16<br>(12)[5] | µs pk-pk. | Frequency range 0Hz to 12.5kHz Measured at RXI_OP± & RXQ_OP± |

[3] Gain is measured from Q input to I or Q output when a signal of equal amplitude and in quadrature is applied to the I channel input

[4] In IQ FM mode I and Q voltage gain can be set to 56dB (default), 68dB, 71dB and 74 dB by the control register CONT<1:0>

[5] A second bandpass filter mode has been included which extends the 3dB BW of the filter by approximately 20% . This improves the group delay deviation to 12us at the expense of the attenuation characteristic (due to extended 3dB BW) and inband gain ripple. The bandpass filter

| 2.6.3 Baseband I & Q (TDMA) & IQ FM Mode AC Specification | | Limits | | | | |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Units | Comments/Conditions |
| 49. | In-band Gain Ripple (Max. sig-min. sig) | | 1.5 | 2.0 | dB pk-pk | Frequency range 0Hz to 12.5kHz, Measured at RXI_OP± & RXQ_OP± |
| 50. | Input Referred Attenuation Characteristic | As Bandpass Filter & AA Filter Specification | | | | |
| 51. | Attenuation of all unwanted mixing products | 50 | | | dB | |
| 52. | LO breakthrough at RXI_OP± & RXQ_OP± Outputs | 22 | 10 | | mVrms | Sum of LO breakthrough @ 60kHz and its harmonics. |
| 53. | Attenuation of switched capacitor output images around 240kHz clock (Fclk) | 40 | | | dB | Relative to in band signal at 60kHz (Fc) at Fclk± Fc, 2Fclk± Fc nFclk+/-Fc |
| | **Input Impedance** | | | | | |
| 54. | Differential IP impedance RXI_IP± and RXQ_IP± | | 10.0 | | kΩ | Balanced @ 60kHz |
| 55. | SE ip impedance to ground RXI_IP± and RXQ_IP± | | 5 | | kΩ | Low impedance is desired to minimize the DC transient at power-up. |
| | **Output Impedance** | | | | | |
| 56. | RXI_OP± and RXQ_OP± | | 1.0<br>2.0 | | kΩ<br>kΩ | Single ended.<br>Differential |

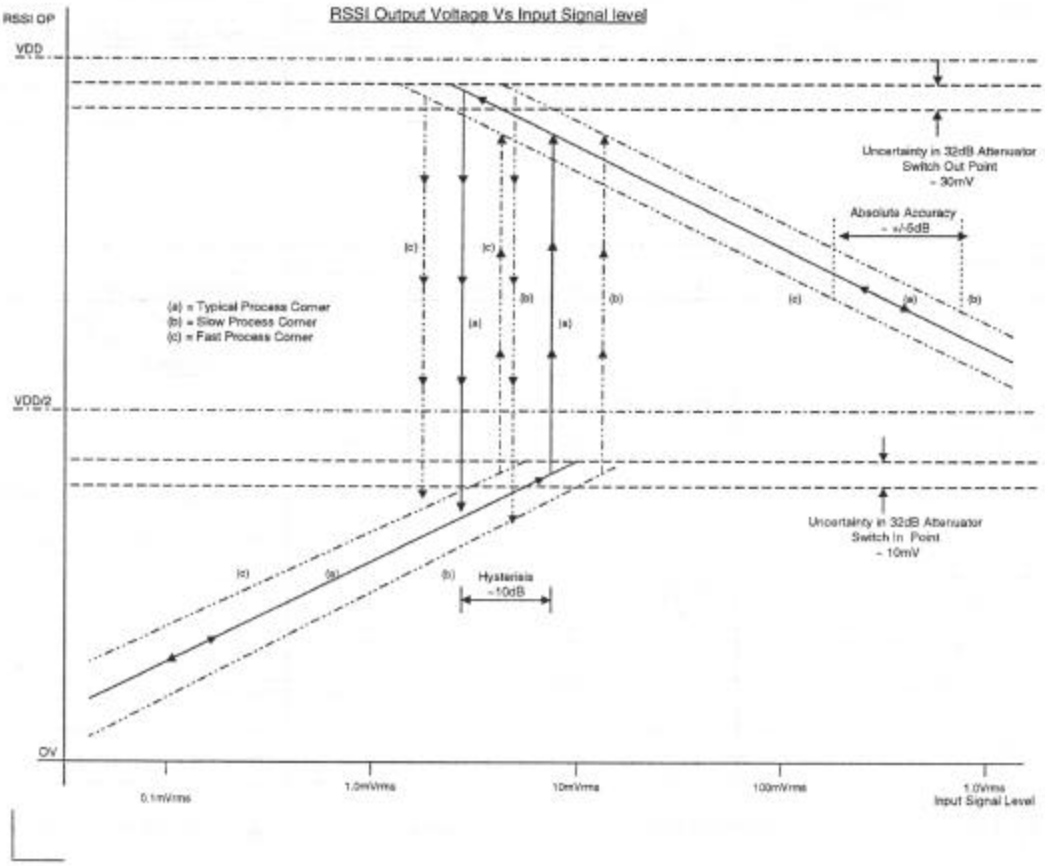
| 2.6.4 IF FM (AMPS) Mode AC Specification | | Limits | | | | |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Units | Comments/Conditions |
| | **Frequency Range** | | | | | |
| 57. | Maximum specified input frequency | | | 10 | MHz | |
| | **Voltage Gain** | | | | | |
| 58. | Input Signal Level at which signal limits prior to detector | 30 | | | uVrms | SINAD 12dB |
| 59. | Typical Input Signal Level FM Sensitivity + 3dB | 120 | | | uVrms | AGC fixed value (open loop) |
| 60. | **Power Supply Rejection Ratio** | As Bandpass Filter & AA Filter Specification | | | | Measured in IF Filter Test Mode |
| 61. | **Noise**<br>Input referred maximum integrated noise. (10Hz to 100kHz) | As Bandpass Filter & AA Filter Specification | | | | Measured in IF Filter Test Mode |
| 62. | **Out of band Compression**<br>Out of band signal at input causing 1dB of in-band compression. | As Bandpass Filter & AA Filter Specification | | | | Measured in IF Filter Test Mode |
| 63. | **Intermodulation**<br>Input referred intermodulation product | As Bandpass Filter & AA Filter Specification | | | | Measured in IF Filter Test Mode |
| | **Filter Characteristics** | | | | | |
| | **Combined Filter Characteristic up to delay line discriminator** | **Combined Response of AA, SC Bandpass Filter** | | | | |
| 64. | Input Referred Attenuation Characteristic | As Bandpass Filter & AA Filter Specification | | | | Measured in IF Filter Test Mode |
| 65. | Group delay Deviation | As Bandpass Filter & AA Filter Specification | | | | Measured in IF Filter Test Mode |
| 66. | In-band Gain Ripple (Max. sig-min. sig) | As Bandpass Filter & AA Filter Specification | | | | Measured in IF Filter Test Mode |
| | **Input Impedance** | | | | | |
| 67. | Differential IP impedance RXI_IP± and RXQ_IP± | | 10.0 | | kΩ | Balanced @ 60kHz |

mode is programmable via the serial interface. For example, low group delay ripple mode could be used in TDMA mode where the attenuation characteristic at 30kHz is not critical, and the higher group delay mode used for AMPs.

| 2.6.4 IF FM (AMPS) Mode AC Specification | | Limits | | | | |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Units | Comments/Conditions |
| 68. | SE ip impedance to ground RXI_IP± and RXQ_IP± | | 5 | | kΩ | Low impedance is desired to minimize the DC transient at power-up. |

| 2.6.5 RSSI AC Specification | | Limits | | | | |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | Comments/Conditions |
| 69. | RSSI Dynamic range | 70 | 73 | | dB | 70dB of dynamic range. Scorpio RSSI noise floor to maximum input signal level. |
| 70. | IDD | | 1.0 | 1.5 | mA | |
| 71. | Conformance to log characteristics | -3 | | +3 | dB | |
| 72. | Settling time | | 150 | | us | |
| 73. | Input Signal Levels | 0.024 | | 110 | mVrms | At input to Scorpio Internal 32dB attenuator enabled. |
| 74. | | 0.024 | | 20 | mVrms | At input to Scorpio Internal 32dB attenuator disabled. |
| 75. | Input referred noise | | 0.024 | | mVrms | |
| 76. | RSSI output signal level[6] | Vdd/2 − 1.2 | | Vdd/2 + 1.2 | V | Single ended. |
| 77. | Point at which 32dB attenuator is switched in | | 4.5 | | mVrms | Referred to input of Scorpio |
| 78. | Point at which 32dB attenuator is switched out | | 2.25 | | mVrms | Referrerd to input of Scorpio |
| 79. | RSSI output impedance | | 1.0 | | kΩ | Single ended. |
| 80. | Attenuator gain | -31.5 | -32 | -32.5 | dB | |

[6] Any RSSI output signal greater than Vdd/2 signified that a 20dB attenuator has been switched into the Rx signal path just prior to the filter. The sense of the RSSI output signal is also inverted .
A monotonic RSSI can easily be reconstructed by using 2's complement arithmetic once the signal has been digitized and taking into account that the 20dB attenuator is switched in by monitoring the sign bit. The MSB signifies the sign bit.




| 2.6.6 FM Discriminator AC Specification | | Limits | | | | |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | Comments/Conditions |
| 81. | Clock frequency | | 2.77714 | | MHz | Divided TXCO of 19.44MHz by 7 |
| 82. | IDD | | 0.7 | 1.0 | mA | |
| 83. | Number of delay stages | | 58 | | | Digital delay line elements |
| 84. | Delay | | 1.2531 | | | Delay as a ratio to IF period, 1/60kHz |
| 85. | Gain | | 125.31 | | uV/Hz | |
| 86. | Input Frequency | 45 | | 75 | kHz | |
| 87. | Input Signal to Noise Ratio | 2.3 | 4 | | dB | SINAD 12dB |
| 88. | Audio signal noise floor | | | -46 | dB | Deviation at input |
| 89. | Audi output signal level | | 36 to 500 | | mVrms | Defined by external feedback components, |
| 90. | Audio output impedance | | 1.0 | | kΩ | Single ended. |

note:- SINAD is defined as the ratio of wanted signal to all unwanted output, measured simultaneously with filters.

## 3. Transmit Path

The transmit circuit has several modes of operation, these are defined by control bits in the serial interface registers:

| TX1 | TX2 | Mode |
|---|---|---|
| 0 | 0 | TDMA Mode ( diff ) |
| 1 | 0 | FM I & Q Mode (diff ) |
| X | 1 | FM Mode ( single ended ) |

| TXG0 | TXG1 | TXG2 | Gain |
|---|---|---|---|
| 1 | X | X | 0 dB |

| TxG0 | TxG1 | TxG2 | Gain |
|---|---|---|---|
| 0 | 0 | 0 | 3 dB |
| 0 | 1 | 0 | 6dB |
| 0 | 0 | 1 | 9 dB |
| 0 | 1 | 1 | 12 dB |

Process and temperature variation can cause a filter cut-off variation of up to +/- 46%. The following calibration circuit reduces this to +/- 5%. The calibration circuit for the transmit filter is a master - slave arrangement, using a replica of a section of the filter to form a ring oscillator. Three stages of the filter plus one gain stage make up the oscillator.

A four bit code is used to switch capacitors into / out of the filter / oscillator in order to tune the cut-off of the filter and the frequency of the oscillator. Initially, this code is set to 1000 and then a successive approximation routine begins. A known, fixed clock frequency is fed into an overflow counter, which is pre-loaded with a programmable number. The counter should reach the 'all ones' state at the same time as a set number of periods of the oscillator output. If the counter overflows, the bit being tested of the four bit output code remains set. The sequence is then repeated for the next bit. The whole routine takes about 0.6 ms to complete.

The cut-off of the filter can be tuned to a different value by changing the pre-load number into the counter, giving extra control.

### 3.1 Sleep Mode

In sleep mode all transmit circuits are powered down in order to save current, this includes any clocked logic and bias circuits and results in a total current (for the transmit circuits) of <25uA.

### 3.2 Baseband I & Q mode (TDMA)

In baseband I & Q mode a variable gain buffer is used which has a 0 to 12dB range in 3dB increments. A lowpass filter will also be provided to reduced data noise from the baseband DAC's. The transmit channel will be tuned internally for optimum corner frequency in TDMA mode.

### 3.3 IF FM mode (AMPS)

In IF FM mode just one signal path is used (the I-channel) and all other channels are turned off. IF FM mode has two input paths, one using the I channel in true differential form and a pseudo single-ended input which uses the TXI_IP+ ac coupled with a 27pF capacitor with TXI_-IP N/C. The modes are set via the Serial Interface. The IF FM filter is the same as that used in baseband I & Q mode except that the filter will have a separate single-ended output. TX_FM.

### 3.4 Transmit Path Electrical Specification

| 3.4.1 DC specification | | Limits | | | | |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Units | Comments/Conditions |
| 91. | Supply Voltage | 2.7 | 3.0 | 3.3 | V | Vdd |
| 92. | Operating temperature | -30 | 27 | 85 | °C | Tamb |
| | **Current Consumption** | | | | | |
| 93. | IDD, Sleep Mode | | | 0.025 | mA | Sleep Mode |
| 94. | IDD, I & Q Mode | | 2.5 | 3 | mA | I & Q signal path 'on' |
| 95. | IDD, FM Mode | | 1.5 | 2 | mA | FM signal path 'on' |
| 96. | Turn on Time, PCA asserted | | | 500 | us | Bandgap and misc. circuits to be already powered up and stable |
| 97. | Turn off time, TX channel operating to Sleep mode, PCA asserted | | | 500 | us | IDD to be <10% of value TX channel operating value, see 94 and 95. |
| 98. | Common-mode DC Voltages TX_IP+, TXI_IP-, TXQ_IP+, TXQ_IP- | | 0.8 | | V | |
| 99. | Common-mode DC Voltages TX_0P+, TXI_0P-, TXQ_0P+, TXQ_0P- | | 1.2 | | V | |

| 3.4.2 I & Q Mode (TDMA) AC Specification | | Limits | | | | |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | Comments/Conditions |
| | **Frequency Range** | | | | | |
| 100. | Maximum specified input frequency | | | 2 | MHz | Follows Butterworth chcs. upto 2MHz |
| | **Voltage gain** | | | | | ZloadExt = 50 kΩ, parallel 5pF |
| 101. | Variable voltage gain | 0 | | 12 | dB | 3dB increments controlled by SI |
| 102. | Output amplitude balance | -0.25 | | 0.25 | dB | TXQ_OP+ to TXQ_OP- (Also I) |
| 103. | Output phase balance | | | 0.5 | deg | TXQ_OP+ to TXQ_OP- (Also I) |
| 104. | Input Signal Level | | 1000 | | mVpk-pk diff. | Require 2Vpk-pk diff, therefore for 1000mVpk-pk diff typical 6dB of gain required (for 500mVpk-pk diff, 12dB of gain required). |
| 105. | DC Offset, output | | +/-20 | | mV | Inputs shorted to i/p common mode voltage |
| | **Power Supply Rejection** | | | | | |
| 106. | Out of band (120kHz) | 12 | | | dB | Supply ripple = 10mVrms, Max Gain |
| 107. | Inband (12.5kHz) | 12 | | | dB | Supply ripple = 10mVrms, Max Gain |
| | **Noise** | | | | | |
| 108. | Total noise power from 10Hz to 15kHz | | | -50 | dBc | Measured in dB relative to 1 kHz full scale tone |
| 109. | Noise power in any 300 Hz band in frequency range of > 20 kHz but < 45 kHz | | | -50 | dBc | Measured in dB relative to 1 kHz full scale tone |
| 110. | Noise power in any 300 Hz band in frequency range of > 45 kHz but < 60 kHz | | | -75 | dBc | Measured in dB relative to 1 kHz full scale tone |
| 111. | Noise power in any 300 Hz band in frequency range of > 60 kHz | | | -85 | dBc | Measured in dB relative to 1 kHz full scale tone |
| 112. | Noise power at 45 MHz | | | -143 | dBV/Hz^2 | Equivalently -155 dBm/Hz into 15 kOhm or -160 dBm/Hz into 50 kOhm. This level of noise produces 2 dB degradation in Tx noise floor in Rx band. |

| | | | | | | |
|---|---|---|---|---|---|---|
| 113. | 1dB Compression | 2.5 | | | Vpk-pk | |
| 114. | Total Harmonic Distortion | | | -40 dBc | dBc | Measured with 1 kHz full scale tone |
| | | | | | | |
| **3.4.2 I & Q Mode (TDMA) AC Specification** | | **Limits** | | | | |
| | **Filter Characteristics** | | | | | |
| 115. | Filter Type | 3rd Order Butterworth | | | | |
| 116. | 3dB Passband Edge | 22 | 25 | 28 | kHz | Measured relative to gain at Fc. |
| 117. | Stop band attenuation | 30 | | | dB | At >=100kHz |
| 118. | Stop band attenuation | 40 | | | dB | At >=2MHz including 45 MHz<br>Assumptions: DAC noise in 1 Hz at 45 MHz was measured to be 110 dB below full signal power.<br>Signal -3 dBV,<br>Need noise floor of < -143 dBV<br>DAC noise attenuated to 12 dB below Scorpio noise |
| 119. | Group Delay Deviation | | | 10 | µs pk-pk. | 0Hz-12.5kHz |
| 120. | Inband Gain Ripple (Max. sig-min. sig) | | | 1.0 | dB pk-pk | 0Hz-12.5kHz |
| 121. | **Input Impedance**<br>TXI_IP+/TXI_IP- & TXQ_IP+/TXQ_IP- | 100 | | | kΩ | Balanced @2kHz,<br>Assumption: BB output impedance may be upto 1.5kOhm depending on what signal level is required.<br>15kOhm load makes possible a 1 pole filter at BB, if needed. |
| 122. | **Output Impedance**<br>TX_0P+/TXI_0P- & TXQ_0P+/TXQ_0P- | | 1.0 | | kΩ | Single ended.<br>External load is 20kΩ and 20pF to ground. |

| **3.4.3 IF FM (AMPS)Mode AC Specification** | | **Limits** | | | | |
|---|---|---|---|---|---|---|
| | | **Min.** | **Typ.** | **Max.** | | **Comments/Conditions** |
| | **Frequency Range** | | | | | |
| 123. | Maximum specified input frequency | | | 2 | MHz | Follows Butterworth chcs. upto 2MHz |
| | **Voltage gain** | | | | | ZloadExt = 50 kΩ, parallel 5pF |
| 124. | Voltage gain | 0 | | 12 | dB | 3dB increments controlled by SI |
| 125. | Input Signal Level<br>Differential Input, TXI_IP+/TXI_IP- to Single-ended output, TX_FM | 0 | 1000 diff | 1000 single-ended | mVpk-pk | Typical signal level input, gain of 0db, typical signal level output at TX_FM is 1000mVpk-pk single-ended |
| 126. | Input Signal Level<br>Single-Ended Input, TXI_IP+ to Single-Ended Output, TX_FM | 0 | 500 single-ended | 500 single-ended | mVpk-pk | Typical signal level input, gain of 0db, typical signal level output at TX_FM is 500mVpk-pk single-ended (Signal ac coupled to TXI_IP+) |
| | **Power Supply Rejection** | | | | | |
| 127. | Out of band (120kHz) | 12 | | | dB | Supply ripple = 10mVrms, Max Gain |
| 128. | Inband (12.5kHz) | 12 | | | dB | Supply ripple = 10mVrms, Max Gain |
| | **Noise+spurious** | | | | | Relative to 1kHz single tone input |
| 129. | DC- 20 kHz | | | -50 | dBc | Total integrated noise relative to signal power |
| 130. | > 20 kHz | | | -80 | dBc | Total noise power in 300 Hz band relative to signal power. |
| | **Compression** | 2.5 | | | Vpk-pk | |
| 131. | Output at 1dB Compression | | | 1.2 | Vpk-pk | |
| 132. | Total Harmonic Distortion | | | -40 | dBc | Measured with 1 KHz full scale tone |
| | **Filter Characteristics** | | | | | |
| 133. | Filter Type | 3rd Order Butterworth | | | | |
| 134. | 3dB Passband Edge | 22 | 25 | 28 | kHz | Measured relative to gain at Fc. |
| 135. | Stop band attenuation | 30 | | | dB | At >=100kHz |
| 136. | | 40 | | | dB | At >=2MHz |
| 137. | Group Delay Deviation | | | 10 | µs pk-pk. | 0Hz-12.5kHz |
| 138. | Inband Gain Ripple (Max. sig-min. sig) | | | 1.0 | dB pk-pk | 0Hz-12.5kHz |
| | | | | | | |

| | | | | | | |
|---|---|---|---|---|---|---|
| 139. | **Input Impedance** TXI_IP+/TXI_IP- | 100 | | | kΩ | Balanced @2kHz,<br>Assumption: The same input is also used in BB I & Q mode |
| 140. | **Output Impedance** TX_FM | | 1.0 | | kΩ | Single ended.<br>External load is 20kΩ and 20pF to ground. |

## 4. IF Synthesis

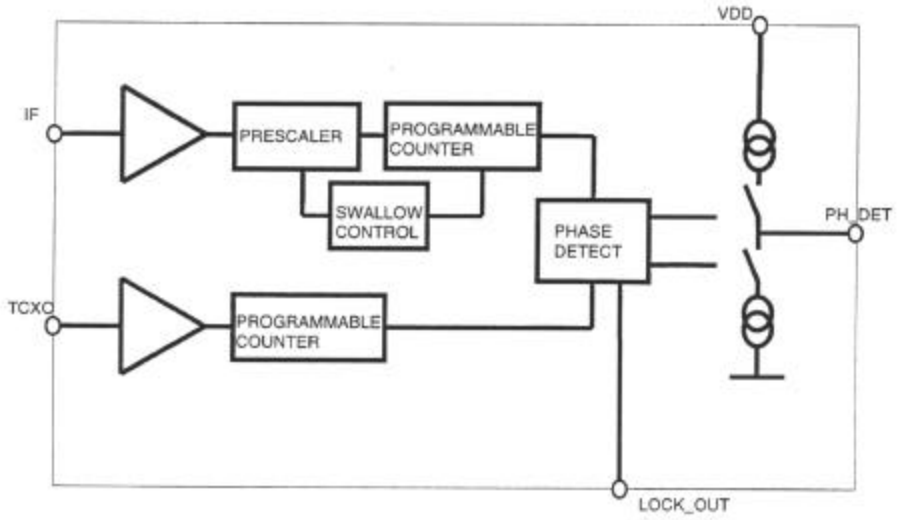



Figure 4 IF Synthesizer

The synthesizers will have several modes of operation, defined by control bits in the serial interface registers and the internal initialization circuits as described in the following tables:

| BIT | CONTROLS | ACTION if '0' | ACTION if '1' |
|---|---|---|---|
| ST<2:0> | LOCK Output(s) | See table (a) below | |
| ST<4:3> | Receive Charge Pump Current | See table (b) below | |
| ST<6:5> | Transmit Charge Pump Current | See table (b) below | |
| ST<7> | Receive Charge Pump Tristate | normal | tristate |
| ST<8> | Transmit Charge Pump Tristate | normal | tristate |
| ST<11:9> | Receive Prescaler Divide Ratio | See table (c) below | |
| ST<14:12> | Transmit Prescaler Divide Ratio | See table (c) below | |
| ST<15> | Receive Power Control | off | operational |
| ST<16> | Transmit Power Control | off | operational |
| ST<17> | Receive Phase Detector Polarity | normal(+) | reverse(-) |
| ST<18> | Transmit Phase Detector Polarity | normal(+) | reverse(-) |
| ST<19> | Receive Prescaler Bypass | normal | bypassed |
| ST<20> | Transmit Prescaler Bypass | normal | bypassed |
| ST<21> | Receive Lock Detect Invert | normal | inverted |
| ST<22> | Transmit Lock Detect Invert | normal | inverted |
| ST<23> | Reference Dividers Test Bit | normal | test |

note :- All bits can only be set from the serial interface

| ST<2> | ST<1> | ST<0> | LOCK |
|---|---|---|---|
| 0 | 0 | 0 | RLOCK |
| 0 | 0 | 1 | RVCO |
| 0 | 1 | 0 | RREF |
| 0 | 1 | 1 | CLK_TEST |
| 1 | 0 | 0 | TLOCK |
| 1 | 0 | 1 | TVCO |
| 1 | 1 | 0 | TREF |
| 1 | 1 | 1 | WOUT |

Table (a)

| ST<6> / ST<4> | ST<5> / ST<3> | Charge Pump Output Current |
|---|---|---|
| 0 | 0 | 496uA |
| 0 | 1 | 176uA |
| 1 | 0 | 96uA |
| 1 | 1 | 16uA |

| ST<14> / ST<11> | ST<13> / ST<10> | ST<12> / ST<9> | Prescaler Divide Ratio |
|---|---|---|---|
| 0 | X | X | 8/9 |
| 1 | 0 | 0 | 16/17 |
| 1 | 0 | 1 | 32/33 |
| 1 | 1 | 0 | 64/65 |
| 1 | 1 | 1 | 128/129 |

Table (c)

The transmit and receive synthesizers will be identical in all respects except for the address of the programming words. As can be see from the diagram (figure 4) the synthesizers will be comprised of:

**4.1 Synthesizer Prescaler**

With a maximum input frequency of 100MHz the prescaler will be able to be programmed in one of two different modes, firstly as a divide by 16/17 and secondly to divide by 8/9. The modulus control input for the prescaler will be generated by the "swallow counter" (see the next section).

**4.2 Main Divider (N Counter)**

The N Counter will consists of an 11 bit programmable counter (M counter) and a 7-bit swallow counter (the A counter), the overflow of the A counter will be used to control the modulus of the prescaler (see previous section). The dividends of the counters will then be loaded via the serial interface (see section 6). The output of the M counter will be compared with the reference frequency by the phase detector (see section 4.4).

**4.3 Reference Divider**

This will be a fully programmable 15 bit counter (the R counter) which will divide the TCXO input by a pre-programmed number between 3 and 32767, where this number will be programmed via the serial interface (see section 6). The output of the R counter will be compared with the output of the main divider by the Phase comparator (see following section).

**4.4 Phase Detector & Charge Pump**

The phase detector compares the two counter outputs and (depending on the relative phase of the two signals) either provides "UP" or "DOWN" signals to the charge pump and a "lock detect" signal to the output. The charge pump operates by providing current pulses of fixed amplitude and a period equal to the width of the up or down input. The charge pump output current will be accurate (+/-10%) to within 200mV of the supply rails.

**4.5 Synthesizer Electrical Specification**

| | | Limits | | | | |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Units | Comments/Conditions |
| 141. | Supply Voltage | 2.7 | 3.0 | 3.3 | V | Vdd |
| 142. | Operating temperature | -30 | 27 | 85 | °C | Tamb |
| | **Current Consumption** | | | | | |
| 143. | IDD, Sleep Mode | | | 0.025 | mA | Sleep Mode (both Synths off) |
| 144. | IDD, RX Synth (locked) | | 1.5 | 2 | mA | |
| 145. | IDD, TX Synth (locked) | | 1.5 | 2 | mA | |
| | **VCO Input** | | | | | |
| 146. | Input Resistance | | TBD | | | |
| 147. | Input Capacitance | | TBD | | | |
| 148. | Input Sensitivity | | 100 | | mV | Suggest -15dBm from 50 Ohm source, VCO design dependent |
| 149. | Input Frequency | 1MHz | | 100 | MHz | |
| | **Charge Pump Output Current** | | | | | |
| 150. | Default mode | | 496 | | uA | Rset=40kohm |
| 151. | Low current mode | | 96 | | uA | Rset=40kohm |
| 152. | Tristate mode | | | ±10 | uA | |
| 153. | Output impedance | 1 | | | MΩ | |
| 154. | Sink to source current matching | | +/- 5 | | % | Measure at VDD/2 |
| 155. | "Off" leakage current | -5 | +/- 1 | 5 | nA | |
| 156. | Compliance range | 0.2 | | vdd-0.2 | | with current within 10% of value at vdd/2 |

## 5. Power Control System

The device current consumption management will be handled by the Power Control System (PCS), which is programmed through the Serial Control Interface and a single dedicated pin, which is called Power Control Assert (PCA). This function will allow Scorpio to be controlled by an accurate system timer rather than through the less accurately timed Baseband microprocessor and Serial Interface control path alone.

The PCS will function as follows. The operating mode that the device is required to be placed in will be loaded through the Serial Interface into the PCS register and not acted upon until the Power Control Assert (PCA) pin is asserted. To change device power control modes the process is repeated.

The table below shows a summary of power-down modes programmable via the Serial Interface:

| PCS<0> | PCS<1> | PCS<2> | PCS Mode | Comments/Conditions |
|---|---|---|---|---|
| 0 | 0 | 0 | Deep Sleep | All circuits powered down except PCS |
| 0 | 0 | 1 | Sleep | TX and RX channels powered down, but support circuits active i.e. Bandgap |
| 0 | 1 | 0 | TX channel Active | TX channel powered up |
| 0 | 1 | 1 | RX Channel Active | RX channel powered up |
| 1 | 0 | 0 | Both TX and RX Channels Active | Power up both TX and RX channels |
| 1 | 0 | 1 | Alternate RX/TX | PCA "0" RX on/TX off, PCA "1" RX off/TX on |
| 1 | 1 | 0 | RSSI Latched Active | RSSI powered up, only when RX Channel on |
| 1 | 1 | 1 | RSSI Latched in Sleep | RSSI powered down |

note :- All bits can only be set from the serial interface, and the mode will be entered when the PCA pin is asserted active high

note :- Definition of RX Channels and TX Channels are mode dependent and are as follows (defined with typical currents):
RX Channel TDMA mode, Bandpass Filter, Mixers and Post Filters, RX PLL, RSSI on, typical current 8mA
RX Channel AMPS mode, Bandpass Filter, FM Discriminator, RX PLL, RSSI on, typical current 7.2mA
TX Channel TDMA mode, I/Q Filters, TX PLL, typical current 4mA
TX Channel AMPS mode, FM Filter, TX PLL, typical current 3mA
Misc. circuits, Power-On-Reset, Serial Interface, Clock Comparator, Clock Generator, Bandgap, typical current 550uA.

## 6. Serial Interface, Control Registers & Reference Circuits

### 6.1 Control Registers

Scorpio will be controlled via a 3-wire serial Interface (SCLK,SDATA & SLATCH), The Following table shows the address and mnemonic of the various control bits within the interface registers. The action of the control bits is further described in the relevant sections of this document.

| Time Order | first | | | | | | | | | | | | | | | | | | | | | | last |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Bit | 23 | 22 | 21 | 20 | 19 | 18 | 17 | 16 | 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| WORD1 | X | X | X | RXDIV<17:0> | | | | | | | | | | | | | | | | | | 0 | 0 | 0 |
| WORD2 | X | X | X | TXDIV<17:0> | | | | | | | | | | | | | | | | | | 0 | 0 | 1 |
| WORD3 | X | X | X | ST<23:21> | | | REFRX<14:0> | | | | | | | | | | | | | | | 0 | 1 | 0 |
| WORD4 | X | X | X | ST<20:18> | | | REFTX<14:0> | | | | | | | | | | | | | | | 0 | 1 | 1 |
| WORD5 | X | X | X | ST<17:0> | | | | | | | | | | | | | | | | | | 1 | 0 | 0 |
| WORD6 | X | X | X | X | OSC<1:0> | | X | | | BYP | TXG<2:0> | | | TXC | TX<2:0> | | | TC<3:0> | | | | 1 | 0 | 1 |
| WORD7 | TEST<2:0> | | | FMT<2:0> | | | PCS<2:0> | | | RSSI<2:0> | | | | RX<1:0> | CONT<3:0> | | | | X | | | 1 | 1 | 0 |
| WORD8 | CALCO<7:4> | | | | CALCO<3:0> | | | | | X | | | | | | RADDR<3:0> | | | TST | X | | | 1 | 1 | 1 |

RXDIV<17:0> = RX main divider divide ratio
TXDIV<17:0> = TX main divider divide ratio
REFRX<14:0> = RX reference divider divide ratio
REFTX<14:0> = TX reference divider divide ratio
ST<23:0> = Synthesizer control bits (see section 4)
OSC<1:0> = TX filter oscillator bits
RADDR<3:0> = Address to select which register of 24 bits is put out serially on WOUT (see table below)
TST = Enables WOUT to be read. WOUT is muxed onto the LOCK_DET pin, when TST is high
TXC,TX<2:0> = TX mode control bits
FMT<2:0> = FMIFSCF filter test bits
PCS<2:0> = Power Control System bits
RX<2:0> = RX mode control bits
TXG<2:0> = TX Gain bits
TC<3:0> = TX Frequency control bits
RSSI<2:0> = RSSI control bits
CONT<3:0> = RX Control bits

TEST<2:0> = RX signal observability test bits
CALCO<7:0> = Preload value for TX calibrate circuit
X = Unused / internal use only

| Read Address | | | | WORD |
|---|---|---|---|---|
| 3 | 2 | 1 | 0 | |
| 0 | 0 | 0 | 0 | 1 |
| 0 | 0 | 0 | 1 | 2 |
| 0 | 0 | 1 | 0 | 3 |
| 0 | 0 | 1 | 1 | 4 |
| 0 | 1 | 0 | 0 | 5 |
| 0 | 1 | 0 | 1 | 6 |
| 0 | 1 | 1 | 0 | 7 |
| 0 | 1 | 1 | 1 | 8 |

### 6.2 Reference Circuits

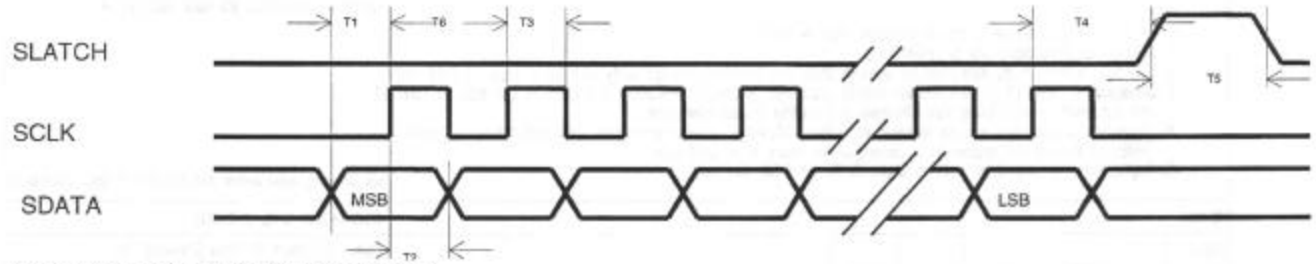
Scorpio will contain a single bandgap reference circuit and precision bias current generator. The bandgap will have a nominal output voltage of 1.22V. For optimal circuit performance the associated pin 'VBG' should be de-coupled to ground using a 100nF capacitor. Both the reference voltage and current will be internally 'slaved' to all circuits requiring their support.

Scorpio requires a precise reference frequency for the synthesizers and the clock of the FM mode switched capacitor filter. This will be provided by an external source which supplies a sinewave or clipped sinewave at 19.44MHz a.c. coupled into the TCXO input by a 480nF capacitor.

### 6.3 Serial Interface

This operates in accordance with the following table and timing diagram.

| Parameter | | MIN | TYP | MAX | Units | Comments/Conditions |
|---|---|---|---|---|---|---|
| T1 | SCLK-SDATA SETUP time | 20 | | | ns | |
| T2 | SCLK-SDATA hold time | 20 | | | ns | |
| T3 | SCLK pulse width | 50 | | | ns | Min. Clock Frequency of 20MHz |
| T4 | SLATCH-SCLK SETUP time | 20 | | | ns | |
| T5 | SLATCH pulse width | 50 | | | ns | |
| T6 | SCLK period | 100 | | | ns | |




### 6.4 Reference Circuits Electrical Specification

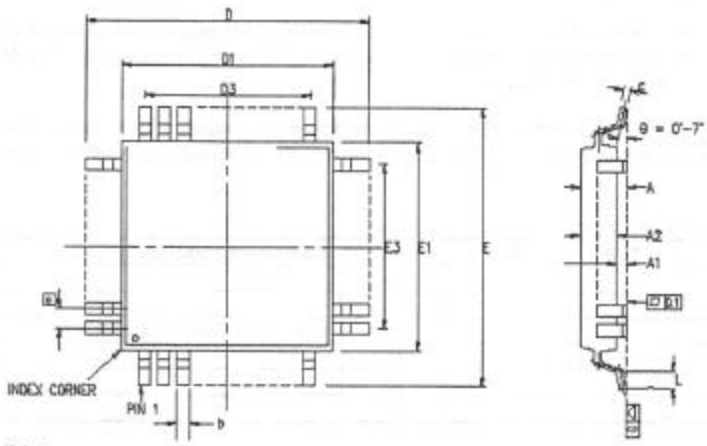
| | | Limits | | | | |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | Units | Comments |
| 157. | Supply Voltage | 2.7 | 3.0 | 3.3 | V | Vdd |
| 158. | Operating temperature | -30 | 27 | 85 | °C | Tamb |
| | **Current Consumption** | | | | | |
| 159. | IDD, Sleep Mode | | | 0.025 | mA | Sleep Mode |
| 160. | IDD, Active | 0.44 | 0.55 | 0.66 | mA | All circuits active |
| | **TCXO** | | | | | |
| 161. | Input Resistance | 10 | | | kΩ | |
| 162. | Input Capacitance | 10 | | | pF | |
| 163. | Input Sensitivity | 0.5 | | 2 | V pk-pk | Sinewave or clipped sinewave |
| 164. | Input Frequency | | 19.44 | | MHz | +/-100ppm |
| | **Voltage & Current References** | | | | | |
| 165. | Bandgap Voltage "VBG" | 1.194 | 1.22 | 1.258 | V | Decouple with a 100nF to gnd |
| 166. | Maximum Change In VBG (-40° to 80°) | | | 20 | mV | |
| 167. | Temperature Coefficient (@20°) | -30 | 13 | 90 | ppm/°C | |
| 168. | External Bias Resistor (RTUNE) | | 100 | | kΩ | Ref to gnd, +/-1%, temp +/-100ppm |
| | **Digital I/O** | | | | | Meets JEDEC Standard |
| 169. | Input high voltage, VIH | 0.7*VDD | | | V | |
| 170. | Input low voltage, VIL | | | 0.3*VDD | V | |
| 171. | Input current, IIH | | | 10 | nA | |

| | | | | | | |
|---|---|---|---|---|---|---|
| 172. | Input capacitance, CIN, | | | 10 | pF | Includes pacaked capacitance |
| 173. | Output high voltage, VOH | 0.8*VDD | | | V | |
| 174. | Output low voltage, VOL | | | 0.4 | V | |
| 175. | Output Drive (Sink/Source) | | 2/2 | 5/4 | mA | |
| 176. | Three-state leakage current, | | | 10 | µA | |

## 7. Package

### 7.1 Package Type

TQFP48 (7x7x1.0 0.5mm pin pitch)




| Symbol | Control Dimensions in millimetres | | | Altern. Dimensions in inches | | |
|---|---|---|---|---|---|---|
| | MIN. | Nominal | MAX. | MIN. | Nominal | MAX. |
| A | 1.00 | | 1.20 | 0.039 | | 0.047 |
| A1 | 0.05 | | 0.15 | 0.002 | | 0.006 |
| A2 | 0.95 | | 1.05 | 0.037 | | 0.041 |
| D | 8.80 | | 9.20 | 0.346 | | 0.362 |
| D1 | 6.80 | | 7.20 | 0.268 | | 0.283 |
| D3 | | 5.50 REF. | | | 0.217 REF. | |
| E | 8.80 | | 9.20 | 0.346 | | 0.362 |
| E1 | 6.80 | | 7.20 | 0.268 | | 0.283 |
| E3 | | 5.50 REF. | | | 0.217 REF. | |
| L | 0.45 | | 0.75 | 0.018 | | 0.030 |
| e | | 0.50 BSC. | | | 0.020 BSC. | |
| b | 0.17 | | 0.27 | 0.007 | | 0.011 |
| c | 0.09 | | 0.20 | 0.004 | | 0.008 |
| | Pin features | | | | | |
| N | 48 | | | | | |
| ND | 12 | | | | | |
| NE | 12 | | | | | |
| NOTE | SQUARE | | | | | |

Conforms to JEDEC MS-026 ABC Iss. A

Notes:
1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. The top package body size may be smaller than the bottom package body size by a max. of 0.15 mm.
4. Dimension D1 and E1 do not include mould protusion. Allowable protusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mould mismatch.
5. Dimension b does not include dambar protusion. Allowable dambar protusion shall not cause the lead width to exceed the maximum b dimension by more than 0.08 mm.
6. Coplanarity, measured at seating plane G, to be 0.08 mm max.

This drawing supersedes 418/ED/51612/002 (Swindon)

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| ©Mitel | | | | | | | ORIGINATING SITE: SWINDON |
| ISSUE | 1 | | | | | MITEL SEMICONDUCTOR | Title: Package Outline Drawing for 48 lds TQFP (TP) (7x7x1.0) mm, Body+2.0 mm |
| ACN | 201365 | | | | | | |
| DATE | 28OCT96 | | | | | | Drawing Number GPD00249 |
| APPROVED | | | | | | | |

### 7.2 Package Diagram

## 9. Appendix A – RSSI Settling Time

The ADC information for a generic baseband device is assumed to be as follows,

> The DACs and ADCs are 10 bits in 2.5v. Digital input is sampled at 2x symbol rate ie 48.6ksps. Analog input is sampled at either 24 ksps or 40 ksps. On transmit digital iterpolation brings the DAC rate to 388.8 ksps digital and 360 ksps analog.

From the above information, the pseudo LSB for a 5 bit ADC made from the above 10 bit ADC can be calculated as,

$$LSB = \frac{2.461}{2^5} = 76.9mV$$

The output ripple must be less than 0.5 LSB to avoid periodic LSB switching. As a result the following requirement for output ripple is set:

$Vout_{ripple} < 38.45$ mV

The output of the RSSI consists of a capacitor across a resistor into which the RSSI output current is driven. The RSSI output voltage is described by the following equation:

$$Vout(s) = \frac{I(s) * \frac{1}{Cs} * R}{R + \frac{1}{Cs}}$$

From this the transresistance can be written as:

$$\left| \frac{1}{g(w)} \right| = \frac{R}{wRC + 1}$$

Now, the action of the rectifiers within the RSSI has the effect of doubling the input frequency from 60KHz to 120KHz. Assuming a maximum RSSI output current of $Iout_{max}$ = 40uA with a maximum ripple of 38.45mV gives a

$$\frac{1}{g(120K)} \approx 961$$

To set the required slope on the RSSI output a resistor of 33K 1% is used (1% is to ensure the absolute slope accuracy). With this resistor value, the above transresistance and a frequency of 120KHz an output ripple of < 38.45mV can be achieved using a C=1.4nF.

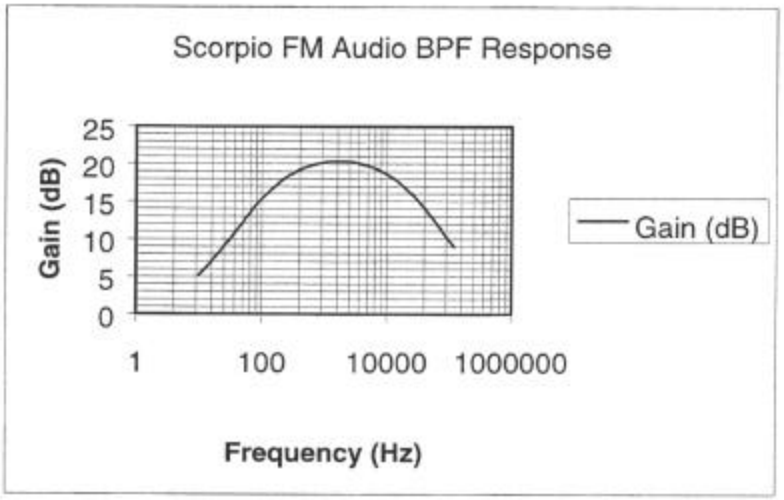
If,

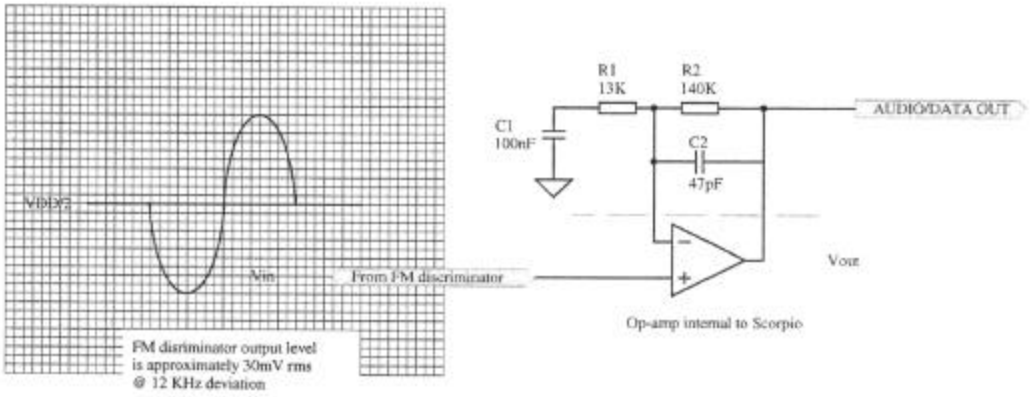
$$F_{3dB} = \frac{1}{2\Pi RC} = 3.6kHz$$

The settling time is therefore:

$$\tau = \frac{1}{F_{3dB}} = 278us$$

## 10. Appendix B – FM Discriminator Component Selection




$$Vout = Vin\left[1 + \frac{Z1}{Z2}\right]$$

$$Z1 = R1 + \frac{1}{2\prod fC1}$$

$$Z2 = \left(\left(\frac{1}{R2}\right) + 2\prod fC2\right)^{-1}$$

MITEL
SEMICONDUCTOR

# Scorpio
## TDMA / AMPS Baseband Interface
Preliminary Information

April 1999

### Features

- IS136 TDMA/AMPS Compatible
- Channel Filtering (30kHz)
- FM Demodulator
- RSSI Output
- Dual IF Synthesisers
- Flexible Power Control
- Fully Programmable via serial bus
- Compatible with Mitel receive and transmit products
- 3 Volt operation
- 48 pin TQFP package

### Applications

- Dual Mode TDMA/MPS Mobile telephones
- Dual Band (PCS1900/900) TDMA/AMPS Mobile telephones
- PCS 1900 TDMA Mobile Telephones

### Description

Scorpio provides channel filtering for IS136 TDMA/AMPS mobile telephones.

**Ordering Information**

SCORPIO/KG/GP1R

The inputs for the receive path are I and Q signals at an IF of 60kHz. These I and Q signals are filtered by a 60 kHz switched capacitor bandpass filter and are then demodulated to give baseband I and Q signals. Scorpio also provides 56dB of voltage gain so that the baseband outputs can be input directly to an A to D converter.
The internal FM discriminator can be used for demodulating AMPS signals. The receive path also provides RSSI.
Transmit I and Q baseband signals from D to A converters can be input directly to Scorpio which provides reconstruction filters and a variable gain buffer.
The two PLL synthesisers are used for generation of the receive and transmit IF LO signals.

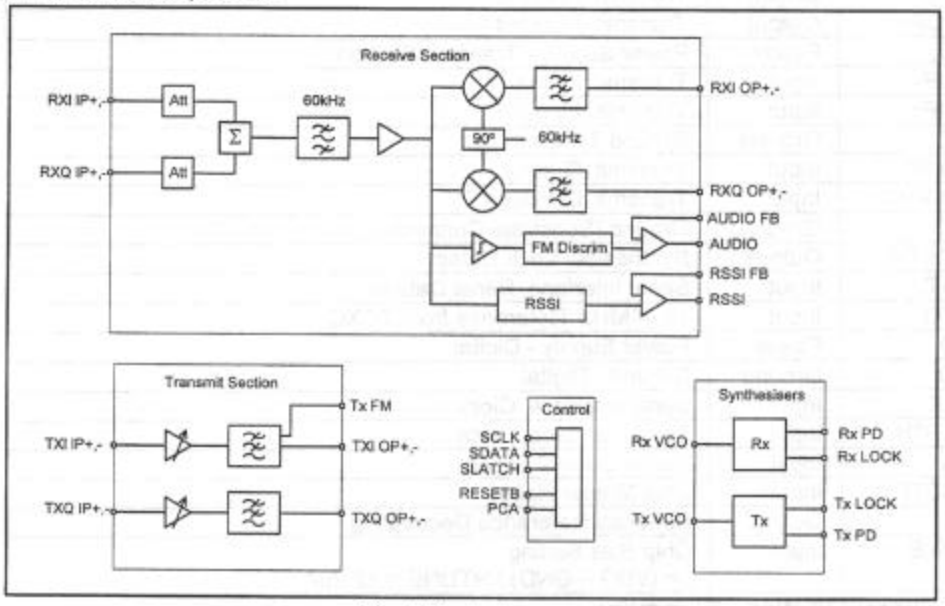



Fig 1 Block diagram

### Pin Assignment

| No | Pin Name | Type | Description |
|---|---|---|---|
| 1 | RXQ OP- | Output | Baseband Receive Q Output - |
| 2 | RXQ OP+ | Output | Baseband Receive Q Output + |
| 3 | RXI OP- | Output | Baseband Receive I Output - |
| 4 | RXI OP+ | Output | Baseband Receive I Output + |
| 5 | GND | Ground | Ground (Substrate Connection) |
| 6 | VDD | Power | Power Supply - RSSI/Demodulator |
| 7 | RSSI | Output | RSSI Output |
| 8 | GND | Ground | Ground - RSSI/Demodulator |
| 9 | AUDIO | Output | Demodulator Audio/Data Output |
| 10 | AUDIO FB | Input | Demodulator Feedback |
| 11 | RSSI FB | Input | RSSI Feedback |
| 12 | GND | Ground | Ground - Receive Section |
| 13 | RXI IP+ | Input | Receive I Input + |
| 14 | RXI IP- | Input | Receive I Input - |
| 15 | RXQ IP+ | Input | Receive Q Input + |
| 16 | RXQ IP- | Input | Receive Q Input - |
| 17 | $VDD_1$ | Power | Power Supply - Receive Section |
| 18 | RX PD | Output | Rx Phase Detector Output |
| 19 | GND | Ground | Ground (Substrate Connection) |
| 20 | RX VCO | Input | Receive IF PLL Input |
| 21 | GND | Ground | Ground - Synthesizer |
| 22 | TX VCO | Input | Transmit IF PLL Input |
| 23 | VDD | Power | Power Supply - Synthesizer |
| 24 | TX PD | Output | Rx Phase Detector Output |
| 25 | UHF LOCK | | UHF Synth Lock Input |
| 26 | TXQ OP+ | Output | Transmit Q Output + |
| 27 | TXQ OP- | Output | Transmit Q Output - |
| 28 | TX FM | Output | Transmit FM Output |
| 29 | TXI OP+ | Output | Transmit I Output + |
| 30 | TXI OP- | Output | Transmit I Output - |
| 31 | $VDD_2$ | Power | Power Supply - Transmit Section |
| 32 | TXI IP- | Input | Transmit I Input - |
| 33 | TXI IP+ | Input | Transmit I Input + |
| 34 | GND | Ground | Ground TX Channel |
| 35 | TXQ IP- | Input | Transmit Q Input - |
| 36 | TXQ IP+ | Input | Transmit Q Input + |
| 37 | GND | Ground | Ground (Substrate Connection) |
| 38 | LOCK DET | Output | Synthesizer Lock Detect |
| 39 | SDAT | Input | Serial Interface, Serial Data In |
| 40 | TCXO | Input | 19.44MHz Reference from TCXO |
| 41 | VDD | Power | Power Supply - Digital |
| 42 | GND | Ground | Ground - Digital |
| 43 | SCLK | Input | Serial Interface, Clock |
| 44 | SLATCH | Input | Serial Interface, Latch |
| 45 | PCA | Input | Power Control Assert |
| 46 | RESETB | Input | Chip Master Reset |
| 47 | VBG | Output | Bandgap Reference Decoupling |
| 48 | RTUNE | Input | Chip Bias Setting<br>I = (VBG – GND) / RTUNE = 12.2uA |

**Electrical Characteristics - Summary**