HELPFUL INFORMATION AND ERRATA:

1. CPU Loading and processor capacity

Processing capacity:

The typical 9050 CPU utilization for an AMPS cellular phone has been measured at 60-65 % in non-turbo mode (MHz clock). The measurements were taken using AMPS software developed by Wireless Link Corporation for the ACE CHIPSET.

The software functions include:

- Dual Tasking O/S
- AMPS Call processing
- Interrupts
- Test Harness

The MMI is not included in the utilization.

Also, the processor cycle time can be dynamically set to 1us or 0.5us in Turbo mode. It should be noted that in Turbo mode (2MHz) the processor utilization drops to less than 30%.

Comments to using the 6303 for other tasks.

Using the 9050 CPU for other tasks is feasible and will depend on the overall system requirements. The main question is CPU utilization. As mentioned, the maximum CPU loading, without an MMI, is 65% when in normal mode, 30% in turbo . The maximum loading occurs when the phone is in the standby mode; (receive only) monitoring the forward control channel. The duty factor is related to processing of the overhead message on the forward control channel. The time to process the OVHD message is about 32 milliseconds. This leaves about 10 milliseconds for non-AMPS processing activities before the next overhead message must be processed..

The other thing to consider is how to interface to the 9050. The preferred approach is through the I2C interface. This allows the 9050 to be either a system controller or it may be controlled as a slave.

The processor has an on board I2C interface so a separate LCD controller may be used if a complex LCD is required with out increasing the load on the 6303.

Furthermore, the processor has been used by a major phone manufacture in a handset which has the following special phone features:

Adjustable ring tone, Voice activated answer mode, 199 memory locations, Alphabetical storage, Personal code protection, short-code dialing, alphabetical search, recall of last 6 numbers.
20 special features accessed by a menu including:

Minute minder, auto retry, call counter, total call time, batter voltage, emergency number. Language select.

Memory requirements for WLC software

The memory code requirement for the ACE CHIPSET AMPS protocol and O/S is less than 40 KB.

Memory address range

The 9050 can address up to 256KB via memory banking.

2. DATA MODEM INFORMATION

Squelch level discussion: relationship between the squelch level setting and the SQRX level.

The SQLEV sets the quality threshold to compare each of the received bits within one byte. SQRX then counts the number of bits within one byte that exceeded the squelch level. For instance, setting the SQLEV to 6 would mean that all 50 samples indicated a logic 1 or 0.

However, when the SQLEV is set to 6, the SQRX registers a 0 even though good data is being transmitted. The Squelch output against RF power in is not a linear function. Also if you set the Squelch levels to the higher values, the only way you can surpass them is by bypassing the discriminator and putting in CMOS levels.

Data Extraction discussion:

The busy/idle bits and dotting and barker code bits are extracted as follows:

1. The busy idle bits are extracted from the data stream. The last value received is available to be read in MODPRT1 bit 6. An optional interrupt can be generated when this location is updated: IRQBISAT

2. The dotting word & barker codes are not extracted from the data stream and so end up in MODPRT2. As the modem hardware re-synchronizes at this point the barker code also get corrupted in MODPRT2, but always in the same way.

   The serial data stream for this will be:

   DATA 1010101010 11100010010 DATA

   This will get split up into 8 bit chunks, so MODPRT2 will get

   10101010: AA
   10111000: B8

   During the third byte the modem re synchronizes the word boundary so that it is correct for the first byte of data in the next frame. It is thus aligned to the end of the barker code. The next byte is thus the last eight bits of the Barker code:

   00010010: 12

SO the MODPRT1 will contain the following 3 consecutive bytes at the end of a frame:
AA
B8
12.

The software has to either discard these bits or use them to indicate a frame end/ beginning.

Word sync detector operation when no RF carrier signal is present:

Please take note. When no RF signal is present, the data discriminator will output random data based on the IF noise. It is quite possible to experience random IRQWS interrupts under these conditions.

When the modem is running at the end of a bit period the modem has to make a decision on the value of the bit. This can be 1 or 0 ! (digital circuits and all that) the barker code is 11 bits long, so with random data and decisions being taken every 100us one would expect barker codes to appear on average every 0.2s.

It is recommend that the synchronization software does not look for only 1 Barker code, but ensures that several barker codes appear with in a time period of around 45 ms after each other.

Also in the ACE9050 the software designer may use RSSI levels and Squelch data to aid his decision of when data synchronization has occurred. During data recovery the software designer should check Work syncs are being generated correctly.

Data Synchronization on the FVC (Forward Voice Channel):

For the AMPS protocol, the FVC message has a significantly different structure to the FCC

There is 101 bit initial dotting sequence
followed by Barker code and then repeat 1 of Word

then the following is repeated a further 10 times:
37 bit dotting
Barker code
Word (40 bits)

The Barker code is repeated for each word repeat. This is different to FCC where it is once per frame only.

The length of the message is therefore:
1032 bits (103.2 ms)

The basic word repeat sequence is now 88 bits i.e. divisible by 8 unlike the FCC.

Now given this information, data synchronization on the FVC depends on how the system designer wants to approach this area, so we cannot make any hard & fast rules. Here are some thoughts;

When on the voice channel, the mobile phone must always monitor the channel for data. One problem that may occur is that when the ENWS is enabled, word sync detection may occur weather or not data is being transmitted.

One way around false word sync is to look for the dotting sequence to occur in the MODPRT2. For instance if you read 4 consecutive dotting sequences (32 consecutive dotting bits) in MODPRT2 you can fairly safely assume you are receiving a valid frame of data. You can then set the SYNDET (MODPRT)[2] to Sync mode and enable ENWS, or you can have ENWS always high. The former should prevent spurious IRQWS interrupts.

3. I2C clock speed

The actual clock speeds on I2C busses is not a fixed quantity; The low time can be stretched by slower devices. Also the I2C spec was originally designed for 100KBs, which is defined as Normal mode. It was then increased to be 400KBs and called fast mode. The ACE9050 I2C can only work in Normal mode (up to 100KBs), but it has the facility to operate on a Multi-Master bus system where another master is working at 400KBs. In this case the internal ACE9050 I2C clock must be faster than 400KHz, i.e. the 500 KHz talked about in the spec.

Note: Even with a defined clock speed set up in the Clock register (CCR) the actual frequency of the SCL may be less as the low time of this clock is stretched by the hardware when the IFLG bit is set. This occurs when one of the 27 I2C states is entered (as per the STAT Register) and is cleared by software.

4. ACE9050 Latch 3 clarification and 9030 synthesizer operation

OVERVIEW:

The Latch 3 of the 9050 is designed to be used as the serial data latched to program the synthesizer of the ACE9030. Only the long latch can be generated from the ACE9050. The minimum programmable latch length is 100 usec. However, both latch 0 and latch 1 can still be exercised while the LATCH [3] is active. The blocks of the ACE CHIPSET may be controlled via the ACE serial interface while LATCH [3] is active, since the 9030 synthesizer latches data on the rising edge of the latch. Furthermore, should circumstances require, an active LATCH [3] may be de-activated.

1) Programming the ACE9030 RFI and ACE9040 while the LATCH [3] is active:

Latch 0 or 1 pulse can be generated during a long LATCH [3] pulse. Data transmission to the radio and audio parts can then continue during this long latch. The procedure is to generate a long LATCH [3] (the shortest possible - 100us), and to transmit the data. When the latch is activated, the interrupt IRQSENDN is generated. This enables the data shift registers to be reloaded with data and the other latches can be enabled. These instructions must be performed in the interrupt handler routine to ensure that the LATCH [3] has been generated. It is important that there aren't too many instructions in the interrupt routine prior to the enabling of the latches because they will cause time delays which may result in the latch pulse occurring after the LATCH [3] pulse has gone low.

2) Shortening the LATCH [3] duration:

It is possible to shorten a long LATCH [3] pulse by setting the latch width register to zero. The command to set the latch width to zero must be **in the interrupt routine, after an IRQSENDN** interrupt. In our case, it resulted in the 100us pulse being shortened to 20us. This time will depend on how the interrupt routine is written. We use C code. If an assembler routine was used this time could be shorter.

FAQ

1. *To Start TX interrupt, do I just set IRQTX to 1?*
   Yes. Setting the IRQPORT1 bit 7 to 1 will enable IRQTX interrupts.

2. *At the beginning or end of a TX data stream, does the TX buffer have to be refreshed?*
   The transmitter sequence is described in section 4.15.1.4. Data must be written to the modem before, or directly after a IRQTX interrupt as it will be transmitted on that interrupt. If no new data is written to MODPRT2 between IRQTX interrupts, the previous data will be re-transmitted.

3. *At the beginning or end of a RX data stream, does the RX buffer have to be refreshed?*
   The RX buffer is read only (also MODPRT2).

4. *While on a Voice channel and when SAT is lost, how often is the SAT interrupt generated?*
   The SAT interrupt will be generated every 10-12ms

5. *When on a control channel, is there any delay between IRQRX and IRQBISAT?*
   An IRQRX is made every time the MODPRT2 is updated. This will be every 8 bits (excluding BI bits) of the incoming message. The IRQBISAT will occur after a BI bit in the data sequence. These occur after 10 data bits in the incoming message. The timing relationship between IRQRX & IRQBISAT can't determined, just as the BI position to a byte boundary can't be determined in the incoming message.

5. *According to the ACE9050 document the value of SRQRX is from 0 to 8. This is supposedly from 1 to 15. Correct?*
   The ACE9050 document is correct. Each byte has 8 bits. Each bit can either reach the squelch threshold or not. Thus the maximum possible number of "good" bits is 8, the minimum 0. I don't know where the figures 1 to 15 come from.

6. *How is ST generated?*
   The ST tone is 10KHz with a 8KHz deviation. To generate it you use the modem Transmitter. Write either FF or 0 to MODPRT2 and enable the transmitter. This will generated, by the fact of being Manchester encoded data, the relevant 10KHz tone

7. *We need to kill the power immediately by SW. The ATO is too slow. Is there another way you can power down?*
   Yes. The POFF output is enabled by PORT3 bit 4, UPOFFN. Only when this is set will POFF be logic 1. IF UPOFFN is set to zero by the software, then POFF will be driven to logic 0. This will occur almost instantaneously. (The watchdog won't change the state of either UPOFFN or POFF)

8. *Please show me the power on sequence.*
   The actual power on sequence depends on the external power regulators used in the system, and their respective control mechanisms. The ACE9050 POFF pin can be used to trigger a powering down of the mobile. POFF is controlled by the ATO and UPOFFN.

   After reset the POFF & UPOFFN will be low. The software write to UPOFFN to enable POFF. POFF will then be disabled by an ATO time out or by the software driving UPOFFN low. The way POFF is used in the system will depend on the external power regulators & keyboard On/Off system used. Care must be taken to ensure the ACE9050 and AC9040 (If this device is used to control MRN) will power on with POFF low.

9. *What is the decision threshold on the BCH Code transmission?*

Each 40 bit word contains 12 parity bits. Data & Parity bits are treated the same in the hardware. Each bit is sampled 50 times. The software can set a threshold between 50 & 32 and read for how many bits this threshold has been exceeded. The software can do what it wants after it has read the bits in terms of using the BCH code for error detection & correction. The software would also be in charge of storing the repeated words and majority voting. On a FOCC the word is repeated 5 times, and on a RVC 11.

ACE9050 DATA SHEET

GEC PLESSEY
SEMICONDUCTORS

JANUARY 1997

DS4290-2.3

ACE9050

SYSTEM CONTROLLER AND DATA MODEM

The ACE9050 provides the control and interface functions needed for AMPS or TACS analog cellular handsets. The device has been designed using GEC Plessey Semiconductors sub-micron CMOS technology for low power and high performance.

The ACE9050 contains an embedded microcontroller and peripheral functions. The controller is of the 6303 type with a Serial Communication Interface, Timer, ROM and RAM. The peripheral functions are: Data Modem, SAT Management, Serial Chip Interfaces, I²C Interface, two Pulse Width Modulators, IFC Counter, Tone generator, I/O ports, Watchdog and Crystal Oscillator.

Several power down modes are incorporated in the device as is a processor emulation mode for software and system development.

An index to this data sheet is given on pages 49 and 50.

FEATURES

- Low Power, Low Voltage (3·6 to 5·0 V) Operation
- 3·0V Memory Interface
- Power Down and Emulation Modes
- 6303R-type Microcontroller
- AMPS or TACS Modem
- Watchdog and Power Control Logic
- SAT Detection, Generation and Loopback
- 6K bytes RAM
- Interface to FLASH and EEPROM Memories
- 512 byte ROM Boot Block
- I/O Ports for Keyboard Scanning
- I²C Controller
- Small Outline 100-pin package

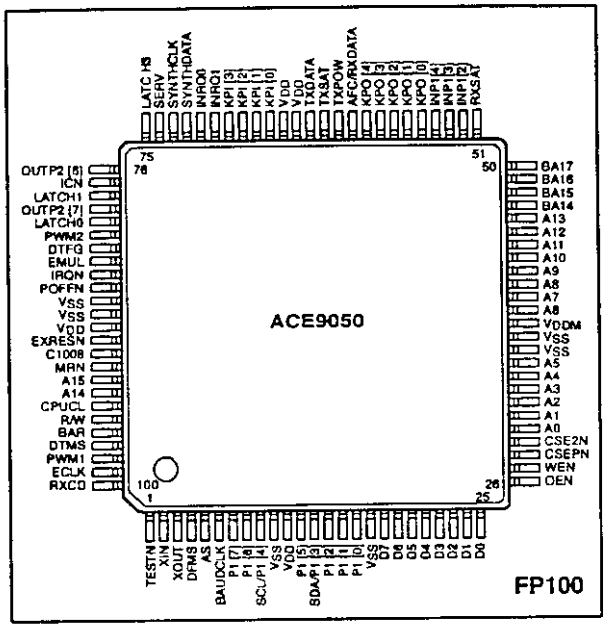


Fig.1 Pin connections - top view. Pin 1 is identified by moulded spot and by coding orientation. See Table 1 for detailed pin descriptions.

APPLICATIONS

- AMPS and ETACS Cellular Telephones
- Two-way Radio Systems

RELATED PRODUCTS

The ACE9050 is part of GEC Plessey Semiconductors' ACE chipset, together with the following:

ACE9010 RF Front End with VCO
ACE9020 Receiver and Transmitter interface
ACE9030 Radio Interface and Twin Synthesiser
ACE9040 Audio Processor

ORDERING INFORMATION

Industrial temperature range.
TQFP 100-lead 14×14mm, 0·5mm pitch package (FP100)
ACE9050 / IG / FP1N: trays and dry packed
ACE9050 / IG / FP1Q: tape mounted and dry packed

ABSOLUTE MAXIMUM RATINGS

Supply voltages V_{DD}, V_{DDM}	−0·5V to +6V
Storage temperature	−55°C to +150°C
Operating temperature	−40°C to +85°C
Voltage on any pin	V_{SS}−0·5V to V_{DD}+0·5V

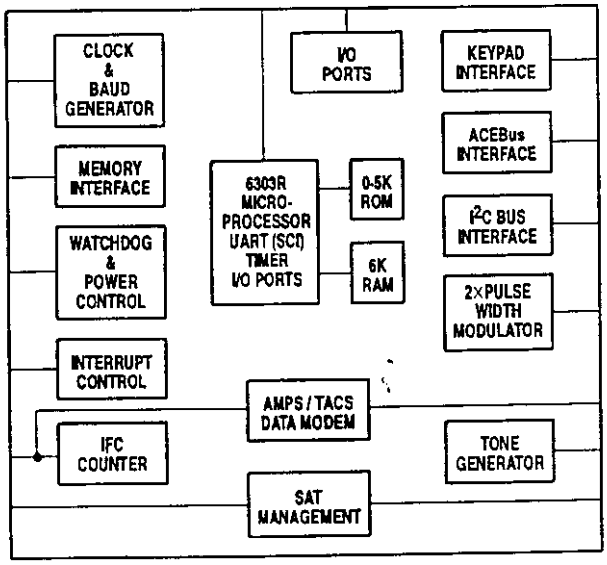


Fig.2 ACE9050 simplified block diagram

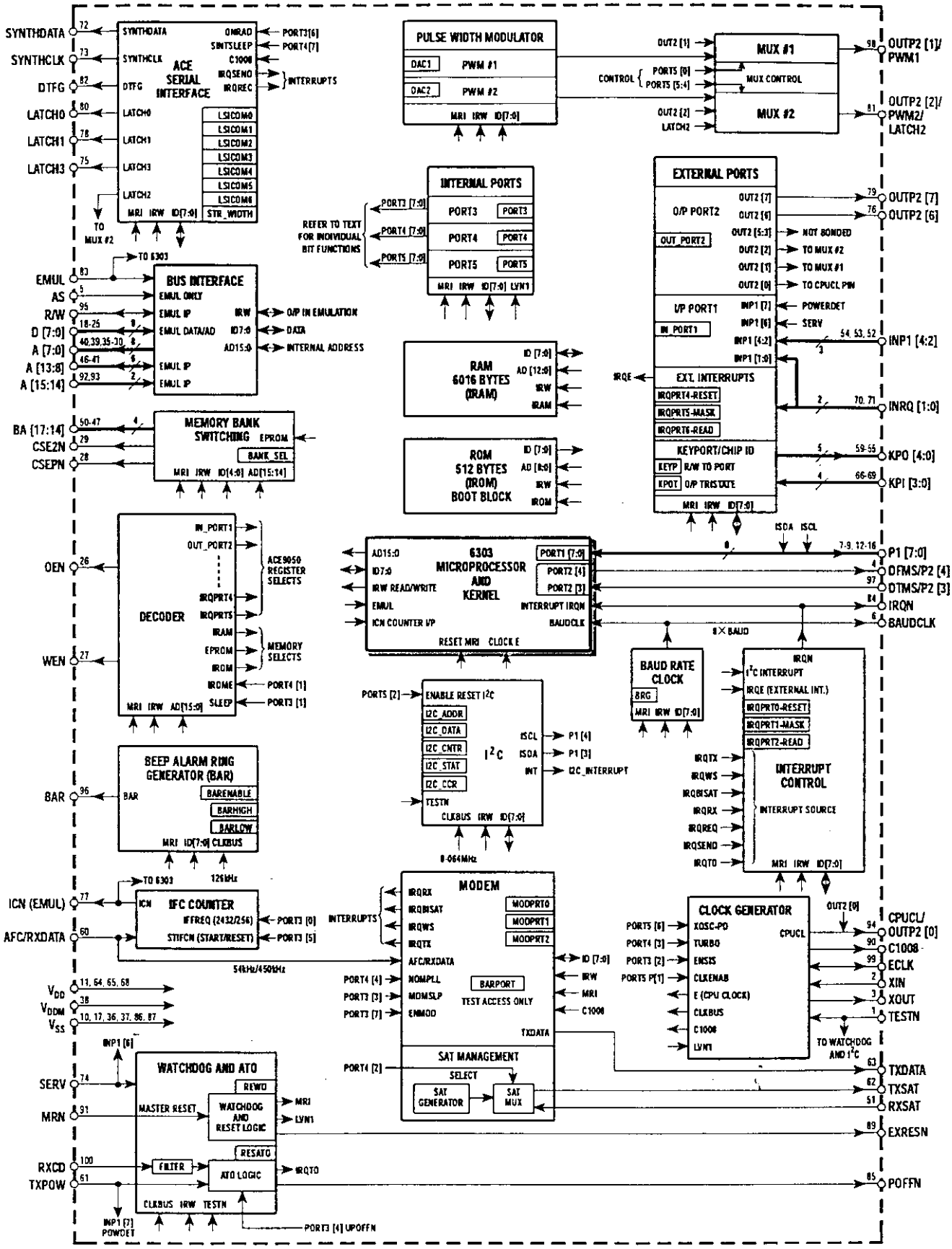


Fig. 3 detailed block diagram of ACE9050

FUNCTIONAL OVERVIEW

MICROPROCESSOR UNIT

The processor unit is program compatible with the standard 6303R. It contains the following hardware:

8-bit CPU
Serial Communication Interface: SCI (UART)
16-bit timer/counter
8-bit I/O port (P1)
2-bit I/O port (P2)

The processor bus speed can be either 1·008 MHz or 2·016 MHz. An Emulation mode is provided whereby the internal 6303 is bypassed to allow software development on a standard 6303 In-Circuit Emulator (ICE).

MEMORY

The ACE9050 contains 512 bytes ofROM and 6144 bytes of RAM internally.

The ROM code facilitates system initiation after a reset and the programming of FLASH memory via the 6303 SCI (UART). The Internal RAM area represents the total RAM requirement anticipated for a cellular phone.

BUS INTERFACE and MEMORY BANK SWITCHING

These blocks create the Data, Address and Control lines for the external memory. The external address bus is expanded from the standard 16 bits up to 18 bits by a banked addressing scheme. This increases the memory address space from 64K to 256K. Two programmable Chip Selects (CSEPN and CSE2N) are generated.

The Memory Interface will operate down to +3V, allowing the use of low voltage memory parts.

In Emulation mode the external processor controls the ACE9050 via the Bus Interface block.

EXTERNAL PORTS

The ACE9050 contains two Keypad Interface ports, two maskable external interrupts, and both Input and Output ports. These are in addition to the 6303 bidirectional Port1 and Port2. The Output port provides two high current outputs for driving LEDs.

DECODER and INTERRUPT CONTROL

The Decoder block memory maps ACE9050 register locations onto the processor's address space.

The Interrupt Control block handles both internal and external interrupt sources. These are fed into control logic allowing individual masking and reset by software. The Interrupt control logic output is internally connected to the 6303 IRQ and also drives an external pin.

ACE SERIAL INTERFACE (SINT) and I²C

Three serial interface protocols are supported: UART, I²C and ACEBus. The 6303 provides a UART interface via the SCI block.

The ACE9050 I²C block provides an I²C interface with both Master and Slave capability.

The ACEBus is designed for use with the ACE Chipset and has a data rate of just over 1MBits/sec. Three Latch pulse are available to target data at the relevant IC and control the ACE9030 Synthesiser.

BEEP, ALARM and RING TONE GENERATOR (BAR)

The BAR Generator is intended to drive an acoustic tone transducer. It has a programmable single digital pulse train output.

MODEM and SAT MANAGEMENT

The Modem provides two way data transfer and SAT management over the radio link between a base station and phone handset. AMPS and TACS data rates are supported .

The Modem block contains: Digital Discriminator, Data Decoder and Word Synchronising hardware. Various modes can be selected by software. A squelch level is also set by software so that the quality of each data byte can be assessed.

SAT detection and generation at the standard three frequencies 5970Hz, 6000Hz and 6030Hz is included.

WATCHDOG and POWER CONTROL (ATO)

The Watchdog function will provide an internal and external Reset if the processor does not make a write access to a defined address every 4 seconds.

An Autonomous Time Out circuit (ATO) will drive the POFFN output low if Transmitter power is detected without Receiver power, independent of any processor operation. POFFN must be used in conjunction with external regulators to control power to the mobile handset.

IF CONTROL COUNTER (IFC)

The Intermediate Frequency Control (IFC) Counter is used as part of an AFC Loop. The IFC Counter provides a pulse after a set number of IF input pulses. The IFC Counter output is connected to the 6303 timer input and an external pin (ICN).

TWIN PULSE WIDTH MODULATORS

Two independently programmable Pulse Width Modulators (PWMs) are available. These provide digital output pulse trains, controllable by software. The output can be filtered externally to provide a DAC function. Typical applications are battery charging control and LCD contrast control.

CLOCK GENERATOR

The Clock Generator provides all the various internal and external clocks from a single 8·064 MHz source. The source can either be an external crystal or the ACE9030.

PIN DESCRIPTIONS

Pin	Name	Type	Block	Description	Internal
1	TESTN	I	CLK/WDATO	Connect to V_{DD}	PU
2	XIN	I	CLK	Crystal connection CMOS input: 8·064 MHz	None
3	XOUT	O	CLK	Crystal connection	-
4	DFMS/P2 [4]	I/O	CPU	CPU Port2 bit 4 or Serial interface (SCI) output	None
5	AS	I	BINT	Address strobe (Latch Address during Emulation)	PU
6	BAUDCLK	O *(I)*	BAUD	Baud Rate Gen. output for Emulation *(Input in test mode)*	PU
7	P1[7]	I/O	CPU	PORT 1 of CPU	None
8	P1[6]	I/O	CPU	PORT 1 of CPU	None
9	P1[4]/SCL	I/O	CPU / I²C	PORT 1 of CPU/I²C SCL	None
10	V_{SS}			Ground	-
11	V_{DD}			Digital Supply	-
12	P1[5]	I/O	CPU	PORT 1 of CPU	None
13	P1[3]/ SDA	I/O	CPU / I²C	PORT 1 of CPU/I²C SDA	None
14	P1[2]	I/O	CPU	PORT 1 of CPU	None
15	P1[1]	I/O	CPU	PORT 1 of CPU	None
16	P1[0]	I/O	CPU	PORT 1 of CPU	None
17	V_{SS}			Ground	-
18	D7	I/O	BINT	Data bus *(and Emulation Address A7 Input)*	None
19	D6	I/O	BINT	Data bus *(and Emulation Address A6 Input)*	None
20	D5	I/O	BINT	Data bus *(and Emulation Address A5 Input)*	None
21	D4	I/O	BINT	Data bus *(and Emulation Address A4 Input)*	None
22	D3	I/O	BINT	Data bus *(and Emulation Address A3 Input)*	None
23	D2	I/O	BINT	Data bus *(and Emulation Address A2 Input)*	None
24	D1	I/O	BINT	Data bus *(and Emulation Address A1 Input)*	None
25	D0	I/O	BINT	Data bus *(and Emulation Address A0 Input)*	None
26	OEN	O	DEC	Output Enable	-
27	WEN	O	DEC	Write Enable	-
28	CSEPN	O	MEMB	C/S External EPROM	-
29	CSE2N	O	MEMB	C/S External EEPROM	-
30	A0	O	BINT	Address bus	-
31	A1	O	BINT	Address bus	-
32	A2	O	BINT	Address bus	-
33	A3	O	BINT	Address bus	-
34	A4	O	BINT	Address bus	-
35	A5	O	BINT	Address bus	-
36	V_{SS}			Ground	-
37	V_{SS}			Ground	-
38	V_{DDM}			Digital Supply for Memory Interface (pins18-35, 38-50)	-
39	A6	O	BINT	Address bus	-
40	A7	O	BINT	Address bus	-
41	A8	O *(I)*	BINT	Address bus *(Input during Emulation)*	None
42	A9	O *(I)*	BINT	Address bus *(Input during Emulation)*	None
43	A10	O *(I)*	BINT	Address bus *(Input during Emulation)*	None
44	A11	O *(I)*	BINT	Address bus *(Input during Emulation)*	None
45	A12	O *(I)*	BINT	Address bus *(Input during Emulation)*	None
46	A13	O *(I)*	BINT	Address bus *(Input during Emulation)*	None
47	BA14	O	MEMB	Address bus (Extended Address: From Bank Select Register)	-
48	BA15	O	MEMB	Address bus (Extended Address: From Bank Select Register)	-
49	BA16	O	MEMB	Address bus (Extended Address: From Bank Select Register)	-
50	BA17	O	MEMB	Address bus (Extended Address: From Bank Select Register)	-
51	RXSAT	I	MODEM	Received SAT input	None
52	INP1 [2]	I	EPORT	Bit 2 Input Port1	None
53	INP1 [3]	I	EPORT	Bit 3 Input Port1	None
54	INP1 [4]	I	EPORT	Bit 4 Input Port1	None
55	KPO [0]	O	EPORT	Keypad scan output/output port	-
56	KPO [1]	O	EPORT	Keypad scan output/output port	-
57	KPO [2]	O	EPORT	Keypad scan output/output pon	-
58	KPO [3]	O	EPORT	Keypad scan output/output port	-
59	KPO [4]	O	EPORT	Keypad scan output/output port	-
60	AFC/RXDATA	I	IFC/MODEM	54/450kHz IF input fromACE9030	None
61	TXPOW	I	WDATO	Power detect from transmitter	None
62	TXSAT	O	MODEM	SAT Output	-
63	TXDATA	O	MODEM	TACS / AMPS Modem Output	-
64	V_{DD}			Digital Supply	-
65	V_{DD}			Digital Supply	-

Table 1

Cont...

Pin	Name	Type	Block	Description	Internal
66	KPI [3]	I	EPORT	Keypad scan input/input port	PD
67	KPI [2]	I	EPORT	Keypad scan input/input port	PD
68	KPI [1]	I	EPORT	Keypad scan input/input port	PD
69	KPI [0]	I	EPORT	Keypad scan input/input port	PD
70	INRQ1	I	EPORT	External Interrupt (also Bit1 Input Port1)	PD
71	INRQ0	I	EPORT	External Interrupt (also Bit0 Input Port1)	PD
72	SYNTHDATA	O	SINT	SynthBus Data Line	-
73	SYNTHCLK	O	SINT	SynthBus 126kHz Clock	-
74	SERV	I	WDATO	1 = Service Mode	None
75	LATCH3	O	SINT	Latch, programmable length. (To ACE9030, LATCHC pin)	-
76	OUTP2 [6]	O	EPORT	Output Port2 Bit 6: High Current Driver	-
77	ICN	O *(I)*	IFC	IF Counter Output for Emulation *(input in Test mode)*	PU
78	LATCH1	O	SINT	Latch O/P (To ACE9030 receiver Interface, LATCHB pin)	-
79	OUTP2[7]	O	EPORT	Output Port2 Bit 7: High Current Driver	-
80	LATCH0	O	SINT	Latch O/P (To ACE9040, LEN)	-
81	OUTP2[2]/PWM2/ LATCH2	O	PWM	Output Port2 Bit 2/Pulse Width Modulator #2 Output/ SynthBus Latch O/P.	-
82	DTFG	I/O	SINT	Bidirectional serial inter-chip data, to/from the ACE9030	None
83	EMUL	I	BINT/CPU	1 = CPU Emulation Mode	PD
84	IRQN	O *(I)*	CPU	CPU Interrupt for Emulation *(input in Test mode)*	-
85	POFFN	O	WDATO	Power On/Off	-
86	V_{SS}			Ground	-
87	V_{SS}			Ground	-
88	V_{DD}			Digital Supply	-
89	EXRESN	O	WDATO	External reset output	-
90	C1008	O	CLK	1.008MHz Clock for ACEBus, ACE9030 and ACE9040	-
91	MRN	I	WDATO	0 = Chip reset	None
92	A15	I	BINT	*Address input for Emulation only*	PU
93	A14	I	BINT	*Address input for Emulation only*	PU
94	CPUCL/OUTP2[0]	O	CLK/EPORT	8.064MHz clock/Out Port 2 bit 0	-
95	R/W	O *(I)*	BINT	Read/Write *(Input during Emulation)*	None
96	BAR	O	BAR	Beep, Alarm, Ring Tone Output	-
97	DTMS	I/O	CPU	CPU Port 2 bit 3 or Serial interface (SCI) input	None
98	OUTP2 [1]/PWM 1	O	PWM	Output Port 2 Bit 1/Pulse Width Modulator #1 Output	-
99	ECLK	O *(I)*	CLK	Processor Clock *(Input during Emulation)*	None
100	RXCD	I	WDATO	Carrier detect from RX	None

Table 1 (continued)

ABBREVIATIONS

BAR	Beep, Alarm and Ring tone generator
BAUD	Baud Rate generator
BINT	Bus Interface
MEMB	Memory Bank switching
CLK	Clock generator
CPU	6303 microprocessor unit
DEC	Decoder
EPORT	External Port
I^2C	I^2C interface
IFC	IF Control counter
MODEM	AMPS/TACS Modem
PWM	Pulse Width Modulator and MUX
SINT	Serial Inter-chip interface
WDATO	Watchdog/Autonomous Time Out
PU	Internal Pullup resistor present
PD	Internal Pulldown resistor present

UNUSED INPUTS

Input or bidirectional pins must have a suitable pullup or pulldown reststor if they are configured as inputs, with no external drive. Some inputs have an internal pullup or pulldown resistor of the order of 100kΩ; this value is suitable if the pin is not subject to excessive noise or residual current greater than 15µA. If the pins shown in Table 2 are not used in the system, an external resistor will be required.

Pin	Name	Pin	Name	Pin	Name
4	DFMS	15	P1 [1]	61	TXPOW
7	P1 [7]	16	P1 [0]	74	SERV
8	P1 [6]	51	RXSAT	82	DTFG (Requires programming resistor)
9	P1 [5]	52	INP1 [2]		
12	P1 [4]	53	INP1 [3]	91	MRN
13	P1 [3]	54	INP1 [4]	97	DTMS
14	P1 [2]	60	AFC_IN/RXDATA	100	RXCD

NOTE: P1 [7:0], DFMS and DTMS are configured as inputs upon reset.

Table 2

ELECTRICAL CHARACTERISTICS

The Electrical Characteristics are guaranteed over the following range of operating conditions (unless otherwise stated):

T_{AMB} = −40°C to +85°C, V_{DD} = 3·6V to 5·5V, V_{DDM} = 3·0V to 5·5V (note 2)

DC CHARACTERISTICS

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current (Normal clock)	I_{DDNOR}		3·5		mA	1·008MHz ECLK, V_{DD} = 5V
Supply current (Turbo clock)	I_{DDTUR}		6·0		mA	2·016MHz ECLK, V_{DD} = 5V
Supply current (Static)	I_{DDSB}		150		µA	No clock & osc. powered down
Input high voltage	V_{IH}	0·7V_{DD}			V	
Input low voltage	V_{IL}	−0·5		0·2V_{DD}	V	
Output high voltage	V_{OH}	0·8V_{DD}	0·92V_{DD}		V	I_{OH} = 2mA, V_{DD} > 3·6V I_{OL} = 1mA, V_{DD} ≤ 3·6V
Output low voltage	V_{OL}		0·2	0·4	V	I_{OH} = 2mA, V_{DD} > 3·6V I_{OL} = 1·5mA, V_{DD} ≤ 3·6V
High current drive O/P source (pins 76 & 79)	I_{OHHI}			10 6	mA	V_{DD} > 3·6V V_{DD} = 3·6V
High current drive O/P sink (pins 76 & 79)	I_{OLHI}			10 9	mA	V_{DD} > 3·6V V_{DD} = 3·6V
Tristate leakage current	I_{OZ}			1	µA	No Pullup/down cell
Input leakage current	I_{IN}			1	µA	No Pullup/down cell
Pullup/down resistance	R_{IN}	35		150	kΩ	V_{DD} = 5·5V, T_{AMB} = 25°C

NOTES
1. The DC Characteristics Min. and Max figures are guaranteed by test.
2. The voltage on V_{DDM} must be less than or equal to V_{DD}.

AC CHARACTERISTICS (CLOCKS and CRYSTAL)

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Oscillator frequency	f_{OSC}		8·064		MHz	External crystal
Oscillator external I/P	f_{IP}		8·064		MHz	CMOS/800mV sine I/P AC coupled
AC coupling capacitor	C_{COUPLE}		10		nF	Sine input
External resistor	R1	470	1000		kΩ	Crystal oscillator
External capacitors	C1, C2		22		pF	Crystal oscillator (note 1)
Crystal ESR	$XTAL_{ESR}$			120	Ω	Crystal oscillator
Startup time	t_{SU}			5	ms	Crystal oscillator
Radio serial control bus	C1008		1·008		MHz	
Microprocessor clock	ECLK1		1·008		MHz	Normal clock
Microprocessor clock	ECLK2		2·016		MHz	Turbo clock
Clock output	CPUCL		8·064		MHz	Output enabled
Watchdog time out	WD_{TO}		4		s	Normal Mode
Autonomous time out	ATO_{TO}		30		s	Normal Mode

NOTES
1. Refer to crystal manufacturer for exact deatils.

TIMING DIAGRAMS

NORMAL MODE PROCESSOR INTERFACE

Read Cycle

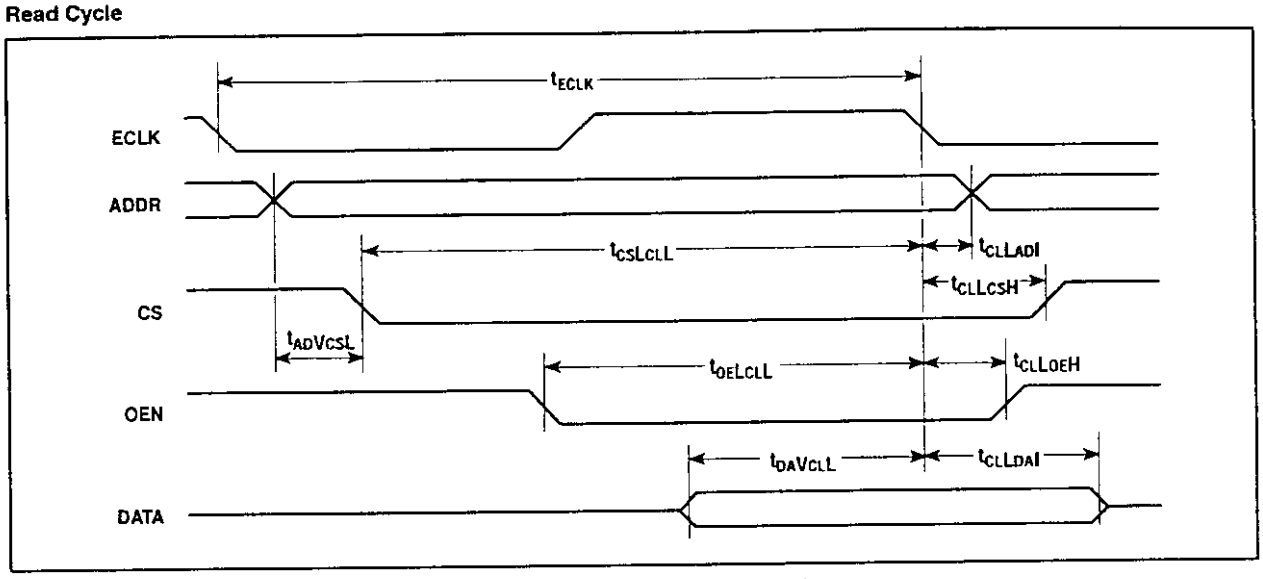


Fig.4 ACE9050 6303 Read cycle timing diagram

Timing Cycle Conditions

Input clock frequency, XIN = 8·064MHz. **Worst case Timings:** T_{AMB} = −40°C to +85°C, V_{DD} = +3·6V to +5·5V
Typical timings: T_{AMB} = +25°C, V_{DD} = +3·75V

Description	Symbol	Normal clock			Turbo clock			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Cycle time	t_{ECLK}		992			496		ns
Address valid to CS low	t_{ADVCSL}	2	4	9	2	4	9	ns
Chip Select set-up time	t_{CSLCLL}	940	972	985	445	480	490	ns
OEN set-up time	t_{OELCLL}	485	492	495	240	245	248	ns
Data set-up time	t_{DAVCLL}	35			35			ns
Data hold time	t_{CLLDAI}	0			0			ns
OEN hold time	t_{CLLOEH}	0	1	4	0	1	4	ns
CS hold time	t_{CLLCSH}	9	24	45	9	24	45	ns
Address hold time	t_{CLLADI}	7	18	42	7	18	42	ns

Table 3 ACE9050 6303 Read cycle timing

Write Cycle (Normal Mode)

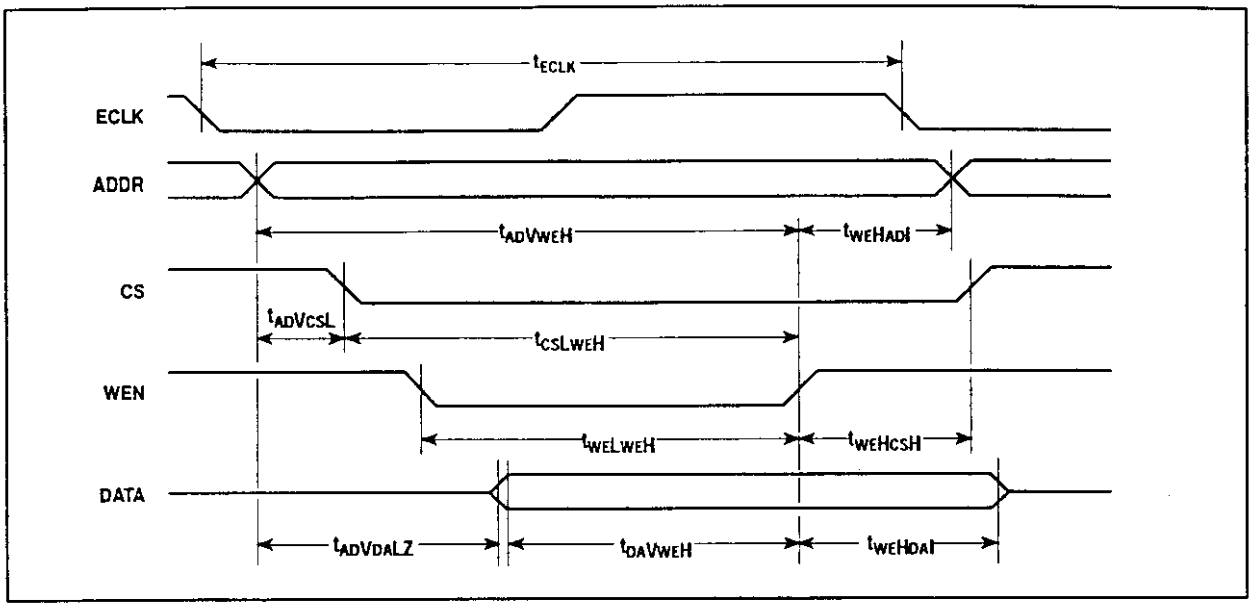


Fig. 5 ACE9050 6303 Write cycle timing diagram

Timing Cycle Conditions

Input clock frequency, XIN = 8·064MHz. **Worst case timings:** T_{AMB} = −40°C to +85°C, V_{DD} = +3·6V to +5·5V
Typical timings: T_{AMB} = +25°C, V_{DD} = +3·75V

Description	Symbol	Normal clock			Turbo clock			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Cycle time	t_{ECLK}		992			496		ns
Address valid to end of Write	t_{ADVWEH}	835	853	862	395	420	427	ns
Address hold time	t_{WEHADI}	125	140	151	63	72	93	ns
Chip enable set-up time	t_{CSLWEH}	825	840	860	390	415	425	ns
WE pulse width	t_{WELWEH}	363	364	371	173	181	184	ns
Data valid set-up time	t_{DAVWEH}	365	368	371	177	183	192	ns
Data hold time	t_{WEHDAI}	120			60			ns
Address valid to data low Z	$t_{ADVDALZ}$	451	473	487	203	225	239	ns
Address valid to chip select	t_{ADVCSL}	0	5	10	0	4	9	ns
WE high to CS high	t_{WEHCSH}	127	140	163	66	72	105	ns

Table 4 ACE9050 6303 Write cycle timing

EMULATION MODE PROCESSOR INTERFACE
Read and Write Cycles

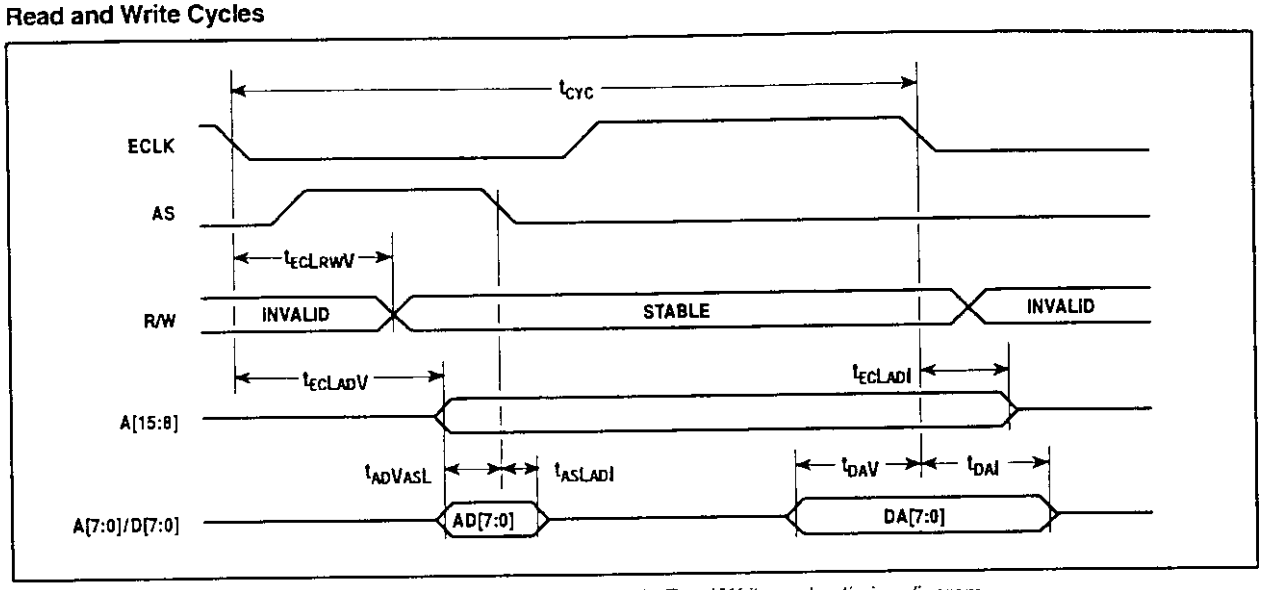


Fig.6 ACE9050 6303 Emulation mode Read/Write cycles timing diagram

Emulation Mode Timing Cycle Conditions

Input clock ECLK frequency = 1·008MHz (Normal clock), 2·016MHz (Turbo clock), T_{AMB} = +25°C, V_{DD} = +5V ±10%

Description	Symbol	Normal clock			Turbo clock			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Cycle time	t_{CYC}		992			496		ns
Read/Write setting time	t_{ECLRWV}			250			160	ns
Address delay time	t_{ECLADV}			250			160	ns
Address hold time	t_{ECLADI}	0			0			ns
Address to latch set-up time	t_{ADVASL}	60			20			ns
Address to latch hold time	t_{ASLADI}	30			20			ns
Data set-up time - WRITE	t_{DAV-W}	50			50			ns
Data hold time - WRITE	t_{DAI-W}	1			1			ns
Data set-up time - READ	t_{DAV-R}	80			80			ns
Data hold time - READ	t_{DAI-R}	1			1			ns

Table 5 6303 Emulation Mode Read/Write cycles timing

SERIAL INTERFACE BLOCK

ACEBus Read and Write Timings

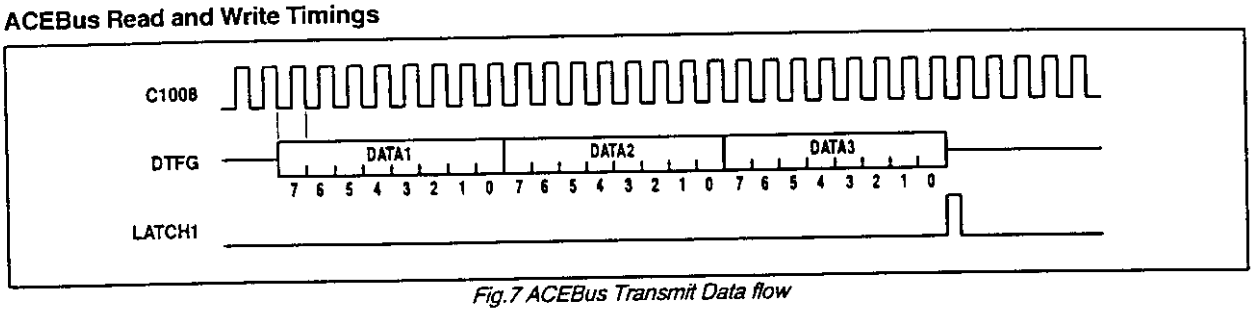


Fig.7 ACEBus Transmit Data flow

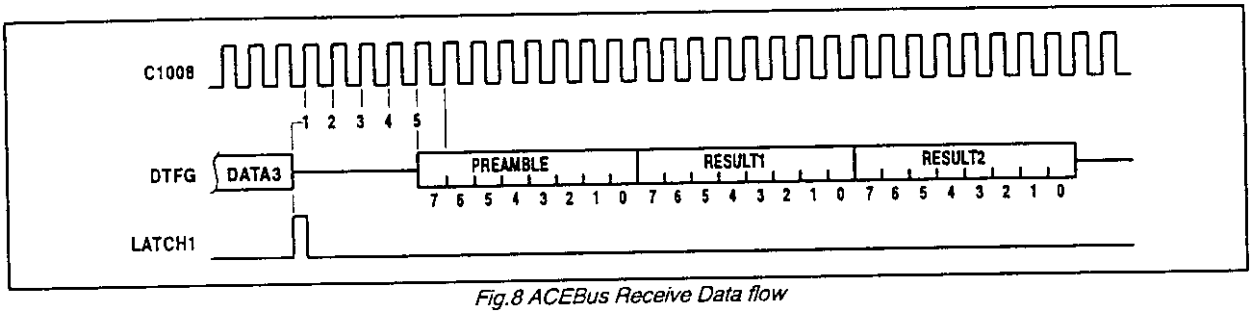


Fig.8 ACEBus Receive Data flow

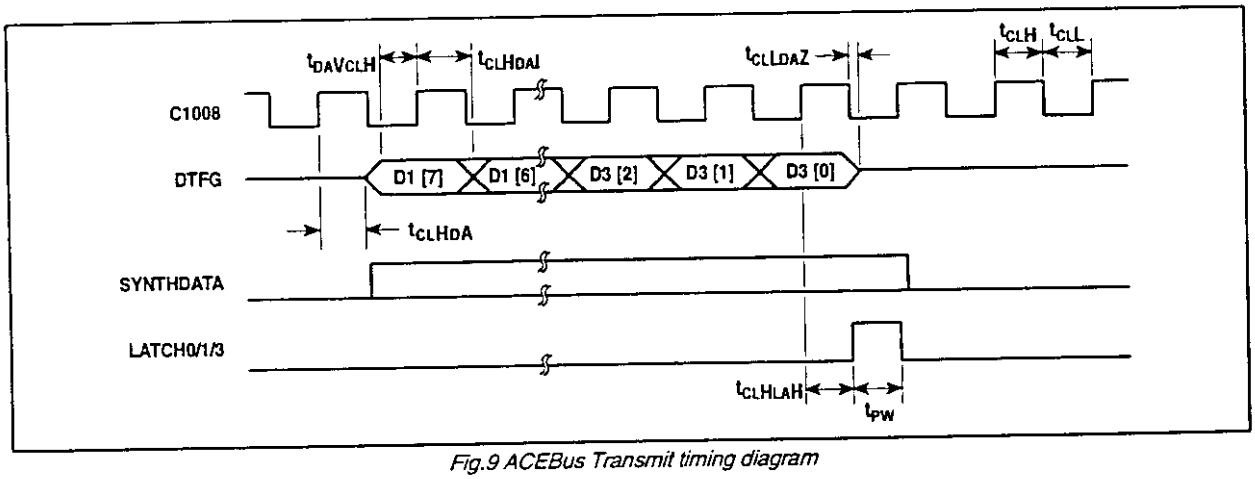


Fig.9 ACEBus Transmit timing diagram

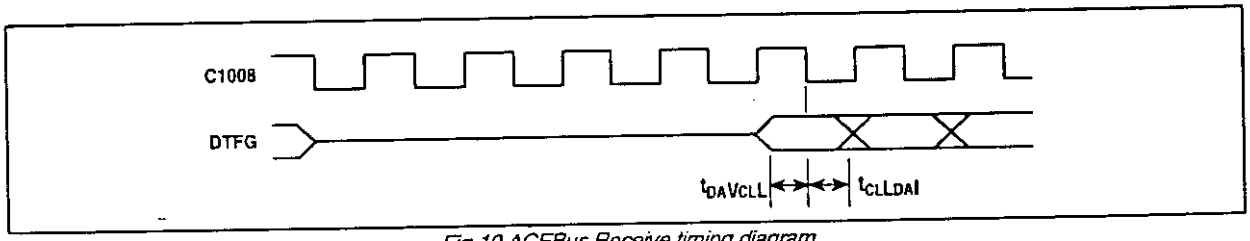


Fig.10 ACEBus Receive timing diagram

ACEBus Timing Cycle Conditions

Input clock frequency, XIN = 8·064MHz. **Worst case Timings:** T_{AMB} = −40°C to + 85°C, V_{DD} = +3·6V to +5·5V
Typical timings: T_{AMB} = +25°C, V_{DD} = +3·75V

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
TRANSMIT						
Clock high to Data bus driven	t_{CLHDA}	491			ns	
Data set-up time	t_{DAVCLH}	488			ns	
Data hold time	t_{CLHDAI}	491			ns	
Clock high to Latch high	t_{CLHLAH}	491			ns	
Latch width 0 and 1	t_{PW01}	491	496		ns	
Latch width 3	t_{PW3}	0·099		12·59	ms	Programmable width
Clock low	t_{CLL}		496		ns	
Clock high	t_{CLH}		496		ns	
Clock high to data line tristate	t_{CLHDAZ}	0		5	ns	
RECEIVE						
Data set-up time	t_{DAVCLL}	14			ns	
Data hold time	t_{CLLDAI}	14			ns	

Table 6 ACEBus Read and Write timings

SynthBus (Note: The SynthBus is not required when the ACE9050 is used as part of the ACE Chipset)

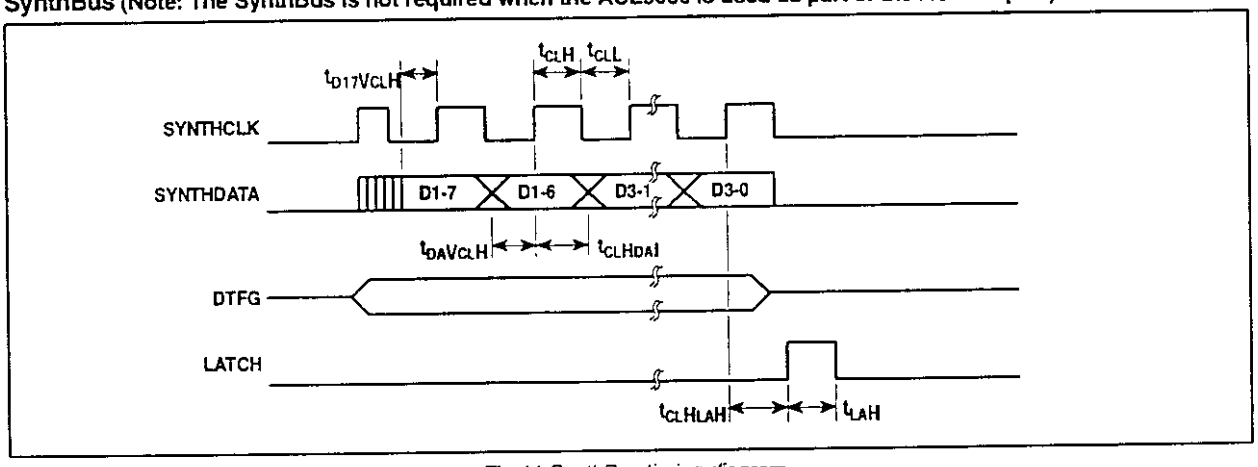


Fig.11 SynthBus timing diagram

SynthBus Timing Cycle Conditions

Input clock frequency, XIN = 8·064MHz. **Worst case Timings:** T_{AMB} = −40°C to +85°C, V_{DD} = +3·6V to +5·5V
Typical timings: T_{AMB} = +25°C, V_{DD} = +3·75V

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
First data bit set-up time	$t_{D17VCLH}$	>0		7·84	µs	
Data bit set-up time (except first)	t_{DAVCLH}		3·9		µs	
Data hold time	t_{CLHDAI}		4·0		µs	
Clock high to latch high	t_{CLHLAH}		4·97		µs	
Latch width	t_{LAH}		952		ns	
Clock low	t_{CLL}		3·99		µs	
Clock high	t_{CLH}		3·93		µs	

Table 7 SynthBus timing

INTERNAL REGISTERS AND RESET STATUS

ACE9050 REGISTERS

Name	R/W	Address	Description	D7-0 reset condition	Notes
IN_PORT1	R	22-23	External IP Port	EE0EEE00	1, 6
OUT_PORT2	R/W	24-25	External OP Port	00000000	
PORT3	R/W	26-27	Internal Port	00000000	2
BARPORT		28-29	Test-Do Not Access		
IRQPRT2	R	2C-2D	Read Int Interrupts	111X111	3, 7
IRQPRT6	R	2E-2F	Read Ext Interrupts	XXXX1111	
MODPRT0	R/W	30-31	Modem	00000000	
MODPRT1	R/W	32-33	Modem	00000000	
MODPRT2	R/W	34-35	Modem	00000000	
KEYP	R/W	36-37	Key Pad IP and Chip ID	0010EEEE	6
LSICOM4	R	3A-3B	ACE Interface RX1	EEEEEEEE	4, 6
LSICOM5	R	3C-3D	ACE Interface RX2	EEEEEEEE	4, 6
LSICOM6	R	3E-3F	ACE Interface RX3	EEEEEEEE	4, 6
PORT4	R/W	40-41	Internal Port	00000010	
PORT5	R/W	42-43	Internal Port	00000011	
BANK_SEL	W	44	Bank Select	XXX00000	7
RESERVED		45	Do Not Access		
BARHIGH	W	50	BAR On	00000000	
BARLOW	W	51	BAR Off	00000000	
BARENABLE	W	52	BAR OE	XXXXXX0	7
BRG	W	53	UART Baud select	XXXXX000	5, 7
I2C_ADDR	R/W	54	I^2C	00000000	
I2C_DATA	R/W	55	I^2C	00000000	
I2C_CNTR	R/W	56	I^2C	00000000	
I2C_STAT	R	57	I^2C	11111000	
I2C_CCR	W	57	I^2C	00000000	
DAC1	W	5B	PWM 1 data	00000000	
DAC2	W	5C	PWM 2 Data	00000000	
LSICOM0	W	60-61	ACE Interface TX1	00000000	
LSICOM1	W	62-63	ACE Interface TX2	00000000	
LSICOM2	W	64-65	ACE Interface TX3	00000000	
LSICOM3	W	66	ACE Interface Control	00000000	
STR_WIDTH	W	67	Latch 3 Width	00000000	
KPOT	W	68-69	O/P type for KPO	XXX11111	7
REWD	W	6A-6B	Reset Watchdog	XXXXXXXX	7
RESAT0	W	6C-6D	Reset Time Out	XXXXXXXX	7
IRQPRT0	W	70-71	Reset Int Interrupts	00000000 (Reset)	
IRQPRT1	W	72-73	Mask Int Interrupts	00000000 (Masked)	
IRQPRT4	W	74-75	Reset Ext Interrupts	XXXX0000	7
IRQPRT5	W	76-77	Mask Ext Interrupts	XXXX0000	7

Table 8 ACE9050 ports

NOTES:

1. Bit 6 is set (1) in SERV mode. Bits 1 and 0 are set (1) if the corresponding interrupt is enabled (inverse of IRQPRT6).
2. Bit 4 (UPOFFN) is set (1) in SERV mode, but reset (0) in Normal mode.
3. Bit 4 is not used and should be treated as undetermined.
4. The LSICOM4, 5 and 6 ports values will depend on the DTFG input.
5. In SERV mode the Boot block will set up BRG to 00000100 (9600 Baud).
6. E = Depends on external input.
7. X = Not used or undetermined.

ACE9050 6303 REGISTERS

Name	R/W	Address	Description	D7-0 reset condition	Notes
DDR1	W	00	Data Dir Register P1	00000000	1
DDR2	W	01	Data Dir Register P2	00000000	1
PORT1	R/W	02	Data Port 1	EEEEEEEE	2
PORT2	R/W	03	Data Port 2	010XXXXX	3, 4
TCSR	R/W	08	Timer Control/Status	00000000	
FRC_HIGH	R/W	09	Free Run Counter MSB	00000000	
FRC_LOW	R/W	0A	Free Run Counter LSB	00000000	
OCR_HIGH	R/W	0B	O/P Compare Reg MSB	11111111	
OCR_LOW	R/W	0C	O/P Compare Reg LSB	11111111	
ICR_HIGH	R	0D	I/P Capture Reg MSB	00000000	
ICR_LOW	R	0E	I/P Capture Reg LSB	00000000	
RMCR	W	10	Rate & Mode Control	XXXX0000	4, 5
TRCSR	R/W	11	Tx/Rx Control and Status	00100000	6
RDR	R	12	Rx Data	00000000	
TDR	W	13	Tx Data	00000000	
RAMCR	R	14	Not Used	00000000	7

Table 9 6303 ports

NOTES:
1. Both ports set to Input (0 = I/P, 1 = O/P)
2. E = external input
3. 6303 internally set to Multiplexed mode
4. X = Unused or undetermined
5. Set to 00001100 in SERV mode
6. Set to 00111010 in SERV mode
7. This register Read only in the ACE9050

MODES OF OPERATION

The ACE9050 has three independent modes of operation: Normal, Emulation, Service.

Mode	Pin	Enabled
Emulation	EMUL	High
Service	SERV	High
Normal	-	Default mode

Table 10 Modes of operation

1, NORMAL MODE

This is intended to be the mode of operation when the ACE9050 is fully commissioned in the application. The internal 6303 Microprocessor is used and the Boot block ensures the program counter goes to the beginning of the ROM code area after initialisation. In Normal mode various blocks can be powered down to save current, and the processor can be programmed to run at 1·008MHz or 2·016MHz.

2. EMULATION MODE

This mode is intended for system and software development work. In Emulation mode the Internal 6303 processor is made redundant and its function is replaced in the system by an external 6303 processor. This is to facilitate using a generic 6303 In-Circuit Emulator (ICE) for software development. Table 11 shows the functionality of external pins that change in this mode. This is to enable all of the internal functions of the ACE9050 to operate as they would in Normal mode. In Emulation mode the external processor or ICE must be set up to operate in Multiplexed mode. This mode is only intended for use at room temperature.

Normal mode			Emulation mode	
Pin	Function	Type	Function	Type
D[7:0]	Data	I/O	Data and A[7:0] I/P	I/O
A[13:8]	Address	O	Address I/P A[13:8]	I
A[15:14]	Not used	I	Address I/P A[15:14]	I
ECLK	6303 Clk	O	ACE9050 Clock I/P	I
R/W	Not used	O	Read/Write strobe	I
AS	Not used	I	Address Latch strobe	I
IRQN	Not used	O	6303 Interrupt	O
ICN	Not used	O	6303 Timer P2 [0]	O

Table 11 Normal and Emulation mode functions

3. SERVICE MODE

This mode is intended for system development and phone service, where reprogramming of a FLASH ROM device is required. The two areas that are affected by Service mode are:

1. The Watchdog and Autonomous Time Out (ATO) resets are inhibited. This is intended for software development work. The POFFN pin (85) is initially programmed to be a 1 by the ROM code in this mode.
2. The internal ROM code facilitates loading of a program into the RAM area from the SCI. This program would normally be a FLASH loading program. The SCI may then be used to load new object code into the FLASH memory of a system.

The ROM code has a time out function so that if a valid start code is not detected on the SCI normal code operation will begin. The ROM code is fully described in the Internal ROM Boot Block section.

4. TEST MODE

Test mode increases the efficiency of volume testing of the part. Pin 1, TESTN, should be hardwired to V_{DD}.

5. POWER DOWN MODES

To reduce overall power consumption, selective power down of various blocks is available under software control. In the power down state each block will go to a predetermined logic state. The following power reduction features are included:

Bus Interface (CSEPN = 1 and Address = 3FFF)
8·064 MHz external Clock Off
1·008 MHz external Clock Off
AMPS/TACS Modem power down
ACE Serial Chip Interface Power down
CPU Sleep Mode
Crystal Oscillator Off
1MHz/2MHz Bus speed

FUNCTIONAL DESCRIPTIONS

1. ACE9050 6303R DESCRIPTION

General Description

The embedded processor in the ACE9050 is functionally equivalent to a generic 6303R micro. This data sheet outlines the functionality of the embedded processor, detailing its operation with the internal peripheral circuitry. It is not intended as a programmers guide for a 6303. If further information is required the following publications are recommended:

HITACHI 8-bit single-Chip Microcomputer Data Book Sept.1989
Motorola Microprocessors Data Manual
Macro Assemblers Reference Manual, Motorola Semiconductors MC68MASR(D).

The 6303 is an 8-bit processing unit which has a completely compatible instruction set with the 6301. It has object code upwardly compatible with the HD6300, HD6801 and HD6802.

The ACE9050 has 6016 bytes of internal RAM (the 6303R has 128 bytes). Other features are: a Serial communications interface (SCI or UART), a 16-bit timer, 8-bit I/O port and a 5-bit I/O port (only 2 are bonded out from the ACE9050). The bus speed can be configured to 1·008 in Normal mode or 2·016MHz in Turbo mode.

The ACE9050 has an Emulation mode whereby its internal 6303 is bypassed and the peripheral functions may be driven externally by a standard 6303 ICE.

ACE9050 6303R Pin Description

The ACE9050 6303 is embedded in a kernel which interfaces to the rest of the circuitry. Table 12 describes the internal connections to the ACE9050 6303. In Emulation mode, none of the output pins drive the internal buses.

Name	I/O	Description
V_{DD}	I	Internal power supply
V_{SS}	I	Internal Ground
XTAL	-	Not connected
External	-	Not Used (System Clock Driven into E directly)
E	I	System Clock IP
NMI	-	Not used: Tied to VDD
IRQ	I	Connected to Interrupt Control block and IRQN pin
RES	I	Connected to Internal Reset MRI
Port2 [0]	I/O*	Internally connected to IFC Counter
Port2 [1]	-	Not connected
Port2 [2]	I/O*	Internally connect to Baud Clk
Port2 [3]	I/O	External Pin (SCI I/P or Port2)
Port2 [4]	I/O	External Pin (SCI O/P or Port2)
Port1 [7:0]	I/O	External Pin (Port1 I/0 Access)
Addr [15:8]	O	Connected to internal address Bus
D/A [7:0]	I/O	Internally connected to Buses
R/W	O	Connected to internal logic and R/W pin
AS	O	Connected to internal logic
STBY	-	Standby mode disabled = V_{DD}

*Port2 bits 0 and 1 must be configured as inputs in the 6303 to use the IFC and Baud rate generator functions.

Table 12 Generic 6303 I/O mapping

clocks.

Clock

The CPU Clock is provided from the Clock Generator Circuit in the ACE9050. This clock is either 1·008MHz or 2·016MHz. It is not further divided down in the 6303, so this clock frequency is the same as the processor bus speed. Refer to the Clock Generator section for details of how to configure the internal

Port 1

This is an eight bit I/O port with the direction of each bit being defined by the data direction register DDR1 as given in Table 13. The Port can be accessed for read and write via the Port1 register. The output buffers have tristate capability, being high impedance when used as inputs. When the processor is reset these are high impedance. Two pins (Bits 3 and 4) associated with this port are also used as I/0 from the I^2C interface on the ACE9050. This is configured by Port 5 bit 2. The 6303 is internally configured to mimic Multiplexed mode of operation, so this port cannot be configured to output the lower address bits. The ACE9050 has dedicated pins for this purpose.

Associated Registers

Name	Description
DDR1 Bits [7: 0]	1: Sets corresponding Port line to output 0: Sets corresponding Port line to input
Port 1 Bits [7:0]	Read and Write access to Port 1

Table 13 Port 1 associated registers

Port 2

This is a five-bit I/O port with the direction of each bit being defined by the data direction register DDR2. Only bit 3 and bit 4 are connected to external pins. This allows access to the I/O port and Serial Interface functions. Bit 0 and bit 2 are internally connected to the IFC and Baud clock. They must be configured as inputs to use these functions. Bit 0 and bit 2 are not externally accessible.

The ACE9050 has an additional Output Port 2, which is separate from the 6303 Port 2.

Associated Registers

Name	Description
DDR2* Bits [4:0]	1: Sets corresponding Port line to output 0: Sets corresponding Port line to input
Port 2* Bits [4:3]	Read and Write access to Port 2

*The TRCSR register overrules these registers.

Table 14 Port 2 associated registers

Programmable Timer

The ACE9050 6303R contains a 16 bit programmable timer which may measure the period of an input waveform, as with a standard 6303R. This counter runs from the ECLK. The counter cannot generate an output waveform. The input to the timer is internally connected to the IFC counter for the AFC loop function. The timer hardware consists of an 8-bit status and control register, a 16-bit free running counter and a 16-bit input capture register.

TCSR (Timer Control and Status Register)

The Control and Status register has three flags: Input capture, Output Compare Match and Timer Overflow. Each flag has an associated interrupt enable. The other two bits in the register are for control of the output level and input edge select. The bits are described in Table 15.

Bit	R/W	Name	Description
7	R	ICF	Transition of appropriate type occurred on input (ICN). Cleared by read of Input Capture register
6	R	OCF	Match between Free Running Counter and Output Compare Register*
5	R	TOF	Timer overflow. Cleared by read of counter.
4	R/W	EICI	Enable an ICF interrupt
3	R/W	EOCI	Enable an OCF interrupt*
2	R/W	ETOI	Enable Timer overflow interrupt
1	R/W	IEDG	0 = Negative edge on ICN trigger ICR 1 = Positive edge on ICN trigger ICR
0	R/W	OLVL	Output level*

*As the timer cannot generate an output these bits are considered non-functional in the ACE9050.

Table 15 TCSR bit descriptions

FRC: Free Running Counter

The FRC is a 16-bit ReadWrite counter; Data can be read from or written to it. The register has extra hardware to load and save both bytes of the counter simultaneously when a double byte store instruction is used. The counter is incremented by the processor clock. Reading from the counter does not affect it.

ICR: Input Capture Register

The ICR is a 16-bit Read register which holds the value of the Free Running Counter when a transition is detected on ICN, i.e. the IFC Counter Output.

Serial Communication Interface (SCI or UART)

The processor contains a full-duplex asynchronous Serial Communications interface. It consists of a transmitter and receiver which operate independently but with the same data format and rate. Both parts communicate with the CPU via the data bus and to the outside world via Port 2. Interrupts generated can be individually masked. The receiver can be sent to 'sleep' by software. No receive interrupts are generated during a message in this state. The Baud rate can be generated within the ACE9050 6303 or the ACE9050 can provide a baud rate generator and selection register external to the processor block. This allows the following standard baud rates to be programmed: 600,1200. 2400, 4800 or 9600.

The hardware consists of four registers: an 8-bit control/status register, 4-bit mode select, an 8-bit receive data and an 8-bit transmit data register.

Bit	R/W	Name	Description
7	R	RDRF	RX Data Register Full*
6	R	ORFE	Overrun/Framing Error*
5	R	TDRE	TX Data Register Empty
4	R/W	RIE	RX Interrupt Enable: Enables an interrupt for both Bit 7 and Bit 6
3	R/W	RE	RX Enable. This sets Port2 bit 3 to Input regardless of the DDR2
2	R/W	TIE	TX Interrupt enable: Bit 5 will generate an Interrupt
1	R/W	TE	TX Enable: This sets Port2 bit 4 to Output regardless of DDR2
0	R/W	WU	Wake Up: Set by software and cleared by hardware.**

* Overrun is where new data is placed in the Receive register before the old data has been read. Framing Error is where the bit counter is not synchronised with the boundary of the byte in the Received bit stream defined in Table 17.

** The Wake Up mode is intended for systems where more than one Processor is on the UART link, and is addressed by the first byte of data. If the address is incorrect the processor can disable the interrupts and effectively ignore the word.

Table 16 TRCSR: Transmit/Receive Control Status Register bit descriptions

Condition	Bit 7	Bit 6
No Data	0	0
Good Data RX	1	0
Framing error	0	1
Overrun error	1	1

NOTE:
Bits 7 and 6 are cleared by reading the Status register, followed by reading the Received Data register

Table 17

RMCR Transfer Rate/Mode Control Register

The mode select register controls the clock source and set-up. This is a write-only register. The processor can use an internally divided down processor clock to give the Baud clock. The Baud rate division ratio can be set to a value from 16 to 4096. However, this could lead to non-standard Baud rate generator.The bit functions of this register are described in Table 18.

Bits	Value	Description
[7: 4]	XXXX	Not used
[3: 2]		**Clock Control mode**
	00	SCI disabled
	01	Use processor Clk for Baud rate
	10	Not used
	11	Use ACE 9050 Baud rate generator
[1: 0]		**Speed Select (Bits 3: 2 = 01)**
	00	E÷16
	01	E÷128
	10	E÷1024
	11	E÷4096

Table 18 RMCR Transfer Rate/Mode Control register

Bits	Description
[7:0] (Data)	**RDR: Received Data Register** Read received bits. First bit received is placed in bit 0, last in bit 7
[7:0] (Data)	**TDR: Transmit Data Register** Write register to store bits before serial transfer from Transmit shift register, bit 0 first

Table 19 Receive and Transmit Data registers

In Normal Mode the SCI should be initialised before operation. This means writing to the mode select and the control/status register. In Service Mode the SCI is configured for 9600 baud, and the receive interrupt enabled. When the transmitter is first initialised it will send a ten-bit preamble of '1's before being ready to transmit data.

Once initialisation is complete data transmission enabled by writing to the transmit data register. TDRE is set to 0. A start bit is transmitted (0). Next the eight bit data starting at bit0 are transmitted followed by a single stop bit (1). The hardware sets the TDRE bit in the TRCSR register. If the CPU does not transfer another word the output goes high.

The receiver is configured during initialisation. If enabled and a start bit is detected (0), the next nine bits will be sampled approximately at the centre of each bit. If the ninth bit is a 1 the data is transferred to the Receive data register. The RDFR bit is set in the TRCSR register. If the ninth bit is not a 1 or the receive data register is full then the ORFE bit is set to indicate an error. A read of the TRCSR register followed by a read of the Received data register (RDR) will clear these flags.

RAM Control Register (RAMCR)

This register is read only in the ACE9050. Bit 6 (RAME) is set to zero: this is because the RAM on the ACE9050 is external to the 6303 block. Bit 7 (STBY) is also set to zero by the ACE9050 because Standby mode is not supported.

Operating Modes

The Generic 6303R has two modes: Multiplexed and non-Multiplexed, where the mode is selected externally using P2[0], P2[1] and P2[2]. This is not required on the ACE9050, where the mode is set to mimic multiplexed internally when the reset (MRN) is released . The ACE9050 processor has two fundamental modes of operation: Emulation and Normal, which are described in the MODES OF OPERATION section.

Low Power Consumption Modes

The generic 6303 Standby mode is not supported by the ACE9050 6303. The STBY pin is not accessible. The Sleep mode is fully supported by the ACE9050 6303. This mode is entered by execution of the SLP instruction. Escape is via an interrupt or reset .

Address, Data and Memory Control

The Address, Data and control lines from the ACE9050 6303 connect to a kernel which interfaces to the on chip bus structures. The Bus Interface block provides suitable buffering to drive required buses externally, and configure the I/0 for Emulation mode.

Interrupt Processing

The interrupt processing in the ACE9050 6303 is essentially the same as a generic 6303, the exception being NMI, which is not available. The IRQN is internally connected to the I^2C interrupt, the External Interrupt and the Internal interrupt blocks.

These blocks combine all the possible sources for interrupts into one line which is connected to IRQN. This is also connected to a pin for use in Emulation mode. The IRQN is maskable. The interrupt mask bit in the Condition Code Register must be zero for the CPU to respond to the Interrupt request, as with a generic 6303.

The Interrupt Vector Memory map is shown in Table 20.

Priority	Vector		Interrupt
	MSB	LSB	
1	FFFE	FFFF	RES
2	FFEE	FFEF	TRAP
3	FFFA	FFFB	Software Interrupt (SWI)
4	FFF8	FFF9	IRQN
5	FFF6	FFF7	ICF (Timer Input Capture)
6	FFF4	FFF5	OCF (Timer OP Compare)
7	FFF2	FFF3	TOF (Timer Overflow)
8	FFF0	FFF1	SCI (UART)

Table 20 Interrupt vector memory map

Error Processing

An interrupt is generated when an undefined op-code is fetched, or when an instruction is fetched from an impossible address. This is in the range 0000-007F for the ACE9050 (0000-001F for a standard 6303).

2. INTERNAL ROM BOOT BLOCK

The ROM code provides a boot block for the ACE9050. Following a reset condition code execution will always start in the internal ROM. The internal ROM data flow depends on the condition of the SERV Input and thus the mode of operation of the ACE9050. The operation flow of the IROM is shown in Fig. 12 and described in the following sections:

Normal Mode

1. Read serial data on ACEBus DTFG line
2. Configure ACE9030 Reference dividers via ACEBus.
3. Set the program counter to the beginning of external ROM (1800_H).

Service Mode

1. Read serial data on ACEBus DTFG line
2. Configure ACE9030 Reference Dividers via ACEBus
3. Configure the UART to RX
4. Wait 2 seconds for special code on UART - if not found go to step 3 of Normal Mode
5. Load Data from UART into RAM

6. Pass control to Program loaded in RAM
7. Map Interrupt Vectors to RAM space.
8. The RAM program can then Program a FLASH memory via the UART.

Steps 1and 2 - Both Modes

The ACE Chipset offers the flexibility of using one of three different crystal frequencies: 12·8, 14·85 or 15·36 MHz. The chosen crystal can be used to generate all the system clocks and local oscillator frequencies required in a cellular phone application. The ACE9050 must detect what crystal is being used and set up the correct value for the OSC8 dividers in the ACE9030. This is handled in the Internal ROM. Upon Reset the ACE9030 sets the OSC8 for a 15·36 MHz Crystal, so the ACE9050 is not clocked faster than 8·064 MHz.

The system designer must set up the DTFG input (the Radio Serial Interface, pin 82), using an external resistor of approximately 10kΩ. The crystal frequency determines where the resistor is terminated, as shown in Table 21. Upon reset the ACE9050 Internal ROM reads the DTFG input and programs the ACE9030 OSC8 accordingly.

Crystal	Serial Data RXed	Resistor from pin 82 to:
12·8MHz	000000	V_{SS} (Gnd)
14·85MHz	0 < Data < FFFFFF	A1 (pin 31)
15·36MHz	FFFFFF	V_{DD}

Table 21

Step 3 - Normal Mode

Program code in the external EPROM at address 1800_H is started. The Internal ROM resides at the top of the processor address space $FE00_H$ - $FFFF_H$. Obviously the main program requires access to this space for Interrupt vectors. The Internal ROM is deselected by setting PORT4 [1] to zero. It is recommended that any external program does this quickly and always before enabling any Interrupt sources.

Step 3 - Service Mode

The Internal ROM will initialise the 6303 SCI (UART) and set up the Baud rate generator to 9600 Baud. The SCI is initialised to the following:

Receiver On
Transmitter ON
Receive Interrupt enabled
9600 Baud rate from ACE9050 Baud Rate Generator

The Receive interrupt will remain enabled after the IROM code execution. The UART is always configured for 8-bit data transfer, no parity and one stop bit.

Steps 4, 5 and 6 - Service Mode

When in service mode the ACE9050 can download a program from the SCI to RAM. To achieve this the first code (start code) must be sent down to the SCI within 2 seconds of releasing Reset. The boot block code will write the subsequent code into RAM. Two code formats are supported:

(a) Motorola S- Record format
(b) Binary dump

(a) Motorola S-Record Format

The start code for this format is 'OA' in ASCII (i.e. 30_H, 41_H).

s0nnppppxxxxxxxxxcc — First Record in file
s1nnppppddddddddddddcc — Data record with 16-bit address
.
.
s9nneeeecc — End of file record (nn = 3)

where:

nn = Number of bytes (xx+pp+dd+cc) in record.
pppp = Load address
dd = data bytes, 1 to 16
xxxx = Name of program (ASCII coded)
eeee = Program entry address
cc=checksum calculated from [255−sum(pp)+sum(dd)+ sum (xx)+sum (ee)+nn)] MOD 256

When the 's9' is read in from the End of File Record, the code will jump to the reset vector. This is mapped to 0FFE by the IROM. The RAM program will then begin execution as for a reset. The last 6 characters of the record file (nneeeecc) will be received while the program is running.

(b) Binary dump file

This format is for the binary representation of the code, not a proprietary binary format code. The start code for this format is 'OB' ASCII (ie 30_H, 42_H) . First two bytes are the start address pointer.

The next two bytes are the end address pointer+1. The next bytes are the data bytes. These are loaded consecutively from the start to the end address. When the last data byte is received the program counter will go to the loaded code start address pointer.

Step7-Interrupt Vector table

The Internal ROM will map the 6303 Interrupt vector table to an address space in RAM so the loaded program can deal with interrupts as shown in Table 22. In general only the SCI interrupt is required for a Flash Loading program.

Vector address	Interrupt
0FFE	Reset
0FEE	Trap
0FFC	Not Implemented
0FFA	SWI Software interrupt
0FF8	IRQN
0FF6	ICF Timer Input compare
0FF4	OCF Timer Output compare
0FF2	TOF Timer overflow
0FF0	SCI

Table 22

RAM Area Reserved for IROM Operation

The IROM code itself requires a small amount of RAM during its operation. This area must not be used for storage of the RAM program.

RAM Reserved area: 080_H to 100_H

Fig. 12 shows the data flow for the internal ROM.

3. DECODER

The Decoder logic creates the memory map for system containing the ACE9050. Internally, it maps the ACE9050 registers, RAM and ROM onto the System Memory map. External ROM is also mapped onto the available address space by the Decoder, but the situation can be complicated by the Bank Address switching circuitry. Refer to Table 23 on the following page for details of memory mapping.

Note that the ACE9050 contains Memory Banked Switching circuitry. Refer to the section 4 'BUS INTERFACE AND MEMORY BANKING' below for details.

The Decoder also creates suitably timed Output Enable and Write Enable signals (refer to Figs. 4 and 5) for parallel read and write cycles to external devices.

Address (hex)	Description
0000-001F	6303 Registers
0020-007F	Internal ACE9050 Registers
0080-17FF	RAM
1800-7FFF	Non Banked external ROM
8000-BFFF	Banked external ROM
C000-FDFF	Non-Banked external ROM
FE00-FFFF	Internal / External ROM

Table 23

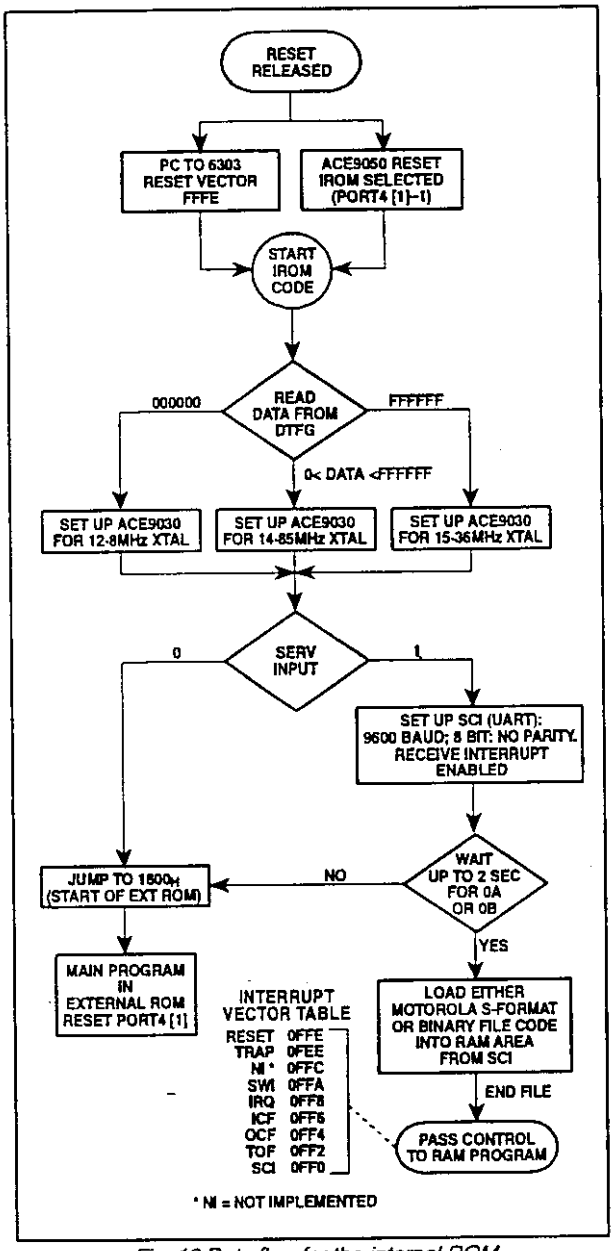


Fig. 12 Data flow for the internal ROM

External Pins

OEN Output Enable, active low (pin 26)
This signal is used when accessing external memory or other suitable devices. Driving the Output Enable input of external memory reduces the possibility of data bus contention conditions.

WEN Write Enable, active low (pin 27)
This output is used to latch data into external memory or other suitable devices.

Associated Registers

IROM Port 4 bit 1

The ACE9050 internal ROM (IROM) is mapped to the top 512 bytes of the address space allowing it to provide interrupt handler routines. Upon reset the IROM select is enabled. It can and should be disabled by software before the interrupts are enabled.

Bit 1	Description
IROM	Address range $FE00_H$-$FFFF_H$: 0 = External ROM 1 = Internal ROM (reset state)

Table 24

SLEEP Port 3 Bit 1

If this bit is enabled then the CSEPN will become inactive during periods when the 6303 is in Sleep mode. When the 6303 Sleep mode is activated, the processor puts $FFFF_H$ on the address bus. The Decoder simply does not activate CSEPN for this address when the SLEEP bit is enabled.

Bit 1	Description
SLEEP	Address $FFFF_H$: 0 = CSEPN active 1 = CSEPN inactive

Table 25

4. BUS INTERFACE AND MEMORY BANKING

The Bus interface logic is responsible for the following:

1. External Interface to ACE9050 Data and Address buses
2. Creating 2 chip selects for external memory parallel devices.
3. The logic for the external banked addressing
4. Emulation Mode: External control of internal buses

Fig. 13 is the block diagram of the circuit. The ACE9050 memory interface can operate at a lower supply voltage than the rest of the chip. This allows the use of low voltage memory parts. The memory interface pads use a separate supply rail, which is connected to V_{DDM}.

External Pins

EMUL Emulation mode (pin 83)
This input changes the function of the external data and address buses. In Emulation mode (EMUL = 1), the internal Address and Data buses are constructed from external stimuli and not the internal 6303.

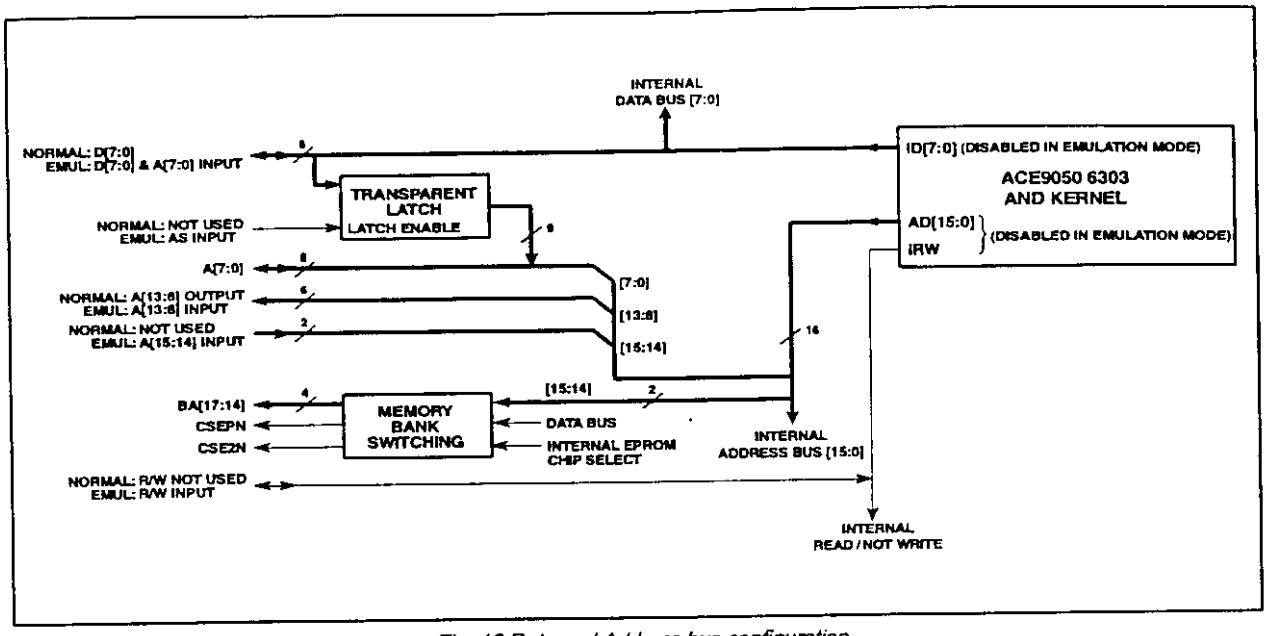


Fig. 13 Data and Address bus configuration

AS Address Strobe (pin 5)
This input is used in Emulation Mode only. Th external D [7:0] will contain both data and the lower 8 bits of the address bus. The Bus Interface provides the transparent latch required to hold the value of the address during the latter part of the cycle. The AS is provided to control the Latch Enable. In a typical system this will be directly connected to the emulating 6303 AS output.

R/W Read/Not Write (pin 95)
This is an output in Normal mode, but an input in Emulation Mode. It is the processor Read/Not Write line. The timing of this output is not guaranteed to be the same as a standard 6303 processor. In Emulation mode it will be directly connected to the Emulating 6303 R/W line.

D [7:0] Data (and Address in Emulation mode) (Pins 18-25)
In Normal mode these pins provide bidirectional data transfer between the ACE9050 6303 and external memory. In Emulation mode they provide the directional data and the lower 8 bits of the address bus into the ACE9050.

A [7:0] Lower 8 address bits (Pins 40, 39, 35-30)
These outputs provide the lower 8 bits of the address bus for external memory. This is the case for both Normal and Emulation modes.

A [13:8] Address Bits 13 to 8 (pins 46-41)
In Normal mode these provide the output of the ACE9050 6303 address bus bits 13 to 8, for addressing external devices. In Emulation mode, A[13:8] provide input for an external 6303 address bus, to address the ACE9050 functions excluding the 6303.

A [15:14] Emulation Address bits 15 and 14 (pins 92 and 93)
These inputs are only used in Emulation mode. The internal 6303 address A[15:14] are fed to the banked address logic and not to an external pin. In emulation mode the host processor must drive the complete 6303 internal address bus so A[15:14] inputs are provided. The host processor will then drive the entire internal bus and the bank select register, so the external memory access will be the same regardless of Emulation or Normal mode.

BA [17:14] Banked address (pins 50 to 47)
The ACE9050 expands the external address bus to 18 bits. This allows up to 256K of memory space. BA [17:14] are the outputs from the bank select register. The operation of the refister is described further in 'Memory Map and Banked Addressing', below.

CSEPN Chip Select (pin 28)
This output provides active low chip select for accessing external program memory. On reset the entire external memory address space is mapped to CSEPN. In the Banked area of the memory map the programmer can select either CSEPN or CSE2N access via bit 4 of the Bank Select register.

CSE2N Chip Select (pin 29)
This output provides an active low chip select for accessing external memory or other suitable device. In the Banked area of the memory map the programmer can select either CSEPN or CSE2N access via bit 4 of the Bank Select register.

V_{DDM} Supply to Memory Interface (pin 38)
The power supply pin for the memory interface, V_{DDM}, provides the power supply for the following pads:

A [13:0], BA [17:14], D [7:0], CSEPN, CSE2N, WEN and OEN

Memory Map and Banked Addressing

The ACE9050 provides the circuitry to create a banked addressing system which will increase the size of the programming space from 16 bit (64K bytes) to 18 bit (256K Bytes) and enable two Chip Select lines to be programmed. This is achieved using an internal register to select the required page of memory and chip select line.

The use of banked addressing and associated circuitry is not mandatory in a system using an ACE9050.

When using banked addressing the external addresses generated and thus the system memory map are different from the 6303 memory map. The banked addressing functions in the same manner for both Normal and Emulation mode with a external processor.

Associated register

BANK_SEL: Bank Select register (Write only)

Bit	Name	Description
[7:5]	-	Not used
4	CS	Chip Select: 1 = CSE2N 0 = CSEPN
3	BA 17	Banked Address A17 (see Table 27)
2	BA 16	Banked Address A16 (see Table 27)
1	BA 15	Banked Address A15 (see Table 27)
0	BA 14	Banked Address A14 (see Table 27)

Table 26

Bank_Sel 3:0	Page Base Address (Hex)	Bank_Sel 3:0	Page Base Address (Hex)
0000	00000	1000	20000
0001	04000	1001	24000
0010	08000	1010	28000
0011	0C000	1011	2C000
0100	10000	1100*	30000
0101	14000	1101*	34000
0110	18000	1110*	38000
0111	1C000	1111*	3C000

*Refer to System Memory Map section for more details

Table 27

The banking is configured to occupy a 16K byte area of the processor memory address space. It will thus create 16K byte pages. This is configured in hardware and cannot be altered. It is achieved by decoding the upper 2 bits of the processor Address bus. If the address is in the range 8000_H to $BFFF_H$ which corresponds to A[15:14] = 10, the bank select circuit is invoked. The bank addressing circuit only affects the upper four bits of the external data bus. The top two A[17:16] are completely new, and the next two A[15:14] are replacements for the processor A[15:14] bits. Fig. 14 is a block diagram of the Bank Select circuitry.

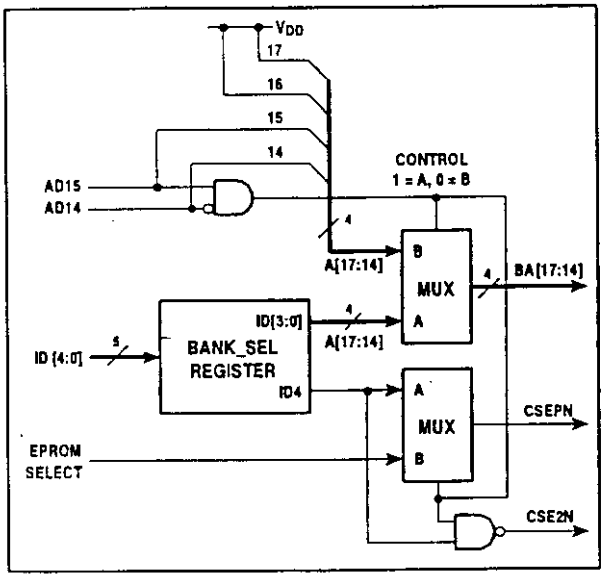


Fig. 14 Banked Addressing block diagram

The processor memory map is thus split into two distinct areas: Non Banked address (Root) and Banked address:

Non Banked address area (Root)

A[17:14]: The address lines A[17:16] are set to 11. The address lines A[15:14] are identical to the corresponding processor address lines. This means the original area of the processor memory map is mapped to the top of the external memory address space.

CSE2N is never active, regardless of the value of the Bank_Sel register bit 4. All access will be with CSEPN.

Banked Address area: A[17:14]

These address lines are the same as Bank Sel register bits [3:0]. The programmer can in theory select up to 16 pages. This is discussed in more detail in System Memory Map section.
CSE2N: The BANK SEL bit 4 determines whether this Chip select line is enabled or the CSEPN.

Table 28 summarises operation in the two areas.

Address area	A[17:16]	A[15:14]	Chip Select
Non-Banked	Set to 11	Same as Micro	Always CSEPN
Banked	Bank Select register bits [3:0]		Bit 4

Table 28

Banked Address System Memory Map

The processor and the system memory map become different because of the memory banking. The system memory map is spit into 16K pages and the original processor Memory map re-targeted. Refer to Fig. 15.

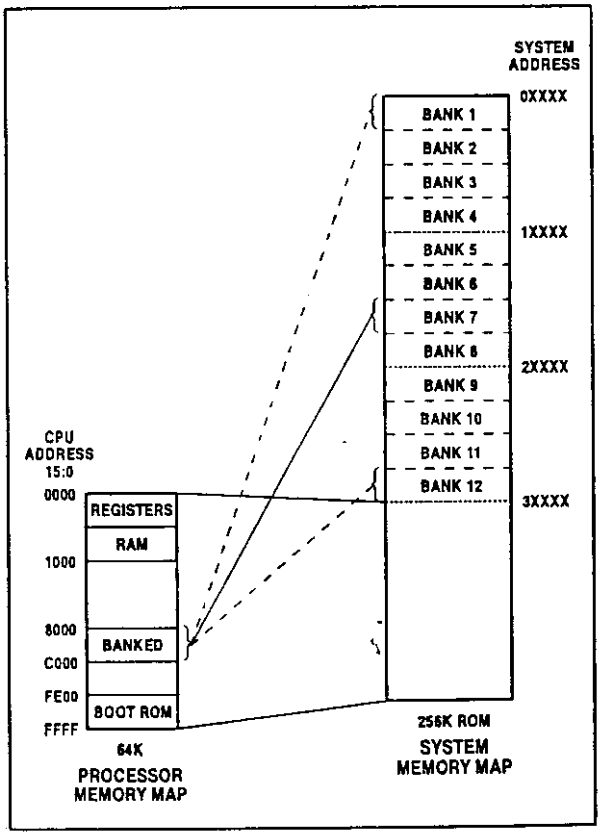


Fig. 15 Memory Map and Banked Addressing

The page addressing can access up to 16×16K pages per Chip Select line in theory; however the original 6303 memory map must also reside in the 256K of CSEPN memory space. This is put to the top of the system memory map by the ACE9050 and represents Pages 13 to 16. So, for example, the 6303 address range $C000_H$ to $FFFF_H$ will access the same memory location as 8000_H to $BFFF_H$ with the bank select register set at $0F_H$. This is useful when programming a FLASH memory device, but care must be exercised in the addressing of run time code. For the top four pages the system designer must decide whether to access the area via its page address or its direct (Root) address. For the original 6303 4 pages:

Page 1 (0000_H-$3FFF_H$) = Page 13 (30000_H-$33FFF_H$)
This must be used for ROOT ROM, as the code will jump to 1800_H after reset. This means the bottom 6K of the page (0000_H-$17FF_H$) cannot be used unless it is accessed via its banked address. It does allow the maximum possible (42K) memory area to be configured as Non Banked.

Page 2 (40000_H-$7FFF_H$) = Page 14 (340000_H-$37FFF_H$)
This page can either be used as Root, or banked.

Page 3 (8000_H-$BFFF_H$) = Page 15 (38000_H-$3BFFF_H$)
This page is banked by definition.

Page 4 ($C000_H$-$FFFF_H$) = Page 16 (30000H-$3FFFF_H$)
The final page could either be accessed via it banked address or Root address, however as this contains the Interrupts it must be Root.

The designer can also allocate any of these or further shadowed 16 pages to the CSE2N chip select. It is up to the system designer whether to use unique pages for CSE2N or shadow a ROM (CSEPN) page .

5. INTERRUPTS

The ACE9050 contains one internal interrupt port, one external interrupt port and one I²C interrupt. This expands the one 6303 maskable interrupt (IRQN) into eight internal and two external interrupts. The Interrupt control logic enables masking, reading and resetting of the potential interrupt sources. Three registers are associated with each of the two interrupt control ports, IRQPRT 0, 1 and 2 for internal and IRQPRT 4, 5 and 6 for external interrupts. Each Interrupt control port will generate an Interrupt request line, as will the I²C interrupt. These three lines are NORed together to produce the 6303 IRQN input. Fig. 16 is a block diagram of the Interrupt Section.

If a source is not masked an interrupt will be generated and the corresponding bit set in the Interrupt register. If it is masked no interrupt will be generated and the correspondincg bit will not get set in the interrupt register. Once an interrupt is generated, it can be read in IRQPRT2, 6 or the I²C section. If both internal and external interrupts are enabled the processor must read both IRQPRT2 and 6; however, if only external or internal interrupts are enabled the software need only read th corresponding register. To reset the interrupt, a write to IRQPRT0 or 4 is required with the correspondin bit set to 0. The interrupts sources are not prioritised in the ACE9050. Handling the I²C interrupt is covered separately in the I²C Interface description, Section 10.

Masking Interrupts

The IRQN input to the 6303 is a level sensitive maskable interrupt line. This means that it is possible to enable and disable all interrupts from the ACE9050 in the 6303. This is useful to avoid nested interrupt situations.

If several interrupts are unmasked in the ACE9050, the interrupt handler routine can disable all interrupt when it is dealing with an interrupt via the 6303. If another valid interrupt occurs during this time the IRQN line will be driven low by the ACE9050. When the IRQN is enabled in the 6303 at the end of processing, the first interrupt the 6303 will detect low IRQN line and re-enter the interrupt handler routine. This will continue until all pending interrup have been serviced when the IRQN line will remain high. If more than one pending interrupt occurs the software can prioritise its response, by the way the interrupt handler is written.

The later interrupts must not be cleared in IRQPRT0, 1, 4 or 5 by the software until they have been serviced. The ACE9050 will not detect more that one pending interrupt from a given source, i.e. it will not tell that two IRQ-WS have been missed, only that an IRQ-WS interrupt has occured.

Internal Interrupt Control Port

The internal interrupt control port facilitates resetting, masking and reading of seven potential internal interrupt sources via three registers. Table 29 describes the possible sources.

Bit	Name	Description
7	IRQ-TX	Modem: Data Transmitted
6	IRQ-WS	Modem: Received Word synchronisation sequence
5	IRQ-BI-SAT	Modem: Busy Idle bit or SAT updated
3	IRQ-RX	Modem: Rx Data registers updated
2	IRQ-REC	ACE Serial Interface Received data
1	IRQ-SEND	ACE Serial Interface Sent data
0	IRQ-TO	Time Out (ATO expired)

Table 29 Internal interrupt sources

Associated Registers (Table 30)

IRQPRT0: Internal Interrupt Reset Register
Writing a zero in a data bit of this register will reset the corresponding interrupt source.

IRQPRT1: Internal Interrupt Mask Register
A write to this register will determine the possible source of interrupts. At reset all interrupts are masked

IRQPRT2: Internal Interrupt Read register
A Read from this register will determine the interrupts source.

IRQPRT0

Bit	Name	Description
[7: 0]	Reset	0 = Reset 1 = No change

IRQPRT1

[7: 0]	Mask	0 = Reset and masked 1 = Enabled

IRQPRT2

[7: 5]	Source	0 = Interrupt 1 = No Interrupt
4	-	Should be masked
[3:0]	Source	0 = Interrupt 1 = No Interrupt

Table 30

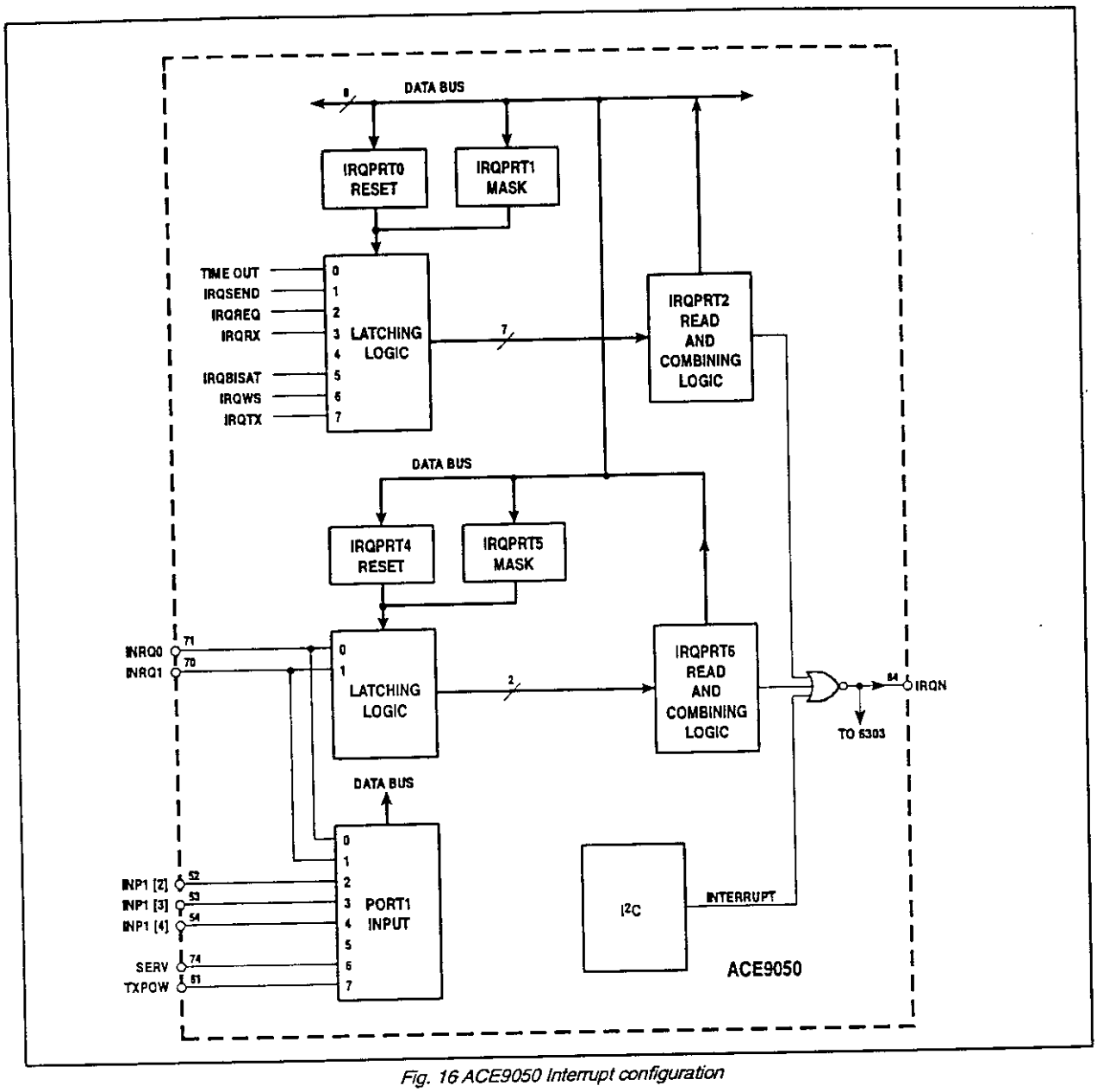


Fig. 16 ACE9050 Interrupt configuration

External Interrupt Control Port

The external interrupt control port facilitates resetting, masking and reading of two potential external interrupt sources via three registers. The external interrupt inputs are edge sensitive. Table 31 describes the possible sources

Bit	Name	Description
1	INRQ1	External Interrupt 1 (INRQ [1])
0	INRQ0	External Interrupt 0 (INRQ [0])

Table 31

External pins

INRQ0 (pin 71)

A rising edge (zero to one transition) on this line will generate an INRQ0 interrupt if the associated bit in the mask register is set to 1. The level of this input can also be read via Port1 bit 0 regardless of whether an interrupt is generated.

INRQ1 (pin 70)

A rising edge (zero to one transition) on this line will generate an INRQ1 interrupt if the associated bit in the mask register is set to 1. The level of this input can also be read via Port1 bit 1 regardless of whether an interrupt is generated.

Associated Registers (Table 32)Bit7: 0

IRQPRT4: External Interrupt Reset Register. A write to this register will reset the interrupts corresponding to 0 written in the data field.

IRQPRT5: External Interrupt Mask Register. A write to this register will determine the possible source of interrupts. After reset all interrupts are masked.

IRQPRT6: External Interrupt Read register. A Read from this register will determine the interrupts source.

Bit	Name	Description
[1: 0]	Reset	**IRQPRT4** 0 = Reset 1 = No change
[1: 0]	Mask	**IRQPRT5** 0 = Masked 1 = Enabled
[1: 5]	Read	**IRQPRT6** 0 = Interrupted 1 = Not Interrupted

Table 32

6. EXTERNAL PORTS AND MULTIPLEXER

The ACE9050 contains 2 external ports, addition to the 6303 Port1 and Port2 which a described in section 1 'ACE9050 6303R Description'. One of the ports is an input register (IN_PORT1), the other an output (OUT_PORT2). Both are 8-bit, but not all bits are accessible from outside the ACE9050.

Two bits from OUT_PORT2 are fed to a multiplexer. This enables multiple functions to share the same external pin, thus reducing the overall pin count. The functions multiplexed with the port are the Pulse Width Modulators and the ACE serial Interface Latch2. Selection is made via the ACE9050 control Port 5.

Further I/O capability can be obtained by using the Keypad interface as standard ports. This is described in the 'Keypad Interface' section of the data sheet.

External Pins

INPUTS

INRQ1, INRQ0: External Port and Interrupt Input (pins 70 & 71)
The logic level of these external inputs are read via IN_ PORT1[1:0], regardless of whether these inputs are configured to generate interrupts or not.

INP1[4], INP1[3], INP1[2]: External Port Inputs (pins 54,53,52)
Uncommitted input. The logic level of these pins can be read via IN_PORT1[4:2].

SERV: Service Input (pin 74)
The state of the mode select line SERV can be read by software via IN_PORT1. The function of SERV is described in 'Modes Of Operation' section.

TXPOW: Power Detect input (pin 61)
The TXPOW input goes to the Watchdog and ATO block, refer to 'Autonomous Timeout' section for more details. The state of the input can be read via IN_PORT1.

OUTPUTS

OUTP2 [0]/CPUCL OUT_PORT2[0] or CPUCL Clock (pin 94)
When the CPUCL Clock Output is disabled in the Clock Generator this pin is driven by the OUT_PORT2 [0]. Refer to 'Clock Generator' section for details of the CPUCL function.

OUTP2 [1]/PWM1 (pin 98)
This pin can be either be driven from OUT_PORT2[1] or the Pulse Width Modulator 1. The selection is made via Port5[0].

OUTP2 [2]/PWM2/Latch2 (pin 81)
This pin can be driven from: OUT_PORT 2[2], Pulse Width Modulator 2 or ACE Serial Interface Latch2. The selection is made via Port 5[5:4].

OUT 2[6] (pin 76), **OUT2[7]** (pin 79)
Output pins High Current inverting output pins. May be used for LED or backlight drivers. Their state is set up via OUT_PORT2. Upon reset OUT_PORT 2[7:6] are reset low. Due to the inverting nature of the outputs this means OUT 2[7] and OUT 2[6] are high.

Associated Registers

IN_PORT1: ACE9050 Input Port: Read Only

Bit	Name	Description
7	POWDET	Logic Level of TXPOW Input pin
6	SERV	Logic Level of SERV Input pin
5	-	Read back as 0
4	INP1 [4]	Logic Level of INP1 [4] pin
3	INP1 [3]	Logic Level of INP1 [3] pin
2	INP1 [2]	Logic Level of INP1 [2] pin
1	INRQ1	Logic Level of INRQ1 pin
0	INRQ0	Logic Level of INRQ0 pin

Table 33

OUT_PORT2: ACE9050 Output Port: Read and Write

Bit	Name	Description
7	OUTP2 [7]	High Current Inverting O/P*
6	OUTP2 [6]	High Current Inverting O/P*
5	OUTP2 [5]	Set to 0: Not used
4	OUTP2 [4]	Set to 0: Not used
3	OUTP2 [3]	Set to 0: Not used
2	OUTP2 [2]	O/P to multiplexer with PWM2 and Latch2)
1	OUTP2 [1]	O/P to multiplexer (with PWM1)
0		O/P when CPUCL disabled

*On reset, these bits are set low and the corresponding output pins driven high.

Table 34

PORT5 [5:4]: OUTP2.2_SEL

Bit 5	Bit 5	OUTP2 [2]/PWM2/LATCH2 pin function
0	0	OUT_PORT2 [2] (Reset state)
0	1	Pulse width modulator 2
1	0	ACE Serial Interface Latch 2
1	1	Not valid

Table 35

PORT5 [0]: PWM 1 MUX

Bit 0	OUT2 [1]/PWM1 pin function
0	Pulse width modulator 1
1	OUT_PORT2 [1] (Reset state)

Table 36

7. CLOCK GENERATOR

The AC9050 provides a clock generator with crystal oscillator circuit. This circuit generates all of the chip clock frequencies to which the logic is synchronised. In Normal mode all the clocks are generated from one external source. In Emulation mode the Master clock is the ECLK which becomes an input.

For AMP and TACS mobile handset applications the input frequency must be 8·064MHz. In Emulation Mode an input frequency of 1·008MHz, or 2·016MHz in Turbo mode, is required on the ECLK pin. Note that, although the ACE9050 will operate with lower frequencies, the radio functions such as the Modem would not then function correctly in a radio system.

The clock generator has a built-in oscillator which requires an external crystal. Alternatively, the oscillator can be powered down and either a 800mv peak-to-peak AC-coupled sinewave or a CMOS logic level applied to XIN may be used. If the ACE9030 is being used this provides a suitable output via CLK8; AC coupling must be used.

The main internal clock (1·008MHz) is derived from the CPU clock, or ECLK. This can either be 1·008 MHz or 2·016 MHz in Turbo mode. In Turbo mode ECLK is divided by 2 to generate the main 1·008MHz clock. This gives correct functionality when in Emulation mode, where the ECLK frequency is generated externally.

The clock generator produces a clock bus with all of the internal clock frequencies required by the ACE9050. Various frequencies are also available externally. If an external crystal is used with the Crystal Oscillator, Fig. 17 shows the external components required. Careful layout rules should be applied to the external Crystal Circuit design. These include mounting the components as close as possible to the ACE9050 and avoiding running signal lines close to the oscillator circuit.

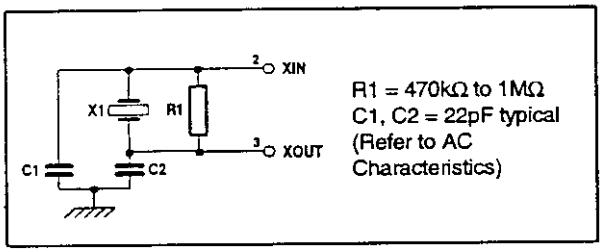


Fig. 17 External crystal components

External Pins

CPUCL 8·064 MHz Output (pin 94)

This output is the buffered crystal or clock input frequency. After reset it is disabled, but can be enabled by software. Refer to Associated Registers.

C1008 1·008 MHz Output (pin 90)

This output is the main clock divided by eight. It must always be 1·008 MHz in a mobile phone application using the ACE chipset. It is intended to drive the ACE Serial interface clock. It is enabled after reset, but can be disabled by software.

ECLK Processor Clock (pin 99)

This is the processor clock. It is an output in Normal mode, but an input in Emulation. The frequency is 1·008MHz, or 2·016MHz in Turbo mode.

XIN Crystal or External source (pin 2)

Input Crystal or external source input. External source must be AC-coupled or CMOS levels.

XOUT Crystal Output (pin 3)

If an external crystal is used connect between XIN and XOUT. If an external source is used this output should be left unconnected.

Associated Registers

Description
TURBO: Port 4 bit 3 0 = 1·008MHz (Reset state) 1 = 2·016MHz (Turbo)
ENSIS: Port 3 bit 2 0 = CPUCL pin: OUT2 [0] (Reset state) 1 = CPUCL pin: 8·064MHz
CLKENAB: Port 5 bit 1 0 = C1008 pin = 0 1 = C1008 pin = 1·008MHz (Reset state)
XOSC PD: Port 5 bit 6 0 = Oscillator active (Reset state) 1 = Oscillator power down

Table 37

8. BAUD RATE GENERATOR

The Baud Rate Generator provides standard baud rate clocks for the SCI in the 6303 block. It is internally connected to the 6303 Port2 bit 2. For Emulation mode the Baud Rate generator clock output is available to drive the shadow 6303. The Baud rate clock output is 8 times the baud rate. This is the requirement for a standard 6303. Baud rates available are shown in Table 38.

For higher baud rates a 6303 transfer rate can be selected in the TRCSR register. As these are referenced to the ECLK they will be non-standard rates.

External Pins

BAUDCLK: Baud rate clock output. (pin 6)

This output is 8×the baud rate. It is used in emulation mode only by the shadow 6303.

Associated Registers

BRG: Baud rate Select port - Write only

Bits	Description
[7: 3] XXXX	Unused
[2: 0] 000 001 010 011 100	 600 Baud (Reset state) 1200 Baud 2400 Baud 4800 Baud 9600 Baud

Table 38

9. EXTERNAL RESET AND WATCHDOG FUNCTION

The ACE9050 contains a Master reset circuit. Upon a reset being applied, all the circuits are reset and the registers put into a known state. These are detailed in Tables 8 and 9 for the ACE9050 and 6303 registers respectively. The mode selection of the 6303 also occurs automatically upon Master reset. An external output (EXRESN) is also asynchronously driven low. The Master reset circuit is activated by one of two means:

(a) The external pin MRN (Master Reset) being driven low.
(b) Watchdog Time out.

The Watchdog circuit provides an automatic means to reset the processor if it gets stuck in an infinite loop, which would be

caused by the software code entering an illegal state. This could be due to an incorrect sequence being entered by the user or a glitch on either the data or address bus causing the wrong instruction to be executed.

The Watchdog is a 4-second counter which is always counting and when it overflows a system reset is generated. This will reset the ACE9050 and drive the external reset low for 100ms. It will not reset POFFN, so the phone will not turn off. Refer to the 'Autonomous Time Out (ATO)' section for more details. To prevent the system reset the Watchdog counter must be cleared. This will prevent the system reset for 4 seconds. The following actions clear the Watchdog counter:

1. In service mode the counter is permanently cleared, preventing the system reset.
2. MRN low clears the Watchdog counter. The counter thus starts when MRN goes high.
3. The processor making a write access to the Watchdog register.

Thus in normal operation the software code must be sure to access the Watchdog register once every 4 seconds to prevent a reset.

External Pins

MRN Master Reset (pin 91)

This active low input completely resets the ACE9050 Inte~rated circuit. It prevents the Watchdog timer from counting. The ACE9050 will be reset for the duration of the MRN pulse plus an additional 100ms. The clock must be running for the device to reset correctly.

EXRESN External Reset (pin 89)

This active low output is provided for an external reset function. It is active for a minimum of 100ms in the case of a Watchdog reset. In the case of a MRN reset EXRESN will be low for the duration of MRN being low plus an additional 100ms, as shown in Fig. 18.

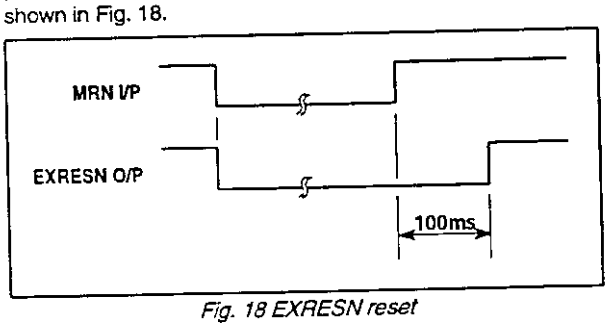


Fig. 18 EXRESN reset

Associated Registers

REWD

A write access to this address will clear the watchdog 4-second counter.

10. I²C INTERFACE

General

The ACE9050 I²C provides an interface between an I²C bus and a microprocessor. Details of the I²C bus specification can be found in the *Philips Components Technical Handbook.*

The I²C bus allows integrated circuits to communicate directly with each other via a bidirectional 2-wire bus. Interfacing the devices in an I²C system is very simple because they connect directly to the two bus lines: a serial data line (SDA) and a serial clock line (SCL). A prototype system or final product version can easily be modified by 'clipping' or 'unclipping' ICs to or from the bus. The I²C is a reliable, multi-Master bus with integrated addressing and data transfer protocols. The multi-Master capability of the I²C is very important, although many designs do not require it.

Both lines of the I²C bus are connected to a positive supply via a pull-up resistor, and remain high when the bus is not busy. Each device is recognised by a unique address, and can operate as either a transmitter or a receiver, depending upon the function of the device.

When a data transfer takes place on the bus, a device can either be a Master or a Slave. The device which initiates the transfer, and generates the clock signals for this transfer, is the Master. At that time, any device addressed is considered to be a Slave. It is important to note that a Master could either be a transmitter or a receiver; a Master microcontroller may send data to an EEPROM acting as a transmitter, and then interrogate the EEPROM for its contents acting as a receiver, in both cases performing as the Master initiating the transfer. In the same manner, a Slave could be both a receiver and a transmitter.

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high period of the clock pulse in order to be valid. Changes in the data line at this time will be interpreted as control signals. A high to low transition of SDA with SCL high indicates a Start condition, and a low to high transition of SDA whilst SCL is high defines a Stop condition. The bus is considered to be busy after a Start condition and free at a certain time interval after a Stop condition. These conditions are always generated by the Master.

Each byte is transmitted serially with the MSB first. The byte is 8 bits long followed by an acknowledge bit. The clock pulse related to the acknowledge bit is generated by the Master. The device acknowledging must pull down the SDA line during this clock pulse, whilst the transmitting device releases the SDA line (pulled high) during this pulse. A Slave receiver must generate an acknowledge after the reception of each byte. If the receiving device cannot receive the data byte immediately, it can force the transmitter to wait by holding the SCL line low.

Each device on the bus has its own unique address. The address of the microcontoller is fully programmable whereas peripheral devices usually have fixed and programmable portions. Before any data is transmitted on the bus, the Master transmits on the bus the address of the Slave to be accessed. The Slave should acknowledge the Master's addressing. The addressing is done by the first byte transmitted by the Master after the start condition.

An address on the network is seven bits long, appearing as the most significant bits of the address byte. The last bit is a direction (R/W) bit, with a 0 indicating that the Master is transmitting (WRITE) and a 1 indicates that the Master is requesting data (READ). When an address is sent, each device on the system compares the address with its own. If there is a match the device will consider itself addressed and send an acknowledge.

In addition to the above 'standard' addressing, the I²C bus protocol allows for 'general call' addressing and interfacing to CBUS devices. Fig. 19 shows a complete data transfer, comprised of an address byte indicating a WRITE and two data bytes. It also indicates the Start and Stop conditions .

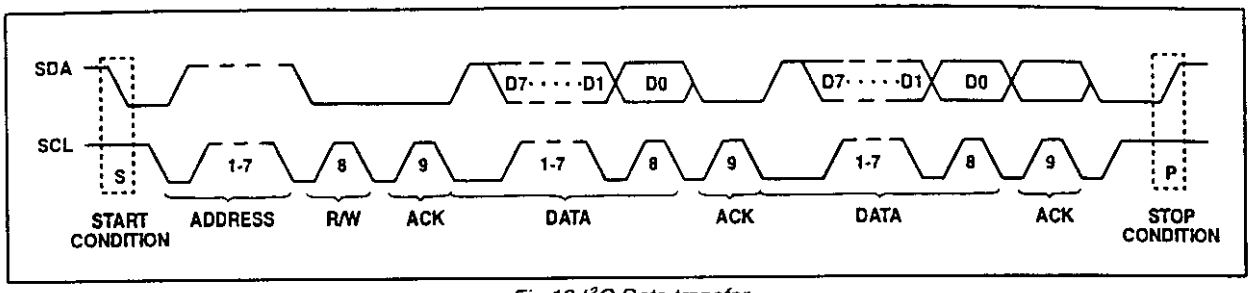


Fig.19 I²C Data transfer

ACE9050 I²C

The ACE9050 I²C can operate in one of four modes:

1. Master Transmit
2. Master Receive
3. Slave Transmit
4. Slave Receive

The ACE9050 can operate in multi-Master systems (where there is more than Master on the bus). The ACE9050 I²C will perform bus arbitration and clock synchronisation. In a mobile handset where the I²C is used to interface to a serial PROM and/or an LCD display it would be sufficient to have the ACE9050 as the sole Master.

The I²C interface consists of the SCL (clock) and SDA (data) lines. These are multiplexed with the 6303 bidirectional Port1 pins to reduce the overall pin count. Selection is made via the ACE9050 Port5.

The internal 6303 microprocessor interface consists of five 8-bit memory mapped registers and a processor interrupt line. The interrupt is connected to the 6303 IRQN interrupt, as are the ACE9050 internal and external Interrupt ports.

External Pins

SCL/6303 Port 1 [4] (pin 9)

Bi-directional pin, used for the I²C clock when selected. This pin requires an external pull up resistor when used as SCL.. The value of the pull up resistor depends on the system and I²C bus implementation. Refer to the I²C bus specification. In a typical system the resistor value would fall between 1kΩ and 20kΩ.

SDA/6303 Port 1 [3] (pin 13)

Bidirectional pin, used for the I²C data when selected. This pin requires an external pull up resistor when used as SDA. The value of the resistor should be the same as the SCL line.

Associated Registers
SEL_I2C Port 5 bit 2

Bit	Name	Description
2	SEL_I2C	0 = I²C Reset, P1 [4] and [3] selected 1 = I²C operational, SCL and SDA selected

Table 39

I2C_CNTR Control Register Read/Write

This register is used to control the ACE9050 I²C. The program can write and read from the register. The hardware can also change the status of the bits in this register (see Table 40).

Note that this register is cleared to 00_H when the I²C is reset.

IEN Interrupt Enable

When IEN is set to 1 an interrupt will occur when the IFLG bit is set. This will cause an interrupt on the 6303 IRQ. When IEN is cleared to zero the I²C interrupt will be disabled.

Position	Bit	Description
D7	IEN	Interrupt Enable
D6	ENAB	Bus Enable
D5	STA	Master Mode Start
D4	STP	Master Mode Stop
D3	IFLG	Interrupt Flag
D2	AAK	Assert Acknowledge
D1	-	Read back only: 0
D0	-	Read back only: 0

Table 40

ENAB Bus Enable

When ENAB = 1 the ACE9050 I²C will respond to calls to its Slave address (SLA6-0) and to the general call address if bit GCE in the I2C_ADDR register is set.

STA Start Master Mode

When STA = 1 the ACE9050 I²C enters Master mode and will send a START condition on the bus when the bus is free. If the STA bit is set to 1 when already in Master mode and one or more bytes have been transmitted then a repeated START condition will be sent. If the STA bit is set to 1 when the ACE9050 I²C is being accessed in Slave mode then the ACE9050 I²C will complete the data transfer in Slave mode and then enter Master mode when the bus has been released.

After the START condition has been sent this bit will be automatically cleared.

STP Stop Master Mode

When STP is set to 1 in Master mode then a STOP condition is transmitted on the I²C bus. If the STP bit is set to 1 in Slave mode then the ACE9050 I²C will behave as if a STOP condition has been received, but no STOP condition will be transmitted on the I²C bus. If both STA and STP bits are set the ACE9050 I²C will first transmit the STOP condition (if in Master mode) then transmit the START condition. The STP bit is automatically cleared: writing a zero to this bit has no effect.

IFLG Interrupt Flag

This bit gets set if an interrupt condition occurs in the I²C; however an interrupt will only be generated if the Interrupt Enable (IEN) is set.

An interrupt condition is defined as one of 26 of the possible 27 ACE9050 I²C states being entered. The only state that does not set IFLG is state $F8_H$. Refer to STAT register for more information on the I²C states.

When IFLG is high then the low period of the I²C bus clock line, SCL, is stretched and the data transfer is suspended.

When IFLG is reset to zero the interrupt is reset and the I²C clock line released.

AAK Assert Acknowledge.
This bit is used to determine whether an Acknowledge bit is sent when the I²C Receives data. It also indicates the last byte to transmit when the I²C is in Slave Transmit mode.

AAK is set to one: An acknowledge (low level on SDA) will be sent during the acknowledge clock pulse on the I²C bus when:

1. The Slave address has been received.
2. The general call address has been received and the GCE bit in the I²C ADDR registers set to one.
3. A data byte has been received in Master or Slave mode.

AAK Is cleared to zero: When a data byte is received a Not Acknowledge (high level on SDA) will be sent, both in Master and Slave modes.
In the Slave Transmitter mode then the byte in the I2C_DATA register is assumed to be the 'last byte'. After this byte has been transmitted the I²C will enter state $C8_H$ then return to the idle state.

I2C_STAT Status Register Read
This read only register contains a 5-bit status code, as shown in Table 41.

Bit	Name	Description
[7:3]	STATUS	State code
[2:0]	-	Read back as zero

Table 41

There are 27 possible status codes. When I2C_STAT contains the status code $F8_H$ no relevant status information is available and the IFLG bit in the I2C_CNTR register is not set. All other status codes correspond to a defined state of the ACE9050 I²C. When each of these states is entered the corresponding status code appears in this register and the IFLG bit in the I2C_CNTR register is set.
When the IFLG bit is cleared the status code returns to $F8_H$. The 27 possible status codes shown in Table 42
If an illegal condition occurs on the I²C bus then the bus error state is entered, status code 00_H. To recover from this state the STP bit in the I2C_CNTR register must be set and the IFLG bit cleared. The I²C will then return to the idle state, no STOP condition will be transmitted on the I²C bus..

Code (Hex)	Status
00	Bus error
08	START condition transmitted
10	Repeat START condition transmitted
18	Address + write bit transmitted, ACK received
20	Address + write bit transmitted, ACK not received
28	Data byte transmitted in master mode, ACK received
30	Data byte transmitted in master mode, ACK not received
38	Arbitration lost in address or data byte
40	Address + read bit transmitted, ACK received
48	Address + read bit transmitted, ACK not transmitted
50	Data byte received in master mode, ACK transmitted
58	Data byte received in master mode, Not ACK transmitted
60	Slave address + write bit received, ACK transmitted
68	Arbitration lost in address as master, slave address + write bit received, ACK transmitted
70	General call address received, ACK transmitted
78	Arbitration lost in address as master, General call address received, ACK transmitted
80	Data byte received after slave address received, ACK transmitted
88	Data byte received after slave address received, Not ACK transmitted
90	Data byte received after General Call received, ACK transmitted
98	Data byte received after General Call received, Not ACK transmitted
A0	STOP or repeat START condition received in slave mode
A8	Slave address + read bit received, ACK transmitted
B0	Arbitration lost in address as master, slave address + read bit received, ACK transmitted
B8	Data byte transmitted in slave mode, ACK received
C0	Data byte transmitted in slave mode, ACK not received
C8	Last byte transmitted in slave mode, ACK received
F8	No relevant status information, IFLG =O

Table 42 Possible values of I2C_STAT Register

I2C_CCR Clock Control Register: Write
This register is write only, the seven LSBs control the clock frequency on the I²C bus when in master mode. The register is cleared to 0 when the I²C is reset.

Position	Bit
D7	-
D6	m3
D5	m2
D4	m1
D3	m0
D2	n2
D1	n1
D0	n0

Table 43

The frequency of the SCL clock is given by:

$$f_{SCL} = \frac{f_{CLK}}{10\times(m+1)\times 2^n}$$

Where:

f_{SCL} is the I²C bus clock frequency,
f_{CLK} is 8·064 MHz,
m is the value stored in CCR D[6: 3] and
n is the value stored in CCR D[2:0]

I2C_ADDR Slave Address: Read/Write
This register sets the slave address of the ACE9050 I²C. This is only valid when the I²C is in Slave mode, allowing the system designer to select the required Slave address and prevent contentions. The register is cleared to 0 when the ACE9050 I²C is reset.

Position	Bit	Description
D7	SLA6	Slave address 1st bit
D6	SLA5	Slave address 2nd bit
D5	SLA4	Slave address 3rd bit
D4	SLA3	Slave address 4th bit
D3	SLA2	Slave address 5th bit
D2	SLA1	Slave address 6th bit
D1	SLA0	Slave address 7th bit
D0	GCE	General Call address enable

Table 44

SLA6 - SLA0 sets the 7-bit address. SLA6 corresponds to the first bit received from the I²C bus after a start condition. When the ACE9050 I²C receives this address after a START condition it will enter Slave mode. If GCE is set to one then the I²C will also recogonise the General Call Address.(00_H).

I2C_DATA Data Register: Read/Write
This register contains the data byte to be transmitted or the data byte which has just been received.

Bits	Name	Description
[7:0] Read	RXData	Data received
[7:0] Write	TXData	Data to transmit

Table 45

In transmit mode the byte is sent MSB first, in receive mode the first bit received will be in the MSB of the register. After each byte is transmitted this register will contain the byte that was actually present on the bus. Therefore in the case of lost arbitration this register will contain the received byte.

Clock Synchronisation
If another device on the I²C bus drives the clock line when the ACE9050 I²C is in master mode the ACE9050 I²C will synchronise its clock to the I²C bus clock. The high period of the clock will be determined by the device that generates the shortest high clock period. The low period of the clock will be determined by the device that generates the longest low clock period.
A slave may stretch the low period of the clock to slow down the bus Master. The low period may also be stretched for handshaking purposes. This can be done after each bit transfer or each byte transfer. The ACE9050 I²C will stretch the clock after each byte transfer until the IFLG bit in the I2C_CNTR register is cleared.

Bus Arbitration
In master mode the ACE9050 I²C will check that each transmitted logic 1 appears on the I²C bus as a logic 1. If another device on the bus overrules and pulls the SDA line low arbitration is lost. If arbitration is lost during the transmission of a data byte or a not acknowledged bit is received the ACE9050 I²C will return to the idle state. If arbitration is lost during the transmission of an address the ACE9050 I²C will switch to slave mode so that it can recognise its own slave address or the general call address.

Bus and Internal Clock Speeds
The I²C bus is defined for bus clock speeds up to 100k bits/s. The clock speed generated by the ACE9050 I²C in master mode is determined by the I2C_CCR register.
All signals within the ACE9050 I²C are synchronised to an internal main clock (MCLK).
The frequency of this clock is given by:

$$f_{MCLK} = \frac{f_{CLK}}{(m+1)}$$

Where:

f_{MCLK} is the MCLK (main clock) clock frequency,
f_{CLK} is 8·064 MHz and
m is the value stored in I2C_CCR D[6: 3]

If the ACE9050 I²C is used in systems where there are other masters on the I²C bus then the frequency of MCLK should not be less than 500 kHz to prevent the ACE9050 I²C from missing a START condition sent by another master.

Modes of Operation

The following section details the operation of the ACE9050 I²C in the four possible modes of I²C transfer, namely: Master Transmit, Master Receive, Slave Transmit and Slave Receive.

Master Transmit
In the master transmit mode the ACE9050 I²C will transmit a number of bytes to a slave receiver. Before the master transmit mode can be entered the I2C_CNTR register should be initialised as shown in Table 46, where X is either 0 or 1.

Position	Bit	State
D7	IEN	X
D6	ENAB	1
D5	STA	0
D4	STP	0
D3	IFLG	0
D2	AAK	X
D1	-	0
D0	-	0

Table 46

1. Transmit Start Condition. The master transmit mode is entered by setting the STA bit to one. The ACE9050 I²C will then test the I²C bus and will transmit a START condition when the bus is free. When a START condition has been transmitted the IFLG bit will be set and the status code in the STAT register will be 08_H. If a repeated START condition has been transmitted then the status code will be 10_H instead of 08_H.

2. Transmit Slave Address and Write The I2C_DATA register should now be loaded, with the address of the slave to be written to in bits[7:1] and bit[0] cleared to zero to specify Write. The IFLG bit should now be cleared to zero before the transfer can continue. When the slave address and write bit have been transmitted and an acknowledge bit received the IFLG will be set again. A number of status codes are now possible in the STAT register, as shown in Tables 47 and 48.

3. Transmit Data If the code 18_H or 20_H has been detected in the STAT, the next byte to be placed in the I2C_DATA register is the first data byte, or a word address in the case of some memory devices. The IFLG can then be cleared. After each additional data byte has been transmitted the IFLG will be set and one of three status codes will be in the START register, as shown in Tables 49 and 50.

Code	ACE9050 I²C state	Micro response	Next I²C action
18_H	Addr and Write transmitted, ACK received	(a) WriteDATA, clear IFLG	Transmit data byte,receive ACK
		(b) Set STA, clear IFLG	Transmit repeated START
		(c) Set STP, clear IFLG	Transmit STOP
		(d) Set STA and STP, clear IFLG	Transmit STOP then START
20_H	Addr and Write transmitted, ACK not received	As for code 18_H	As for code 18_H

Table 47 Possible status codes after Slave address has been transmitted with the ACE9050 as the only bus Master

Code	ACE9050 I²C state	Micro response	Next I²C action
38_H	Arbitration lost	(a) Clear IFLG	Return to idle.
		(b) Set STA, clear IFLG	Transmit START when bus free.
68_H	Arbitration lost, Slave Addr and	Clear IFLG: AAK = 0	Receive data byte, transmit Not ACK
	Write received: ACK transmitted	Clear IFLG: AAK = 1	Receive data byte, transmit ACK
78_H	Arbitration lost, GCA, ACK transmitted	As for code 68_H	As for code 68_H
$B0_H$	Arbitration lost, Slave Addr and	Write byte to DATA, clear IFLG, AAK = 0	Transmit last byte, receive ACK
	Read received: ACK transmitted	Write byte to DATA, clear IFLG, AAK = 1	Transmit data byte, receive ACK

Table 48 Possible status codes after Slave address has been transmitted with Multiple Bus Masters

Code	ACE9050 I²C state	Micro response	Next I²C action
28_H	Data byte transmitted, ACK received	(a) Write byte to DATA, clear IFLG	Transmit data byte,receive ACK
		(b) Set STA, clear IFLG	Transmit repeated START
		(c) Set STP, clear IFLG	Transmit STOP
		(d) Set STA and STP, clear IFLG	Transmit START then STOP
30_H	Data byte transmitted, ACK not received	As for code 28_H	As for code 28_H

Table 49 Possible status codes after Data has been transmitted with the ACE9050 as the only bus Master

Code	ACE9050 I²C state	Micro response	Next I²C action
38_H	Arbitration lost	(a) Clear IFLG	Return to idle
		(b) Set STA, clear IFLG	Transmit START when bus free

Table 50 Possible extra status codes after Data has been transmitted with multiple bus Masters

4. Transmit Stop When all bytes have been transmitted the STP bit should be set. The ACE9050 I²C will then transmit a STOP condition, clear the STP bit and return to the idle state. If the Slave receiver cannot receive any more data it must indicate this to the Master by generating the Not Acknowledged condition.

Master Receive

In the Master receive mode the ACE9050 I²C will receive a number of bytes from a Slave transmitter. The sequence is not dissimilar to that for Transmit. For some memory devices a 'dummy write' may be required to transmit the word address before the read operation.

Before the master receiver mode can be entered the I2C_CNTR register should be initialised as for entering master transmit mode.

1. Transmit Start Condition The master receive mode is entered by setting the STA bit to one. The ACE9050 I²C will then test the I²C bus and will transmit a START condition when the bus is free. After the START condition has been transmitted the IFLG bit will be set and status code 08_H will be in the I2C_STAT register. If a repeated START condition has been transmitted then the status code will be 10_H instead of 08_H.

2. Transmit Slave address and Read The I2C_DATA register should be loaded with the address of the Slave in bits[7:1] and bit[0] set to 1 to specify read. The IFLG bit should now be cleared to 0 before the transfer can continue. When the Slave address and read bit have been transmitted and an acknowledge bit received, the IFLG bit will be set again. A number of status codes are possible in the STAT register; these are shown in Tables 51 and 52.

3. Receive Data If the code 40_H has been detected it can be assumed that a Slave has detected its address and when the IFLG is cleared the ACE9050 will begin to clock in valid data on the SDA line. After each data byte has been received the IFLG will be set, and require clearing. One of three status codes wil be in the I2C_STAT register, as shown in Tables 53 and 54.

Code	ACE9050 I²C state	Micro response	Next I²C action
40_H	Addr and Read transmitted, ACK received	Clear IFLG, AAK = 0 Clear IFLG, AAK = 1	Receive Data byte, transmit Not ACK Receive Data byte, transmit ACK
48_H	Addr and Write transmitted, ACK not received	(a) Set STA, clear IFLG (b) Set STP, clear IFLG (b) Set STA and STP, clear IFLG	Transmit repeated START Transmit STOP Transmit STOP then START

Table 51 Possible status codes after Slave address has been transmitted with the ACE9050 as the only bus Master

Code	ACE9050 I²C state	Micro response	Next I²C action
38_H 68_H 78_H $B0_H$	As for Master transmit	As for Master transmit	As for Master transmit

Table 52 Possible extra status codes after Slave address has been transmitted with multiple bus Masters

Code	ACE9050 I²C state	Micro response	Next I²C action
50_H	Data byte received, ACK transmitted	Read Data, clear IFLG, AAK = 0 Read Data, clear IFLG, AAK = 1	Receive Data byte, transmit Not ACK Receive Data byte, transmit ACK
58_H	Data byte received, Not ACK transmitted	(a) Read Data, set STA, clear IFLG (b) Read Data, set STP, clear IFLG (b) Read Data, set STA and STP, clear IFLG	Transmit repeated START Transmit STOP Transmit STOP then START

Table 53 Possible status codes after Data has been received in multi-Master system

Code	ACE9050 I²C state	Micro response	Next I²C action
38_H	Arbitration lost	As for Master transmit	As for Master transmit

Table 54 Possible status codes after Data has been received in multi-Master system

4. Transmit Stop When the Master has finished receiving data it must signal the end of data to the Slave transmitter by generating a not acknowledge on the last byte that was clocked out by the Slave. The Slave transmitter must release the data line to allow the Master to generate the STOP condition. When all bytes have been received the I2C_STAT register should return a 58_H. The microcontroller is then free to set the STP bit. The ACE9050 I²Cwill transmit a STOP condition, clear the STP bit and return to the idle state.

Slave Transmit

In the Slave transmit mode a number of bytes are transmitted to a Master receiver. The Slave transmitter has control of the SDA line and must ensure the bits are correctly acknowledged. Before the Slave transmit mode can be entered the CNTR register should be initialised as shown in Table 55, where X is either 0 or 1.

Position	Bit	State
D7	IEN	X
D6	ENAB	1
D5	STA	0
D4	STP	0
D3	IFLG	0
D2	AAK	1
D1	-	0
D0	-	0

Table 55

1. Entering Stave Transmit Mode The ACE9050 I²C will enter Slave transmit mode when it receives its own Slave address (SLA6-0) and the read bit (bit 0 = 1) after a START condition. The ACE9050 I²C will then transmit an acknowledge bit and set the IFLG bit in the I2C_CNTR register and status code $A8_H$ (Slave address and read bit received, ACK transmitted) will be in the I2C_STAT register.

Slave transmit mode can also be entered directly from a Master mode if arbitration was lost in Master mode during the address byte, and the Slave address and read bit were received. The status code in the I2C_STAT register will then be $B0_H$.

2. Sending Data The data byte to be transmitted should then be loaded into the I2C_DATA register and the IFLG cleared. When the ACE9050 I²C has transmitted the byte and received an acknowledge the IFLG will be set and the STAT register will contain $B8_H$.

3. Completing Transfer Slave Termination When the last byte to be transmitted is loaded into the DATA register the AAK bit should be cleared when, or immediately before the IFLG is cleared. After that last bit has been transmitted the IFLG will be set as usual but the STAT should contain $C8_H$.

When this IFLG flag is cleared the ACE9050 I²C will then return to the idle state. The AAK bit must be set to one before Slave mode can be entered again.

4. Master Termination If no acknowledge is received after transmitting any byte: the SDA line is released to allow the Master to generate, the Stop condition IFLG will be set and the STAT register will contain $C0_H$. When the IFLG is cleared the ACE9050 I²C will return to the idle state. If the STOP condition is detected after an acknowledge bit then the ACE9050 I²C will return to the idle state.

Slave Receive

In the Slave receive mode a number of data bytes are received from a Master transmitter. Before the Slave receive mode can be entered the CNTR register should be initialised as for Slave transmit mode.

1. Entering Slave Receive Mode The ACE9050 I²C will enter Slave receive mode when it receives its own Slave address (SLA6-0) and the write bit (bit = 0) after the START condition. The ACE9050 I²C will then transmit an acknowledge bit and set the IFLG bit in the I2C_CNTR register and status code 60_H (Slave address + write bit received, ACK Transmitted) will be in the STAT register.

The ACE9050 I²C will also enter Slave receive mode when it receives the general call address 00_H (if bit GCE in the ADDR register is set). The status code will then be 70_H.

Slave receive mode can also be entered directly from a Master mode if arbitration was lost in Master mode during the address byte, and the Slave address and write bit or general call address were received. (For the general call condition the GCE bit in the I²C_ADDR register must be set to one)

The status code in the I2C_STAT register will then be 68_H if the Slave address was received or 78_H if the general call address was received. The IFLG bit must be cleared to zero to allow the data transfer to continue.

2. Receiving Data If the AAK bit in the I2C_CNTR register is set to 1 then after each byte is received an acknowledge bit (low level on SDA) is transmitted and the IFLG bit is set, the I2C_STAT register will contain status code 80_H (or 90_H if Slave receive mode was entered with the general call address). The received data byte can be read from the I2C_DATA register and the IFLG bit must be cleared to allow the transfer to continue.

3. Competing Transfer When the STOP condition or a repeated START condition is detected after the acknowledge bit, then the IFLG bit is set and the I2C_STAT register will contain status code $A0_H$. If the AAK bit is cleared to 0 during a transfer then the ACE9050 I²C will transmit a not acknowledge bit (high level on SDA) after the next byte is received, and set the IFLG bit. The I2C_STAT register will contain status code 88_H (or 98_H if slave receive mode was entered with the general call address). When the IFLG bit has been cleared to 0 the ACE9050 I²C will return to the idle state.

RADIO FUNCTIONS

The ACE9050 provides the following Radio Functions, which will typically be required in a mobile phone implementation, all of which are controlled by internal configuration registers:

Modem and SAT management,
ACE Serial Interface,
IFC counter,
2 pulse width modulators,
Key pad interface and
Tone generator.

These functions are described in the following sections

1. INTERNAL CONFIGURATION REGISTERS

The ACE9050 contains 3 internal configuration registers. These allow the hardware to be configured via software write instructions. The function of the bits is described in the relevant section in more detail. This section provides an overview of the 3 internal configuration registers.

Associated Registers

PORT3 Read/Write

Bit	Name	Block	Logic state
7	ENMOD	Modem	0 = No action* 1 = Modem fully enabled
6	ONRAD	ACE serial interface	0 = Latch pulse 3 generated* 1 = Latch 3 set to 1
5	STIFC	IFC counter	0 = IFC counter reset* 1 = Enable IFC counter
4	UPOFFN	ATO and Watchdog	0 = POFFN set to 0* 1 = POFFN set to 1
3	MDMSLP	Modem	0 = Active* 1 = Sleep
2	ENSIS	Clock Gen	0 = OUT2 [0]* 1 = 8·064MHz Clock
1	SLEEP	Decoder	0 = No action* 1 = CSEPN Inactive for address $FFFF_H$
0	IFFREQ	IFC counter	0 = 256 period count* 1 = 2432 period count

*Reset state in Normal mode

Table 56

PORT4 Read/Write

Bit	Name	Block	Logic state
7	SINTSLP	ACE serial interface	0 = Active* 1 = Sleep
6	-	Not used	
5	-	Not used	
4	NOMPLL	Modem (Data Clk)	0 = Clk sync to data* 1 = Clk not sync to data
3	TURBO	CPU clock	0 = 1·008MHz* 1 = 2·016MHz
2	SATMUX	Modem (SAT Mux)	0 = TXSAT selected* 1 = RXSAT selected
1	IROM	Decoder	0 = External ROM 1 = Internal ROM*
0	-	Not used	

*Reset state in Normal mode

Table 57

PORT5 Read/Write

Bit	Name	Block	Logic state
7	-	Not used	
6	XOSC_PD	Clock Gen	0 = Active Oscillator* 1 = Power down
[5:4]	OUT2.2_SEL	Output Mux #2	00 = OUT2 [2]* 01 = PWM 2 10 = Latch 2
3	-	Not used	

Table 58

PORT5 Read/Write (continued)

Bit	Name	Block	Logic state
2	SEL_I2C	I^2C	0 = I^2C Reset* 1 = I^2C Enabled, SCL and SDA selected
1	CLKENAB	Clock Gen	0 = C1008 Low 1 = C1008 Enabled*
0	PWM1MUX	Output Mux #1	0 = PWM 1 1 = OUT_PORT2 [1]*

*Reset state in Normal mode

Table 58 (continued)

2. AMPS/TACS MODEM AND SAT CONTROLLER

General Description

The Modem function supports both AMPS and TACS mobile phone systems. Selection is made via software; no external component changes are necessary. The Modem provides the following hardware:

CPU interface
Data Receiver
Data Transmitter
SAT Decoder
SAT Transmitter

The Data Receiver contains a Digital Discriminator, Data Decoder and Word Sync Detector (see Fig. 20). The Transmitter generates Manchester encoded data. The SAT receiver measures the incoming SAT signal. The SAT transmitter can either re-transmit the received SAT or generate one of the 3 standard SAT tones .

External Pins

AFC/RXDATA Data Input (pin 60)
Data is fed into the digital Discriminator via this input pin. The data can be a composite Voice, Data and SAT modulated carrier mixed down to either 54kHz or 450 kHz. The signal must be of the CMOS input levels described in the AC Characteristics section. The ACE9030 provides such an output on its AFCOUT pin. The ACE9030 samples the 450kHz IF with a 504kHz clocked register to produce a 54kHz CMOS output.

TXDATA Transmit Data Output (pin 63)
When enabled this output generates Manchester encoded Data at the appropriate data rate. This produces a digital output which must be filtered and combined with the other sources of TX modulation. The ACE9040 provides these functions via the DATI input.

RXSAT Received SAT Input (pin 51)
This input is for the received SAT which, must have been filtered to give the appropriate SAT tone with CMOS level swings. The ACE9040 provides the filtering and amplification to provide a suitable signal on the RSO output.

TXSAT Transmit SAT output (pin 62)
This output provides a CMOS level SAT frequency output. The source can either be the Received SAT, or a totally independent SAT tone generated locally in the ACE9050. This output which must be filtered and combined with the other source of TX modulation. The ACE9040 provides these functions via the TSI input.

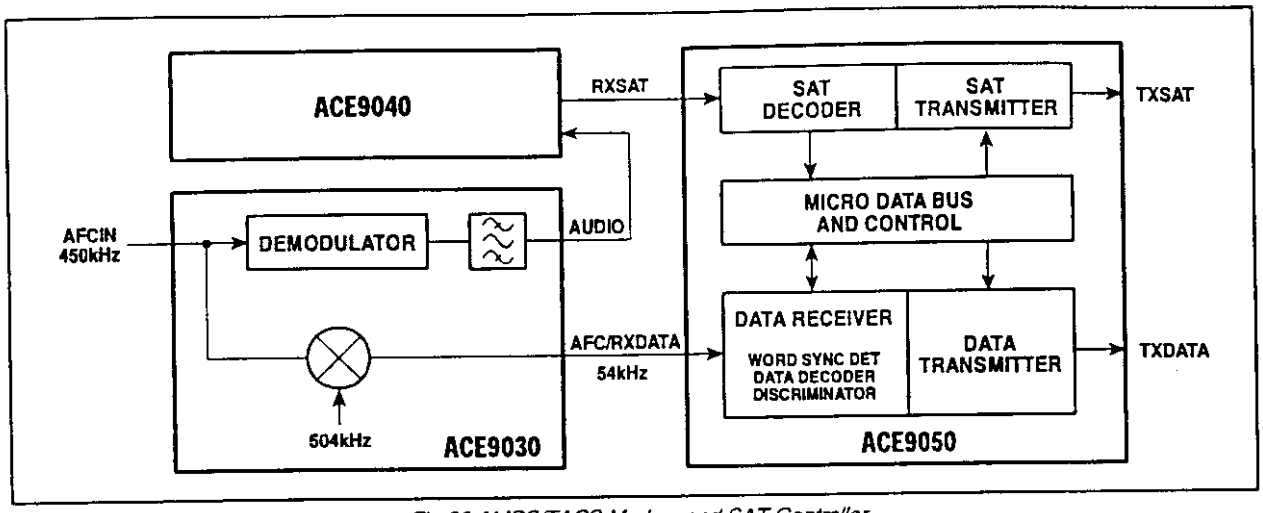


Fig.20 AMPS/TACS Modem and SAT Controller

Associated Registers

The Modem has 3 dedicated registers for control and data transfer. There are also bits in the general registers PORT3 and PORT4 which are used to set up the Modem. The bits are described in more detail in the relevant section.

MDMSLP PORT3[3] (Table 59)

This bit determines whether the modem is active or in sleep mode. The modem is put into sleep mode by turning off the clock to the Modem and associate circuitry.

MDMSLP	Modem mode
0	Active
1	Sleep

Table 59

ENMOD PORT3[7]

This bit is used to set up the Modem. It must be set to 1 by the software after a reset and before the Modem is used. It should then remain at 1.

SATMUX PORT4[2] (Table 60)

This bit is used to control the source of the Transmitted SAT signal.

SATMUX	Multiplexer output
0	Locally generated SAT
1	RXSAT

Table 60

NOMPLL PORT4[4] (Table 61)

In the Data Decoder the modem uses a locally generated clock to recover the data. NOMPLL selects whether this clock is forced to lock to the extract Data clock or not. Refer to Data Decoder section for more detail.

NOMPLL	Decoder clock
0	Normal mode: Data clock locked to incoming clock
1	Free-running: Data clock unlocked

Table 61

MODPRT0 (Table 62)

This is a dedicated read/write port used for controlling the Modem;

Bit	Name	Function
7	MDRESN	0 = Reset Modem 1 = Modem enabled
6	A_TN	0 = TACS Modem 1 = AMPS Modem
[5: 4]	SCCTX [1:0]	[5:4] bits: SAT generator 00 = 5·97kHz 01 = 6·00kHz 10 = 6·03kHz 11 = No SAT transmitted
3	ENAMPI	0 = TX output disabled 1 = TX output enabled
2	SYNDET	0 = Capture mode 1 = Sync mode
1	ENWS	0 = Word sync disabled 1 = Receiver will re-synchronise
0	VC_CCN	0 = Control channel 1 = Voice channel

Table 52

MODPRT1

This is a dedicated read/write port used for controlling the Modem.

Write (Table 63)

Bit	Name	Function
7	MDMTST	Must always be set to 0
6	TXDINV	0 = TX Data not inverted 1 = TX Data inverted
5	RXDINV	0 = RX Data not inverted 1 = RX Data inverted
4	LF1_2	0 = Discriminator enabled 1 = Discriminator bypassed (Test)
3: 0	SQLEV [3: 0]	Set the squelch threshold level

Table 63

MODPRT1 (continued)
Read (Table 64)

Bit	Name	Function
7	-	Not used
6	B_I	0 = Busy/idle bit = 0 1 = Busy/idle bit = 1
[5:4]	SCCRX [1:0]	Bits [5:4]: SAT generator 00 = 5·97kHz 01 = 6·00kHz 10 = 6·03kHz 11 = No SAT received
[3:0]	SQRX [3:0]	Number of Data bits in a word that have exceeded the pre-set Squelch threshold

Table 64

MODPRT2 This is a read/write port used for data transfer
Write (Table 65)

Bit	Name	Function
[7:0]	TXD [7:0]	Data byte to transmit

Table 65

Read (Table 66)

Bit	Name	Function
[7:0]	RXD [7:0]	Received Data byte (note 1)

NOTE 1. When VC_CCN and ENWS = 0, busy/idle bits are extracted from the data stream and are not present in RXD.

Table 66

Interrupts

The modem has 4 interrupt lines which feed into the Internal Interrupt Control block. The interrupts can be read, reset and individually masked in this block

IRQ-RX Bit3
This interrupt is generated every time the data (RXD [7:0]) and squelch values (SQRX [3:0]) are updated. This will be approximately every 800µs for AMPS and 1ms for TACS. If busy/idle bits are extracted, these times will vary by a maximum of one bit period.

IRQ-BI-SAT Bit5
This interrupt has a dual function, dependent on whether the Modem is set up for a control channel or a voice channel.
On a control channel the interrupt occurs every time the busy/idle bit B_I is updated in MODPORT1. This will occur nominally every 1ms in an AMPS system and 1·25ms in TACS.
On a voice channel this interrupt indicates there is an updated SAT value present in SCCRX. This will occur every 10 to 12ms.

IRQ-WS Bit6
This interrupt occurs every time the 11-bit Barker code is detected in the incoming data stream. Refer the Word Sync Detector for more details.

IRQ-TX Bit7
This interrupt occurs every time the first bit of a byte is transmitted from the Modem Transmitter. The software must ensure that the data in TXD is valid prior this interrupt. When enabled it will generate an interrupt every 800µs for AMPS and 1ms for TACS. The Data transmission sequence is discussed in more detail in the Modem Transmitter section.

MODEM BLOCK DESCRIPTIONS

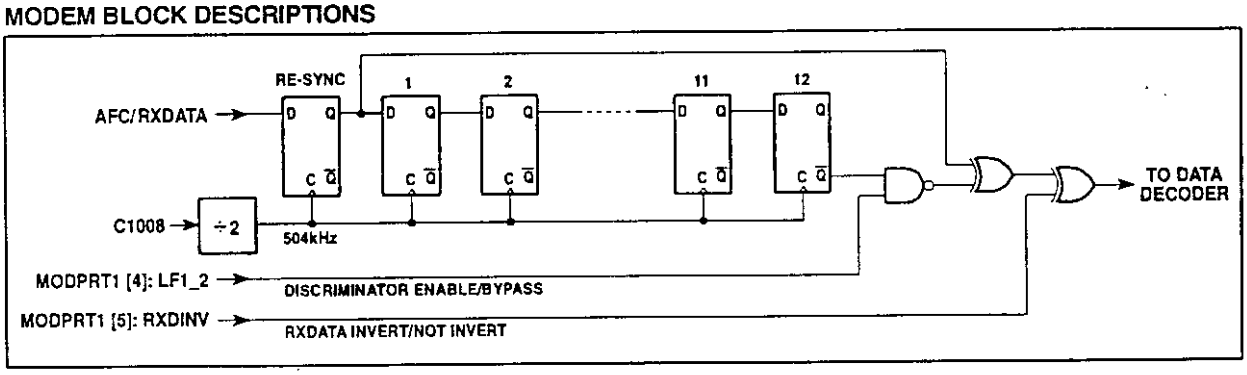


Fig. 21 Modem discriminator

Control Block

The Modem can be configured for either AMPS or TACS systems. Various clocks and timing blocks are configured depending on whether the data has a 10kHz or an 8kHz Bit rate for AMPS/TACS respectively. The Modem can also be entirely reset under software control.

If the Modem is not required the clock to the associated circuitry can be stopped, thus reducing the current consumption of the ACE9050.

Discriminator (Fig. 21)

The Discriminator uses a digital delay technique. The incoming signal is first sampled at 504kHz. This means the input can either be the 450kHz IF at CMOS levels or the 54kHz output from the ACE9030; it makes no difference to the operation of the discriminator.

In the ACE9030 the signal is initially sampled at 504kHz, which is below the Nyquist frequency, so effectively a mixing function occurs. 504kHz mixed with 450kHz gives a frequency component at 54kHz. Further sampling of the signal at 504kHz in the ACE9050 then has no effect.

The signal is then passed through a delay line of 12 D-type flip-flops, clocked at 504 kHz, giving a delay of 23·8µs, or 1·286 nominal 54kHz cycles. The non-delayed and delayed signals are then EXORed together, which produces a digital version of the analog equivalent FM demodulator: a 90 degree phase shifter and mixer. The ACE9030 contains a similar discriminator, optimised for the speech content of the signal. The ACE9030 data sheet contains a full description of the operation of such a circuit.

Associated Register bits
LF1_2 MODPRT 1[4] (Table 67)

Bit	Name	Function
4	LF1_2	0 = Discriminator enabled 1 = Discriminator bypassed (test)

Table 67

For test purposes the discriminator can be bypassed. This is achieved by setting LF1_2. In this case the Modem requires 10kHz or 8kHz Manchester encoded data, i.e. the baseband data signal.

RXDINV MODPRT 1[5] (Table 68)

Bit	Name	Function
5	RXDINV	0 = RX Data not inverted 1 = RX Data inverted

Table 68

The phase of the Data from the Discriminator is determined by the RF architecture of the receiver. The data can be inverted to cater for both high side and low side VCO architectures.

Data Decoder

The Data Decoder is responsible for clock and data extraction from the discriminated baseband Manchester encoded data stream. Manchester encoded data inherently contains the clock. The Data Decoder extracts the clock timing from the incoming data stream and regenerates an appropriately phased clock. The circuit then EXORs the extracted clock with the data. This yields a 1 for the bit period if the data bit is in phase, or a 0 if the data is out of phase. It then samples the output from the EXOR at 504kHz.

Thus, nominally 50·4 or 63 samples are taken per bit period for AMPS or TACS respectively. The data decoder will then decide if the bit is a 1 or a 0, on the state with the highest number of samples. If the number of 'correct' samples is over a certain threshold then a flag is set. The required threshold can be set by software and is referred to as the squelch level. The flag is passed to the Word Sync Detector along with the value of the bit.

The Data Decoder uses a digital transition tracking loop to regenerate the correctly phased clock. A clock at 90 degrees to the data extraction clock and an integrate-and-dump function are used. This 90 degree clock is again EXORed with the incoming data stream. The result of this is fed into an up/down counter. The output of the counter, along with the bit value, will determine whether the phase of the incoming clock was early or late. The phase of the clock over the next bit period will be altered to pull the clock in the appropriate direction. This process repeats for every bit period. The amount the clock is pulled is determined by the SYNDET bit.

Manchester encoded data transitions occur on the bit boundaries as well as in the centre of the bit. This is especially true for a string of 1s or 0s. There is a chance the clock will lock on to these, 180 degrees out of phase. The word structure contains a dotting sequence; this is a 1010... pattern which is devoid of incorrect transitions. The hardware can recognise the error condition during this time and automatically correct the clock phase.

Associated Registers
SYNDET MODPRT 0 [2] (Table 69)

Bit	Name	Function
2	SYNDET	0 = Capture mode 1 = Sync mode

Table 69

The digital tracking loop can be configured in two modes: Capture or Sync, as detailed in Table 70.

Mode	Regenerated clock shift	
	TACS (125µs)	AMPS (100µs)
0 = Capture mode	±4% (12µs)	±5% (10µs)
1 = Sync mode	±1·6% (4µs)	±1% (2µs)

Table 70

In Capture mode the regenerated clock is shifted by a greater percentage of the cycle than in Sync mode. This will allow the regenerated clock to slip over and then acquire the incoming clock phase faster. For example, to re-acquire phase in the AMPS system would take around 2ms with good signal levels.

In Sync mode the regenerated clock is not shifted as much, allowing more accurate data extraction over the bit period. If the regenerated clock becomes out of phase in this mode it will of course take longer to re-acquire the correct phase. For example in the AMPS system, to re-acquire phase would take around 10ms.

The clock rate for the circuit is 504kHz, hence the circuit works to a resolution which is a multiple of 2µs in all cases. In general, the SYNDET bit should be set to Capture mode until the system design is satisfied that the Modem is in Word Sync. Then the SYNDET should be switched to Sync mode before data reading begins.

NOMPLL Nominal PLL Port 4 [5]

The Digital Tracking loop's operation can be turned on or off with the NOMPLL bit, as shown in Table 71.

NOMPLL	Mode
0	Data Clock synchronising enabled
1	Data Clock free-running

Table 71

The NOMPLL bit will generally be set to 0 to allow normal operation of the digital tracking loop and clock synchronisation circuit.

With NOMPLL set to 1 the regenerated clock will not try to lock to the incoming data clock, but will keep its current phase. If there is a short period of time when data is not present it may be advantageous to set the NOMPLL bit. The Digital tracking loop will then be prevented from 'hunting' for a non-existent data clock. When the data then reappears, the regenerated clock should still be in phase and data can be immediately decoded without the need to re-synchronise. This facility is of use in systems where the receiver can power down for short periods of time in Standby mode, thus reducing the overall current consumption of the phone unit.

SQLEV [3: 0] MODPRT1 [3:0]

The software can set a 'squelch level' for the incoming data. This sets the number of samples of a bit that have to be 'correct' for the bit to be approved. The Data Decoder sets a flag at the end of a bit period if the squelch level has been reached. The Word Sync Detector then sums the number of approved bits that occur in a byte and updates the SQRX register at the same time as the data register.

Four bits are used to determine the squelch threshold, giving 16 different levels. The number of samples for AMPS and TACS systems is 50 and 63 respectively.

Table 72 on the following page shows the number of samples required for a bit to meet the level set, and the percentage of the total number of samples for both AMPS and TACS settings that this represents.

SQLEV [3:0]	Samples	AMPS % (50 samples)	TACS % (63 samples)
0000	62	-	98
0001	60	-	95
0010	58	-	92
0011	56	-	89
0100	54	-	86
0101	52	-	83
0110	50	100	79
0111	48	96	76
1000	46	92	73
1001	44	88	70
1010	42	84	67
1011	40	80	63
1100	38	76	60
1101	36	72	57
1110	34	68	54
1111	32	64	51

Table 72 Squelch level settings

Word Sync Detector

The Word Sync Detector contains the hardware to detect the Barker code, synchronise the received bytes to the incoming data frame, extract Busy/Idle bits and update the RXD and SQRX registers. It also generates the IRQ-WS, IRQ-RX and IRQ-BI-SAT interrupts. The hardware has four modes of operation which can be selected by software.

The Barker code sequence is used for achieving frame synchronisation to the incoming data word boundaries. It occurs in a message after the dotting sequence and before the first data word. The hardware detection circuit is an 11-bit serial shift register with appropriate asynchronous decode logic to detect the Barker code (11100010010). The action upon detecting word sync depends on the mode of the hardware.

The Word Sync Detector contains a parallel register, into which the incoming data, RXD, is clocked. When the hardware is in the appropriate mode the Busy/Idle bits are removed from the data sequence before being fed to the Data Receive (RXD) register. The Word Sync Detector also tallies the number of times the Squelch level flag is set for an eight-bit byte and stores this in the SQRX register. The Word Sync Detector contains byte and frame counters which generate the IRQ-RX interrupt when the data and squelch registers are updated. The software must ensure these registers are read within the suitable time frame after IRQ-WS to avoid losing data.

Associated Registers

VC_CCN Voice/Control Channel MODPRT0 bit0 (Table 73)

This bit allows the software to control the mode of the Word Sync Detector between Control channel and Voice channel. It also operates in conjunction with the ENWS bit; VC_CCN must be set to reflect the category of the current channel.

VC_CCN	Mode
0	Control channel
1	Voice channel

Table 73

ENWS Enable Word Sync MODPRT 0 [1] (Table 74)

This bit allows the software to control the mode of the Word Sync Detector between 'Sync on Barker' and ' Not Sync on Barker'. It also operates in conjunction with the VC_CCN bit.

ENWS	Description
0	Data will not reframe if a Barker code is detected
1	Data will reframe if a Barker code is detected

NOTE: Regardless of the setting of ENWS the IRQ-WS will be generated on detection of a Barker code.

Table 74

RXD[7:0] MODPRT2 Read (Table 75)

This register contains the data from a forward channel (FVC or FOCC) segmented into 8-bit chunks.

Bit	Name	Function
7: 0	RXD[7:0]	Data byte received

Table 75

The first bit received goes to the most significant bit of the register. On a Control channel the Busy/Idle bits can be extracted. All other data on the Control channel and all data on the voice channel will be present in the registers. This includes the dotting and Barker sequences. The IRQ-RX interrupt occurs when the registers have been updated.

SQRX[3:0] MODPRT1[3:0] Read (Table 76)

These four bits contain the number of bits in the present received byte that have surpassed the Squelch threshold set. It will thus contain a number between 0 and 8. This register is updated at the same time as the RXD register.

SQRX [3:0]	Number of bits surpassing Squelch level
0000	0
0001	1
0010	2
0011	3
0100	4
0101	5
0110	6
0111	7
1000	8
1001 to 1111	Not valid

Table 76 Possible Squelch readings

B_I MODPRT1[6] Read (Table 77)

This bit is the extracted Busy/Idle bit from a Control channel data stream. Note that an IRQ-BI-SAT interrupt occurs when this bit is updated.

B_I	Busy/Idle bit
0	0
1	1

Table 77

Modes of Operation

The Word Sync Detector has four modes of operation. The modes affect how Busy/Idle bits a handled, the function of the IRQ-BI-SAT interrupt and the action of the Word Sync Detector upon finding a Barker code in the incoming data stream. The modes are selected via the VC_CCN and ENWS bits, as shown in Table 78.

VC_CCN	ENWS	Mode	Description
0	0	Control channel syncronised	Data reframe = disabled IRQ-BI-SAT = Busy/Idle Busy/Idle bits extracted
0	1	Control channel unsynchronised	Data reframe = enabled IRQ-BI-SAT = Not Valid Busy/Idle bits not extracted
1	0	Voice channel	Data reframe = disabled IRQ-BI-SAT = SAT update
1	1	Voice channel	Data reframe = enabled IRQ-BI-SAT = SAT update

Table 78

Control Channel

When on a Control channel the software must decide when to switch between the synchronised and unsynchronised modes. The Modem does not give any direct indication that bit synchronisation has been achieved; however, the IRQ-WS provides indication that a Barker code has been detected. The system designer can look for the IRQ-WS being generated regularly in a suitable time window corresponding to the frame time, RSSI levels and squelch levels, before determining the Modem is in synchronisation.

Once the software has determined that the Modem is in synchronisation the ENWS bit must to be set to zero. The Word Sync Detector will then remove the Busy/Idle bits from the incoming data stream and not re-synchronise on Barker codes. The software must disable ENWS before the first Busy/Idle bit occurs after the Barker Code in the control channel frame. The time for this is 1ms on AMPS or 1·25ms on TACS systems. The software does not then have to re-enable ENWS unless synchronisation is lost.

As the number of bits in a frame is not divisible by eight the Word Sync Detector circuit uses frame counters to realign the data on subsequent frames instead of Barker codes. This ensures spurious Barker codes occurring in the data do not upset the synchronisation of the Modem. Due to this action Barker codes will appear distorted when read in the RXD registers. The dotting and Barker code will appear as the following three consecutive bytes: AA_H, $B8_H$ and 12_H. Once in synchronisation, the software must ensure that the IRQ-WS still occur within the time window set up. If a number of IRQ-WS are missed, the software must assume the Modem has become unsynchronised and take appropriate action. It is up to the system designer to decide on the threshold for the number of IRQ-WS dropped, or any other type of software averaging . Table 79 shows a typical sequence for locking onto data when on a Control channel.

Voice Channel

Data is not a continuous stream on a Voice channel, as on a Control channel. The data sequence also does not contain Busy/Idle bits. The software designer has to determine when valid data is present on the voice channel. The IRQ-WS interrupt timing cannot be used for this purpose, as the data stream is not continuous. Also IRQ-WS interrupts will occur sporadically, even when no data is present, due to the probability of an incoming signal being decoded as a valid Barker code.

The voice channel data sequence begins with a long dotting sequence. The software can monitor the data present in the RXD registers, and when these reliably yield a pattern of AA_H or 55_H it can be assumed a data sequence is being transmitted. The software should then ensure an IRQ-WS occurs to indicate valid data is being received. Other system parameters such as RSSI, RX audio level and SAT can also be measured by the software.

ENWS may be left enabled, or disabled after synchronisation. As there are no Busy/Idle bits and the frame is divisible by eight it is not critical to the hardware operation.

	Function	Description
1	Set up	ENMOD = 1 MDMSLP = 0 MDMRESN = 1 LF1_2 = 0 RXDINV = Setup to system NOMPLL = 0 SQLEV[3:0] = Set as required A_TN = Set as Required Disable all Modem Interrupts
2	Initialise	VC_CCN = 0 SYNDET = 0 ENWS = 1
2	Acquire	Enable IRQ-WS interrupt
5	Verify	Ensure the IRQ-WS interrupts are occurring in the correct time window. It is up to the system designer to determine the exact criteria.
6	Lock	When this occurs set: ENWS = 0 within 1ms SYNDET = 1 Enable IRQ-RX interrupt within 800µs.
7	Read Data	Read and Squelch on interrupt
8	Check	Ensure IRQ-WS occurs in correct time window. The data registers should contain AA_H, $B8_H$ & 12_H at the end of a frame.

Table 79 Data sychronisation and acquisition sequence

Data Transmitter

The Modem transmitter is considerably simpler than the receiver. It contains a data register for writing data 8 bits at a time and Manchester encoding circuitry. It also contains timing and interrupt circuitry.

Data to be transmitted is written one byte at a time to TXD[7:0]. This data is then transmitted on the next IRQ-TX interrupt, if the output is enabled. Bit 7 (most significant) is transmitted first. The Data Transmitter generates the IRQ-TX interrupts at the correct rate for the chosen system (800µs for AMPS or 1000µs for TACS) regardless of whether the transmitter is enabled or not. The Transmitter encodes the data into Manchester format before transmission. This is achieved by

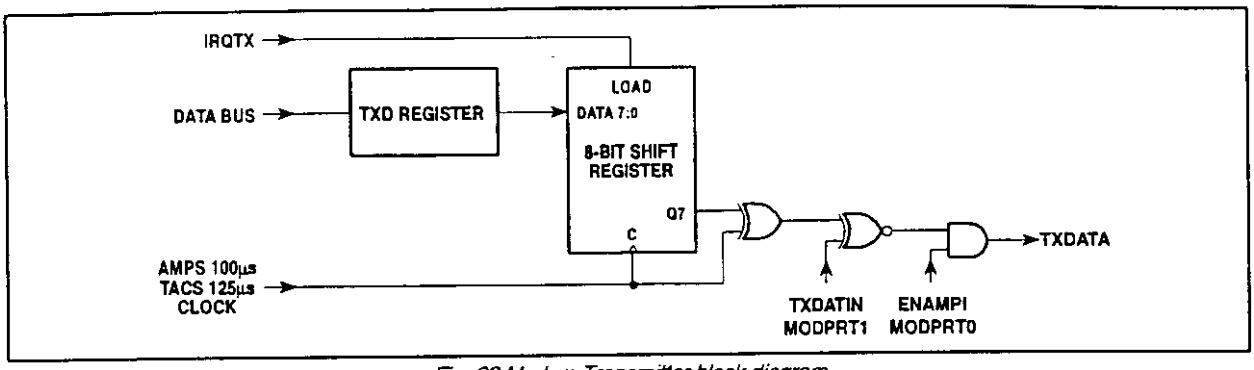


Fig. 22 Modem Transmitter block diagram

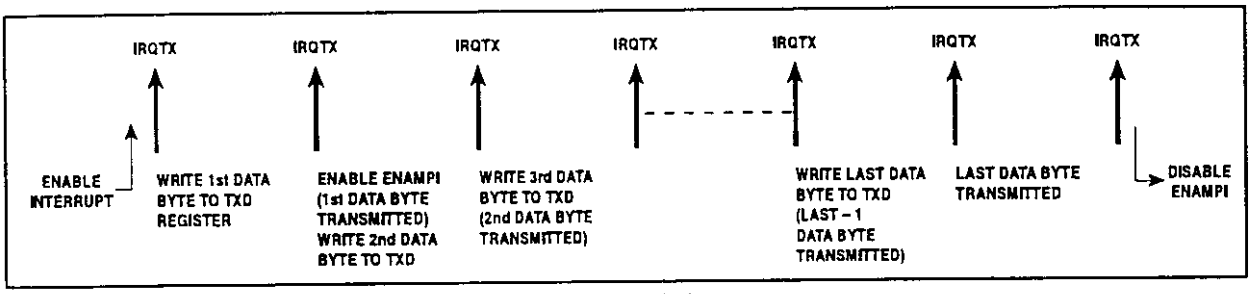


Fig. 23 Modem transmission sequence

generating a square wave at the bit rate and EXORing the generated clock with the relevant bit, for the bit period. The output can then be inverted, if this is required by the system designer. A block diagram is shown in Fig. 22.

No data manipulation is made by the encoder hardware. The software must generate the dotting and Word sync patterns and the BCH coding.

If the Transmitter is enabled the contents of the TXD register will be transmitted on an IRQ-TX interrupt, regardless of whether this register has been updated. This enables the generation of an ST tone with no overhead on the processor, other than timing the required duration. The software must simply write FF_H or 00_H to the TXD.

Associated Registers (Tables 80, 81 and 82)
MODPRT2 This is a read/write port used for data transfer
Write

Bit	Name	Function
7:0	TXD[7:0]	Data byte to transmit (bit 7 transmitted first)

Table 80

ENAMPI MODPRT 0 bit 3

Bit	Function
0	TX output-disabled
1	TX output enabled

Table 81

TXDINV MODPRT 1 bit 6

Bit	Function
0	True Data output
1	Inverse Data output

Table 82

Data transmission sequence

Table 83 and Fig. 23 describe the correct sequence for transmitting a Data message. Note that in the 5th step (Set ENAMPI high quickly) the latency between the IRQ-TX and setting ENAMPI will cause part of the first byte not to be transmitted. This byte will always be part of a dotting sequence, so this will not cause a degradation in data, however it is desirable to reduce this time to a minimum.

Step	Action
1	Enable IRQ-TX interrupt
2	Wait for IRQ-TX interrupt
3	Write Data byte to TXD
4	Wait for IRQ-TX interrupt
5	Set ENAMPI high quickly
6	Write Data byte to TXD
7	Wait for IRQ-TX interrupt
8	Repeat steps 6 and 7 until last byte
9	Write last byte
10	Wait for IRQ-TX interrupt
11	Wait for IRQ-TX interrupt
12	Disable ENAMPI

Table 83 Modem transmission sequence

SAT MANAGEMENT

The SAT Management circuitry consists of a SAT detector, SAT generator and a multiplexer. Refer to the External Pins section of the General Description for details of the two external pins: RXSAT and TXSAT .

SAT Detector

The SAT Detector measures the frequency of the signal on RXSAT input. When the Modem is configured for a Voice channel (VC_CCN high) a SAT measurement will occur every 10 to 12 ms. The SAT receiver measures the duration of 64 SAT cycles and depending on the result determines the SAT value.

Further software filtering may be required. The result of the measurement will reside in MODPRT1 bits 5 and 6. If the IRQ-BI-SAT interrupt is not masked an IRQ-BI-SAT interrupt will occur at the end of each measurement period, after the MODPRT1 has been updated.

Associated Register
SCCRX [1:0] MODPRT1 [5:4]
Read

SCCRX [1:0]	SAT tone (Hz)	Limits (Hz)
00	5970	5955-5984
01	6000	5985-6014
10	6030	6015-6045
11	No SAT	< 5955 > 6045

Table 84

SAT Transmitter

The ACE9050 has an on-chip SAT generator which can generate 5·97kHz, 6kHz, or 6·03 kHz signals. The selection is made via bits SCCTX [1:0] in MODPRT0. Alternatively the received SAT can be looped around and re-transmitted. The ACE9050 provides a multiplexer so either source can be selected under software control via the SATMUX bit in PORT4.

The generator circuit consists of a series of preset counters running from the system clock. The ACE9050 makes no allowance for varying the phase of the regenerated SAT tone as this not a requirement for current AMPS or TACS protocols.

When the Received SAT is looped around the ACE9050 only buffers the incoming SAT signal on RXSAT before feeding it to the TXSAT output pin.

Associated Registers
SCCTX[1:01 MODPRT0 [5:4]
Write

SCCTX [1:0]	Generated SAT tone (Hz)
00	5970
01	6000
10	6030
11	No SAT generated

Table 85

SATMUX PORT 4[2]

SATMUX	TX SAT source
0	Internally generated SAT
1	RX SAT

Table 86

3. ACE SERIAL INTERFACE BLOCK

General Description

The ACE Serial Interface contains two serial interfaces: The ACEBus and the SynthBus. The ACEBus is used to distribute data to and from ICs in the ACE chipset. The SynthBus is redundant when using the ACE chipset.

The ACE9050 contains the Master Transmitter/Receiver unit for the ACEBus. The ACE9040 and ACE9030 contain slave units. The bus is used for programming the devices into the required state. This will be required when the phone is powered up, and during phone operation. The ACE9030 can also transmit ADCs values to the ACE9050 on the ACEBus.

The buses can be used for data transfer between any ICs that have the appropriate interface logic; however, In a system using the ACE Chips the following words are valid on the ACEBus:

ACE9030
- Sleep Word
- Normal (ADC Values Read)
- Set-up
- Synth Word A
- Synth Word B
- Synth Word C
- Synth Word D
- Synth Dummy word (Low Noise Mode)

ACE9040
- Operating mode
- Initialising Mode 0
- Initialising Mode 1
- Handsfree

For more information refer to the ACE9030 and ACE9040 data sheets.

The ACEBus consists of a 1·008MHz clock, a bidirectional data line and 4 latch outputs. The clock and data lines are common, while the latch outputs are connected as follows:

- Latch 0: Control (ACE9040, LEN)
- Latch 1: Radio interface section (ACE9030, LATCHB)
- Latch 2: Internally connected to MUX #2
- Latch 3: Synthesiser section (ACE9030, LATCHC)

Valid data is transmitted in a stream of 24 continuous bits. At the end of the last bit the relevant latch is activated. This will latch the data into the target device. The data line will become tristate after the data transfer so that data may be received from a bus driver.

The block contains eight ACE9050 registers. Three are for serial data transmit, three for receive and two are for bus control. The block also contains interrupt generating circuitry. The SynthBus contains a data line Synthdata, clock line Synthclk and associated Latch2, which is multiplexed with OUT2[2] and PWM2.

The clock to ACE Serial Interface block can be disabled to reduce the overall power consumption of the ACE9050. Turning off this clock will disable the ACE Serial Interface but will not turn off the C1008 clock.

External Pins

C1008 (pin 90)
Refer to Clock Generator Section. This clock is used for data transfer. In the ACE9030 and ACE9040 it is also used for clocking other functions so care must be exercised in turning this clock off.

DTFG (pin 82)
Bidirectional data line. The ACE9050 clocks out data loaded into the 3 registers. Data is clocked in and out of the ACE9050 on the falling edge of C1008.

LATCH 0 (pin 80)
Latch pulse used to target data transfer. In a system using the ACE chip set Latch0 is connected to the LEN input of the ACE9040. The latch is nominally a 500ns pulse.

LATCH 1 (pin 78)
Latch pulse used to target data transfer. In a system using the ACE chip set Latch1 is connected the ACE9030 Radio Interface (LATCHB). The latch is nominally a 500ns pulse.

LATCH 3 (pin 75)
Latch pulse used to target data transfer and optimise the performance of the synthesiser. In a system using the ACE chip

set Latch3 is connected to the LATCHC input of the ACE9030 Synthesiser. The length of the latch can be varied and the latch can be set permanently high. Latch 3 can be used with the SynthBus, but is fixed at 500ns.

SYNTHCL (pin 73)
SynthBus clock line at nominally 126kHz. This is not a continuous clock. It is only activated when data transfer is required.

SYNTHDAT (pin 72)
SynthBus Data line. Contains valid data from the ACE9050, or is set to zero.

Transmitter Section

The transmitter consists of five write registers, interrupt and latch generating logic, clock divider and timer, and three shift registers connected in series. These form the 24-bit message that is sent out on DTFG. The most significant bit of LSICOM 0 is transmitted first (refer to Fig. 7).

Associated Registers
Write

Register	Bits	Description
LSICOM 0	7:0	First byte to transmit
LSICOM 1	7:0	Second byte to transmit
LSICOM 2	7:0	Third byte to transmit

Table 87

SINTSLEEP Port 4 [7]

Bit	Name	Function
7	SINTSLEEP	0 = ACE Serial Interface enabled 1 = ACE Serial Interface powered down

Table 88

STR_WIDTH Write
The pulse width of Latch 3 is programmable between 99·2µs and 12·6ms, with 99·2µs increments. This register only works with the ACEBus, not the Synthbus.

Bits	Description
6:0	Pulse duration in increments of 100 C1008 periods. This register is decremented when a pulse is generated. Writing a value of 0 in this register terminates the pulse.

Table 89

LSICOM 3 Write
This register is the control register. This is used to define the mode of the data transfer, select which latch to activate and also is used to initiate the transfer.

Bit	Name	Function
7	Go	0 = No data transfer 1 = Begin data transfer
6	CL	Must be 1
5	ANS	0 = No Answer request 1 = Answer request
4	Not used	Must be 0

Table 90 Valid bit fields for ACEBus data transfer

LSICOM 3 (continued)

Bit	Name	Function
3	Not used	Must be 0
2	Not used	Must be 0
1	Latch 1	Latch 1 enabled for data transfer
0	Latch 0	Latch 0 enabled for data transfer

Table 90 (continued)

Bit	Name	Function
7	Go	0 = No data transfer 1 = Begin data transfer
6	CL	Must be 0
5	Not used	Must be 0
4	Not used	Must be 0
3	Latch 3	Latch 3 enabled for data transfer
2	Latch 2	Latch 2 enabled for data transfer
1	Not used	Must be 0
0	Not used	Must be 0

Table 91 Valid bit fields for SynthBus

Sending Data
To begin the transmitting sequence the appropriate word has to be written to LSICOM 3. If a Latch 3 is required for the ACEBus a non-zero value must be written to STR_WIDTH prior to writing the control word in LSICOM 3.

When LSICOM 3[7] (GO) is set, the clock to the serial shift registers is enabled. Data from LSICOM 0, 1 and 2 are clocked out on the falling edge of C1008. After the 24 data bits have been clocked out, the appropriate latch is generated on the next falling edge of C1008. At the same time as the latch the IRQ-SEND interrupt is generated internally. This is fed to the interrupt control block where it can be masked. The LSICOM 3 will then be reset, so as to be ready for the next data transfer.

Receiver Section

The receiver consists of three serial registers which can be read via LSICOM 4, 5 and 6. It also contains a counter, clocking and interrupt generating circuitry.

Associated Registers
Read

Register	Bits	Description
LSICOM 4	7:0	First byte received (ACE9030 preamble)
LSICOM 5	7:0	Second byte received (ACE9030 result 1)
LSICOM 6	7:0	Third byte received (ACE9030 result 2)

Table 92

Receiving Data
In order to receive, LSICOM 3[5] (ANS) must be set. After the transmission sequence, data on the DTFG line is clocked into the receiver on the falling edge of C1008. This process begins on the fifth negative clock edge after the latch pulse, to allow a response time from the slave (Fig. 8).

After 24 clock cycles the complete word will have been clocked into the ACE9050. The data in the shift registers is latched into the three read registers. At the same time the IRQ-REC interrupt is generated.

The IRQ-SEND interrupt is generated in the receive sequence with the relevant latch in the same way as for a transmit only sequence.

PROGRAMMING

Programming Constraints

The programming of the interface is relatively straightforward when used with the ACE Chipset. However, the following constraints apply:

(a) To activate a Latch 3 transfer on the ACEBus, the STR_WIDTH register must be written to with a non-zero value prior to writing to LSICOM3 [7] (GO) set.
(b) After writing to LSICOM3 with the GO bit set, registers LSICOM0 to 3 must not be written for 25µs or until an IRQ-SEND interrupt has been generated.
(c) After writing to LSICOM3 with the GO and ANS bits set, LSICOM0 to 3 must not be written to until 6 clock cycles after an IRQ-SEND. LSICOM3 cannot be written to with bit 7 (GO) set until 55µs or the IRQ-REC interrupt has been generated. This is because the DTFG will contain the slave data until this time.
(d) A value greater than 0 must not be written to the STR_WIDTH register preceding a LATCH0, 1, 2 transfer or a Latch3 transfer with the SynthBus.
(e) The ACEBus and the SynthBus cannot be used simultaneously.

Programming Sequences

ACEBus Transfers

Latch 0 Data Transfer

(1) Write Data to LSICOM0,1 and 2
(2) Write to LSICOM3 control word:

GO	CL	ANS				L1	L0
1	1	0	0	0	0	0	1

(3) Service IRQ-SEND interrupt if enabled

Latch 1 Data Transfer

(a) Without answer request

(1) Write Data to LSICOM0, 1 and 2
(2) Write LSICOM3 Control word:

GO	CL	ANS				L1	L0
1	1	0	0	0	0	1	0

(3) Service IRQ-SEND interrupt if enabled

(b) With answer request

(1) Write Data to LSICOM 0, 1 and 2
(2) Write LSICOM 3 Control word:

GO	CL	ANS				L1	L0
1	1	1	0	0	0	1	0

(3) Service IRQ-SEND interrupt if enabled
(4) Wait for IRQ-REC interrupt
(5) Read data from LSICOM 4, 5 and 6

Latch 3 Data Transfer (ACEBus)

(1) Write Data to LSICOM 0 to 2
(2) Write Strobe Width to STR_WIDTH(non-zero value)
(3) Write LSICOM 3 Control word:

GO	CL	ANS				L1	L0
1	1	0	0	0	0	0	0

(4) Service IRQ-SEND interrupt if enabled

The Strobe width will be a minimum of 100µs, However data can be transmitted to the other slave units during the Latch3 high time. Alternatively the Latch3 may be terminated prematurely by writing 0 into the STR_WIDTH register. This may only be done after the IRQ-SEND interrupt, to ensure the latch is not terminated prematurely.

The ONRAD bit (PORT 3 [6]) can be used to keep the Latch 3 line high. Care must be taken when enabling Latch3 in this way so that spurious data is not clocked into the synthesiser. By setting the STR_WIDTH register to a suitably large value and enabling ONRAD before the STR_WIDTH time expires, the Latch 3 line can be permanently asserted. The STR_WIDTH time begins when the data transfer has completed.

SynthBus Transfers

Latch 3 Data Transfer

(1) Write Data to LSICOM 0 to 2
(2) Write LSICOM3 Control word:

GO	CL	ANS		L3	L2		
1	0	0	0	1	0	0	0

(3) Service IRQ-SEND interrupt if enabled

Latch 2 Data Transfer

(1) Write Data to LSICOM 0 to 2
(2) Write LSICOM 3 Control word:

GO	CL	ANS		L3	L2		
1	0	0	0	0	1	0	0

(3) Service IRQ-SEND interrupt if enabled

4. IFC COUNTER

The IFC counter is used as part of the Automatic Frequency Compensation loop, in conjunction with 6303 timer. The IFC counts a predetermined number of periods of the AFC_IN/RXDATA signal. By timing this duration the frequency of the input can be determined. In a system using the ACE chipset this input frequency will be 54kHz. The Number of periods counted can be either 256 or 2432. This will give measurement times over a period of approximately 5ms or 45ms when using the ACE chipset. Other input frequencies are possible, but would give different time periods and thus accuracy could be affected.

External Signals

AFC/RXDATA Input (pin 60)

This signal also feeds to the AMPS/TACS modem. This pin can be directly connected to the AFCOUT pin of the ACE9030, when this device is being used.

ICN Output (pin 77)

This output is used in emulation mode only. It is output of the IFC counter, which should be connect to the Emulator 6303 PORT2 [0]. It is internally connected to the ACE9050 6303.

Associated Registers

Register	Bit	Description
STIFCN PORT 3 [5]	0	Reset counter*
	1	Enable counter
IFFREQ PORT 3 [0]	0	2432 counts
	1	256 counts

*The counter must be reset before it can be enabled

Table 93

TCSR 6303 Timer Control Status Register
Register used to control and read the status of th 6303 Timer block. Refer to '6303 Processor Unit' section of Hitachi or Motorola data book for full details .

ICR 6303 Input Capture register
16 bit read only register used to hold the value of the free running counter captured when the proper transition of the ICN input occurred. Refer to '6303 Processor Unit' section or Hitachi or Motorola data book for full details.

Detailed Operation

Once the IFC counter is set the next rising edge of the AFC/ RXDATA input pin will generate a negative transition on ICN. The IFC counter will then count the required number of transitions and create a positive edge on ICN at the end of the count period.

The program has to control the 6303 timer in such a way that first the negative and then the positive transition of ICN is captured. The software can then calculate the difference between the two readings, which will give the elapsed time.

Programming Example
Initialise

(a) Set IFFREQ to the determine the required Count
(b) Reset STIFCN bit. This bit is reset by a hardware reset or by writing 0. It is not reset by the counter finishing execution.
(c) Ensure the 6303 TCSR register is configured so as to capture a falling edge on ICN.

Begin Count

(a) Write 1 to STIFCN
(b) Read the ICR after the negative transition on ICN
(c) Set TCSR register so as to capture a rising edge on ICN (Within 5 or 45 ms)

End of Count

(a) When a capture has occurred the ICR register can be read.

Calculate

From the difference between the two ICR values captured, the elapsed time for the count period can be calculated. It is then possible to estimate the offset of the system crystal and cancel out this error using the ACE9030 DACs.

If the crystal is off frequency it will have little effect on the timer accuracy. It will however affect the main synthesiser as the error is multiplied by the divider ratio set in the main synthesiser. The absolute error is then mixed down to appear on the 54kHz directly.

5. PULSE WIDTH MODULATOR

Two Pulse Width Modulators are available in the ACE9050. These provide CMOS type outputs whose average high time can be set by software. External components can be used to filter the output and give a mean DC level. The values chosen for these components depend on the ripple and response time required in the application. Typical applications for such outputs are LCD contrast control and battery charging control. The PWM outputs are fed to output multiplexers; the corresponding external pin function is selected by software.

The PWM circuits are designed to minimise the low frequency components of the output wave form. The PWM works on a 254µs cycle time, with 0·992µs pulse duration. The number of pulses is programmed using the appropriate register. The hardware ensures that the pulses are distributed as evenly as possible within a cycle. This is shown in Fig. 24 for some simple programming examples.

With suitable external components the following formula can be used to obtain the mean DC level of a PWM output:

$$V_{MEAN} = (DAC[7:0] \div 256) \times V_{DD}$$

External Pins

OUT2[1]/PWM1 Output (pin 98)
Selection for the source for this pin is made via the PWMIMUX bit in PORT5. This pin is also described in the External Ports and Multiplexer section.

OUT[2]/PWM2/LATCH[2] Output (pin 81)
Selection for the source for this pin is made via the OUT2.2_SEL bits in PORT5. This pin is also described in the External Ports and Multiplexer section.

Associated Registers

Write

Register	Bits	Description
DAC1 PORT	7:0	Number of output pulses in a cycle period
DAC2 PORT	7:0	Number of output pulses in a cycle period

Table 94

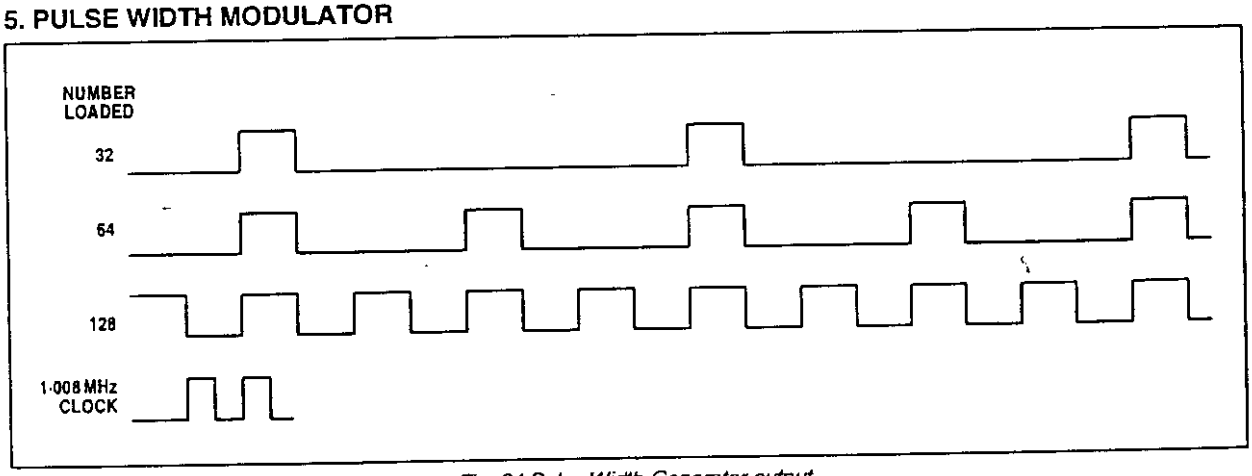


Fig. 24 Pulse Width Generator output

PORT5 Read/Write (Note 1)

Bits	Name	Description
5:4	OUT2.2_SEL	00 = OUT_PORT2[2] (Note 2) 01 = PWM2 10 = Latch 2 11 = Not valid
0	PWM1MUX	0 = PWM1 1 = OUT_PORT2[1] (note 2)

NOTES
1. These register bits are also described in the External Ports and Multiplexer section.
2. Reset state.

Table 95

6. BEEP ALARM RING (BAR) TONE GENERATOR

The ACE9050 provides a Beep Alarm and Ring Tone generator unit. This provides a digital output pulse train. The high and low time can be programmed with software. It is thus possible to vary the output tone frequency, period and volume. The pulse train can also be disabled whereupon the output will be set low. Within the system this output can be used to control a buzzer driver.

External Pin

BAR Output (Pin 96)
CMOS output which is determined by the state of the registers in the BAR block (BARHIGH, BARLOW and BARENABLE).

Associated Registers

Write

Register	Bits	Description
BARHIGH	7:0	BAR ON time
BARLOW	7:0	BAR OFF time
BARENABLE	0	0 = BAR output low 1 = BAR output pulsing

Table 96

Programming

The two programmable 8-bit registers determine the ON and OFF times in steps of approximately 8µs (7·9µs). The maximum ON and OFF times are approximately 2ms each (2·02ms). The following formula is used to calculate the actual times:

BAR ON Time = (256−BARHIGH[7:0])×7·93µs

BAR OFF Time = (256−BARLOW[7:0])×7·93µs

7. KEYPAD INTERFACE AND CHIP IDENTITY

The Keyboard interface consists of a 5-bit output port, a 4-bit input port and associated registers to read, write and configure the ports (see Fig. 25).

Alternatively these ports can be used for general I/O. The output port drive configuration can be set via software to provide the system designer with full flexibility. The port has tristate output buffers, controlled by the KPOT register. By programming KEYP and KPOT appropriately the outputs can be configured to drive in the following ways:

High impedance
Driving logic output (high or low)
Open drain
Open source.

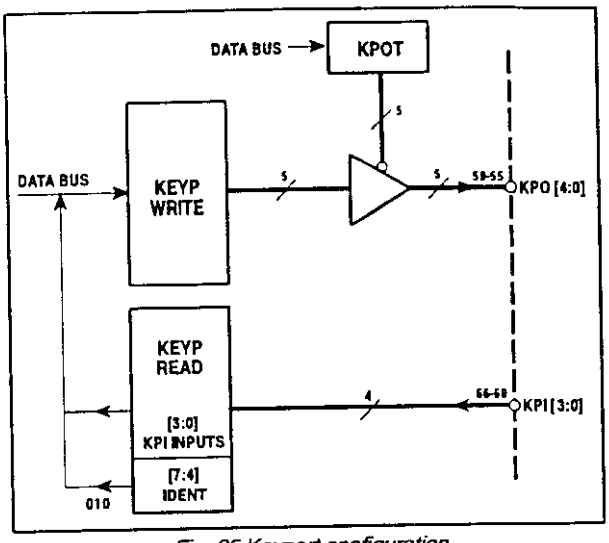


Fig. 25 Keyport configuration

Output Port

The output port has five individual outputs, which can be used as scanning outputs connected to a keyboard matrix, or can be used for other general purposes .

External Pins

KP0[4: 0] Outputs (Pins 59: 55)
The state of these outputs are defined by the respective bits in the internal registers KEYP and KPOT.

Associated Registers

KEYP Write
Keypad output port register

Bits	Description
4:0	Sets or clears associated bit in Output Port register

Table 97

KPOT Write
Output Port driver configuration

Bits	Description
4:0	0 = Output driven to level set by relevant KEYP bit 1 = Output tristate

Table 98

Programming Examples

The following bit patterns thus yield the following output configurations:

KEYP Write	KPOT	Output	Description
0	0	0	Logic drive
1	0	1	Logic drive
0	0	0	Open drain
0	1	Z	Open drain
1	0	1	Open source
1	1	Z	Open source
X	1	Z	High impedance

Table 99

Input Port

The Keyboard interface has four inputs. These inputs can also be used as general inputs. The upper four bits of this port are hard wired and provide a means of identifying the present variant of the ACE9050.

External Pins

KPI[3:0] 4-bit Input port (pins 66 to 69)

The state of this input port can be obtained by reading the respective bits in the internal register KEYP.

Associated Registers

KEYP [7:0] Read

Keypad input port register

Bits	Description
[7:4]	Chip Identity code (See Table 101)
[3:0]	Reads the level of the associated input on KPI [3:0]

Table 100

Identity code

Bits	Description
7	Read back 0
6	Read back 0
5	Read back1
4	Read back 0

Table 101

8. AUTONOMOUS TIMEOUT (ATO)

The Autonomous Time Out circuit (ATO) is provided to facilitate an automatic power down of the phone in the event of the phone entering an illegal transmitting state. The ATO block requires external functions to implement its intended operation.

The ATO monitors the status of the RXCD and TXPOW inputs; in a typical system these will indicate the presence of received and transmitted signals, respectively. If a transmitted signal is detected, without the presence of a received signal the ATO circuitry can change the state of the output pin, POFFN. This should be used to remove power from the phone system via external power control circuitry.

The main block in the ATO is a 30-second counter. It is reset by an accepted processor write to the RESATO register. The state of the external inputs RXCD and TXPOW determine whether the processor access is accepted. If the processor does not attempt to access the register, or access is blocked for a period of 30 seconds, the ATO Timer expires and an ATO reset occurs.

External Pins

RXCD Receive Path Carrier Detect Input (pin 100)

Digital input to indicate the presence of a carrier in the receiver part of the Radio as shown in Table 102.

Level	Description
0	Receive signal absent
1	Receive signal present

Table 102

A typical source for the receive signal strength would be the RSSI output from the IF Strip. However this will need to be compared to a predefined level and the logical output fed to the ACE9050. The ACE9030 provides an ADC, programmable threshold register and comparator for this purpose via RXCD.

TXPOW TX power level input (pin 61)

Digital input to monitor the presence of a Transmitted signal, as shown in Table 103.

Level	Description
0	Transmit signal absent
1	Transmit signal present

Table 103

A typical source for the transmit signal presence would be a detector in the TX path. However this will need to be compared to a predefined level and the logical output fed to the ACE9050. The ACE9030 provides two Op Amps that may be used for this purpose. One may be used as a buffer/amp and the other as a comparator in conjunction with a DAC, which is also on the ACE9030. The level of TXPOW can be directly determined via IN Port1[7], POWDET.

POFFN Power Off output (pin 85)

This pin is intended to be used to control external power regulators for the phone. It is reset low by an MRN reset. The software and the ATO then control the state of POFFN:

The software can set the state of POFFN directly via Port 3[4].

The ATO reset can only drive POFFN output low.

POFFN is not cleared by a Watchdog reset, so that this type of reset will not power down the phone. When in Service mode the ATO Reset is disabled and the IROM code sets POFFN to logic 1.

Associated Registers

RESATO Reset ATO: Write

Bit	Description
-	Write access resets the 30s ATO timer.

Table 104

UPOFFN Port 3

Bit 4 of this register sets the state of the POFFN output, as shown in Table 105.

Bit	Name	Description
4	UPOFFN	0 = POFFN output set low 1 = POFFN output set high

Table 105

Block Descriptions

ATO Timer

The ATO timer is a 30 second resetable counter. If the ATO counter reaches 30 seconds, an ATO Reset is generated. The counter is reset by the following actions:

(a) External MRN Reset
(b) Accepted Processor Write to the RESATO register

The levels of the two external signals RXCD (pin 100) and TXPOW (pin 61) are used to determine whether a processor Write to RESATO is accepted or not, as shown in Table 106.

RXCD	TXPOW	RESATO access
0	0	Accepted
0	1	Denied
1	0	Accepted
1	1	Accepted

NOTE: The CPU cannot tell whether a hardware access has been accepted or not.

Table 106

The RXCD input is filtered prior to use in the ATO Timer logic by the RXCD Filter.

The ATO timer is NOT reset by Watchdog reset.

ATO Reset

When the ATO Times Out the ATO reset circuit is trigered and the following occurs:

(a) A Time Out Interrupt is generated.
(b) If the POFFN is high it will be driven low.

The Time Out interrupt is generated at least 1 second before the POFFN is driven low. This is to give the processor time to clean up before power is removed. The processor cannot prevent the ATO reset at this stage.

The ACE9050 design assumes that the ATO Reset will remove power from the phone system. If the system is designed in such away that power is not removed from the ACE9050 the POFFN pin is only guaranteed to stay low for approximately 1 second. The state of the internal circuitry is not guaranteed after an ATO Reset.

RXCD Filter

The purpose of the filter is to smooth out short glitches in the RXCD input. The filter waits for 1 second of RXCD becoming high before the filter output is asserted. Once the output has been asserted for more than 1 second, if the RXCD goes low for more that 1 second the filter output will go low.

The filter hardware consists of a 10-bit up-down counter clocked at 492Hz. If the RXCD input is high the counter increments. If it is low the counter decrements. Thus, assuming the counter begins at zero, with a fixed high on the RXCD the counter's MSB will assert after 1 second and will overflow after approximately 2 seconds. When the counter overflows and RXCD is high it will continue to hold the maximum count value and conversely, when it reaches zero and RXCD is low, it will contain zero. The MSB of the counter is the filter output which is fed to the ATO.

Programming Guide

Although the processor only needs to access the ATO register once every 30 seconds to prevent the reset, the access should occur more frequently. This would ensure a spurious error condition unfortunately timed would not cause an ATO turn-off. Servicing the ATO with the Watchdog would be the sensible approach.

PROGRAMMER'S GUIDE TO CONTROL PORTS AND REGISTERS

IN_PORT 1 External Inputs

Read

Bit	Name	Description
7	POWDET	Level of TXPOW pin
6	SERV	Level of SERV pin
5	0	Read back 0
4	INP1 [4]	Level of INP1 [4] pin
3	INP1 [3]	Level of INP1 [3] pin
2	INP1 [2]	Level of INP1 [2] pin
1	INRQ [1]	Level of INRQ [1] pin (interrupt or INP1 [1])
0	INRQ [0]	Level of INRQ [0] pin (interrupt or INP1 [0])

Table 107

OUT_PORT 2 External Outputs

Read

Bit	Name	Description
7	OUTP2 [7]	Inverted drive to OUTP2 [7] pin
6	OUTP2 [6]	Inverted drive to OUTP2 [6] pin
5	Reserved	Should be set to 0
4	Reserved	Should be set to 0
3	Reserved	Should be set to 0
2	OUTP2 [2]	Drive level of OUTP2 [2] pin when selec ted by Port 5
1	OUTP2 [1]	Drive level of OUTP2 [1] pin when selec ted by Port 5
0	OUTP2 [0]	Drive level to CPUCL pin when CPUCL is disabled in Port 3

Table 108

PORT 3 ACE9050 Configuration

Read/Write

Bit	Name	Description	Logic state
7	ENMOD	Modem on	0 = No action* 1 = Modem fully enabled
6	ONRAD	ACE serial interface	0 = Latch 3 pulse generated* 1 = Latch 3 set to 1
5	STIFC	Start IFC count	0 = IFC counter reset* 1 = Enable IFC counter
4	UPOFFN	Power control	0 = POFFN set to 0* 1 = POFFN set to 1
3	MDMSLP	Modem mode	0 = Active* 1 = Sleep
2	ENSIS	CPUCL pin	0 = OUT2 [0]* 1= 8·064MHz Clk
1	SLEEP	Sleep	0 = CSEPN active for address $FFFF_H$* 1 = CSEPN inactive for address $FFFF_H$
0	IFFREQ	IFC counter	0 = 256 period count* 1 = 2432 period count

* Reset state in Normal mode

Table 109

PORT 4 ACE9050 Configuration

Read/Write

Bit	Name	Description
7	SINTSLEEP	0 = ACE serial interface active* 1 = Sleep
6	Not used	Read back 0
5	Not used	Read back 0
4	NOMPLL	0 = Clock synchronised to data* 1 = Clock free running
3	TURBO	0 = 1·008MHz processor bus* 1 = 2·016MHz processor bus
2	SATMUX	0 = TXSAT selected* 1 = RXSAT selected
1	IROM	0 = External ROM 1 = Internal ROM*
0	Not used	-

* Reset state in Normal mode

Table 110

PORT 5 ACE9050 Configuration

Read/Write

Bit	Name	Description	Logic state
7	-	Not used	-
6	XOSC	Power down oscillator	0 = Active* 1 = Power down
[5:4]	OUT2.2_SEL	Multiplex control	00 = OUT2 [2]* 01 = PWM 2 10 = Latch 2*
3	-	Not used	-
2	SEL_I2C	Select I^2C	0 = I^2C reset* 1 = I^2C enabled
1	CLKENAB	CLK enable	0 = C1008 low 1 = C1008 enabled*
0	PWM1MUX	Multiplexer control	0 = PWM 1 1= OUT_PORT 2 [1]*

* Reset state in Normal mode

Table 111

MODPRT 0 Modem Control

Read/Write

Bit	Name	Function
7	MDRESN	0 = Reset Modem* 1 = Modem enabled
6	A_TN	0 = TACS Modem* 1 = AMPS Modem
[5:4]	SCCTX 1 [0]	**Bits 5: 4 = SAT generator** 00 = 5·97kHz* 01 = 6·00kHz 10 = 6·03kHz 11 = No SAT transmitted
3	ENAMI	0 = TX output disabled* 1 = TX output enabled

* Reset state in Normal mode

Cont...

Table 112

MODPRT 0 Modem Control (continued)

Bit	Name	Function
2	SYNDET	0 = Capture mode* 1 = Sync mode
1	ENWS	0 = Word sync disabled* 1 = Receiver will resynchronise
0	VC_CCN	0 = Control channel* 1 = Voice channel

* Reset state in Normal mode

Table 112 (continued)

MODPRT 1 Modem Control Write

Bit	Name	Function
7	MDMTST	Must always be set to 0
6	TXDINV	0 = TX data not inverted* 1 = TX data inverted
5	RXDINV	0 = RX data not inverted* 1 = RX data inverted
4	LF1_2	0 = Discriminator enabled* 1 = Discriminator bypassed (Test)
[3:0]	SQLEV [3:0]	Set the squelch threshold level

* Reset state in Normal mode

Table 113

MODPRT 1 Modem Status Read

Bit	Name	Function
7	-	Not used
6	B_I	0 = Busy/Idle bit = 0 1 = Busy/Idle bit = 1
[5:4]	SCCRX [1:0]	**Bits 5: 4 = SAT received** 00 = 5·97kHz 01 = 6·00kHz 10 = 6·03kHz 11 = No SAT received
[3:0]	SQRX [3:0]	Number of data bits in a word that have exceeded the preset Squelch threshold

Table 114

LSICOM 3 ACE Serial Interface Control Register
Write

Bit	Name	Function
7	GO	0 = No data transfer 1 = Begin data transfer
6	CL	0 = SynthBus (126kHz) 1 = ACEBus (1·008MHz)
5	ANS	0 = No answer request 1 = Answer request
4	Not used	Must be 0
3	Latch 3	SynthBus: Latch 3
2	Latch 2	SynthBus: Latch 2
1	Latch 1	Latch 1 enabled for data transfer
0	Latch 0	Latch 0 enabled for data transfer

Table 115

BANK_SEL Bank Select Register
Write only

Bit	Name	Description
[7:5]	-	Not used
4	CS	Chip Select: 1 = CSE2N, 0 = CSEPN
3	BA17	Banked address A17
2	BA16	Banked address A16
1	BA15	Banked address A15
0	BA14	Banked address A14

Table 116

ACE9050 REGISTERS BY BLOCK

6303

Name	R/W	Addr	Description
DDR 1	W	00	Data Dir register P1
DDR 2	W	01	Data Dir register P2
PORT 1	R/W	02	Data Port 1
PORT2	R/W	03	Data Port 2
TCSR 1	R/W	08	Timer Control/Status
FRC_HIGH	R/W	09	Free run counter MSB
FRC_LOW	R/W	0A	Free run counter LSB
ICR_HIGH	R	0D	IP Capture register MSB
ICR_LOW	R	0E	IP Capture register LSB
RMCR	W	10	Rate and mode control
TRCSR	R/W	11	TX/RX Control and Status
RDR	R	12	RX data
TDR	W	13	TX data

Table 117

ACE9050 Internal Ports

Name	R/W	Addr	Description
PORT 3	R/W	26	ACE9050 configuration
PORT 4	R/W	40	ACE9050 configuration
PORT 5	R/W	42	ACE9050 configuration

Table 118

Bus Interface

Name	R/W	Addr	Description
BANK_SEL	W	44	Bank select

Table 119

External Ports

Name	R/W	Addr	Description
IN_PORT 1	R	22	External I/P Port
OUY_PORT 2	R/W	24	External O/P Port
KEYP	R/W	36	Keypad I/P and chip ID
KPOT	W	68	O/P type for KPO

Table 120

Watchdog and ATO

Name	R/W	Addr	Description
REWD	W	6A	Reset Watchdog
RESATO	W	6C	Reset Time Out

Table 121

Interrupts

Name	R/W	Addr	Description
IRQPRT0	W	70	Reset internal interrupts
IRQPRT1	W	72	Mask internal interrupts
IRQPRT2	R	2C	Read internal interrupts
IRQPRT4	W	74	Reset external interrupts
IRQPRT5	W	76	Mask external interrupts
IRQPRT6	R	2E	Read exernal interrupts

Table 122

ACE Serial Interface

Name	R/W	Addr	Description
LSICOM0	W	60	ACE interface TX1
LSICOM1	W	62	ACE interface TX2
LSICOM2	W	64	ACE interface TX3
LSICOM3	W	66	ACE interface Control
LSICOM4	R	3A	ACE interface RX1
LSICOM5	R	3C	ACE interface RX2
LSICOM6	R	3E	ACE interface RX3
STR_WIDTH	W	67	Latch 3 width

Table 123

PWM

Name	R/W	Addr	Description
DAC1	W	5B	PWM 1 data
DAC2	W	5C	PWM 2 data

Table 124

I²C

Name	R/W	Addr	Description
I2C_ADDR	R/W	54	I²C Slave address
I2C_DATA	R/W	55	I²C Data Tx/Rx
I2C_CNTR	R/W	56	I²C Control
I2C_STAT	R	57	I²C Status
I2C_CCR	W	57	I²C Clock

Table 125

Modem

Name	R/W	Addr	Description
MODPRT0	R/W	30	Configuration
MODPRT1	R/W	32	Control/Status
MODPRT2	R/W	34	Data Tx/Rx

Table 126

BAR

Name	R/W	Addr	Description
BARHIGH	W	50	BAR on
BARLOW	W	51	BAR off
BARENABLE	W	52	BAR Output Enable

Table 127

Baud Rate Generator

Name	R/W	Addr	Description
BRG	W	53	UART Baud select

Table 128

INDEX

	Page
FUNCTIONAL OVERVIEW	3
PIN DESCRIPTIONS	4
ELECTRICAL CHARACTERISTICS	6
DC Characteristics	
AC Characteristics	
TIMING DIAGRAMS	
Normal Mode Processor Interface	
Read Cycle	7
Write Cycle	8
Emulation Mode Processor Interface	
Read and Write Cycles	9
Serial Interface Block	
ACEBus Read and Write Timings	10,11
SynthBus Timing	11
INTERNAL REGISTERS AND RESET STATUS	
ACE9050 Registers	12
6303 Registers	13
MODES OF OPERATION	
1.Normal Mode	13
2.Emulation Mode	13
3.Service Mode	13
4.Test Mode	14
5.Power down Modes	14
FUNCTIONAL DESCRIPTIONS	
1. ACE9050 6303	
General Description	14
Pin Description	14
Clock	14
I/O Port 1	14
I/O Port 2	14
Programmable Timer	15
Serial Communication Interface SCI (UART)	15
RAM Control Register	16
Operating Modes	16
Low Power Consumption Modes	16
Address Data & Memory Control	16
Interrupt Processing	16
Error Processing	16
2. INTERNAL ROM BOOT BLOCK	
Normal Mode	16
Service Mode	16
Steps 1 and 2	17
Step 3 Normal Mode	17
Step 3 Service Mode	17
Steps 4,5 and 6	17
Motorola S Format	17
Binary Dump	17
Step 7 Interrupt Vector table	17
RAM Area Reserved for IROM Operation	17
3. DECODER	17,18
4. BUS INTERFACE AND MEMORY BANKING	18
Memory Map and Banked Addressing	19
Non-Banked Area (Root)	20
Banked Area	20
Banked Address System Memory Map	20

	Page
5. INTERRUPTS	21
Masking Interrupts	21
Internal Interrupt Control Port	21
External Interrupt Control Port	22
6. EXTERNAL PORTS & MULTIPLEXER	23
7. CLOCK GENERATOR	24
8. BAUD RATE GENERATOR	24
9. EXTERNAL RESET	24
10. I²C INTERFACE	
General	25
SEL_I2C Register	26
I2C_CNTR Register	26
I2C_STAT Register	27
I2C_CCR Register	28
I2C_ADDR Register	28
I2C_DATA Register	28
Clock Synchronisation	28
Bus Arbitration	28
Bus and Internal Clock Speeds	28
Modes Of Operation	
Master Transmit	
1. Transmit Start Condition	28
2. Transmit Slave Address and Write	29
3. Transmit Data	29
4. Transmit Stop	30
Master Receive	
1. Transmit Start Condition	30
2. Transmit Slave Address and Read	30
3. Receive Data	30
4. Transmit Stop	31
Slave Transmit	
1. Entering Slave Transmit Mode	31
2. Sending Data	31
3. Completing transfer	31
Slave Receive	
1. Entering Slave Receive Mode	31
2. Receiving Data	31
3. Completing transfer	31
RADIO FUNCTIONS	
1. INTERNAL CONFIGURATION REGISTERS	31
2. AMPS TACS MODEM AND SAT CONTROLLER	
General Description	32
Interrupts	34
Modem Block Descriptions	
Controller	34
Discriminator	34
Data Decoder	35
Word Sync Detector	36
Modes of Operation	36
Control Channel	37
Voice Channel	37
Data Transmitter	37
Data Transmission Sequence	38
SAT Management	38
SAT Detector	38
SAT Transmitter	39

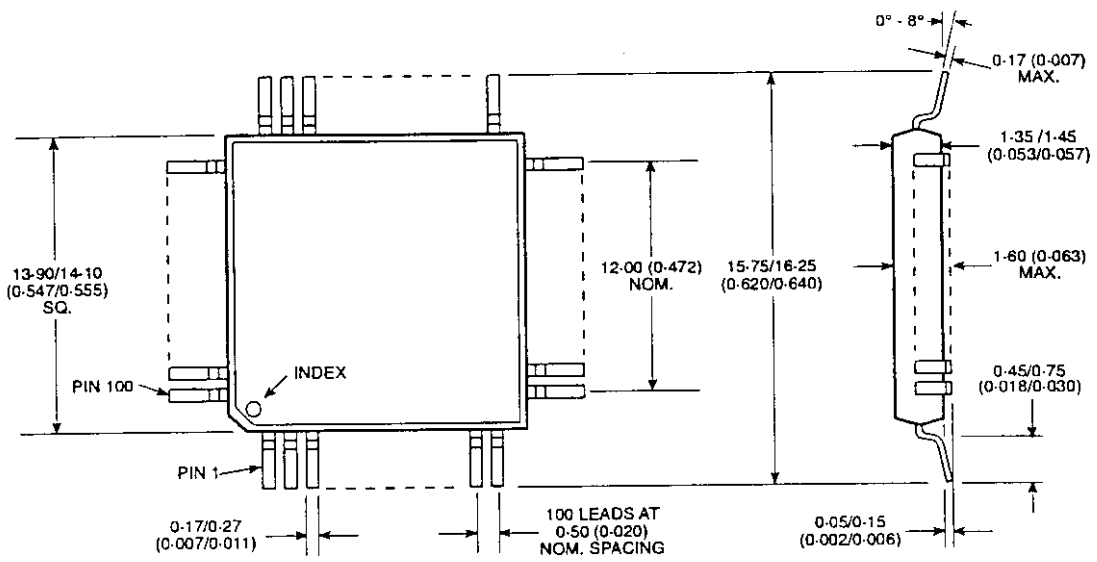
	Page
3. ACE SERIAL INTERFACE BLOCK	
General Description	39
Transmitter Section	40
Sending Data	40
Receiver Section	40
Receiving Data	40
Programming	41
Programming Constraints	41
Programming Sequences	41
ACEBus Transfers	41
SynthBus Transfers	41
4. IFC COUNTER	41
Detailed Operation	42
Programming Example	42
5.PULSE WIDTH MODULATOR	42
6. BEEP ALARM RING (BAR) TONE GENERATOR	43
7. KEYPAD INTERFACE AND CHIP IDENTITY	43
Output Port	43
Programming Examples	43
Input Port	44
Identity Code	44
8. AUTONOMOUS TIMEOUT (ATO)	44
Block Descriptions	
ATO Timer	45
ATO Reset	45
RXCD Filter	45
PROGRAMMER'S GUIDE TO CONTROL PORTS AND REGISTERS	46
ACE9050 REGISTERS BY BLOCK	47

LIST OF ILLUSTRATIONS

		Page
Fig. 1	Pin connections	1
Fig. 2	ACE implified block diagram	1
Fig. 3	Detailed block diagram	2
Fig. 4	ACE9050 6303 Read cycle timing diagram	7
Fig. 5	ACE9050 6303 Write cycle timing diagram	8
Fig. 6	ACE9050 6303 Emulation Mode Read/Write cycle timing diagram	9
Fig. 7	ACEBus Transmit Data flow	10
Fig. 8	ACEBus Receive Data flow	10
Fig. 9	ACEBus Transmit timing diagram	10
Fig. 10	ACEBus Receive timing diagram	10
Fig. 11	SynthBus timing diagram	11
Fig. 12	Data flow for the internal ROM	18
Fig. 13	Data and Address Bus configuration	19
Fig. 14	Banked Addressing block diagram	20
Fig. 15	Memory Map and Banked Addressing	20
Fig. 16	ACE9050 Interrupt configuration	22
Fig. 17	External crystal components	24
Fig. 18	EXRESN Reset	25
Fig. 19	I^2C Data transfer	26
Fig. 20	AMPS/TACS Modem and SAT controller	33
Fig. 21	Modem discriminator	34
Fig. 22	Modem Transmitter block diagram	38
Fig. 23	Modem Transmission sequence	38
Fig. 24	Pulse Width Generator output	42
Fig. 25	Keyport configuration	43

PACKAGE DETAILS

Dimensions are shown thus: mm (in).



NOTES
1. Controlling dimensions are millimetres.
2. This package outline diagram is for guidance only. Please contact your GPS Customer Service Centre for further information.

100-LEAD FINE PITCH PLASTIC QUAD FLATPACK – FP100

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ACE9050 DEVELOPMENT PLATFORM

Tools:

Pentica offers an In Circuit Emulator suitable for the 6303 CPU.. The software compiler used comes from IAR. Pentica has a sales office in the US, in Boston Mass. The phone number is 617-275-4419.

IAR may be contacted at:

IAR Systems Software Inc.
One Maritime Plaza
San Francisco
CA 94111
415-765-5500
info@iar.com

Here are a few tips in regards to the Pentica ICE:
We have used the Mime 610-6303R-PRX-256K-H40D.
610 is for 8 bit machines.
6303R is the processor
256K :- This is the model that can emulate the full memory space of the ACE9050. It interfaces with the banked addressing circuit . To use the banked addressing you need to buy Instrumentation pod with user signal inputs.

HD40 :- This is the header for the pod. The 40 way DIL interfaces with the Eval board.

The hardware comes with MimeView which is a PC based GUI.

SOFTWARE:

The C compiler assembler linker & librarian is an IAR product. It is designed for either the 6301 of 6303 processor.

The compiler has a start up file CSTARTUP that can be customized. We looked at this and found we did not need to change it.

The linker uses an .XCL file for defining program segments. We had to make a minor change.

The library contains the normal C headers and pr compiled blocks. We created simple Getchar, Putchar and Printf routines and compiled them in the library. These interface to the UART.

You can buy the CSPY product with the Compiler at a bundle price. It is available in two versions. One is compatible with the ICE as an alternative to the MimeView. We have never used this. The other version is a PC simulator, which should enable you to test your program before loading it on the hardware. I have this version, but as yet have not used it.

Power up sequences:

We have not found the Demo Board or ICE to be particularly sensitive to the Power up sequence. Generally we power up the ICE. Plug it into the board. Turn on the board, Load up the program and run

the ICE. We have plugged and unplugged the ICE into the board with no ill effects. We were told the ICE should not be running when you do this; however we have inadvertently done this as well !

Only other suggestions:
The pod must be plugged in the right way round.
The ICE MUST be in Multiplexed mode (Mode 2)
The ICE must have a suitable clock source selected (Internal or external). If no external clock is available the internal clock works fine.
The DMAP must be set up for target between 0 to 17FF
The ACE9050 board must be in Emulation mode
In Emulation mode the ACE9050 gets the clock form ECLK, no external 8 MHz is required.
The ICE should be reset with: RSYS & RESE instructions & the red button pushed before G1800 is issued.

Using the Emulator clock cautions:

Please note that the Emulator is the same as a standard 6303 with a divide by four. Thus to achieve the standard 1.008MHz ECLK for the ACE9050 you need a 4.032 MHz input to the ICE. This can either be from a sig gen, or the ACE9030 but the ACE9030 requires buffering and dividing by 2. Otherwise, the ACE9050 buss will operate at 2 Mhz resulting in the UART operating at 19.2 K baud. You can also use the internal ICE clock set at 4MHZ, which is close enough to make the ACE9050 run at 1MHz. (the AMPS modem won't lock onto control channels too well with 1MHz clock).

To run the development platform in emulation mode you must also put the ACE9050 into emulation via the SIL switch. The other optional thing to do is to put a jumper on J23 and remove any from J22 and J21 if you want the ICE to reset the board.

Once in emulation mode the ICE removes ALL of the 6303 functionality from the ACE9050, that includes the 6303 ports, Timer counter and RS232 modem. The modem on the ICE is supported on the board via the MAX233, but the wires on the J13 need to be changed over to select the Number 2 tranciver which is connected to the ICE. We have found that the internal ACE9050 6303 outputs do shadow the ICE ones, but the inputs don't have any effect, so for reliable operation use the ICE ones.

With regards to the ICE knowing about Turbo mode the answer is no, because it doesn't have to! I think you can run the ICE with an external 8.064 MHz clock which will give a 2.016MHz ECLK running into the ACE9050. Now what you must do is to set the TURBO bit in the ACE9050 (Port4 bit3) and this will then interanlly divide the ECLK by 2 and everything will come out in the wash.

The 8MHz clock in XIN on the ACE9050 does not need to be running when the ACE9050 is is Emulation mode EXCEPT if you are using the I2C, where upon you must provide this clock.

ACE9050 I/O in emulation mode:

In emulation mode the ACE9050 6303 is effectively bypassed and the Emulator 6303 functions are 'live'. This includes the SCI, timer and I/O ports (Port 1 & 2).In other words you must connect to the ICE port 1 in Emulation mode, not the ACE9050. Unfortunately there is no socket to this directly on the Development platform. What you will have to do is connect the wires to the pins of the 6303 socket, or sandwich a socket between the board socket and the ICE. The socket in the middle can have wires soldered on which can gain access to the port.

The port will work when set to output because it still hangs on the bus and shadows the emulator port because it has the same address, but is not really the 'active' address location

6303 PORTS

The ACE9050 6303 Port 1 is NOT tri-state in Emulation mode. The ports actually shadow the emulator ports. This means that If the ports are configured for output, then both will drive. However they should drive the same logic levels. There still may be switching time differences so it is recommended not to link the lines together. If the ports are always read, then there would be no contention issue. In Emulation mode the Emulator Ports get read and not the ACE9050 6303 ports.

The GPS Tools Package

1.Overview

The GPS Tool Package contains several files aiding the software development of the ACE 9050. These include header files containing register addresses and batch files simplifying the compile and link operations.

This document describes the modifications made to the compiler and linker functions. It also gives a description of the various commands used and the reasoning behind the changes.

Upon the ACE DESIGN FILE disk you should find the following archived files within the GPSTOOLS.ZIP :

lnk6303.xcl	compile.bat	putchar.c
cl6303	1.bat	getchar.c
stdio.h	2.bat	printf.c
io9050.h	3.bat	demosof.c
io6303.h	lib.bat	

2.File descriptions

2.1 lnk6303.xcl

This file is a modification upon the linker file for the 6301 processor and is the non-banked version for the ACE 9050. The main changes to the file are the definitions for the ROM and RAM start addresses, these being set at 1800H for ROM and 80H for RAM. The other modification loads the C library for the 6303 rather than that for the 6301. The CPU definition is left unchanged since the 6303 is completely compatible with the 6301.

2.2 cl6303

This is the C library for the 6303 processor. It is left largely unmodified from the cl6301 library and renamed for continuity and clarification purposes, the only alteration being the configuring for the source files printf, putchar and getchar.

2.3 Stdio.h

This header file of standard I/O function declarations is left unchanged from the original version.

2.4 io9050.h

This is a header file defining all register addresses for the ACE 9050. Inclusion of this file enables the development software to be written without continual declarations of the register addresses.

2.5 io6303

In a similar fashion to the io9050.h file, this header file contains definitions of the internal registers for the 6303 processor.

2.6 Batch files

Several batch (.bat) files are included in the GPS Tool Package. Each batch file compiles and links a desired C program. The purpose of these files is to allow the developer to perform the compile and link commands without having to type the relevant line commands each time. Running the compile.bat file presents the developer with a menu. Choosing an option from this menu will run a specific batch file , either 1.bat, 2.bat or 3.bat corresponding to options 1,2, and 3 respectively.

2.6.1 1.bat

This file simply compiles and links the desired C program. This is achieved by selecting option 1 from the compiler menu and writing 1 followed by the program name (minus the extension). The batch file will then perform the compile and link commands reporting any errors and warnings before returning to the DOS prompt. The file includes the standard compile command line:

```
icc6303 %1.c -r07
```

The line simply compiles the source program to a .r07 format, with the %1 section pulling in the program name. Added to the basic command are several switches that perform useful functions, these being -e and -P. The -e switch enables target dependent extensions whilst the -P switch generates PROMable code such that objects can be mapped to RAM and then to ROM therefore eliminating the problem of C language not being able to be put into ROM directly. The linker command includes the standard line:

```
xlink %1.r07 -f lnk6303.xcl
```

which links the compiled file (file.r07) with the non-banked memory model for the 6303 processor. As with the compiler command, several switches are added. The options include -r, -o %1.d07, -l %1 and -x. The -r switch generates a file adapted for the C-SPY high level debugger whilst the -o switch writes the output to a defined file (.d07 selected here). Including the -l switch generates a list on file.lst and the -x option allows the contents to be controlled. The other important line in the batch file is the following :

```
..\iar_key\iar_key %1.do7
```

which generates symbol files such that the program can be viewed in several formats (C, assembly or a combination), allowing a greater degree of analysis when using the emulator.

2.6.2 2.bat

This batch file is a useful variation to the 1.bat file. It is effectively the same with an additional line at the end. The line :

```
..\mv6x01
```

is added allowing the user to compile and link their desired software and transfer automatically to the ICE emulation package. This file is run similarly to 1.bat by typing 2 followed by the filename.

2.6.3 3.bat

This is again a useful variation upon the 1.bat file in that it compiles the program to Motorola S format so that it can be used with an EPROM emulator.A -P option is addled to the compile line to enable the generation of PROMable code for this purpose. In addition the line :

```
..\epem32
```

is added to enable the EPROM software to be run. Again the file is run by typing 3 followed by the file the user wishes to compile.

2.6.4 lib bat

This is a useful batch file that adds a -b switch to the compiler command line. This allows the software in question to be compiled for library modules.The file is executed by typing lib followed by the program filename.

2.7 Source files

The source files are the modified versions of the printf.c, putchar.c and getchar.c files. The changes are made such that they can be interfaced with the RS232. The files have been configured to the C library (cl6303).

2.8 Demosof.c

This is a framework that glues together the software for the hardware drivers developed by GPS for demonstration purposes. The program allows the user to demonstrate the performance of a number of blocks that make up the ACE 9050. These include the data modem transmitter and receiver, SAT transmitter and receiver, pulse width modulator and Beep,Alarm,Ring (BAR).

Pentica System emulator setup tips:

2.bat shows what switches we used for the compiler & linker. The iar_key utility is then called so that the symbol table is generated & loaded.

There is no Configuration file to set up the emulator for the evaluation board. There are a few set ups and we entered them on the Emulator command line. I think when you power up the emulator you can load in the last setup.

You can create a & run a batch file to do these, but you will have to read the Pentica Documentation.

We set up:
Mode 1 (Multiplexed mode of Data/address operation)
cloc 4 or E (depending on whether you use an external clock of the Emulator))
Dmap 0 - 17FF (Map the addresses from 0 to 17FF to external memory)

Then we reset the ICE:
rsys (Reset within emulator)

Then reset the HW:
reset (or push the button)

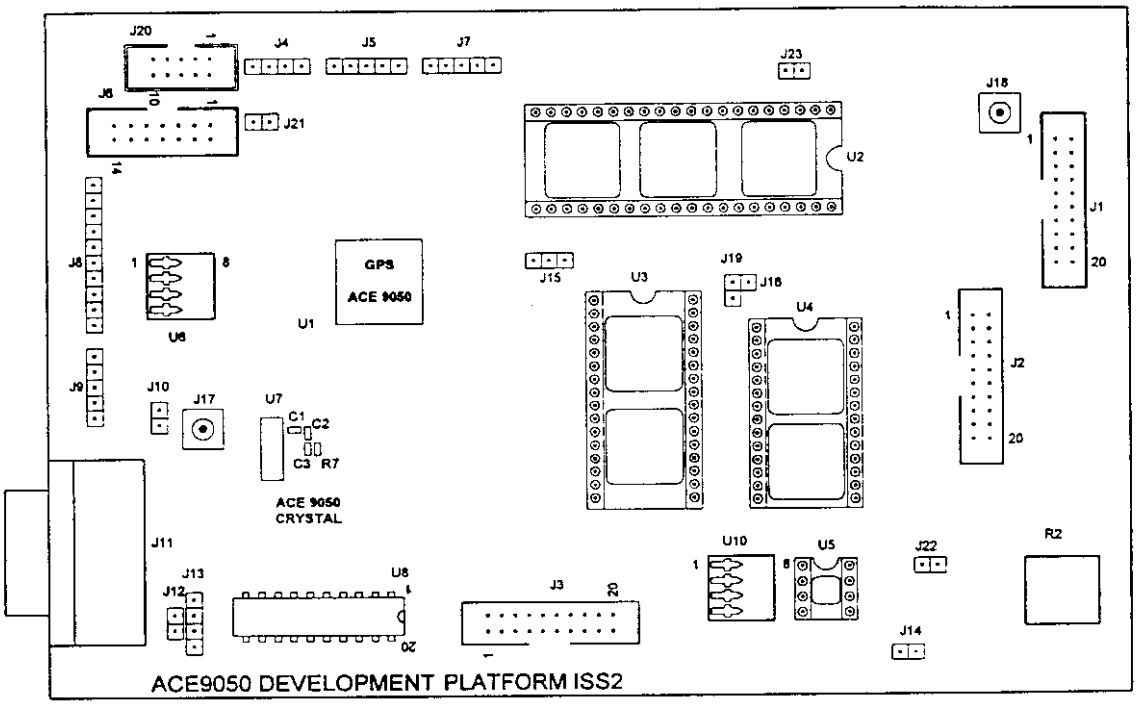
Then to Run code:
g 1800 (Start from address 1800, which is where ROM starts)

GEC PLESSEY
SEMICONDUCTORS

March 1996

PRELIMINARY INFORMATION

USER GUIDE
For
ACE9050 DEVELOPMENT PLATFORM



1) General Description

The ACE9050 Development platform is designed for Software development and system integration of the ACE Chip set. The main features are:

- Provision for an external processor or In Circuit Emulator
- Access to Data, Address and Control bus Via standard HP Logic analyser connectors
- RS232 Driver provides standard RS232 levels
- DIL sockets provided for EEPROM & FLASH
- Direct Interface with ACE Radio Platform
- I2C PROM Socket
- Direct Access to all ACE9050 External Ports & Functions
- Multiple clocking & reset schemes

2) Power

Power is applied to the board via J14:

1 Vdd (5v)
2 Vss (0v)

The power is a single supply that supplies all devices present on the board.

3) Clock

When running in a Radio system the ACE9050 requires an 8.064 MHz clock. The device will function with an 8 MHz clock for software development. The input source can either be an Crystal or logic level input. The Development platform provides numerous clocking schemes:

Crystal:

U7 provides a site for a crystal with peripheral components

External source

J17 provides an SMC connector for a signal generator (+5 dBm)

Radio Board

J10 provides a jumper to connect the clock supply from the radio board header J6.

Emulator

The Emulator can be clocked from its own internal source, or externally via the crystal site U9 or an external source via J18. The external source is AC coupled via C5.

4) Reset

The master reset can be driven from 3 different sources, which are selectable via Jumper connections:

On Board Reset

This will be used typically when developing code using EPROM, ROM Emulator or FLASH. A jumper on J22 selects this reset.

ICE Reset:

If the selected ICE has a system reset function via software command this can be selected by a jumper on J23

Radio Board Reset:

The ACE9040 has a Voltage comparator and reset function on board. This can be used as the system reset by placing a jumper on J21

5) Modes Of Operation

The ACE9050 Has four modes of operation. These are selected with U6: Each mode is selected with a corresponding switch. Putting the switch in the On position enables that mode. If all Switches are OFF then Normal mode is selected.

1 On = Test
2 On = Service Mode
3 On = Emulation Mode

6) RS232 Interface

U8 is a Dual RS232 Transmitter & Receiver. This is configured to access either the internal ACE9050 Serial Interface or an External 6303 Serial Interface via J13 & J12. This also allows for swapping over the RX and TX lines if required. The following mapping is implemented:

J12	J13
	1 : Emulator RX Data In
RX Data : 1	2 : ACE9050 RX data In
TX Data : 2	3 : ACE9050 TX data Out
	4 : Emulator TX data Out

J12 is then connected to J11, a 9 way D-type RS232 connector. Only the data and ground terminals of this connector are used.

J11
2: RX Data
3: TX Data
5: Ground.

The boards when shipped are configured for the ACE9050 Serial interface using a straight (Non-Swapping) cable.

7) MEMORY & I2C

U3, U4 and U5 provide sockets for PROM and EEPROM type memory devices. U5 also provides access to the I2C interface.

Program Memory:

U3 Provides a socket for a 128K x 8 Program memory. Provision is made for programming a 5v or 12v FLASH memory via the ACE9050. A link will be required on J19 to connect the WEN pulse. The programming voltage is required on J15 pin2. J15 also provides a convenient ground connection and a 5v supply which may be used in the case of 5v FLASH.

If a 64K x 8 memory is used a link will be required from pin 32 to pin 30 for Vdd. The Boards shipped HAVE THIS LINK IN PLACE.

If a 256K x 8 memory is required a link will need to be place from J1 pin18 to U3 pin 30. It is considered that not many customers will require this size of memory.

Electrically Erasable Memory:

The board supports both serial and parallel format of EEPROM. U3 provides a socket for an 8K x 8 device. This is hardwired to the CSEEPN line from the ACE9050. The Ready signal is accessible via J16. This output could be fed to an input port of the ACE9050 if this type of handshaking is required.

U5 provides a socket for a Serial PROM such as the XICOR X24 series. Pins 1-3 may be used to set up an address on the device via U10. If, however, these pins are required to be connected to ground this can be achieved by connecting 0R links in R4, R5 & R6 and ensuring the Switch is in the OFF position, or removed.

I2C

Pins 5 and 6 provide access to the I2C connections SDA and SCL respectively.

8) IN CIRCUIT EMULATOR INTERFACE

U2 Provides an interface for an external 6303 or ICE. The ACE9050 has to be in Emulation mode. Service mode is optional. The ICE must be set into Multiplexed Mode. Provision is made for driving the ICE with a external clock or Crystal if required.

9) LOGIC ANALYSER INTERFACE

Three 20 way header are provide for a Logic analyser. These were designed to be used with the HP 16500 (or equivalent) Logic analyser series, and the 100KOhm Termination adapter (01650-63202). The following signal mapping will then occur:

CON	SIGNAL	LSA
J1 19	ADDR 16	D0
J1 18	ADDR 17	D1
J1 17	EMUL_ADDR 14	D2
J1 16	EMUL_ADDR 15	D3
J1 15	DATA 0	D4
J1 14	DATA 1	D5
J1 13	DATA 2	D6
J1 12	DATA 3	D7
J1 11	DATA 4	D8
J1 10	DATA 5	D9
J1 09	DATA 6	D10
J1 08	DATA 7	D11
J1 07	OEN	D12
J1 06	WEN	D13
J1 05	CSE2N	D14
J1 04	CSEPN	D15
J1 03	E CLK	CLK 1

CON	SIGNAL	LSA
J2 19	ADDR 0	D0
J2 18	ADDR 1	D1
J2 17	ADDR 2	D2
J2 16	ADDR 3	D3
J2 15	ADDR 4	D4
J2 14	ADDR 5	D5
J2 13	ADDR 6	D6
J2 12	ADDR 7	D7
J2 11	ADDR 8	D8
J2 10	ADDR 9	D9
J2 09	ADDR 10	D10
J2 08	ADDR 11	D11
J2 07	ADDR 12	D12
J2 06	ADDR 13	D13
J2 05	ADDR 14	D14
J2 04	ADDR 15	D15

CONN	SIGNAL	LSA
J3 19	UP PORT1 0	D0
J3 18	UP PORT1 1	D1
J3 17	UP PORT1 2	D2
J3 16	UP PORT1 3	D3
J3 15	UP PORT1 4	D4
J3 14	UP PORT1 5	D5
J3 13	UP PORT1 6	D6
J3 12	UP PORT1 7	D7
J3 11	ICN	D8
J3 10	IRQ	D9
J3 09	R/W	D10
J3 08	ADDR STROBE	D11

10) Radio Board Interface

J10 provides a direct interface to the Ver3A radio board connector J24. J10 is in parallel with the J8 so that the inter board connections can be monitored even with a IDC connector in J10. The following lines are connected between the Radio board and ACE9050:

Reset IP: Pin 1
From ACE9040 LVN. This will also require J21 in place

RXSAT IP: Pin 3
Received SAT input from ACE9040 RSO (Pin 36) to ACE9050 Modem SAT RX Block (pin 51)

Data IP: Pin 5
54 KHz data from ACE9030 AFCOUT (Pin 7) to ACE9050 AFCIN (Pin 60). This is both for data and the AFC loop.

TXSAT OP: Pin 7:
TX SAT Output to ACE9040 TSI (Pin 9) for filtering & combining with Audio and Data TX.

TXDATA OP: Pin 9:
DATA Output to ACE9040 DATI (Pin8) for filtering & combining with SAT & Audio TX.

J6 Provides the digital interface with the Radio board. This connector allows the ACE9050 or the PC Interface card to be used to control the Radio Board.

3	C1008	O/P:	1MHz Serial Data Clk
5	lat0	O/P:	ACE9040 Latch
7	Lat1	O/P:	ACE9030 Latch
9	Lat3	O/P:	ACE9030 Latch
11	Data	I/O:	Data
13	8.064	I/P:	UP Clock Input

11) General ACE9050 I/O

J4, J5, J7, J8 & J9 Provide a means to access the other function of the ACE9050 that are required to implement a complete phone solution. These are listed below:

Pin	Description	ACE9050 Pin
J4: Key Pad Connector (Input)		
1	KPI 0	69
2	KPI 1	68
3	KPI 2	67
4	KPI 3	66

J5 Key Pad Connector (Output)

1	KP0 4	59
2	KP0 3	58
3	KP0 2	57
4	KP0 1	56
5	KP0 0	55

J7 Input Port & Interrupt

1	INRQ0	71
2	INRQ1	70
3	IP Port1 4	54
4	IP Port1 3	53
5	IP Port1 4	52

J8 RADIO PORT

1	Beep Alarm Ring O/P	96
2	External Reset O/P	89
3	Power Off O/P	85
4	TX Data O/P	63
5	TX Sat O/P	62
6	DATA IN I	60
7	RX SAT I	51
8	TX Power Detect I/P	61
9	RX Power RSSI I/P	100
10	GND	

J9 OUTPUT PORT

1	OP Port2 7	79
2	OP Port2 6	76
3	OP Port2 2/PWM2/L2	81
4	OP Port2 1/PWM1	98
5	CPUCLK (disabled at res)	94

ACE9050 DEVELOPMENT BOARD DEMO SOFTWARE

Description

This software is a combination of the low level routines used to characterize & evaluate the ACE9050 and some higher level routines written to exercise parts of the radio board. The code is menu driven from a PC. All that is required on a PC is a terminal emulator. The RS232 interface uses standard ASCII characters. All the operation routines and menus are generated by the 6303 embedded software. All the code is in the C programming language including interrupt routines. The IAR compiler & linker were used. The Compiler requires that the target specific options are enabled to allow the interrupts to work. The CSTARTUP.S07 provided with the compiler was used with minor modification; as was the LNK6303.XCL. Batch files were written to speed up the compile & linking process.

The software is simple to use and operate. A radio board is required to utilize all the functions, but the code will work with a radio board if a suitable clock source is used.

Hardware Configuration:

1. **J20 (10 pin header) of ACE9050 board should be connected to J24 of the RF evaluation board**
2. **J6 (14 pin header) of ACE9050 board should be connected to J23 of the RF evaluation board.**
3. **Power should be supplied to J4 of the RF evaluation board and J14 on the ACE9050 development board**
4. **J11 RS 232 should be connected to COM port of PC. Note the cable should be a standard 9 pin cable. The board is already configured for null modem.**
5. **Windows Terminal Communications software or equivalent may be used to communicate through the COM port. The COM port settings should be set for 9600 baud, 8 bit , no parity and 1 stop bit.**

Menus & Description:

Modem Receive 1
This menu option will pull one complete frame of data from a FCC and display the data in its raw form. This includes the word repeats, dotting and Barker code.

The Menu gives the option of Discriminator bypass. The discriminator should be enabled. Once the software has locked onto the channel data can be grabbed. If the signal is lost and then recovers the software will automatically re-synchronize when required.

Modem Transmit 2
This allows CW data, or a burst to be Transmitted. Up to 10 data words can be transmitted. The data is not formatted in any way before transmission. In CW mode the same data byte is continually TXed.

SAT Management 3

This allows the SAT generator to be enabled and the SAT tone chosen; or an automatic mode where the same SAT received is Transmitted. In the latter the SAT is measured and re-generated; not just transponded as this gives a cleaner TX SAT.

Pulse Width Mod 4
This enables both Pulse width modulators to be programmed to the mean DC level required.
Vav = (number /256) * Vdd

Beep Alarm Ring 5
This enables the Beep alarm Ring tone to be generated of the users choice. The high & low times can be programmed:
ON = (256 - Barhigh) * 7.9us
OFF = (256 - BarLow) * 7.9us

Watchdog & ATO 6
For this the chip must be in NORMAL mode. Ensure No2 (Red) switch on the select bank is Off. Either the Watchdog, or ATO service can be demonstrated. Once this occurs a 1 second counter starts until the desired time-out occurs. Note: IF the ATO hit is prevented the Watchdog still occurs. The Chip will drive the POFFN line low after 30 seconds. If the Watchdog is stopped the chip will reset after 4 seconds.

Program Up Radio Board 7
This is used to program a .FIL file into the radio board. Once this is done a further menu of Radio functions (8) will appear.

The Programming of the board will either be from a serial EEROM or via the PC serial interface. If valid data is detected in an EEROM then this can be loaded, if not a .FIL file must be sent down from the PC. When data is loaded from the PC this is stored in RAM in the most compact form possible. The user has the option of saving this data in the EEROM. This will delete previous EEROM data.

Radio Board Operations 8
This menu appears after the radio board has been loaded. It will produce a sub menu of radio functions

AFC Demonstration
This will run the Automatic Frequency Compensation, if the RSSI is high enough. The XTAL will be pulled until the main VCO is on frequency. The software uses averaging of the received data and will complete when the VCO is within 100 Hz of the desired frequency. The VCO frequency will be monitored every second, until the function is halted.

Channel Changing Demonstration
This allows any valid channel in the range 1 to 1024 to be selected. The RF will then be tuned to the required frequency and the new channel number displayed.

Power Control
Two Mobile power states can be selected: Full on or standby.

RSSI Results:
This allows the present Radio board RSSI figure to be displayed. The RSSI is updated every second.

Code Structure

The code is split between many functions residing in several C files, all in the same directory. Several Header files are also required. These are logically named; but described below for completeness.

GPSDEMO.C
This contains the main() function and the menu generation functions.

DEM_BITS.C
This mops up all the routines to exercise the relatively simple ACE9050 blocks: PWM, BAR, ATO & Watchdog.

FIL_DEMO.C
This contains the functions required to load a .FIL file from the PC; strip off the comments and combine the data into valid words for the ACEBus. It also contains the functions for programming the Radio board and management of the EEPROM. The WLC drivers were used to actually write & read the EEPROM data. This is why some of WLC software is in the sub directory. The Radio board data is stored in a global array called WORDS. The contents of words are chars. These are formatted correctly for the ACEBus, but with the word ID bits not set. The bit manipulation of the data from the .FIL format occurs before the data is stored, using the .FIL line number for labeling. If the received .FIL line number does not tally with the internal counter, the data is of dubious origin and the load will abort. The WORDS array numbers are given labels in Define statements for clarity of code.

GENERICS.C
This contains all the generic functions used throughout the code. These are generally to convert data to and from various number formats from the ASCII codes used on the RS232 interface.

INT_ROUT.C
This contains the interrupt routines for 3 of the 6303 interrupts:

SCI: If the UART is programmed to generate an interrupt this will service it. Generally the SCI is polled, but for downloading a .FIL file the interrupt must be used. A circular buffer is created to prevent overrun errors.

IRQ: This case statement services all the ACE9050 internal interrupt sources. The external interrupts are not supported by software.

TIC: This supports the Timer interrupt generated when measuring the AFC.

MOD_SAT.C
This contains the functions for the modem transmitter, receiver & SAT control. When in modem receive the function uses the timer to create a time window for the IRQ-WS. If this does not occur the modem will automatically go into the synchronization function. The SAT receiver takes ten measurements of the incoming SAT and the SAT with greatest number of samples out of the ten in its 'bin' wins. If less tan 8 are in any one bin then NO SAT is recorded. The SAT routine also times the SAT interrupt interval. If this is too long again NO SAT is recorded.

RAD_DEMO.C
This contains the routines for the Radio Demo menu: AFC, Channel change, Power Control and RSSI.

GLOBALS.C

This contains the definitions & initializes all the Global variables used in the program. These have been kept to a minimum. Buffers, variables & Boolean operators used in interrupts form the bulk of the Global variables.

Header Files:

GLOBALS.H
This include file is the mirror image of the Globals.c file, but with the variables defined as EXTERN and are not initialized. All the .C files (except Globals.c) require this file to be included to allow them to compile on their own.

GPSDEC.H
This contains the prototype declarations for functions that are called in more than one file. Functions only used within one file are declared in that file. All the .C files require this file to be included to allow them to compile on their own.

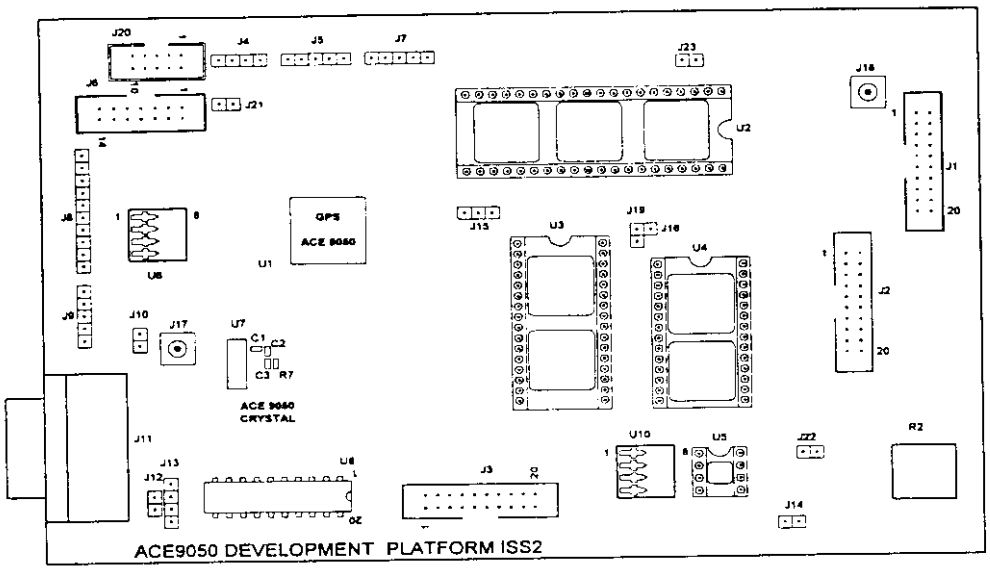
GPSDEMO.H
This contains all the defines used within the programmes to make the code more readable. It also contains the pre processor directive to determine the time window to validate a IRQ-WS interrupt. The defines are grouped as per the file they are predominately used in.

DRIVERS.H & HARDWARE.H
These are header files required by the WLC software.

BATCH files & LNK6303.XCL

The all.bat compiles & links all the files together. The C files are compiled to .R07 files which are linked to produce a .MOT file for loading a FLASH in the Motorola format. If a compiler error occurs in any of the files the linker won't be invoked. The LNK6303.XCL file has been edited to include the .R07 files for all the C files required to produce the software; both GPS & WLC files.

1.BAT:	Compile & link 1 file, named on command line
2.BAT:	As 1.BAT, but the errors get piped to ERRORS.TXT
ALL.BAT	Compiles & links all the files in the software.



NAME	DESCRIPTION	
U1	ACE 9050	
U2	6303 EMULATION SOCKET 40W DIL	
U3	EXTERNAL EPROM SOCKET 32W DIL	
U4	EEPROM SOCKET 28W DIL	
U5	I^2C BUS SOCKET 8W DIL	
U6	4 WAY SINGLE POLE SWITCHES	ACE9050 Mode Select
U7	8MHz CRYSTAL	
U8	RS232 DRIVER 20W DIL	
U10	4 WAY SINGLE POLE SWITCHES	
J1	20 WAY BOXED HEADER	LSA Data & Control Bus
J2	20 WAY BOXED HEADER	LSA Address
J3	20 WAY BOXED HEADER	LSA Emulation & Ports
J4	4 WAY HEADER PINS	Key Pad connector (input)
J5	5 WAY HEADER PINS	Key Pad Connector (Output)
J6	14 WAY BOXED HEADER	Radio Board Digital interface
J7	5 WAY HEADER PINS	input & Interrupt
J8	10 WAY HEADER PINS	Radio Port
J9	5 WAY HEADER PINS	Output port
J10	2 WAY HEADER PINS	Radio Clock Linker
J11	9 WAY D-TYPE PLUG	RS232
J12	2 WAY HEADER PINS	RS232 configure
J13	4 WAY HEADER PINS	RS232 Configure
J14	2 WAY HEADER PINS;	Supply Connection
J15	3 WAY HEADER PIN	FLASH Programming Vpp
J16	1 HEADER PIN	EEPROM Ready
J17	SMC CONNECTOR;	EXTERNAL CLOCK I/P
J18	SMC CONNECTOR;	EXTERNAL CLOCK FOR 6303 EMULATION
J19	2 WAY HEADER PINS	FLASH WEN Linker
J20	10 WAY BOXED HEADER	Radio Board Radio Interface
J21	2 WAY HEADER PINS	Radio Board Reset Linker
J22	2 WAY HEADER PINS	On Board Reset Linker
J23	2 WAY HEADER PINS	ICE Reset Linker
C1	10nF;	EXTERNAL ACE9050 Clock AC Coupling
C2,C3,R7	CRYSTAL SET-UP COMPONENTS	
R2	PUSH SWITCH	Push-To-Reset System switch

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