FCC Type Approval Application Information - QR450 Remote Data Radio (FCC ID:NI8QR450)

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(Version A)

Version History

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A	14 Nov 2014	DR	

Review History

Version	*Review Date*	*Reviewer(s)*	*Review Comment Summary*
A			

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References

All referenced Trio documents must have a registered document number

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Abbreviations

Abbreviation	*Description*
ADC	Analogue-to-Digital Converter
AFC	Automatic Frequency Control
BPS	Bits Per Second
CPM	Continuous Phase Modulation
CPLD	Complex programmable logic device
DAC	Digital-to-Analogue Converter
DSP	Digital Signal Processor
FCC	Federal Communications Commission
FM	Frequency Modulation
FPGA	Field Programmable Gate Array
IF	Intermediate Frequency
PA	Power Amplifier
PC	Personal Computer
PHY	Physical Layer
PIN	P-type semiconductor Intrinsic semiconductor N-type semiconductor
PLL	Phase Locked Loop
RX	Receiver
SDRAM	Synchronous Dynamic Random Access Memory
SMA	Sub-Miniature type A
TX	Transmitter

1 Introduction

This document covers the requirements or makes reference to the documents which fulfil the requirements of FCC application for type approval Section 2.963 Parts 1 to 12.

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2 FCC Application for type approval Section 2.963

Text in italic in this section is the requirement from Federal Communications Commission Section 2.963.

2.1 Part 1 (Types of emission)

Type(s) of emission.

The radio supports operation of the following types of emissions.

Description	Channel Bandwidth	Designator
8 kbps CPM 2 Level	12.5 kHz	11K2F1D
16 kbps CPM 4 Level	12.5 kHz	11K2F1D
24 kbps CPM 8 Level	12.5 kHz	11K2F1D
32 kbps CPM 16 Level	12.5 kHz	11K2F1D

Frequency range.

- 421 MHz to 512 MHz

There are 2 Hardware builds where some components may have slightly different values but are otherwise identical.

- 421 to 450MHz
- 450MHz to 512 MHz

2.2 Part 3 (Range of operating power)

Range of operating power and description of means provided for variation of operating power.

- Operating power 50mW (+17dBm) to 10W (+40dBm).
- Operating power is programmed to a value in the range above by the system integrator using a PC.

2.3 Part 4 (Maximum power rating)

Maximum power rating as defined in the applicable rules.

10W (+40dBm)

2.4 Part 5 (Voltage/Current of final PA)

The voltages applied to and currents into the several elements of the final radio frequency amplifying device for normal operation over the power range. Indicate whether these voltages and currents are AC or DC.

Power O/P	***Remote PA Voltage (PA Module)***	***Approximate Control Pin Voltage (In feedback loop)***	***Remote PA Current (PA Module)***
50 mW	12.5V DC	3.0V DC	1A DC
1W	13.8V DC	3.0V DC	1A DC
10W	13.8V DC	4.5V DC	3.0A DC

2.5 Part 6 (Function of each active circuit)

Function of each electron tube, semiconductor or other active circuit device.

Circuit Device	***Designator(s)***	***Function***
Microprocessor	U1	High Level Microprocessor runs operating system
Flash Memory	U2	Storage for U1.
Linear regulator	U3	Linear regulator for PLL charge pump supply
Switch mode power supply	U4	Power Supply to PA
Switch mode power supply.	U5	Supply for 1.2,1.8,3.3 and 5 volt rails

Circuit Device	*Designator(s)*	*Function*
Reset generator	U6	Shuts down radio when supply voltage out of spec.
Linear regulator	U7	Linear supply for 1.8 volt analogue rail.
Clock Distribution	U8	Distribution of 50 MHz clock.
I/Q (Quadrature) Modulator	U9	Modulator for transmitter.
Linear Regulator	U10	5 Volt Linear regulator for VCOs
DC Switch	U11,U13,U15, U17	Power Supply Switch for VCO
RF Switch	U12,U16	RF Switch to select VCOs
Frequency Synthesiser	U14	Frequency Synthesiser for RX VCO phase looked loop.
Frequency Synthesiser	U18	Frequency Synthesiser for TX VCO phase looked loop.
Ethernet PHY	U19,U20	Physical interface for LAN ports.
FPGA	U21	FPGA Implements modem DSP.
Digital to Analogue converter	U22	DAC for TX I/Q lines.
Digital to Analogue converter	U23	DAC Controls receiver functions and system reference.
Voltage reference	U24	3.0 volt reference for TX/RX
Microprocessor	U25	Microprocessor for low level radio functions.
DC Switch	U26	Power Supply switch for TX driver.
Temperature Sensor	U27	Monitors temperature of final RF power amplifier.
RF Switch	U28	Switches in/out 6 dB attenuator in TX path.
RF Amplifier	U29	RF Driver before final PA device.
Operational Amplifier	U30	Op amp for DC control in TX
Current Sensor	U31	Current Sensor for RF Power amplifier.
RF Switch	U32	Switches in/out 6 dB attenuator in feedback path.
RF Power detector	U33	RF Power detector for TX power monitoring.
RF Power detector	U34	RF Power detector for TX reverse power monitoring.
RF Attenuators	U35,U36	IF gain control for RX AGC.
RF Amplifier	U37,U38	IF Amplifier for RX.
High Speed Analogue to digital converter	U39	ADC for IF signal processing,

Circuit Device	*Designator(s)*	*Function*
RF Switch	U40,U42	Switches out RX low noise amplifier at high levels.
RF Amplifier	U41	Low noise amplifier for RX front end.
Operational Amplifier	U43	Provides buffering of RX tracking filter control lines.
RS232 Convertor	U44	Physical RS232 Interface.
RS485 Convertor	U45	Physical RS485 Interface.
Temperature Sensor	U46	Monitors temperature RX SAW filter.
Operational Amplifier	U47	General DC Buffering
Linear regulator	U48	Linear supply for SDRAM
Linear regulator	U51	Analogue supply for frequency synthesisers (PLLs)
Analogue Switch	U52	Selects reference output.
SDRAM	U53	Memory for U1
DC Switch	U54	Power Supply switch for RX.
Watch Crystal	Y1	Crystal for microprocessor real time clock.
Frequency Reference	Y2,Y4	Frequency references for RX/TX frequency synthesizer, ADC and FPGA.
Frequency Reference	Y3	Clock for Microprocessor (U1),FPGA,LAN Phy
Voltage controlled oscillator	OSC1,OSC2	VCO for Transmitter
Voltage controlled oscillator	OSC3,OSC4	VCO for Receiver
Power Fet	Q1	Switching transistor for U1
PNP Transistor	Q2	Switches DC Supply for reference buffers Q16,Q17
NPN Transistor	Q3	Capacitance Multiplier for PLL charge pump supply
PNP Transistor	Q4,Q7	Supply switch for Y2 and Y4.
NPN Transistor	Q5	Logic NOT for U6 input (PSU Shut down)
NPN Transistor	Q8	Switching DC rail for receiver.
MOSFET	Q9,Q10	Buffer for VCO sampling on RX/TX PLL
NPN Transistor	Q11	Capacitance Multiplier for TX driver supply
RF PA Module	Q12	Final transmitter power amplifier
NPN Transistor	Q13	DC Switching for PIN Diode TX/RX switch
MOSFET	Q14	Post Mixer amplifier for RX mixer.

Circuit Device	*Designator(s)*	*Function*
MOSFET	Q15	Clock Buffer for receiver's ADC
NPN Transistor	Q16,Q17	Reference Buffers
NPN Transistor	Q18	DC Switching to remove final PA bias.
NPN Transistor	Q19	Switching DC rail for receiver
NPN Transistor	Q20	Switching Power LED supply.
MOSFET	Q21	Transmit VCO Buffer.
PNP Transistor	Q26	Switching LED supply
NPN Transistor	Q27	Current limiting for USB supply
NPN Transistor	Q28	Switching DC rail for receiver.
NPN Transistor	Q30,Q33	RS232 DCD Interface
PNP Transistor	Q31,Q32	RS232 DCD Interface
PIN Diodes	D23,D25	PIN Diode TX/RX switching.

2.6 Part 7 (Complete circuit diagram)

Complete circuit diagram.

- See schematics provided

2.7 Part 8 (Instruction books)

Instruction books. If the instruction book(s) is not available when the application is filed a set of draft instructions should be provided and the complete instruction book should be submitted as soon as available.

- See Q series User Manual provided

2.8 Part 9 (Tune up procedure)

Tune up procedure over the power range or at specific operating power levels.

- Refer to RF Parameters setup procedures in the Q Series User Manual
- There are no mechanical adjustments required.
- Calibration and alignment performed is performed using “Production tools” software at the factory.

2.9 Part 10 (Description of circuitry)

A description of all circuitry and devices provided for determining and stabilising frequency.

- **Frequency Reference –** A pair of Commercial VTCXO 20.0MHz/20.1 MHz frequency reference modules are used to provide a stable reference to the transmit synthesiser/PLL. The VTCXOs also have a fine trim input which is controlled by a microprocessor analogue output, the initial level that the trim input is set to is determined during factory setup. The TCXO module is internally temperature compensated to better than 0.5ppm.
- **Transmit VCO –** The transmit VCO is phased locked to the main reference with a PLL. If the PLL is out of lock the transmitter is prevented from operating.

2.10 Part 11 (Description of circuitry)

A description of any circuits employed for suppression of spurious radiation, for limiting modulation, and for limiting the operating power.

- **Low pass filter –** The low pass filter consists of 2 stages with a PIN switch in between. Each stage has a commercial high tolerance wire wound inductor, high Q shunt capacitors. Frequency notches (Zeros) are implemented by high Q capacitors in parallel with the inductors, this enables a sharp cut off for harmonics generated by the PA.

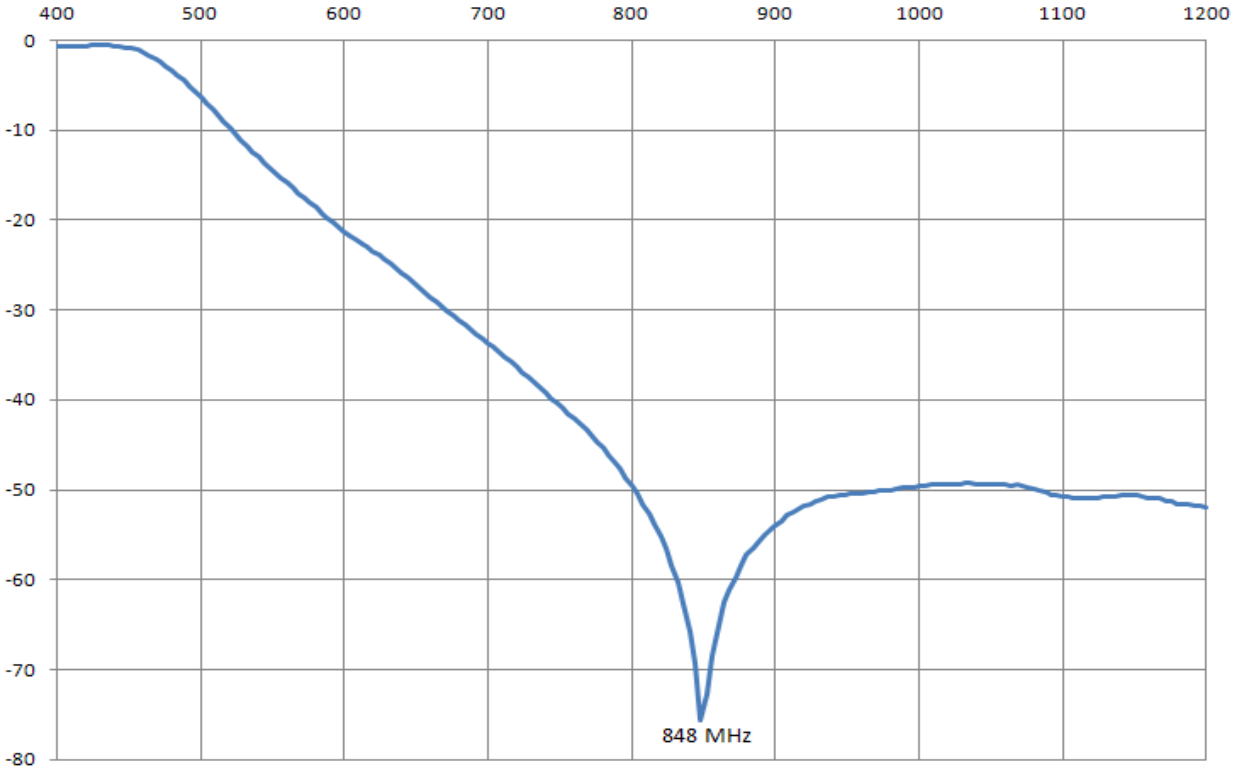

Figure 1 – Low-Pass Filter stop-band response for Low Band builds (Radios covering 421-450MHz)
(Horizontal axis in frequency in MHz Vertical axis is transmission in dB)

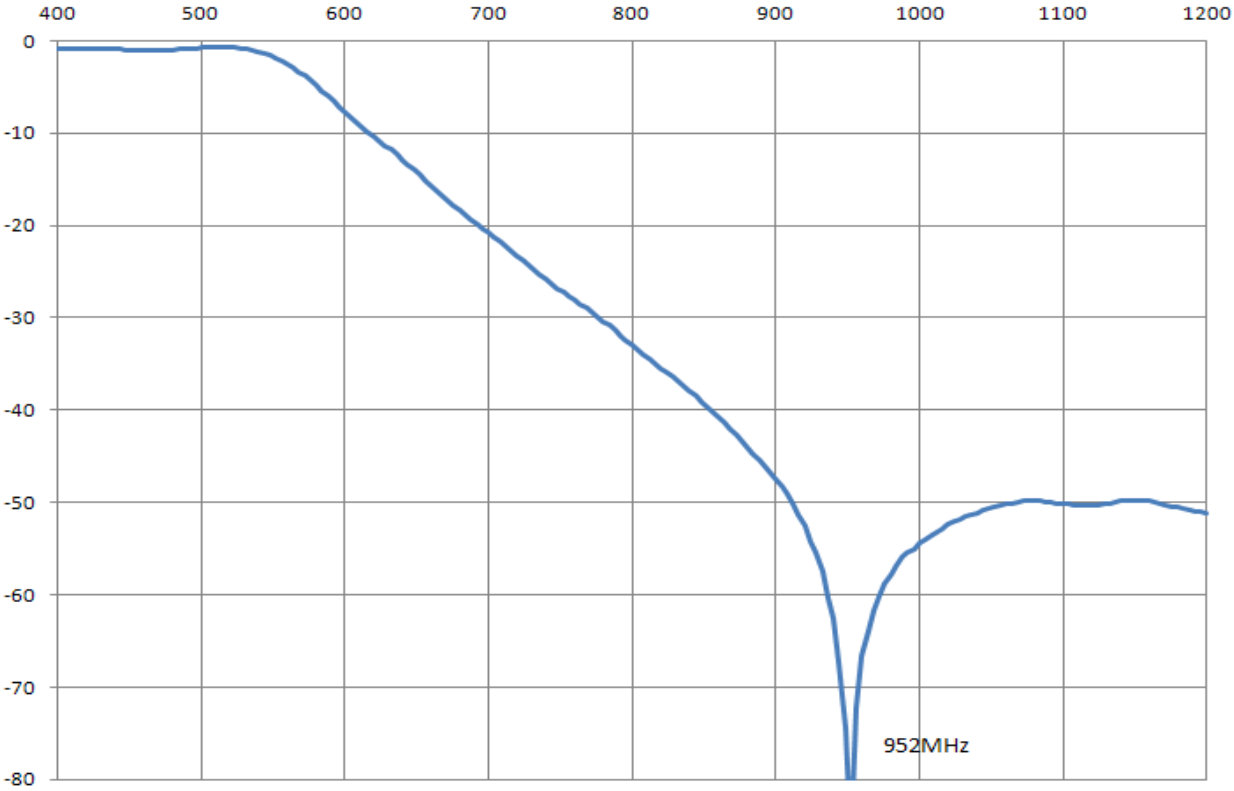

Figure 2 – Low-Pass Filter stop band response for High Band Builds (Radios covering 450-512MHz)
(Horizontal axis in frequency in MHz Vertical axis is transmission in dB)

- **Modulation:** Modulation is generated numerically in the FPGA and is therefore not subjected to component uncertainties. As digital modulation is employed a limiter is not required.

Numerically Generated I-Q Modulation

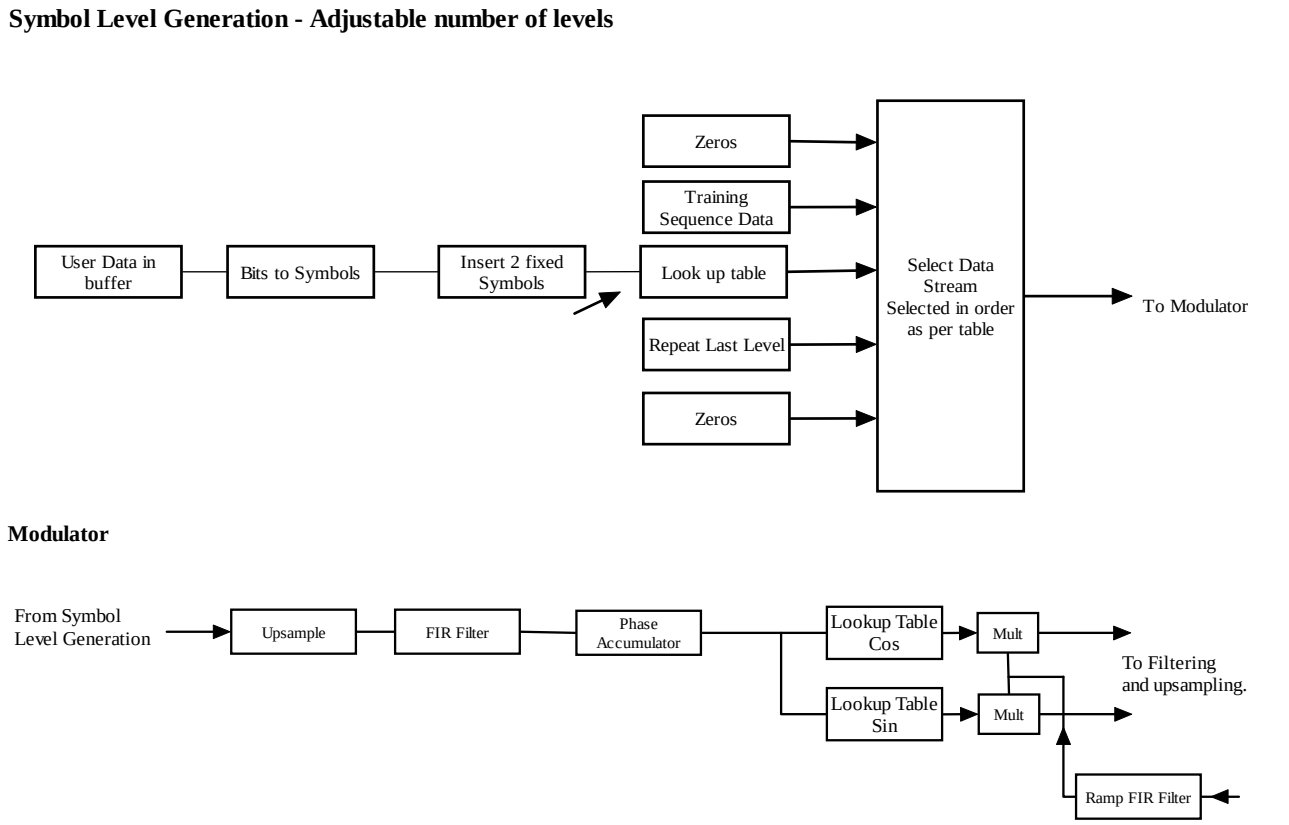

Figure 3 - Numerically Generated I-Q CPM Modulation

Modulation is controlled by a FPGA implementing DSP algorithms as shown in block diagram form above.

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- **RF power control:** The power is controlled by a Cartesian feedback loop as implemented in the commercially available IQ modulator. The power is set by the IQ signal levels and the settings of the IQ modulators internal and external attenuator settings. The power level is set by software using a calibrated power measuring instrument in production.

2.11 Part 12 (Identification label)

A photograph or drawing of the equipment identification plate or label showing the information to be placed thereon.

Please see Label drawing provided.