TECHNICAL OPERATIONAL DESCRIPTION

FCC ID: NCMOGE0301

About this document

Overview and Purpose

This document describes the most important technical operation descriptions of GE0301. This document will be used for FCC approval of GE0301.

Confidentiality

Version History

Date	Version	Author(s)	Revision(s)	Remarks
June 18., 2007	V01 – D1	J. Boeckx		Initial version
June 20., 2007	V01 – D2	J. Boeckx		
June 20., 2007	V01 – F1	J. Boeckx		Final Version
August 8., 2007	V02 – F1	J. Boeckx		Final Version extra comments on antenna part

1 GENERAL

1.1 Product Description

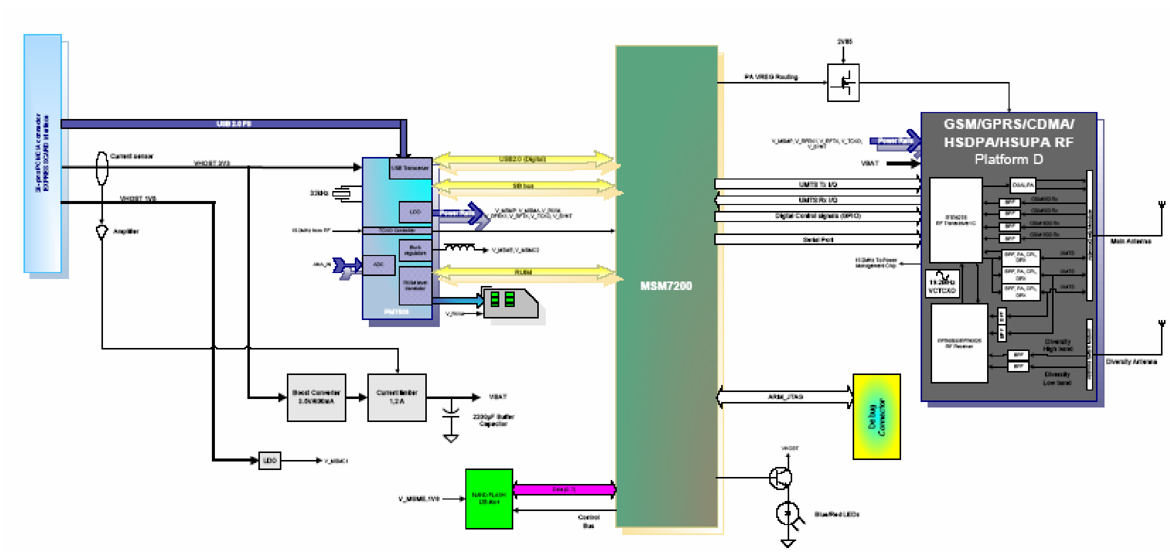
The OPTION GlobeTrotter Express HSUPA E (GE0301) is a quad-band PC Card supporting GSM/(E)GPRS in the 850, 900, 1800 and 1900 MHz frequency bands and WCDMA in the 850, 1900 and 2100 MHz frequency bands. In addition, this device supports HSDPA category 8, HSUPA Category 5 and antenna receiver diversity (supporting diversity on 2100 MHz).

The card is an (E)GPRS class 12 terminal supporting circuit switched (CS) and packet switched (PS) data.

The PC card has a foldable antenna with one dedicated position and provisions for an external antenna. The external GSM/EGPRS/WCDMA antenna connector can be used to connect to external test equipment. The antenna connector, when in use, disconnects the internal modem antenna.

The electronic functions are divided into an RF and a logic part. The PC card consists of one main PCB with components placed on both sides.

The diagram below shows the high level functional blocks.



Block Diagram

1.2 Mechanical Construction

Mechanically the data card is built up as an Express Card

Dimensions and weights:

Length: 95 mm

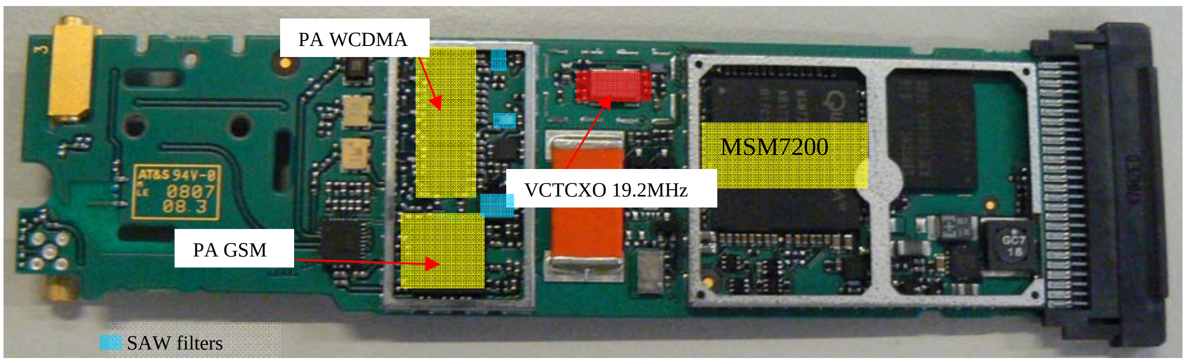
Width: 54 mm

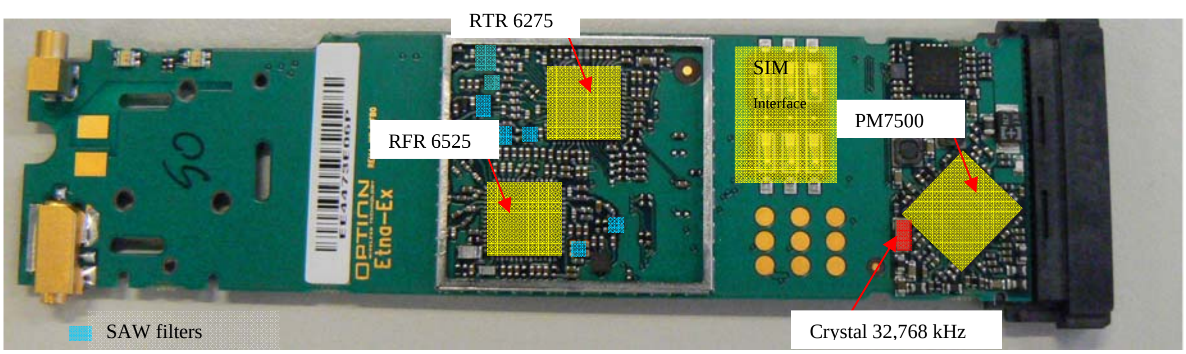
Thickness (max): 4 mm

Weight: 41g

1.3 Main Circuit Board

This diagram provides the location information for the hardware blocks described in this document.



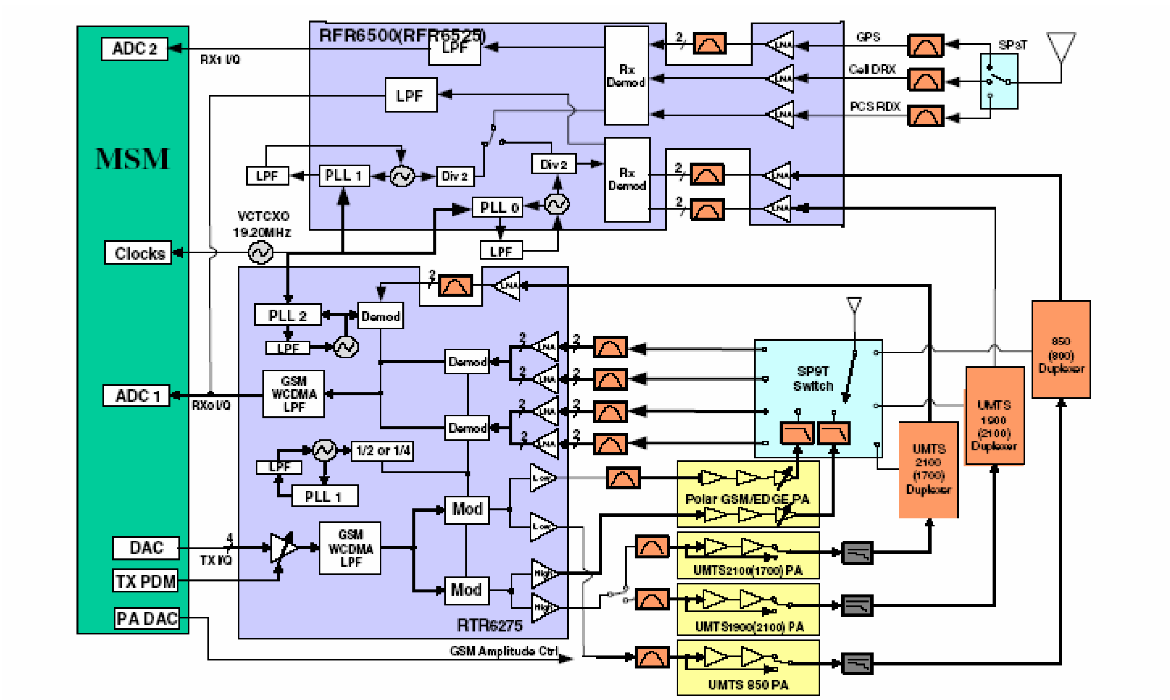


These are internal pictures with an indication of the individual components: oscillators, antenna switch, SIM interface, power amplifiers, SAW filters, Power Management chipset, Baseband processor, etc.

The receivers are located at the RFR6525 and at the RTR6275. The transmitter is located at the RTR6275.

2 GSM / EGPRS / WCDMA Transceiver

The following block diagram shows the high level block within the GSM/EGPRS/WCDMA radio transceiver. (RFR6525 and RTR6275)



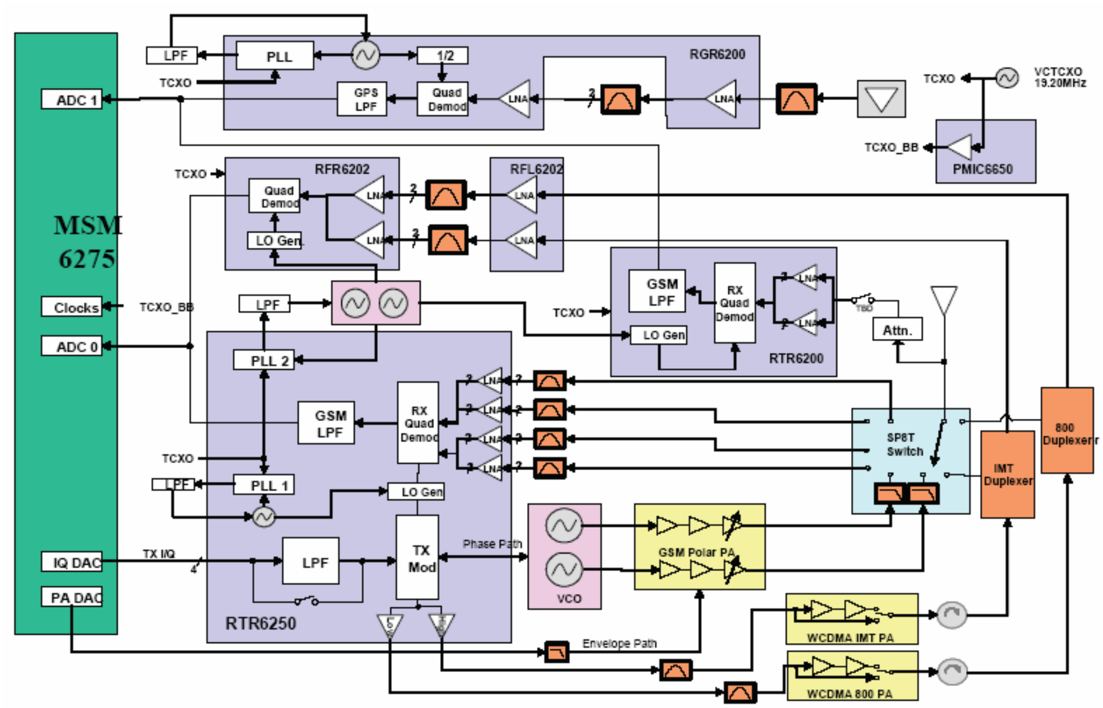
2.1 RF parts

Transceiver

The RTR6275 transceiver solution uses low-cost RF CMOS process technology, a low-cost, high-volume digital process technology used for a majority of today's digital computer microchips. The RTR6275 integrates low-noise amplifiers (LNA), receivers, transmitters, voltage controlled oscillators (VCO) and phase locked loops (PLL), and is packaged in an 8mm x 8mm, 56-pin Quad Flat No-Lead (56QFN) package for further space savings advantages.

The RTR6275 integrates a Quadband GSM/GPRS/EGPRS receiver, one band UMTS receiver and a GSM/GPRS/EGPRS transmitter.

All receivers and the UMTS transmitter use the radioOne ZIF architecture to eliminate intermediate frequencies, directly converting signals between RF and baseband. The quad-band GSM transmitters use a baseband-to-IF up conversion followed by an offset phase-locked loop that translates the GMSK-modulated or 8-PSK-modulated signal to RF. The polar modulation technique is used to generate the required EDGE signal. A calibration receiver path is deployed for achieving Polar transmitter calibration in the design.



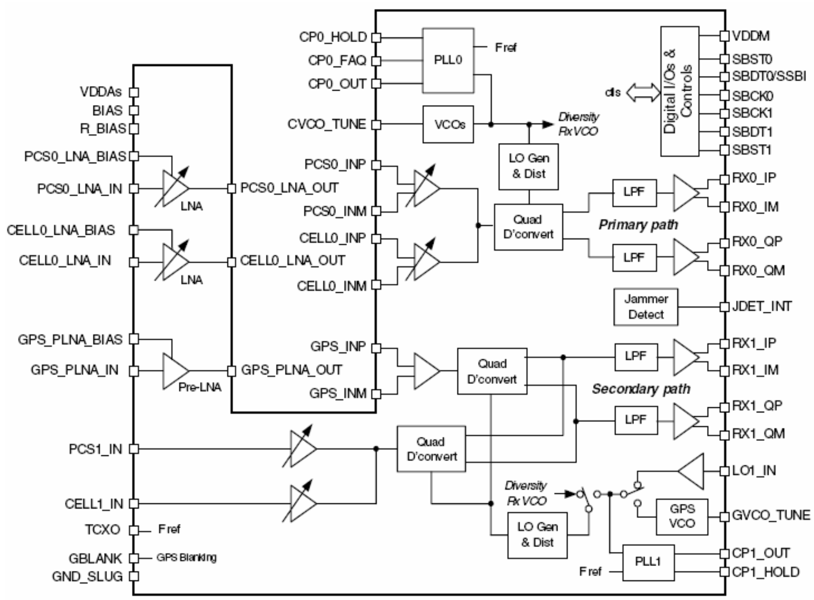
High level RTR6275 functional block diagram

Receiver

The RFR6525 solution incorporates dual-band, dual-diversity receive components (receivers for both cellular and PCS bands) into a single chip - reducing bill-of-materials (BOM) costs and enabling smaller form factor designs. This device also integrates low noise amplifiers, direct down converters, phase locked loop and voltage control oscillator.

The RFR6525 IC is also an integral component of diversity-capable radioOne CDMA/UMTS chipsets that can also be used as a substitute for the previous generation RFL-plus-RFR combination in multi-band applications. All radioOne ICs are highly integrated and fulfill specific functions; functional requirements are partitioned between the ICs to yield complete, optimal transceiver implementations. Overall radioOne performance depends on the combined, complementary performance of all ICs in the chipset.

The RFR6525 IC provides five RF inputs: four for CDMA/UMTS and one for GPS. There are two primary CDMA/UMTS inputs: one for cellular bands and one for PCS bands. Both primary CDMA/UMTS inputs include a gain-stepped LNA that is followed by an off-chip inter-stage filter, and then a gain-stepped second-stage RF amplifier. There are also two secondary CDMA/UMTS inputs, cellular and PCS, each with a gain-stepped RF amplifier. The GPS input is very similar to the primary CDMA/UMTS paths: a pre-LNA, off-chip inter-stage filter, and second-stage RF amplifier.



RFR6525 Block Diagram

2.1.1 GSM 850

The GSM/EGPRS 850, receiver has frequency channels, with 200 kHz separation, from 869.2 to 893.8 MHz. The transmitter frequency channels, with the same separation, are 824.2 to 848.8 MHz. This gives 124 frequency channels.

2.1.2 EGSM 900

The GSM 900, including E-GSM, receiver has frequency channels, with 200 kHz separation, from 925.2 to 959.8 MHz. The transmitter frequency channels, with the same separation, are 880.2 to 914.8 MHz. This gives 174 frequency channels.

2.1.3 DCS 1800

The GSM 1800 receiver has frequency channels, with 200 kHz separation, from 1805.2 to 1879.8 MHz. The transmitter frequency channels, with the same separation, are 1710.2 to 1784.8 MHz which gives 374 frequency channels.

2.1.4 PCS 1900

The GSM 1900 receiver has frequency channels, with 200 kHz separation, from 1930.2 to 1989.8 MHz. The transmitter frequency channels, with the same separation, are 1850.2 to 1909.8 MHz which gives 299 frequency channels.

2.1.5 WCDMA 850

The UMTS 850 receiver has frequency channels, with 200 kHz separation, from 871,4 MHz to 891,6 MHz. The transmitter frequency channels, with the same separation, are 826,4 to 846,6 MHz which gives 204 frequency channels.

2.1.6 WCDMA 1900

The UMTS 1900 receiver has frequency channels, with 200 kHz separation, from 1932,4 MHz to 1987,6 MHz. The transmitter frequency channels, with the same separation, are 1852,4 to 1907,6 MHz which gives 554 frequency channels.

2.1.7 WCDMA 2100

The UMTS 2100 receiver has frequency channels, with 200 kHz separation, from 2112,4 MHz to 2167,6 MHz. The transmitter frequency channels, with the same separation, are 1922,4 to 1977,6 MHz which gives 554 frequency channels.

2.1.8 HSDPA

HSDPA will go beyond the data rates of UMTS, with an average throughput of 800 kbps and even 1.5 Mbps in the field, thanks to high peak data rates with 3.6 Mbps for a Category 6 Mobile and up to 14.4 Mbps for a Category 10 Mobile. In addition, HSDPA provides lower latency with Round Trip Delays of 70 ms, enabling great interactive applications like multi-user gaming.

HS-DSCH category	Maximum number of HS-DSCH codes received	L1 peak rates (Mbps)	QPSK/16QAM
Category 1	5	1.2	Both
Category 2	5	1.2	Both
Category 3	5	1.8	Both
Category 4	5	1.8	Both
Category 5	5	3.6	Both
Category 6	5	3.6	Both
Category 7	10	7.3	Both
Category 8	10	7.3	Both
Category 9	15	10.2	Both
Category 10	15	14.0	Both
Category 11	5	0.9	QPSK
Category 12	5	1.8	QPSK

On MSM7200 chipset, Qualcomm implemented HSDPA R5 Category 8 (up to 7.2MBps).

2.1.9 HSUPA

The table below indicates the different E-DCH categories.

E-DCH category	Maximum number of E-DCH codes transmitted	Minimum spreading factor	Support for 10 and 2 ms TTI E-DCH	Maximum number of bits of an E-DCH transport block transmitted within a 10 ms E-DCH TTI	Maximum number of bits of an E-DCH transport block transmitted within a 2 ms E-DCH TTI
Category 1	1	SF4	10 ms TTI only	7110	-
Category 2	2	SF4	10 ms and 2 ms TTI	14484	2798
Category 3	2	SF4	10 ms TTI only	14484	-
Category 4	2	SF2	10 ms and 2 ms TTI	20000	5772
Category 5	2	SF2	10 ms TTI only	20000	-
Category 6	4	SF2	10 ms and 2 ms TTI	20000	11484
NOTE: When four codes are transmitted in parallel, two codes shall be transmitted with SF2 and two with SF4.					

On MSM7200, and consequently also on our datacard, category 5 is used.

2.1.10 Frequency generation

A voltage controlled temperature compensated crystal oscillator (VCTCXO), running at 19.2 MHz, is used as a reference for all frequencies generated in the GSM/EGPRS/WCDMA transceiver. The external VCTCXO signal is input to one of the crystal oscillator input pins on the RF transceiver. The internal oscillator serves as a clock buffer in this configuration. The voltage control signal for the VCTCXO comes from the Logic part.

We add the main specifications of the 5405ASX3SVT Kyocera crystal oscillator that is used on this datacard as a reference:

Symbol	Item	Condition	Specification	Unit	Remarks
Vcc	Power Supply Voltage		2.8+/-0.14	V	
F0	Nominal Frequency		19.200000	MHz	
Topr	Operating Temperature		-30 to +80	deg.C	
Tstg	Storage Temperature		-40 to +85	deg.C	
Vout	Output Voltage	Load:10pF/10k ohm	0.8(min)	V	Ta=-30 to 80deg.C
Icc	Power Supply Current		1.5(max)	mA	
f0	Frequency Tolerance	Preset Frequency and after 2 Reflow soldering	+/-2.5	ppm	Ta=25+/-2deg.C Vcon:1.4V
df/F	Frequency Stability	vs Temp -30 to +80deg.C	+/-2.0	ppm	
		vs Load 10pF+/-10% 10Kohm+/-10%	+/-0.2	ppm	
		vs Voltage 2.8V+/-5%	+/-0.3	ppm	
---	Frequency Stability Slope	Ta=-10 to +60deg.C	+/-0.15	ppm	
		Ta=-30 to -10, +60 to +80deg.C	+/-0.3	ppm	
---	Allan Variance	τ=1sec	0.5(max)	ppb	
dfag	Frequency Aging Rate	Ta=25+/-5deg.C	+/-0.7	ppm/Y	One Year
df/V	Voltage Control Range	Vcon=0.4V	-12 to -5.5	ppm	ref:Vcon=1.4V
		Vcon=2.4V	+5.5 to +12	ppm	
Tst	Start up Time	90%*Vp-p(min) Within +/-0.5ppm	3.0(max)	msec	
---	Harmonics		-5.0(max)	dBc	
---	SSB Carrier Noise	@10Hz offset	-86(max)	dBc/Hz	
		@100Hz offset	-113(max)	dBc/Hz	
		@1kHz offset	-130(max)	dBc/Hz	
		@10kHz offset	-144(max)	dBc/Hz	
		@100kHz offset	-144(max)	dBc/Hz	

Specifications Kyocera crystal oscillator

2.1.11 GSM / EGPRS / WCDMA Receiver

2.1.11.1 GSM / EGPRS Receiver

The GSM/EGPRS receiver is located at the RTR6275.

The first stage of the receiver is an antenna front-end switch which directs the signal to one of four SAW pre-selector filters. One SAW filter is included for each of the four bands. The pre-selector filter suppresses unwanted frequencies. The receiver is a homodyne receiver. The local oscillator is generated by a frequency synthesizer, which allows the receiver to be set at frequencies in intervals of 200 kHz. The synthesizer is controlled from the logic part.

Quadrature drive for the mixers is achieved by 90 degree splitters on the VCO output to generate on-channel LO signals for the 1800/1900 MHz and 850/900 MHz receive bands. Conversion to baseband I and Q channels is performed in the mixer stage. There are two integrated receiver mixer pairs, one for high band (1800/1900 MHz) and the other for low band (850/900 MHz). The output of each mixer pair feeds a common baseband circuit.

2.1.11.2 WCDMA receiver

WCDMA receiver part has been split up in two parts. One band WCDMA receiver is positioned on the RTR6275, two bands WCDMA, additionally with received diversity, are positioned on the RFR6525.

2.1.11.2.1 WCDMA receiver on RTR6275

The RTR6275 IC accepts its UMTS 2100/1900/1800 input signal from the handset RF front-end filters. The UMTS Rx input is provided with an on-chip LNA that amplifies the signal before a second stage filter that provides differential downconverter. This second stage input is configured differentially to optimize second-order intermodulation and common mode rejection performance. The gain of the UMTS frontend amplifier and the UMTS second stage differential amplifier are adjustable, under MSM control, to extend the dynamic range of the receivers.

The second stage UMTS Rx amplifiers drive the RF ports of the quadrature RF-to-baseband downconverters. The downconverted UMTS Rx baseband outputs are routed to lowpass filters having passband and stopband characteristics suitable for UMTS Rx processing. These filter circuits allow DC offset corrections, and their differential outputs are buffered to interface shared with GSM Rx to the MSM IC. The UMTS baseband outputs are turned off when the RTR6275 is downconverting GSM signals and on when the UMTS is operating.

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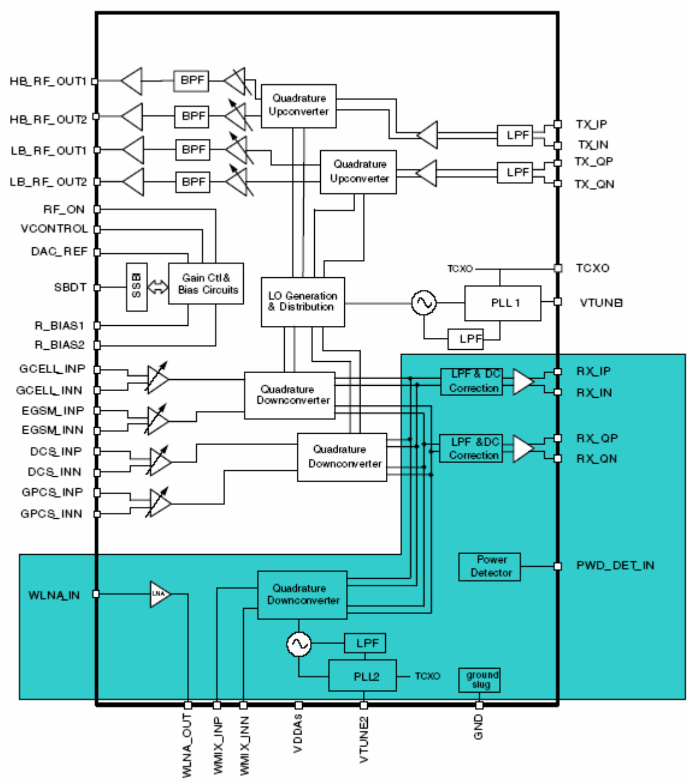


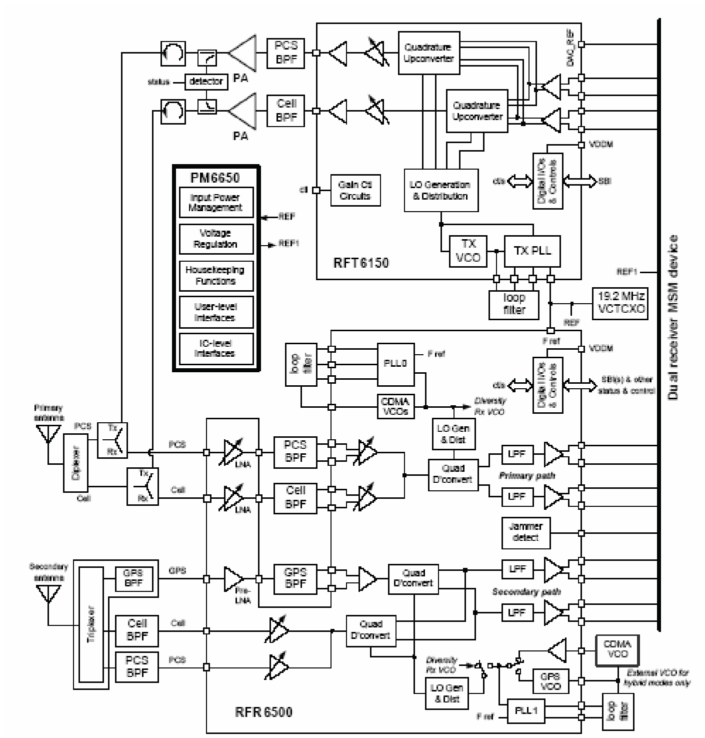
Receiver on RTR6275

2.1.11.2.2 WCDMA receiver on RFR6525

The two primary CDMA/UMTS input paths share a single RF-to-baseband quadrature downconverter; only one input path is active at a time. The downconverter outputs are routed to baseband circuits, including in-phase (I) and quadrature (Q) lowpass filters followed by baseband amplifiers that drive the MSM device's primary receiver input. This baseband interface (RX0) always supports the active CDMA/UMTS mode.

2.1.11.2.3 WCDMA receiver diversity on RFR6525

The two secondary CDMA/UMTS input paths stay on-chip; off-chip inter-stage filtering is not required. The two LNA outputs are routed to a single RF-to-baseband quadrature downconverter; again, only one LNA is active at a time. The GPS input path is followed by a dedicated downconverter. The GPS downconverter and secondary CDMA/UMTS downconverter outputs are multiplexed to drive a single set of baseband filter and buffer circuits. The secondary baseband output (in-phase and quadrature differential signals) is routed through the RX1 pins to the MSM device for further processing. This baseband interface supports the CDMA/UMTS or GPS mode for whichever mode is active on the secondary path.



Receiver diversity functional block diagram

2.1.12 GSM / EGPRS / WCDMA Transmitter

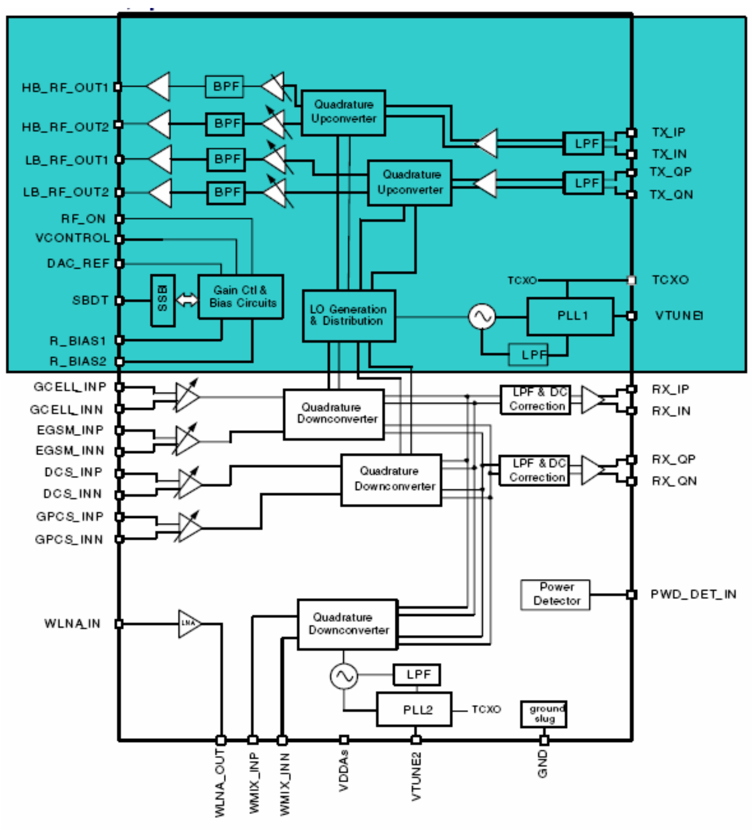
The RTR6275 transmitter includes four transmit signal paths (two high bands and two low bands) supporting multibands and multimodes GSM/GPRS/EDGE polar transmit and WCDMA/HSDPA/HSUPA transmitter architectures.

The transmit path begins with differential baseband signals (I and Q) from the MSM device. These analog input signals are buffered, filtered by low-path filter, corrected for DC offsets, amplified, and then applied to the quadrature upconverter mixers.

The upconverter outputs are amplified by multiple variable gain stages that provide transmit AGC control. A pulse density modulated (PDM) signal coming from the MSM IC is used to generate the gain range control signal. The AGC outputs are then applied to the high-band and low-output driver amplifiers; the specified driver amplifier output level is achieved while supporting the GSM/EDGE and UMTS transmit standard's requirements for GSM ORFS, carrier and image suppression, WCDMA ACLR, spurious emissions, Rx-band noise, and so forth.

The low-band drive amplifiers are used to transmit the polar phase modulated (PM) signal for GSM/EDGE 850/900 while the high-band driver amplifiers are for the GSM/EDGE 1800/1900. By using the radioOne architecture, the same high-band transmit path can be used to transmit the UMTS 2100/1900/1800 signal, and the low-band transmit path can be used to transmit the UMTS 800/850 signal, depending on the application.

The envelope path is used in polar mode of operation for GSM and EDGE. Input from the MSM IC, the baseband envelope (AM) current signal, is applied directly to the ramp control pin of the GSM/EDGE polar PA to modulate the power supply of the PA so that the polar modulated GSM/EDGE signal in the MSM can be recovered and transmitted.



Transmitter on RTR6275

2.1.13 Variable Gain Amplifier

The RF VGA stage is a quad-band dual PA driver amplifier for GSM850/900/1800/1900 with low noise limiting function in GMSK mode and linear VGA in 8PSK mode (EDGE). Together with the transceiver ASIC, a direct conversion transmitter system is formed. This amplifier provides a high output power to drive the PA. In linear transmit systems (e.g. 8PSK) the transmit power can be adjusted by the VGA function. The VGA circuit includes matching networks for the inputs and outputs.

2.1.14 Power Amplifier

2.1.14.1 Power Amplifiers UMTS

2.1.14.1.1 U1900

The Anadigics AWT6278R PA incorporates ANADIGICS' HELP3TM technology to provide low power consumption without the need for an external voltage regulator. The device is manufactured on an advanced InGaP HBT MMIC technology offering state-of-the-art reliability, temperature stability, and ruggedness. There are three selectable bias modes that optimize efficiency for different output power levels, and a shutdown mode with low leakage current, increase handset talk and standby time. The self-contained 4 mm x 4 mm x 1.1 mm surface mount packages incorporates matching networks optimized for output power, efficiency, and linearity in a 50 Ω system.

2.1.14.1.2 U2100 & U850

The ACPM-7881 is a high performance W-CDMA power amplifier module offered in a 4x4x1.1mm package. Designed around Agilent Technologies' GaAs Enhancement Mode pHEMT process, the ACPM-7881 offers premium power added efficiency and linearity in a very small form factor.
The PA is fully matched to 50 Ohms on the input and output.

The amplifier has excellent ACLR and efficiency performance at max Pout, 28.5dBm, and low quiescent current (50mA) with a single bias control voltage, Vctrl = 2.0V. No regulated voltages are required to set the bias; Vdd2 can be connected directly to the battery.

Designed in a surface mount RF package, the ACPM-7881 is very cost and size competitive.

2.2 Logic part

2.2.1 Functions

The purpose of the logic part is to control and monitor the transmission and reception functions of the modem and to maintain contact with the network. The logic therefore has links to all the relevant parts of the radio. Its functions, with reference to the radio, include selection of radio channel and control of the transmitter power. It also generates the base-band modulation after burst building, encryption, channel coding and demodulates the received base-band signal including equalization, decryption and channel decoding.

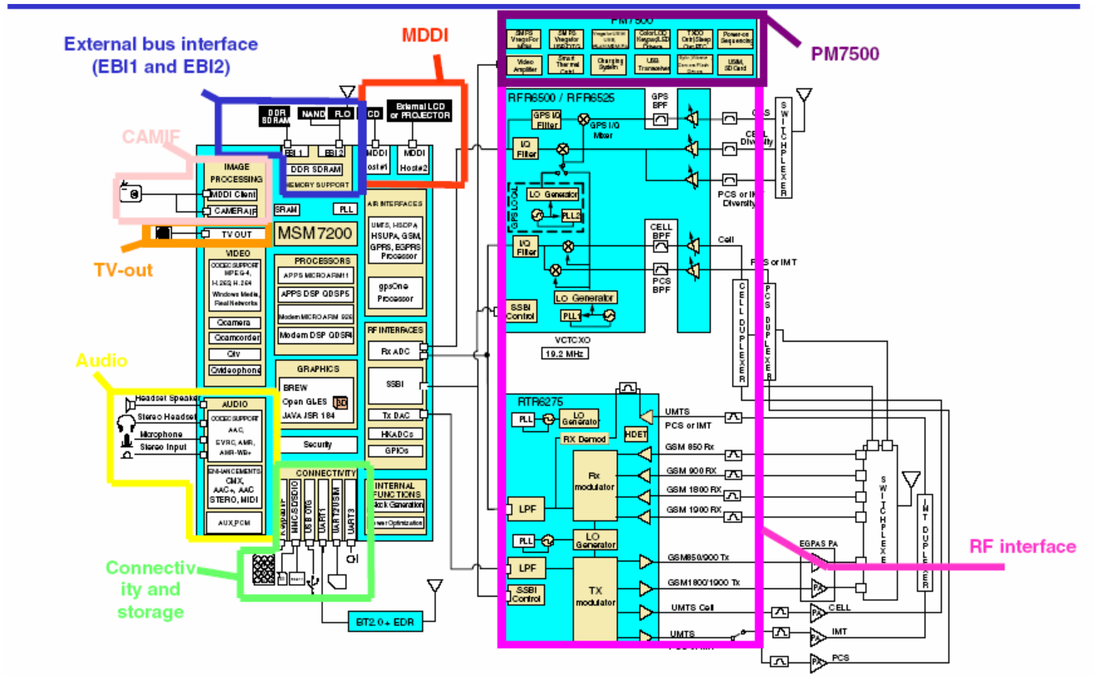
The external tasks of the logic part include monitoring and control of links with the control unit and power supply and also the communication to the SIM and external units connected to the external connectors.

The Logic part handles internal power supply control. The Logic part also includes a 32.768 kHz XTAL used for the real time clock and sleep timing.

QUALCOMM's PM7500™ IC is a member of QCT's family of advanced power management chips, providing a highly optimized, high-quality systems solution for high-end mobile handsets when interfaced with Convergence Platform Mobile Station Modem™ (MSM™) chipsets. The PM7500 solution integrates all power management, general housekeeping, and functions supporting handset-level user interfaces into a single mixed-signal IC, including charging functions and voltage regulation for the various Convergence Platform MSM products, radioOne® RF chips and all other MSM-supported peripheral features designed for 3G wireless devices.

2.2.2 Baseband Processor

The Baseband Processor MSM7200 contains the following hardware functions:



MSM7200 and his interfaces

Transceiver Control

The Baseband Processor MSM7200 has an interface to operate the RF transceiver ASIC.

Automatic Frequency Control (AFC)

The baseband MSM7200 maintains an automatic frequency control algorithm that computes frequency corrections for the external 19,2 MHz voltage controlled crystal oscillator. Frequency error is due primarily to temperature and Doppler variations. The baseband ASIC adjusts the oscillator frequency by applying an updated control voltage for the VCXO using the AFC DAC.

Automatic Gain Control (AGC)

The RF transceiver utilizes a programmable Gain Amplifier (PGA) in the IF stage to compensate for the very wide range of average received signal strength that is possible for the GSM radio channel. The software maintains AGC algorithms, which generate updates to the desired PGA setting to maintain a target signal level in the receiver. Dynamic General Purpose Output (GPO) pins are used to generate the digital control signals for the AGC. GPO pins also support gain control in the LNA for variable LNA gain.

Power Amplifier Ramping Control

The Power Amplifier (PA) output must be ramped up and down during burst transmission, and the ramping profile must be stringently controlled to meet GSM specifications of the spectral mask and time domain template for the signal envelope. The ramping profile is downloaded into the ramping RAM, which provides 16 ramp-up values and 16 ramp-down values. A state machine causes the RAM addresses to be scanned at the appropriate time and rate with interpolation samples inserted between successive readout values. The digital ramping samples are converted to an analogue PA control signal by the PA DAC.

Frequency Synthesizer Control

A serial interface controls the transceiver frequency synthesizer for both transmit and receive modes.

Auxiliary Monitoring

The ADC has multiplexed inputs brought out to five pins on the baseband. The ADC is used for temperature and voltage monitoring on the transceiver.

SIM Card Digital Interface

The SIM interface on the baseband interfaces with the SIM card through a level converter IC. The SIM interface automatically adapts to any of two SIM card voltages: 3V or 1.8V. The SIM interface can put the SIM into GSM stop-clock mode to save power.

Transceiver I/Q Analogue Interface

The baseband CODEC interfaces with the transceiver baseband I and Q analogue signals for the uplink and downlink. The baseband receive operation, automatic calibration is performed for compensation of I and Q biases generated in the baseband circuitry or the RF/IF path. For baseband transmit operation, automatic calibration is similarly performed.

UART

Two UARTs are utilized in the design. One is for communications and control and one is for debug logging. The main UART signals are channelized per the GSM 07.10 multiplex protocol.

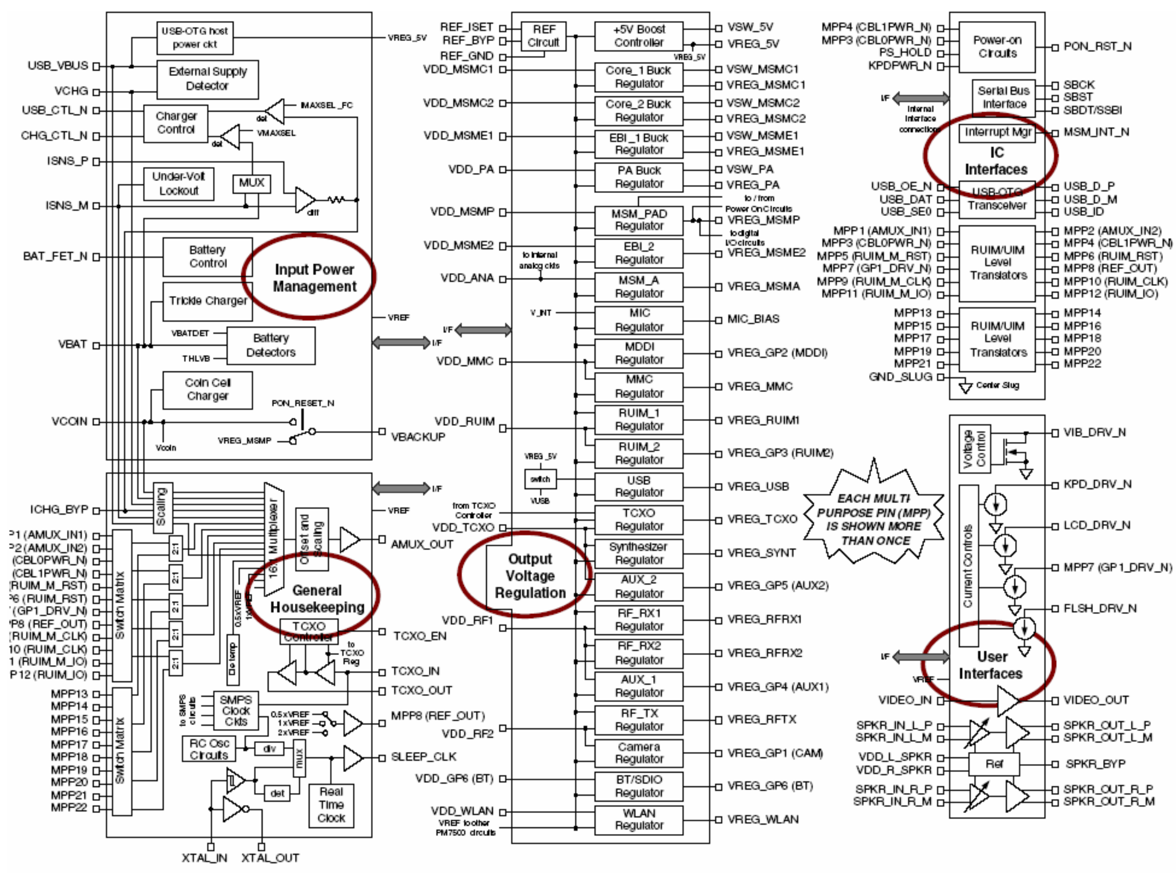
General Purpose I/O

Programmable GPIO signals are used for special functions such as SIM power control

2.2.3 Power management IC

The PM7500 IC integrates advanced capabilities such as TV-out amplifier, camera flash support, full charging system, backlighting, USB On-the-Go (OTG) transceiver and stereo far-field speaker amplification. Independently controllable buck regulators are designed specifically to support the multiple power regimes of the Company's Convergence Platform MSM solutions resulting in optimized system power consumption, while an additional 21 fully programmable regulators support the remainder of the chipset's numerous other functions. The PM7500 IC features a compact 9mm x 9mm package and a high level of integration in order to provide support for advanced wireless capabilities with fewer external components, delivering reduced bill-of-materials costs and quicker time to market

The MSM7200 chipset supports data rates of 7.2 Mbps on the downlink and up to 5.76 Mbps on the uplink for speeds that are faster than wireline broadband connections. Part of the Convergence Platform, the MSM7200 also supports third-party operating systems to further merge consumer electronics features with wireless functionality

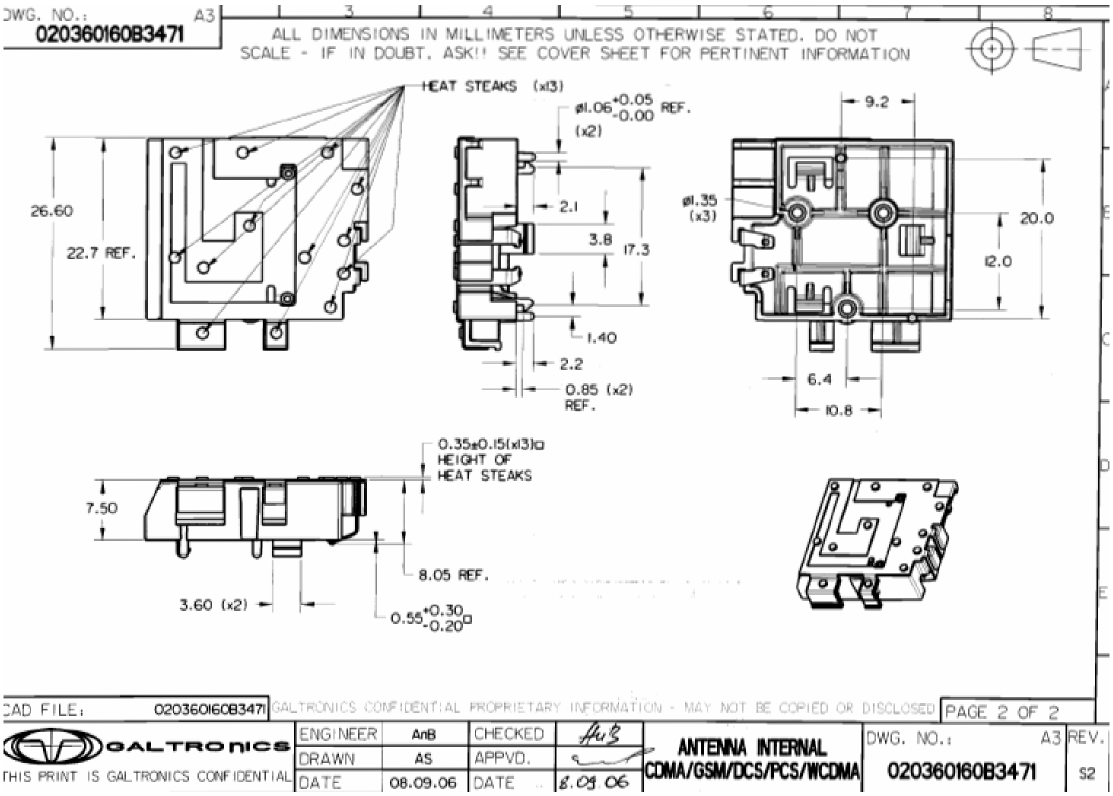


Block diagram PM7500

2.3 Antenna

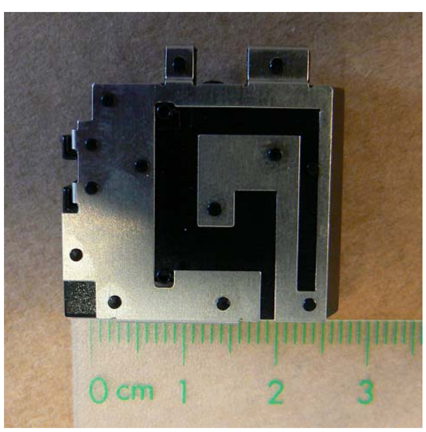
As an internal antenna, we use Galtronics.

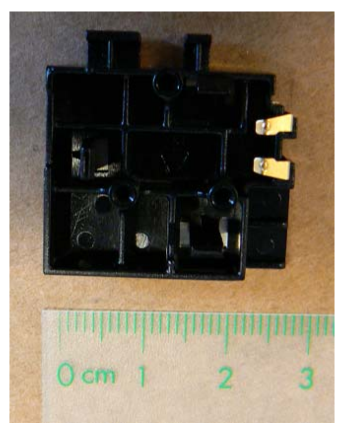
2.3.1 Antenna specifications



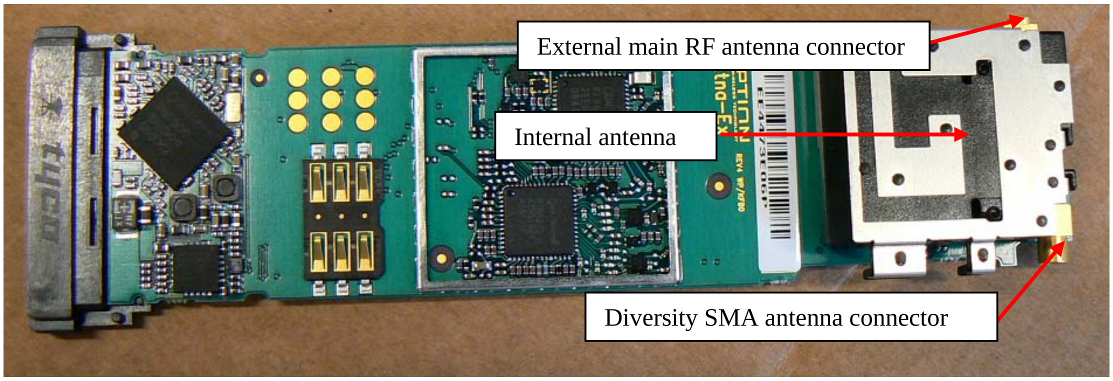
Maximum measured value: 2,18dB

Frequency range: 824–960 MHz; 1710 – 2170 MHz





2.3.2 Antenna positioning



In normal use, the permanent main antenna will be used. It is directly connected to a switchplexer that switches between transmitter/receiver and between frequency bands.

When a main external antenna will be used through the MC card connector, the path from the switchplexer to the internal antenna will be switched to a path between the external antenna and the switchplexer.

The antenna used for receiver diversity is a permanent external antenna, connected to a SMA connector. This antenna is a receiver-only antenna and is directly connected through a switch to the RFR.

3 Power Supply

The transceiver is powered from the PCI express card slot. Circuitry on the PC card performs boost, buck, linear regulation and filtering functions to ensure compliance to the PC express card slot requirements as well as GSM specifications.

4 External connectors

4.1 Express card connector

The PC card interface is described below.

Pin Signal Function

Pin No.	Signal	I/O	Interface Type(s) on module			Host	Notes
			PCI Express	USB	Both		
26	GND		R	R	R	R	
25	PETp0	I	R	NC	R	R	4
24	PETn0	I	R	NC	R	R	4
23	GND		R	R	R	R	
22	PERp0	O	R	NC	R	R	5
21	PERn0	O	R	NC	R	R	5
20	GND		R	R	R	R	
19	REFCLK+	I	R	NC	R	R	
18	REFCLK-	I	R	NC	R	R	
17	CPPE#	O	R	NC	R	R	3
16	CLKREQ#	O	R	NC	R	Opt	2
15	+3.3V		R	R	R	R	
14	+3.3V		R	R	R	R	
13	PERST#	I	R	NC	R	R	
12	+3.3VAUX		Opt	Opt	Opt	R	
11	WAKE#	O	Opt	NC	Opt	Opt	2
10	+1.5V		Opt	Opt	Opt	R	
9	+1.5V		Opt	Opt	Opt	R	
8	SMBDATA	I/O	Opt	Opt	Opt	Opt	6
7	SMBCLK	I/O	Opt	Opt	Opt	Opt	6
6	RESERVED		NC	NC	NC	NC	1
5	RESERVED		NC	NC	NC	NC	1
4	CPUSB#	O	NC	R	R	R	3
3	USBD+	I/O	NC	R	R	R	
2	USBD-	I/O	NC	R	R	R	
1	GND		R	R	R	R	

"I" indicates that the signal is input to the module, "O" indicates that the signal is output from the module.
"R" indicates the signal is required, "Opt" indicates the signal is optional, and "NC" indicates the signal is not to be connected.

4.2 Antenna connector

There is an accessible antenna connector which can be used to connect to external test equipment (e.g. in factory). When using this, the internal antenna is disconnected. The connector type is an MC card connector. The mating connector must have an extended barrel to engage the on-card connector without interfering with the radome housing.