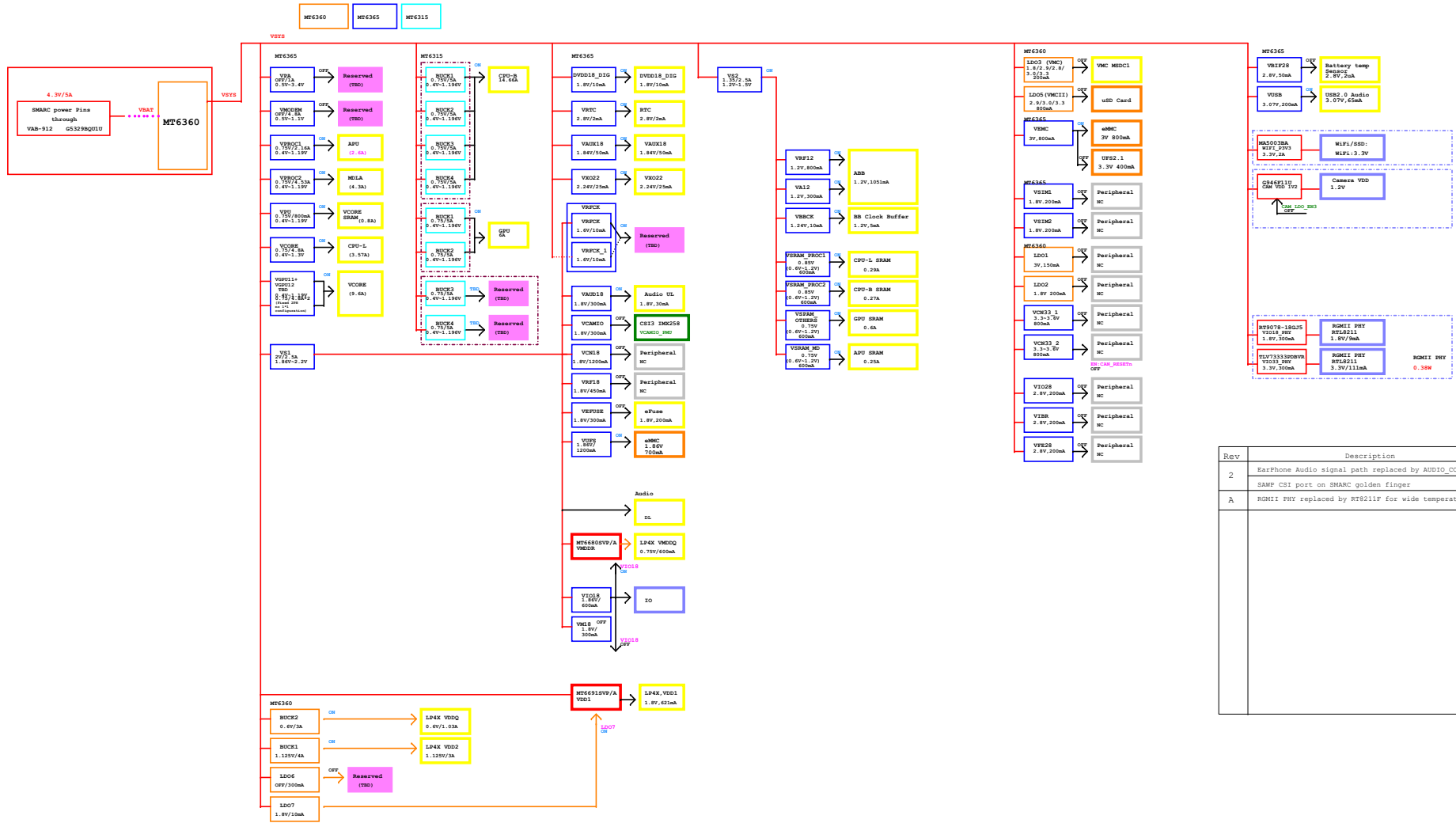
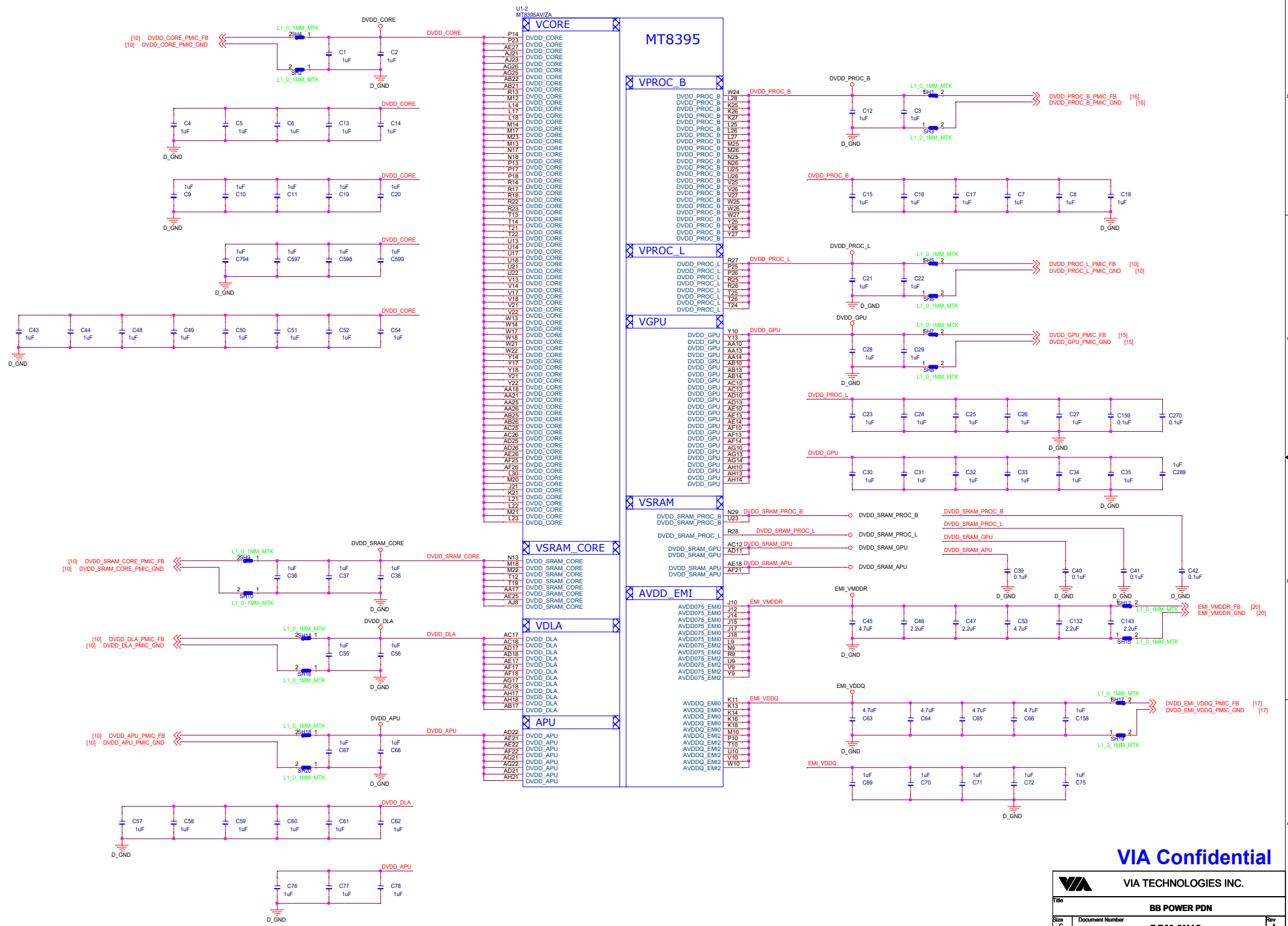


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Rev	Description	Page
2	Earphone Audio signal path replaced by AUDIO_COM	24
	SMMP CSI port on SMARC golden finger	7 & 35
A	RGMII PHY replaced by RT9211F for wide temperature	31

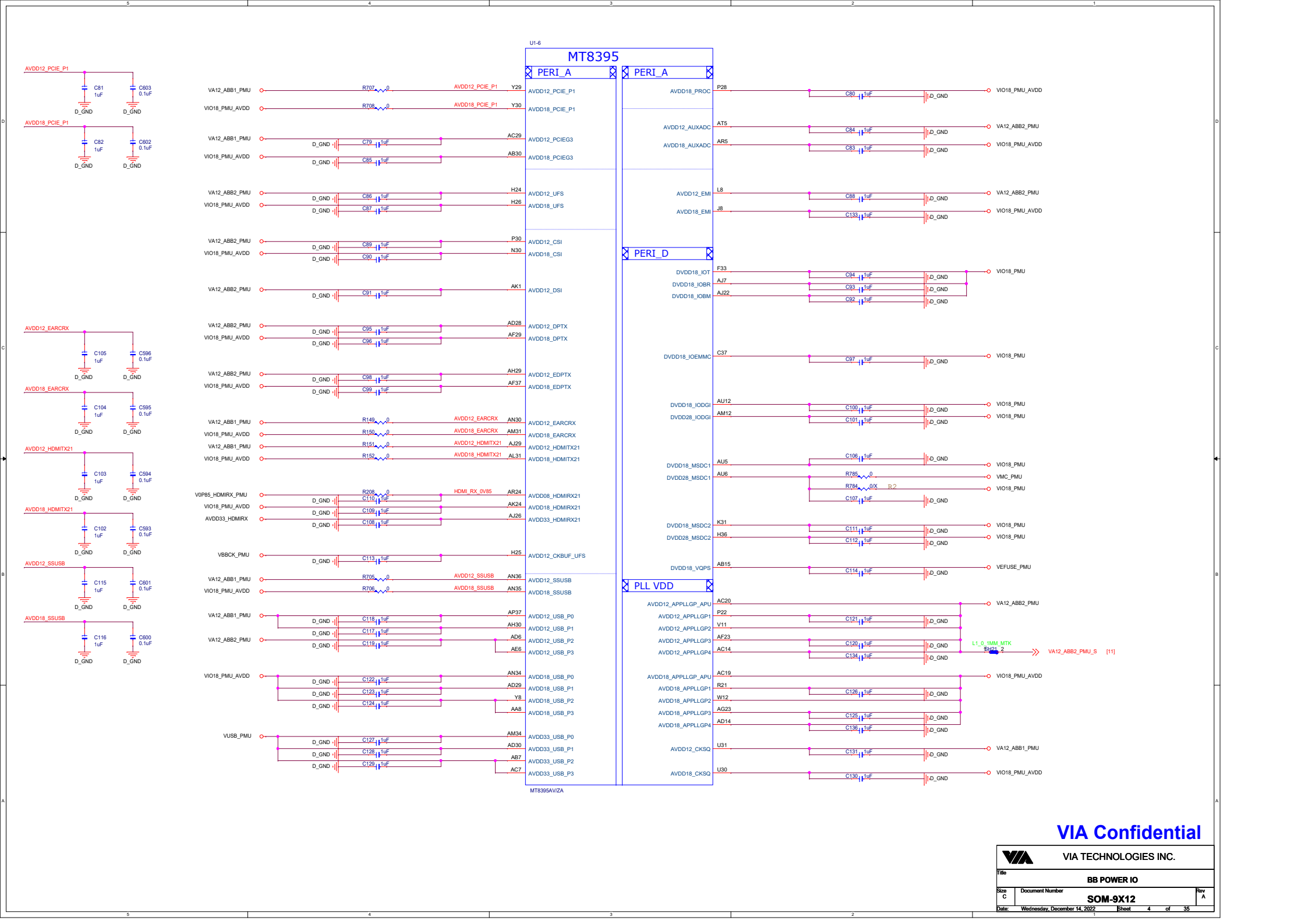
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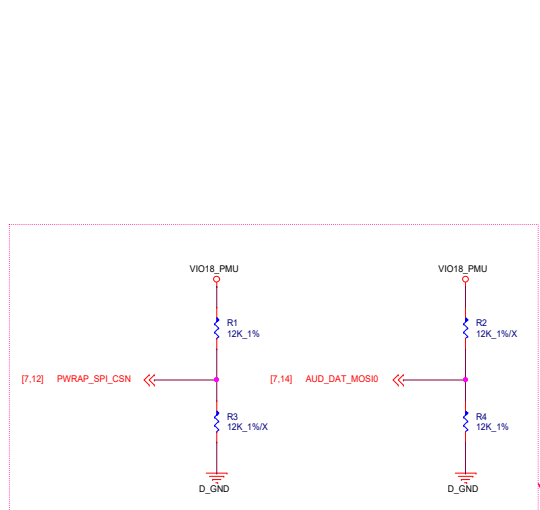
VIA TECHNOLOGIES INC.

Title		BB POWER PDN	
Size	Document Number	SOM-9X12	
C		Rev A	
Date:	Wednesday, December 14, 2022	Sheet	3 of 35

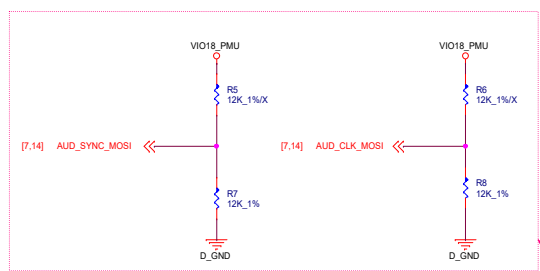


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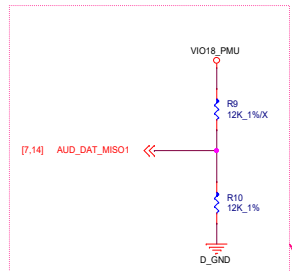
 <b>VIA TECHNOLOGIES INC.</b>	
<b>Title</b> <b>BB POWER IO</b>	
<b>Size</b> C	<b>Document Number</b> <b>SOM-9X12</b>
<b>Date</b> Wednesday, December 14, 2022	<b>Rev</b> A
<b>Sheet</b> 4 of 35	



Note: 1



Note: 2



Note: 3

**Schematic design notice:**

Note 1: "PWRAP\_SPI\_CSN" and "AUD\_DAT\_MOSI0" pin features in trapping pin to enable JTAG.

PWRAP_SPI0_CSN	AUD_DAT_MOSI0	AP JTAG	ADSP or SCP JTAG
H (Default)	L (Default)	N/A	N/A
H	H (by external PU)	DMIC2_SCK, PCM_DO, PCM_CLK, PCM_DI, PCM_SYNC	N/A
L (by external PD)	L	MSDC1_CLK, MSDC1_CMD, MSDC1_DAT0, MSDC1_DAT1, MSDC1_DAT2	ADSP JTAG: PCIE_WAKE_N, PCIE_PERESET_N, PCIE_CLKREQ_N, CMMRST, CMMPDN
L (by external PD)	H (by external PU)	MSDC1_CLK, MSDC1_CMD, MSDC1_DAT0, MSDC1_DAT1, MSDC1_DAT2	SCP JTAG: SPIM1_CSB, SPIM1_CLK, SPIM1_MO, SPIM1_MI, USB_DRV_VBUS_1P

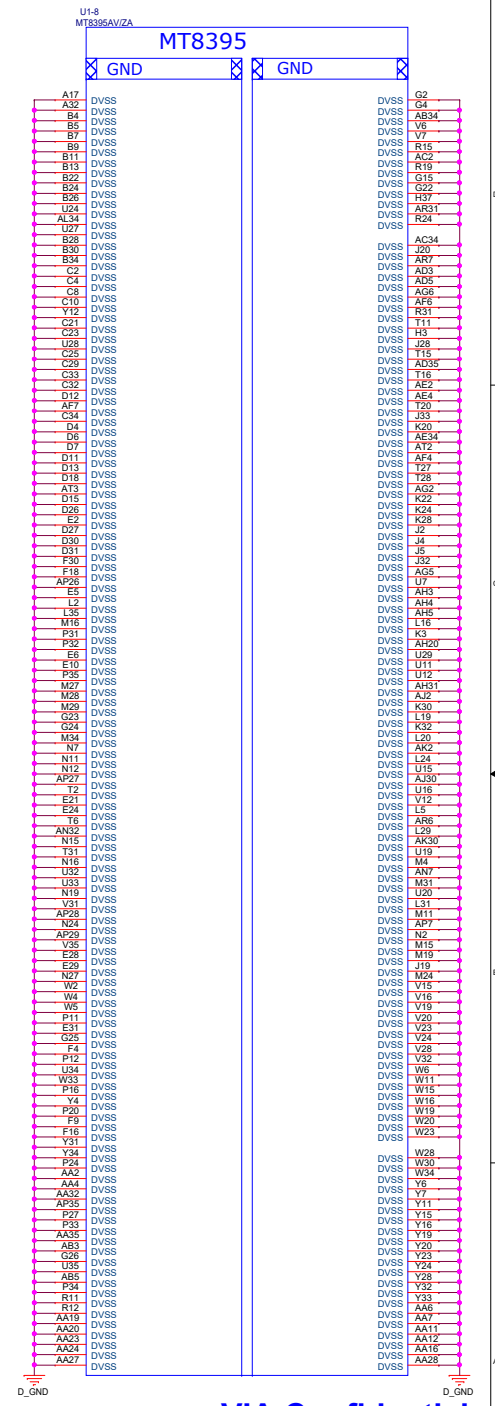
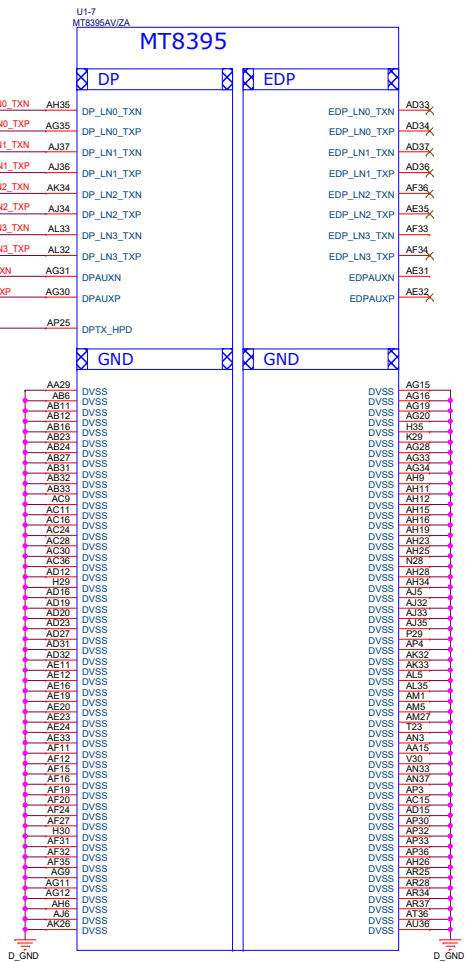
Note 2: "AUD\_SYNC\_MOSI" and "AUD\_CLK\_MOSI" pin features in trapping pin to booting (eMMC/UFS/SPI NOR).

AUD_SYNC_MOSI	AUD_CLK_MOSI	Storage Booting
L (Default)	L (Default)	Only eMMC boot
L	H (by external PU)	Only UFS boot
H (by external PD)	L	Only SPI NAND boot
H (by external PD)	H (by external PU)	Only SPI NOR boot

Note 3: "AUD\_DAT\_MISO1" is trapping pin to select VEMC Voltage.

AUD_DAT_MISO1	VEMC Voltage
L (Default)	VEMC=3.0V
H (by external PU)	VEMC=2.5V

- [35] DP\_LN0\_TXN <<< DP\_LN0\_TXN AH35
- [35] DP\_LN0\_TXP <<< DP\_LN0\_TXP AG35
- [35] DP\_LN1\_TXN <<< DP\_LN1\_TXN AJ37
- [35] DP\_LN1\_TXP <<< DP\_LN1\_TXP AJ36
- [35] DP\_LN2\_TXN <<< DP\_LN2\_TXN AK34
- [35] DP\_LN2\_TXP <<< DP\_LN2\_TXP AJ34
- [35] DP\_LN3\_TXN <<< DP\_LN3\_TXN AL33
- [35] DP\_LN3\_TXP <<< DP\_LN3\_TXP AL32
- [35] DP\_AUXN <<< DP\_AUXN AG31
- [35] DP\_AUXP <<< DP\_AUXP AG30
- [33,35] 1ST\_CAM\_VXS <<< DP\_TX\_HPD AP25



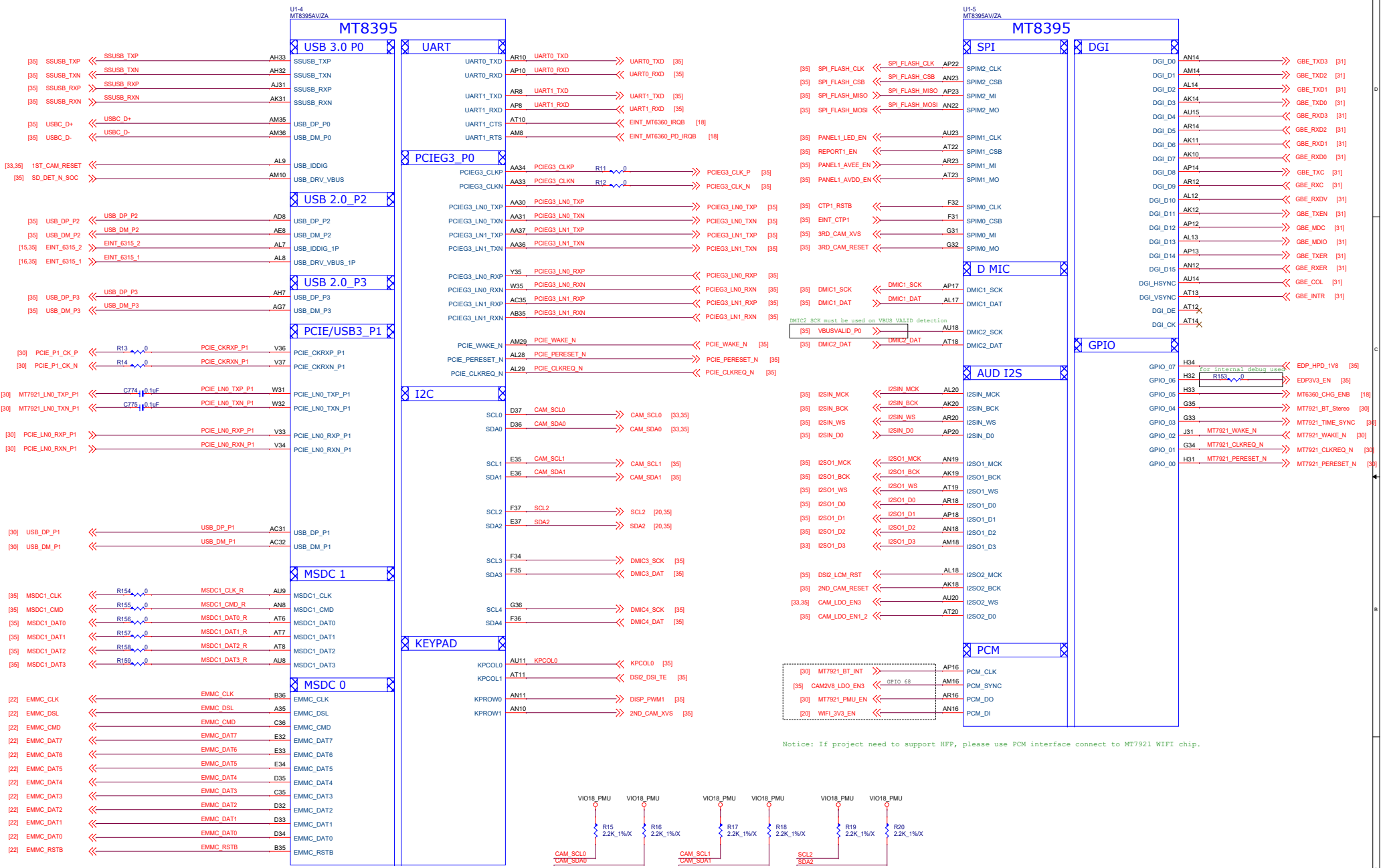
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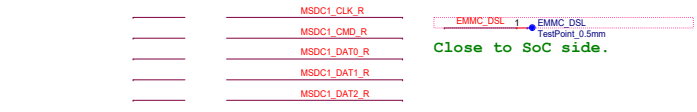
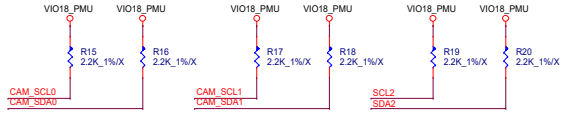
Title: Baseband Part 1 & Trapping

Size C Document Number SOM-9X12 Rev A

Date: Wednesday, December 14, 2022 Sheet 5 of 35



Notice: If project need to support HFP, please use PCM interface connect to MT7921 WIFI chip.



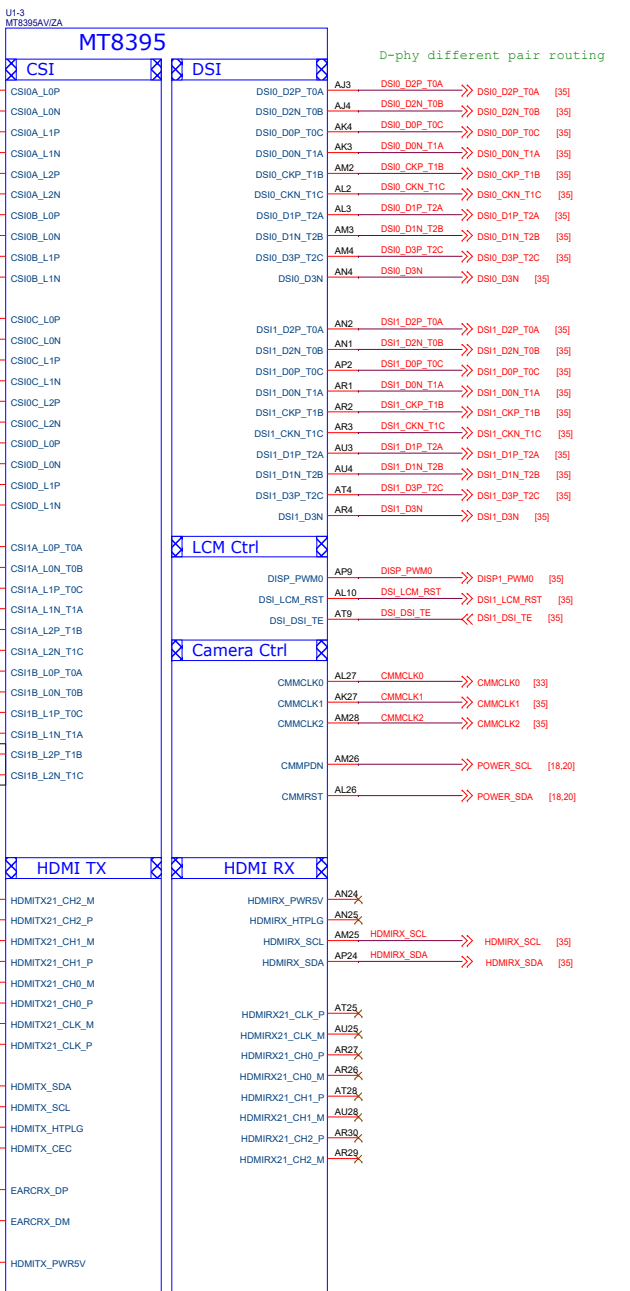
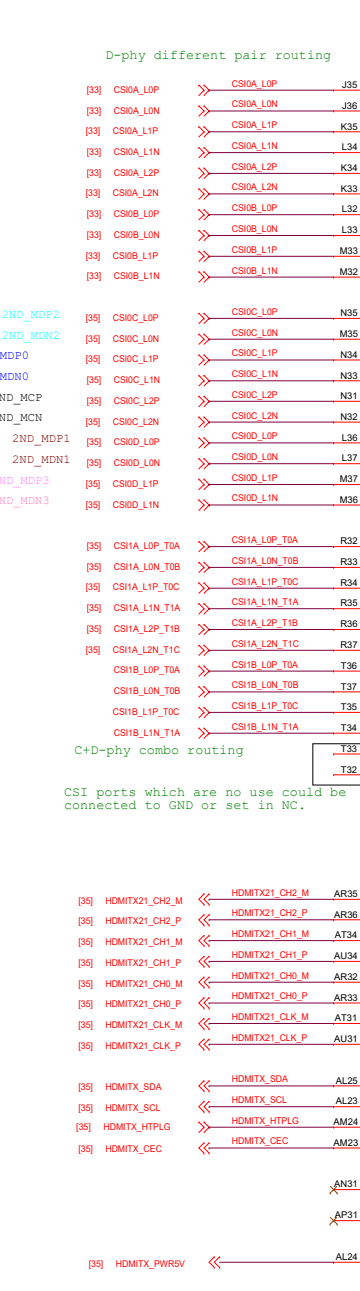
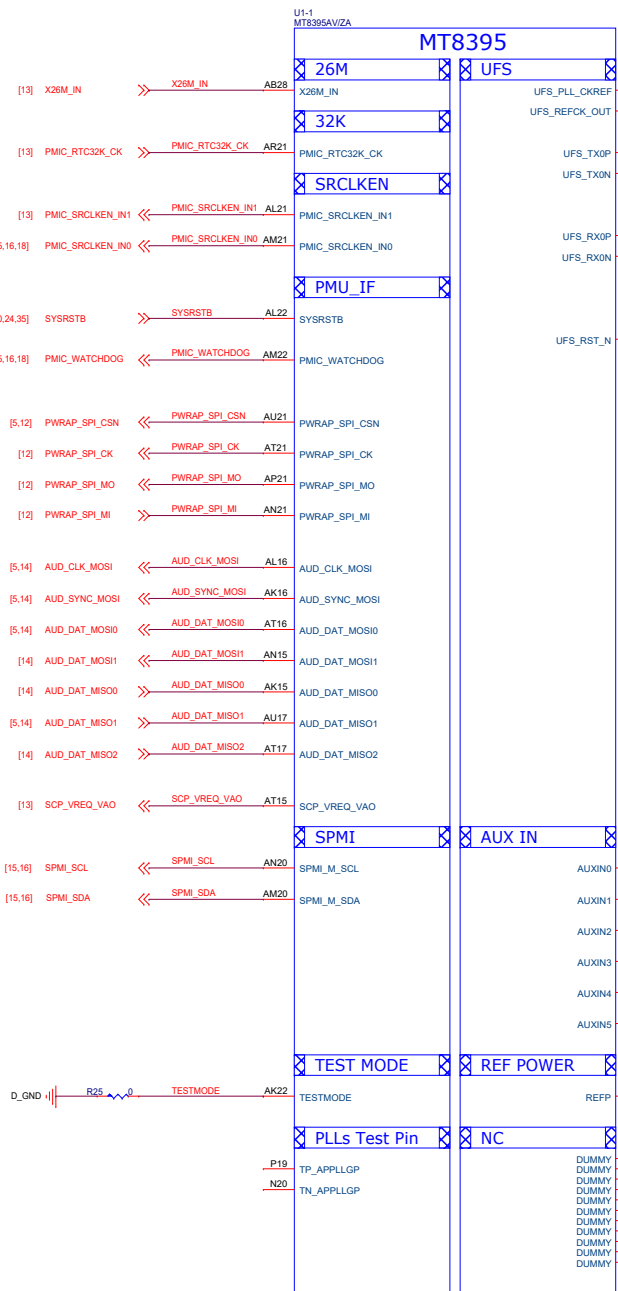
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Title: **Baseband Part 2**

Size C | Document Number: **SOM-9X12** | Rev A

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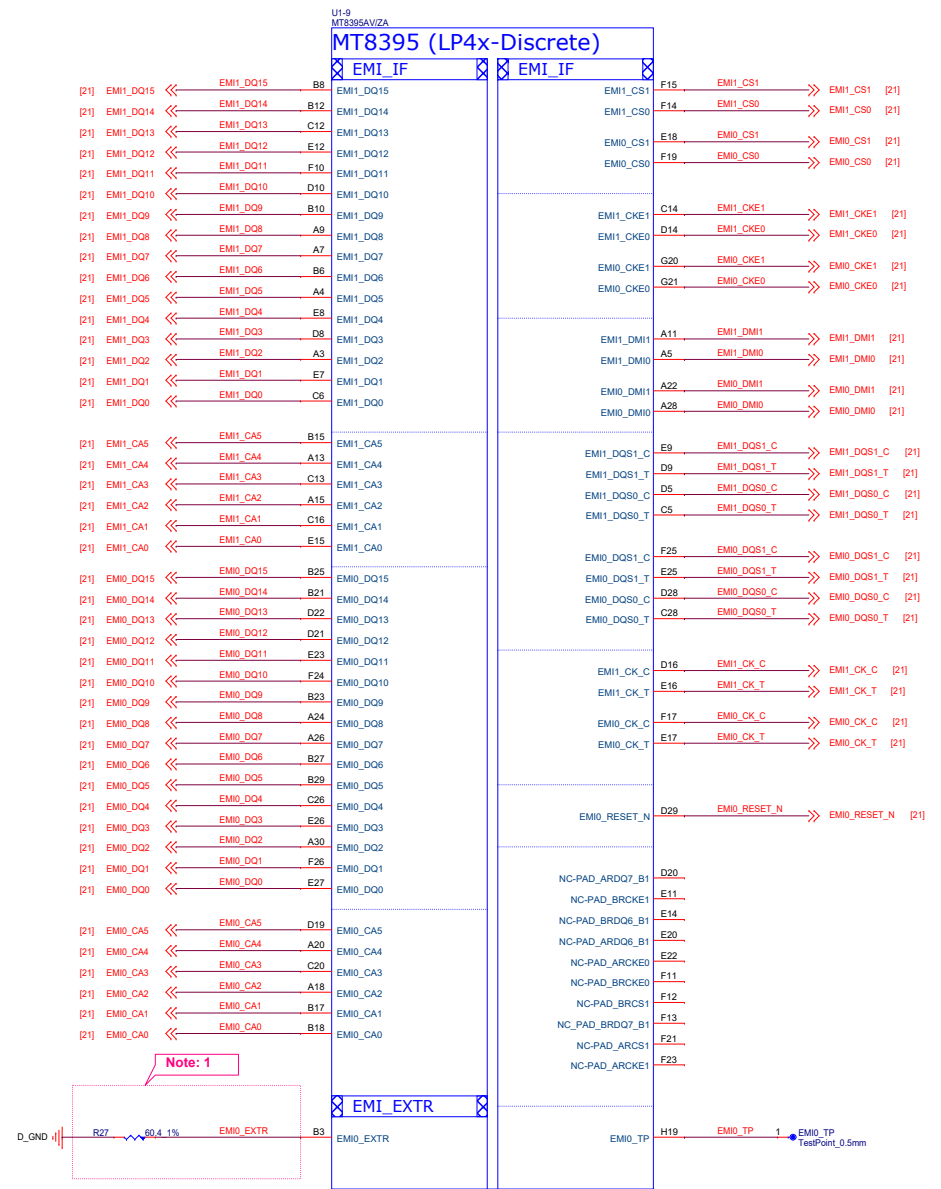
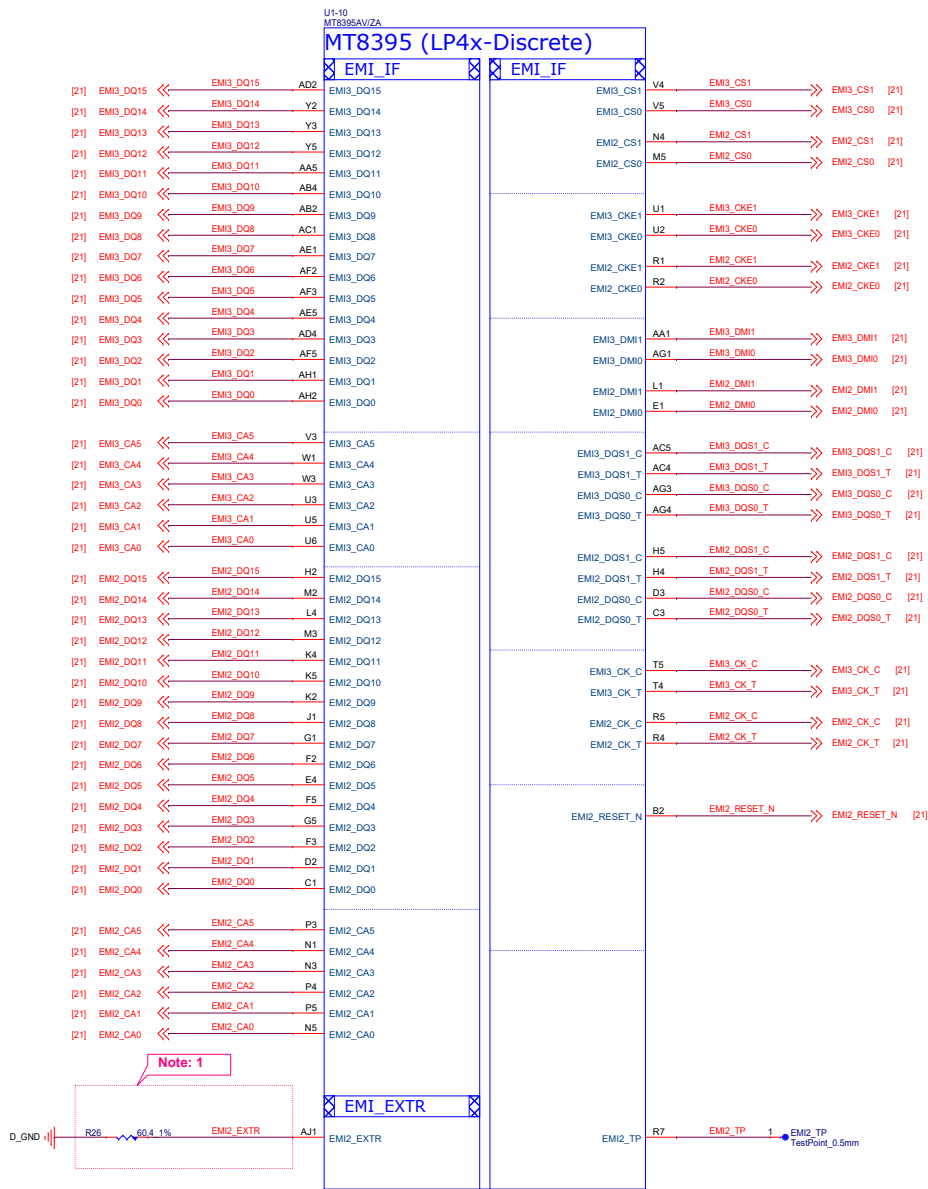
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VIA TECHNOLOGIES INC.

Title: Baseband Part 3

Size: C Document Number: SOM-9X12 Rev: A

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Title Baseband Part 4

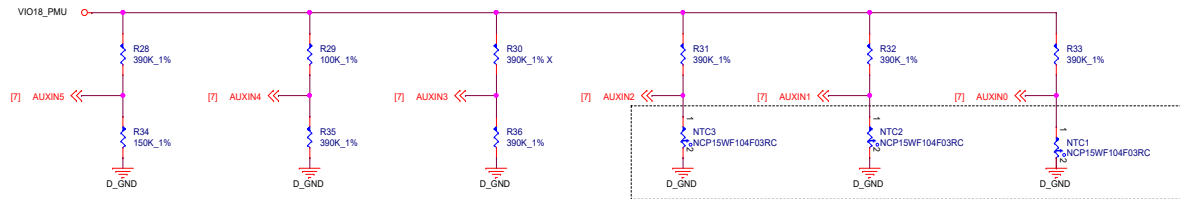
Size C Document Number SOM-9X12 Rev A

Date: Wednesday, December 14, 2022 Sheet 8 of 35

Schematic design notice of "BB\_4\_Interface" page:

Note 1: R26, R27 please select 60.4 ohm (1%) resistor





**AUX5 for eMMC/DRAM Config. Table**

<0.7v 4CH, DSC  
 0.7~1.2v 2CH, eMCP  
 >1.2v 2CH, DSC


**AUX4 for DemoBoard SKU**

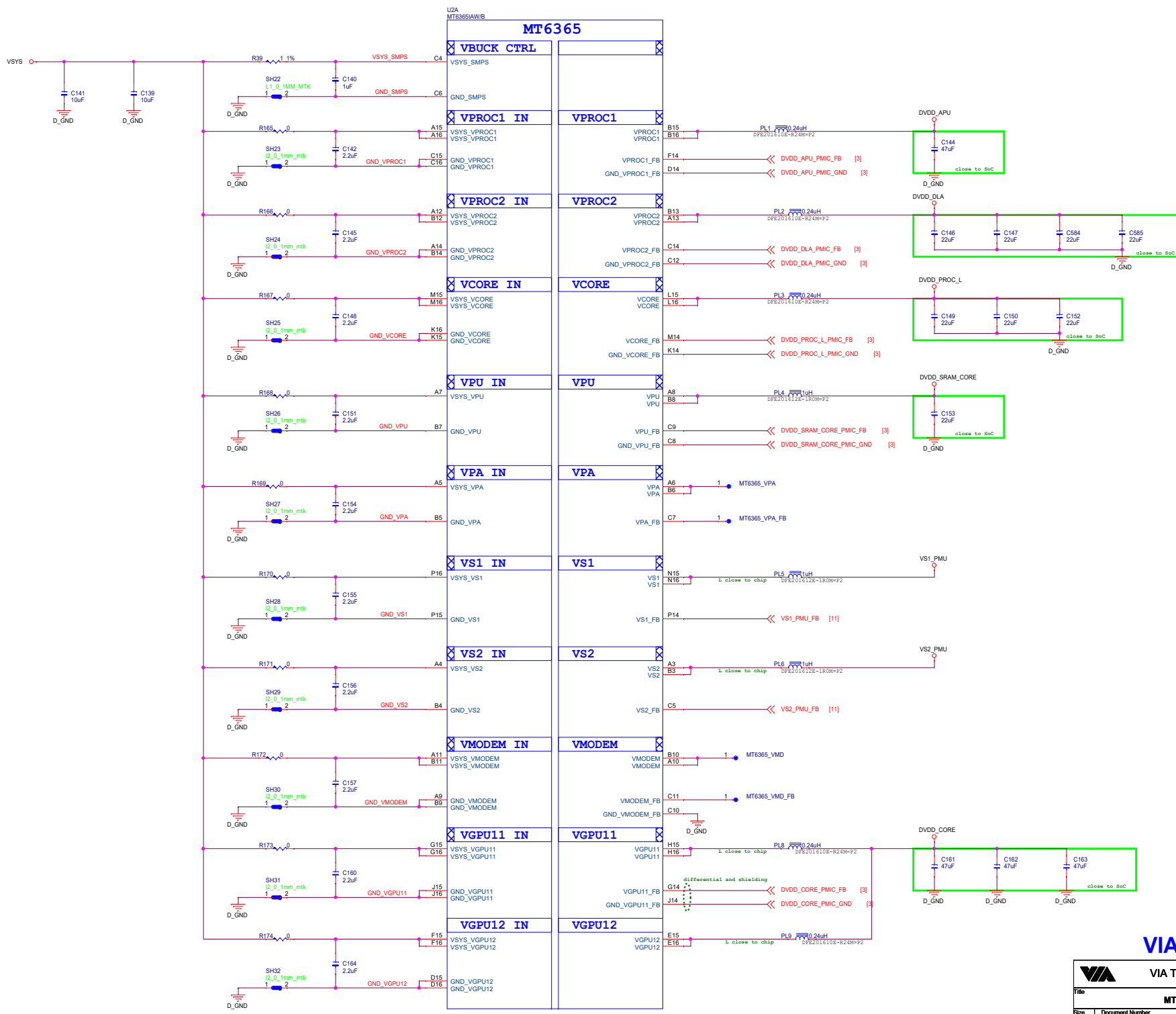
<0.2V SMT0  
 0.2~0.7V SMT1 (default ICE)  
 0.7~1.2V SMT2 (default SD)  
 >1.2V SMT3 (default SD)

**Thermistor to sense AP temperature**

1. NTC1 must keep a distance about 6-8 mm away from AP and far from other heat sources 10 mm at least.
2. The distance is the shortest distance from package edge to edge.

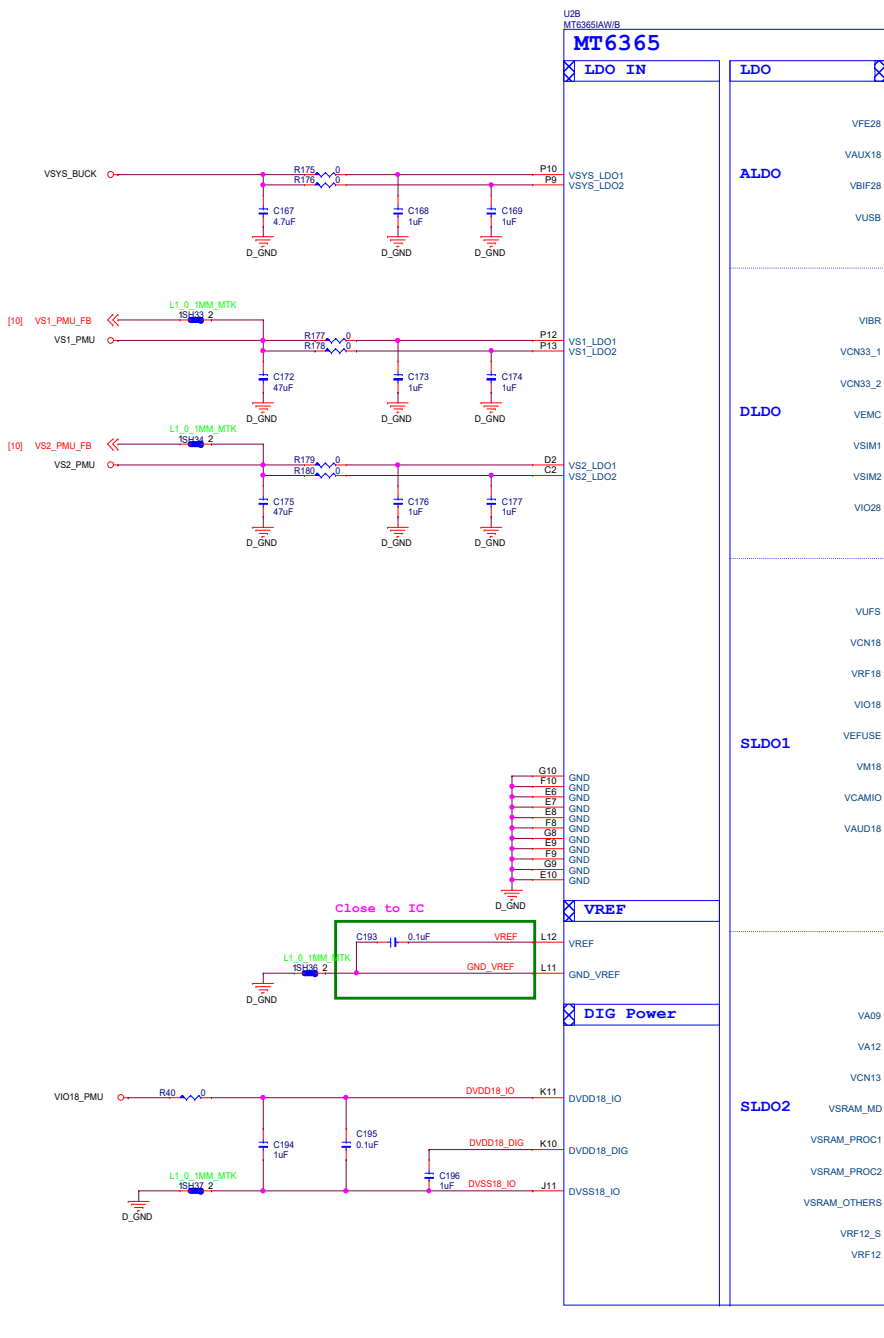
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		VIA TECHNOLOGIES INC.	
Title			
AUXADC Thermal			
Size	Document Number		Rev
C	SOM-9X12		A
Date:	Wednesday, December 14, 2022	Sheet	9 of 35

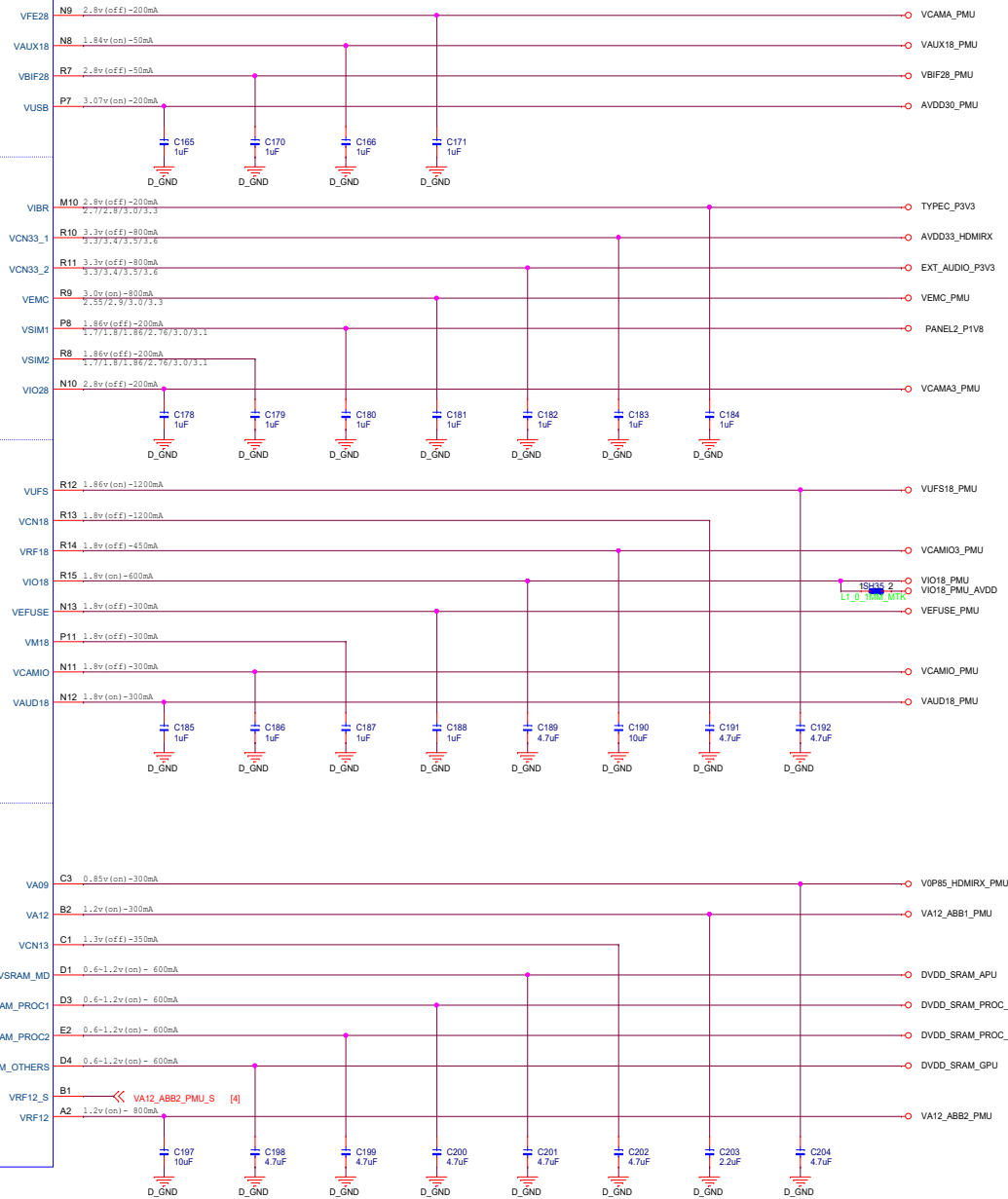


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		<b>VIA TECHNOLOGIES INC.</b>	
<b>Title</b> MT6365 Buck			
<b>Size</b> C	<b>Document Number</b>		<b>Rev</b> A
<b>SOM-9X12</b>			
<b>Date:</b> Wednesday, December 14, 2022 <b>Sheet</b> 10 <b>of</b> 35			

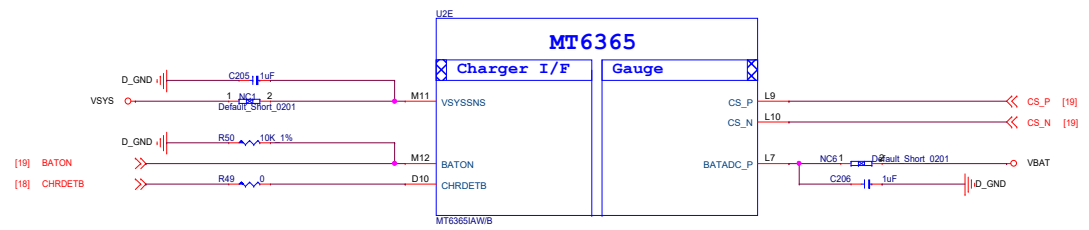
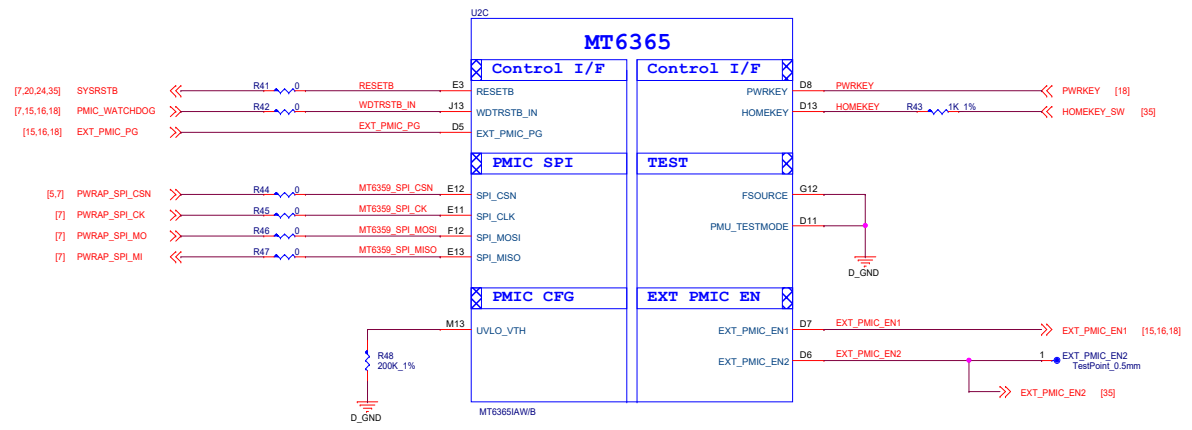


1. "Typical Cap" defined in design notice is the minimum cap. to LDO Cout.
2. NC cap can move to application, if (PCB L<20nH, PCB R<0.2mohm)  
=> value and placement of Cap, please refer design notice

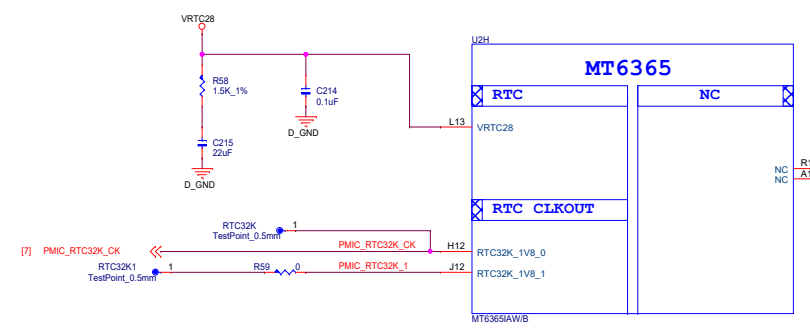
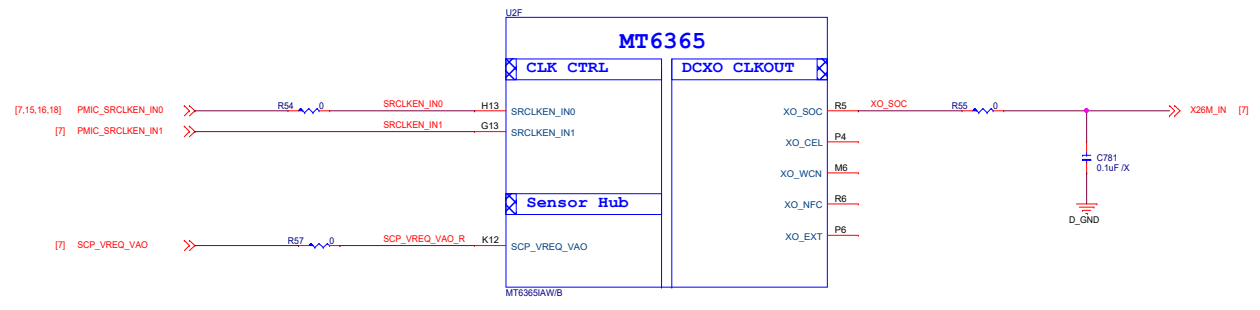
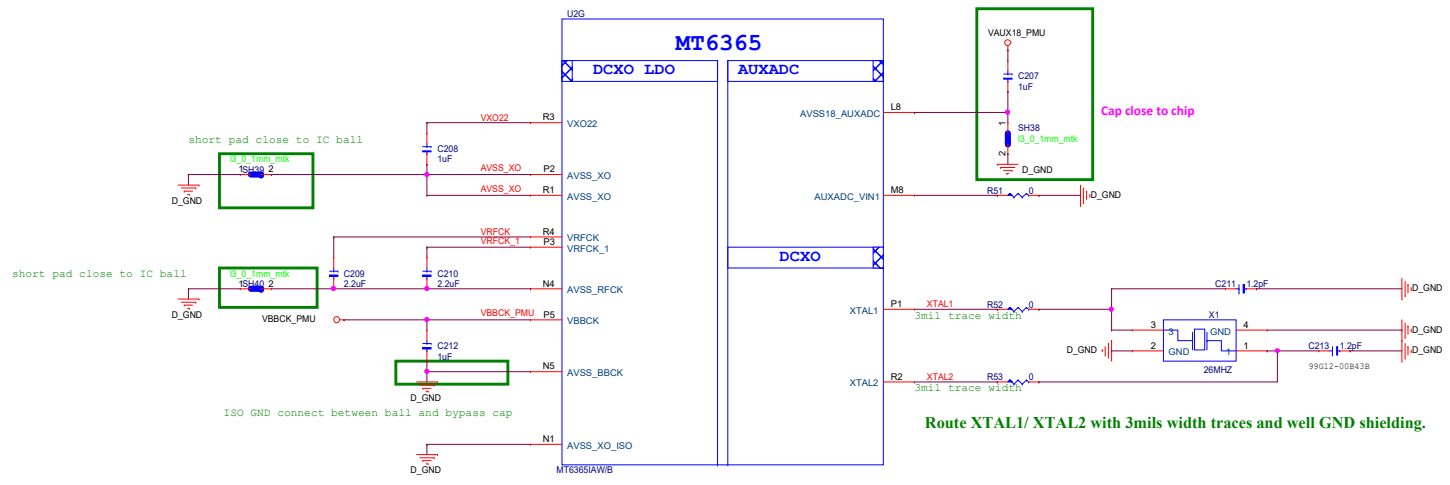


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<b>VIA</b>		VIA TECHNOLOGIES INC.	
Title <b>MT6365 LDO</b>			
Size C	Document Number <b>SOM-9X12</b>	Rev A	
Date:	Wednesday, December 14, 2022	Sheet	11 of 35

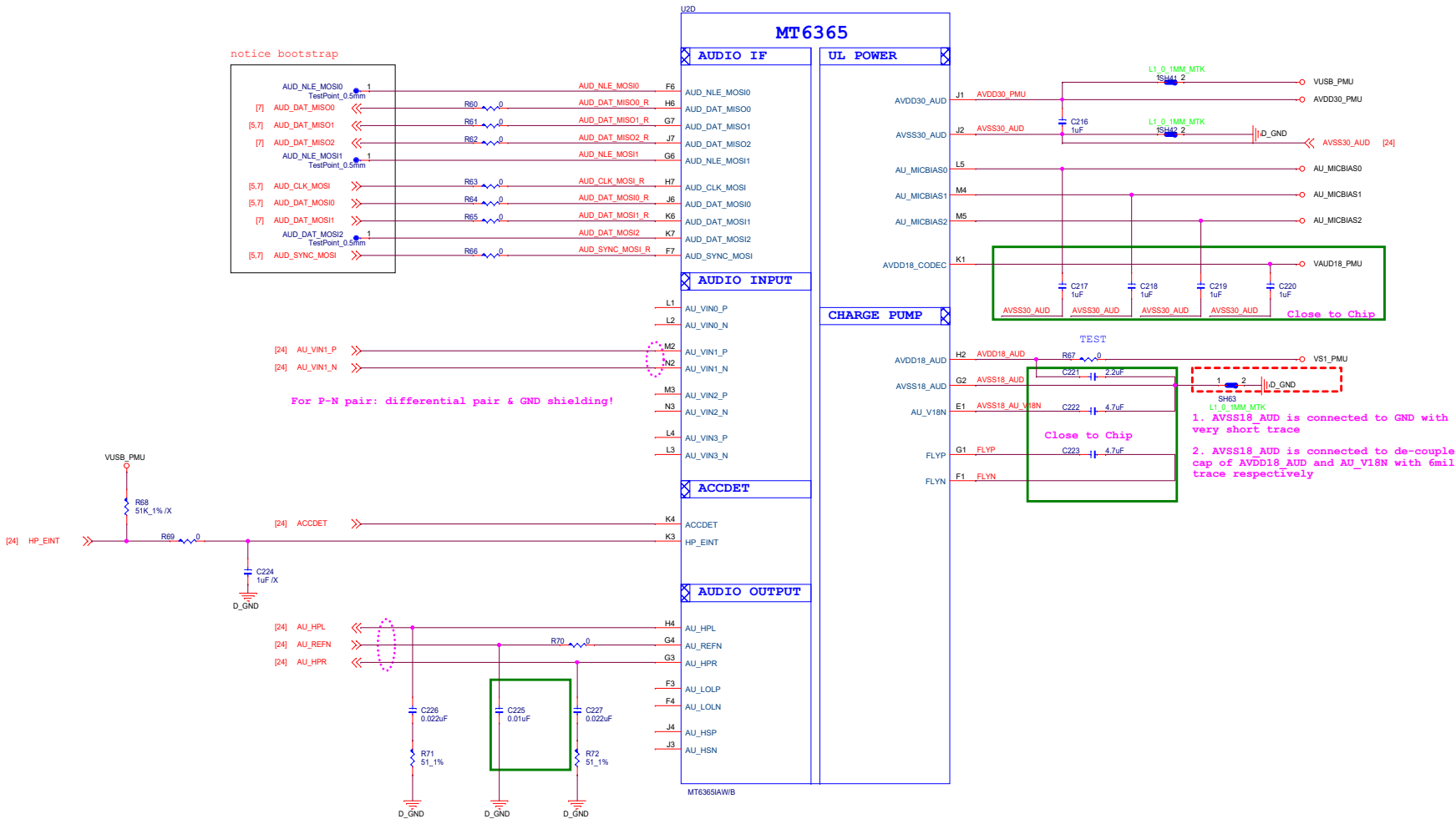


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<b>VIA TECHNOLOGIES INC.</b>	
Title: <b>MT6365 Clock</b>	
Size: C	Document Number: <b>SOM-9X12</b>
Date: Wednesday, December 14, 2022	Rev: A
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notice bootstrap

AUD_NLE_MOSI0	TestPoint_0.5mm	1	AUD_NLE_MOSI0	F6	AUD_NLE_MOSI0	H6
AUD_DAT_MISO0		[7]	AUD_DAT_MISO0_R	R60	AUD_DAT_MISO0_R	G7
AUD_DAT_MISO1		[5,7]	AUD_DAT_MISO1_R	R61	AUD_DAT_MISO1_R	G7
AUD_DAT_MISO2		[7]	AUD_DAT_MISO2_R	R62	AUD_DAT_MISO2_R	J7
AUD_NLE_MOSI1	TestPoint_0.5mm	1	AUD_NLE_MOSI1	G6	AUD_NLE_MOSI1	H6
AUD_CLK_MOSI		[5,7]	AUD_CLK_MOSI_R	R63	AUD_CLK_MOSI_R	H7
AUD_DAT_MOSI0		[5,7]	AUD_DAT_MOSI0_R	R64	AUD_DAT_MOSI0_R	J6
AUD_DAT_MOSI1		[7]	AUD_DAT_MOSI1_R	R65	AUD_DAT_MOSI1_R	K6
AUD_DAT_MOSI2	TestPoint_0.5mm	1	AUD_DAT_MOSI2	K7	AUD_DAT_MOSI2	K7
AUD_SYNC_MOSI		[5,7]	AUD_SYNC_MOSI_R	R66	AUD_SYNC_MOSI_R	F7

[24] AU\_VIN1\_P  
[24] AU\_VIN1\_N

For P-N pair: differential pair & GND shielding!

AVSS30\_AUD AVSS30\_AUD AVSS30\_AUD AVSS30\_AUD  
C217 1uF C218 1uF C219 1uF C220 1uF  
Close to Chip

TEST  
AVSS18\_AUD AVSS18\_AUD\_V18N  
C221 2.2uF C222 4.7uF  
Close to Chip  
C223 4.7uF

1. AVSS18\_AUD is connected to GND with very short trace  
2. AVSS18\_AUD is connected to de-couple cap of AVDD18\_AUD and AU\_V18N with 6mil trace respectively

Close to Chip

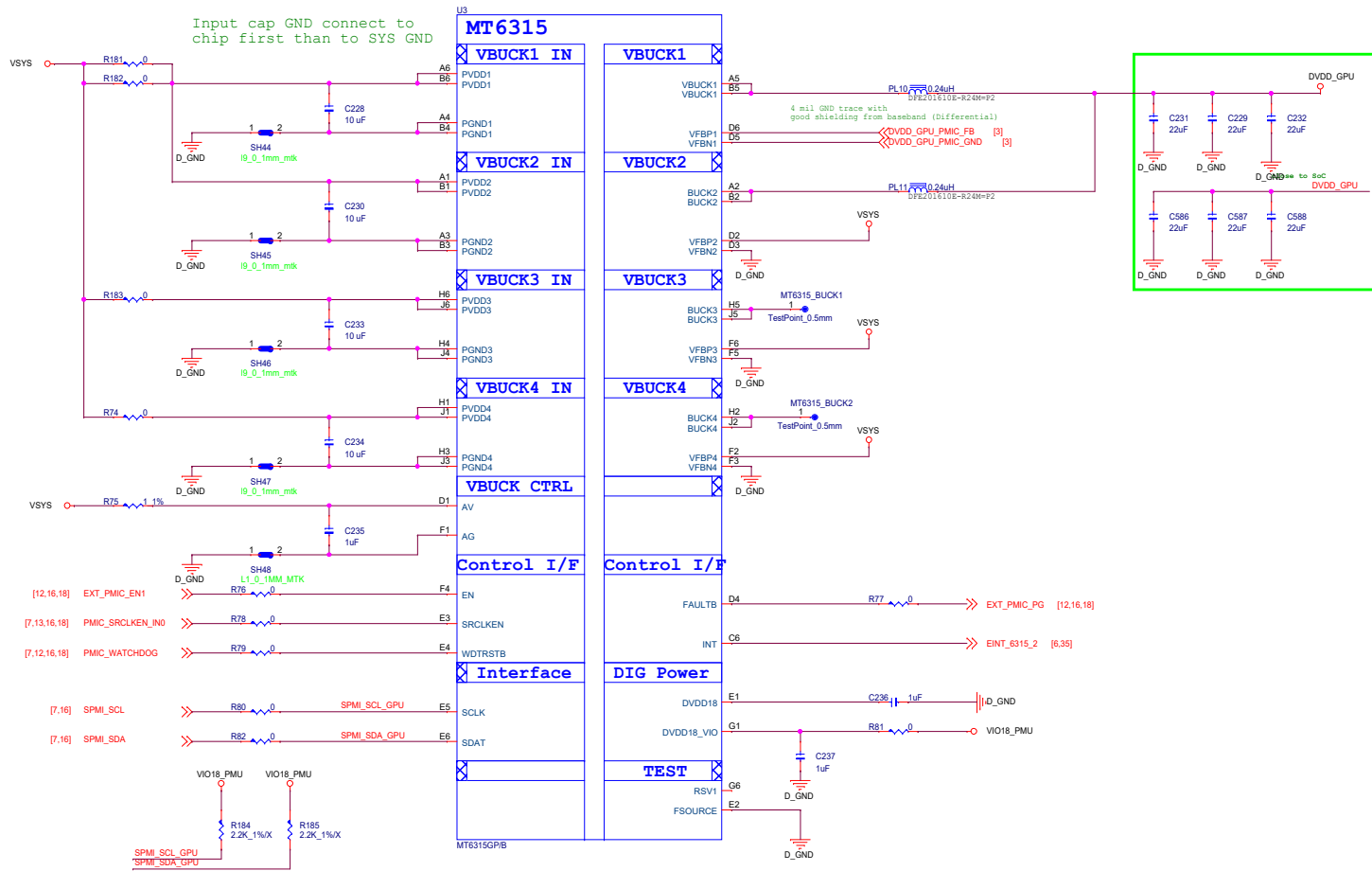
-AU HPL and AU HPR should be routed as single end signal and be guarded by GND, up and down, left and right respectively

-The suggested layout pattern of AU HPL/ AU\_HPR/ AU\_REFN is " GND AU\_HPL AU\_REFN AU\_HPR GND"

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VIA TECHNOLOGIES INC.	
Title MT6365 Audio	
Size C	Document Number SOM-9X12
Date: Wednesday, December 14, 2022	Sheet 14 of 35

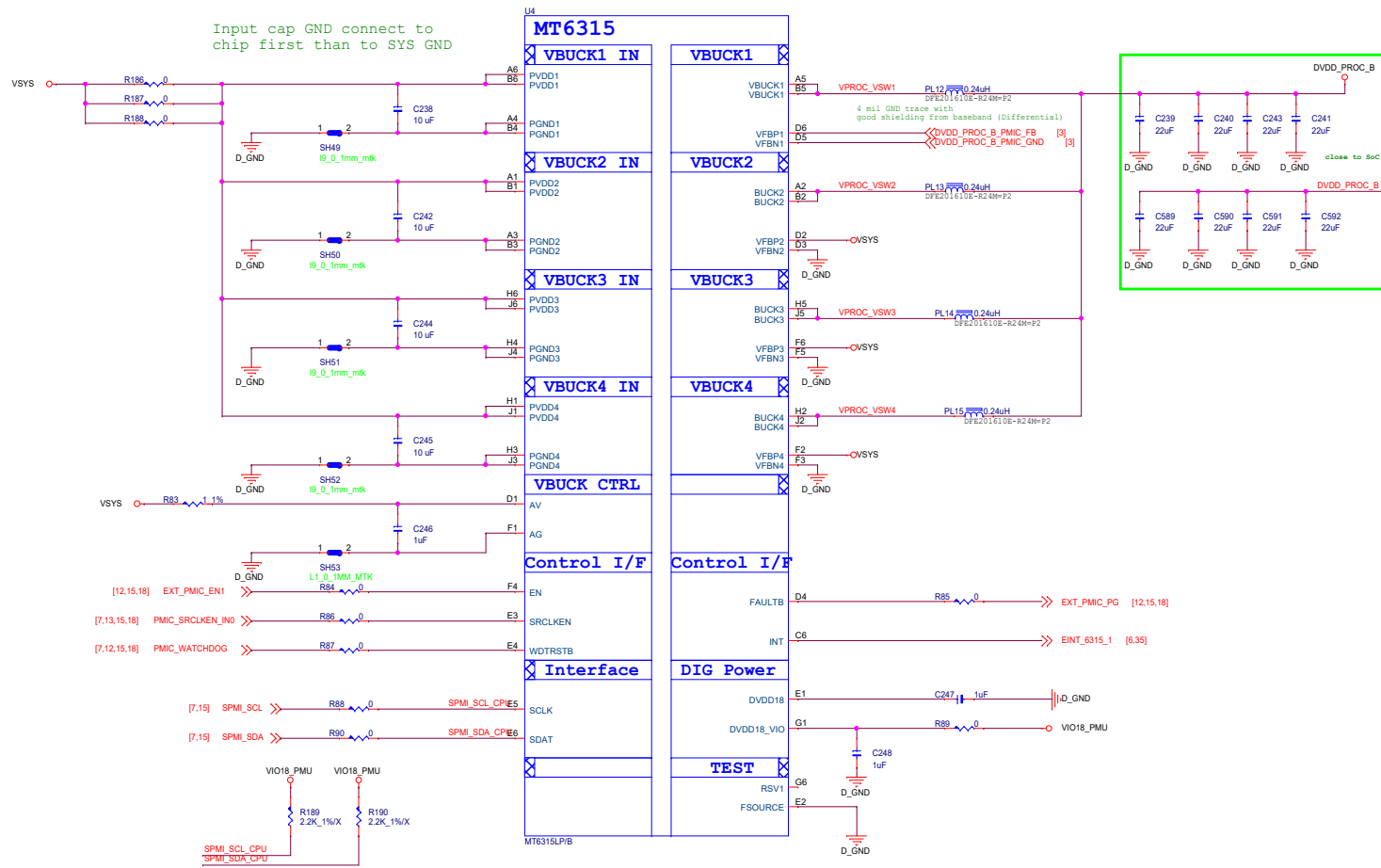
# MT6315 4-Phase Buck



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VIA TECHNOLOGIES INC.	
Title	MT6315_0 GPU
Size C	Document Number
Date	Rev A
<b>SOM-9X12</b>	
Date: Wednesday, December 14, 2022 Sheet 15 of 35	

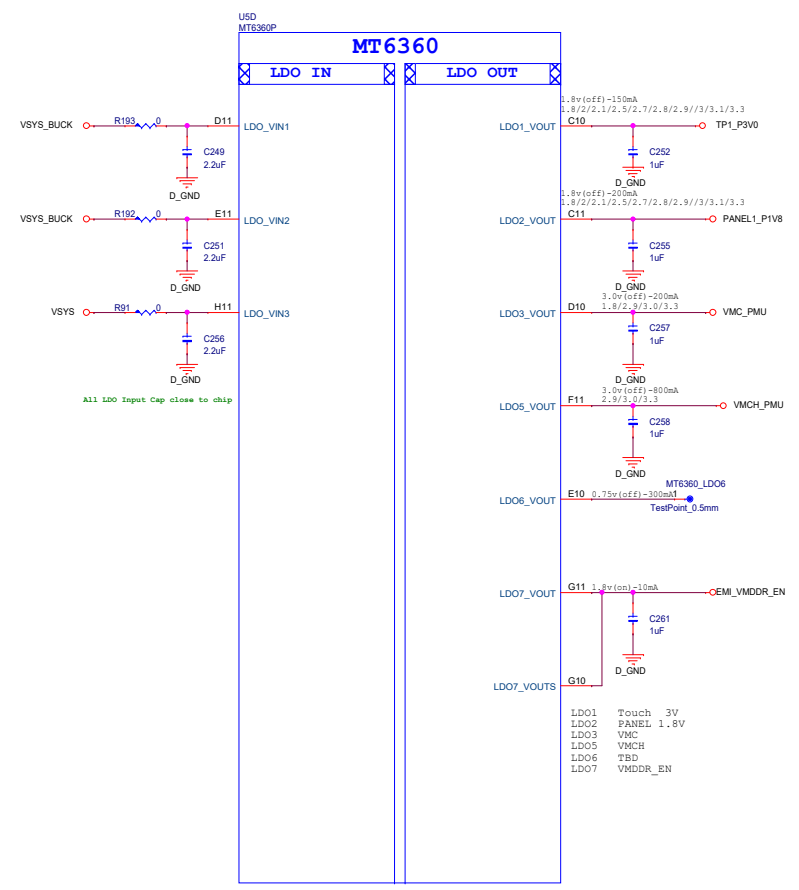
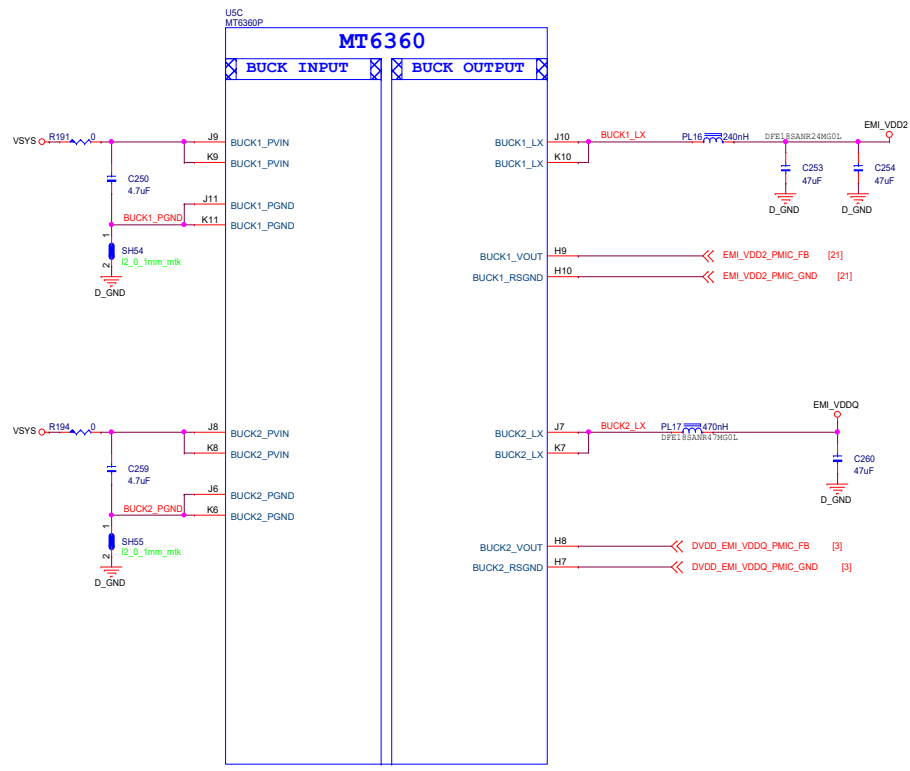
# MT6315 4-Phase Buck



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VIA TECHNOLOGIES INC.	
Title	MT6315_1 CPU-B
Size	Document Number
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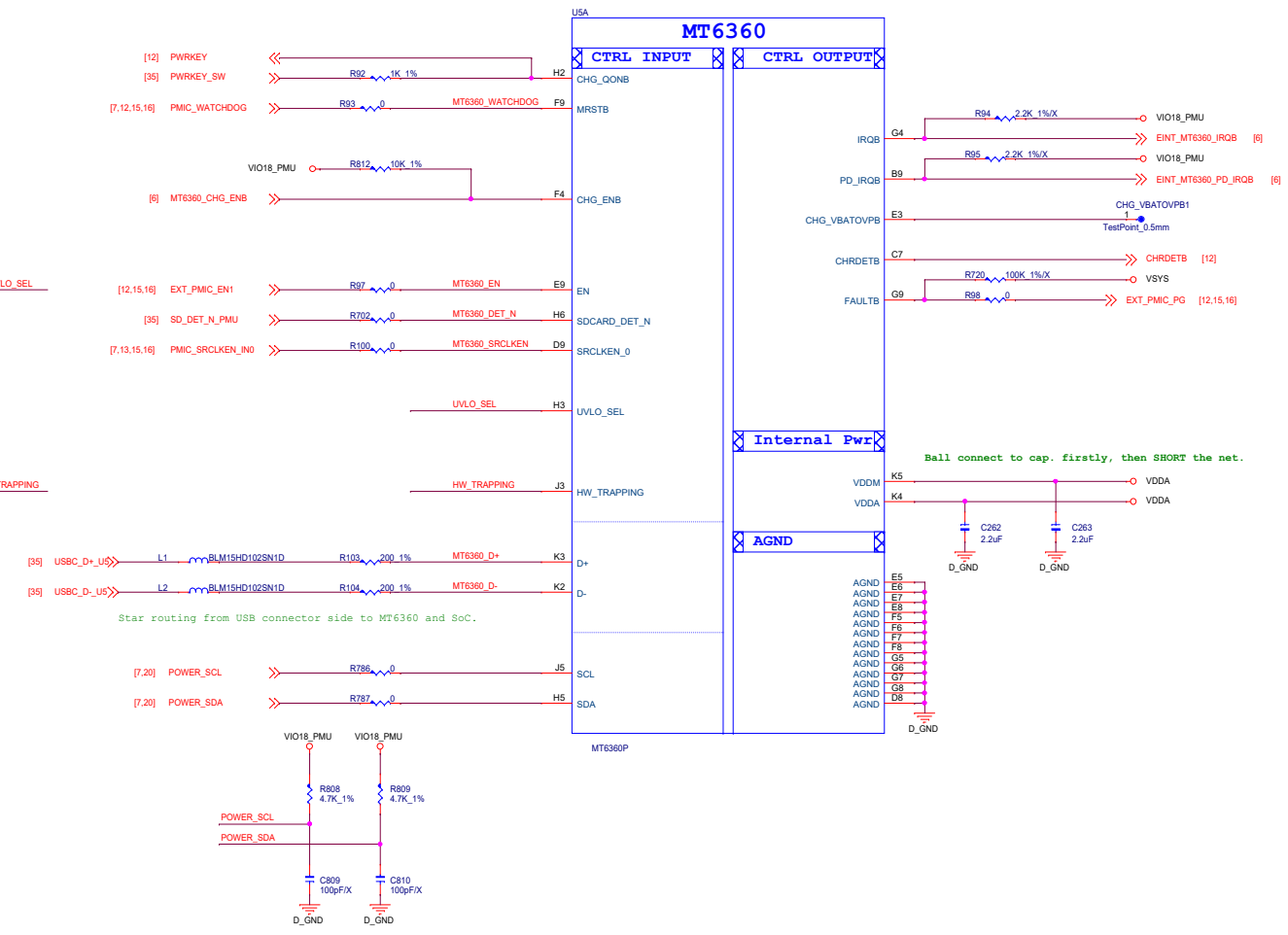
- LDO1 Touch 3V
- LDO2 PANEL 1.8V
- LDO3 VMC
- LDO5 VMCH
- LDO6 TBD
- LDO7 VMDDR\_EN

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Title: MT6360 BUCK & LDO	
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UVLO SEL R (G) to GND  
 000 (2.8V) Short to VDDA  
 001 (2.9V) 1.8M  
 010 (3V) 430K  
 011 (3.1V) 100K  
 012 (3.2V) 28K  
 100 (3.3V) 28K  
 101-111 (3.3V) 7.9K

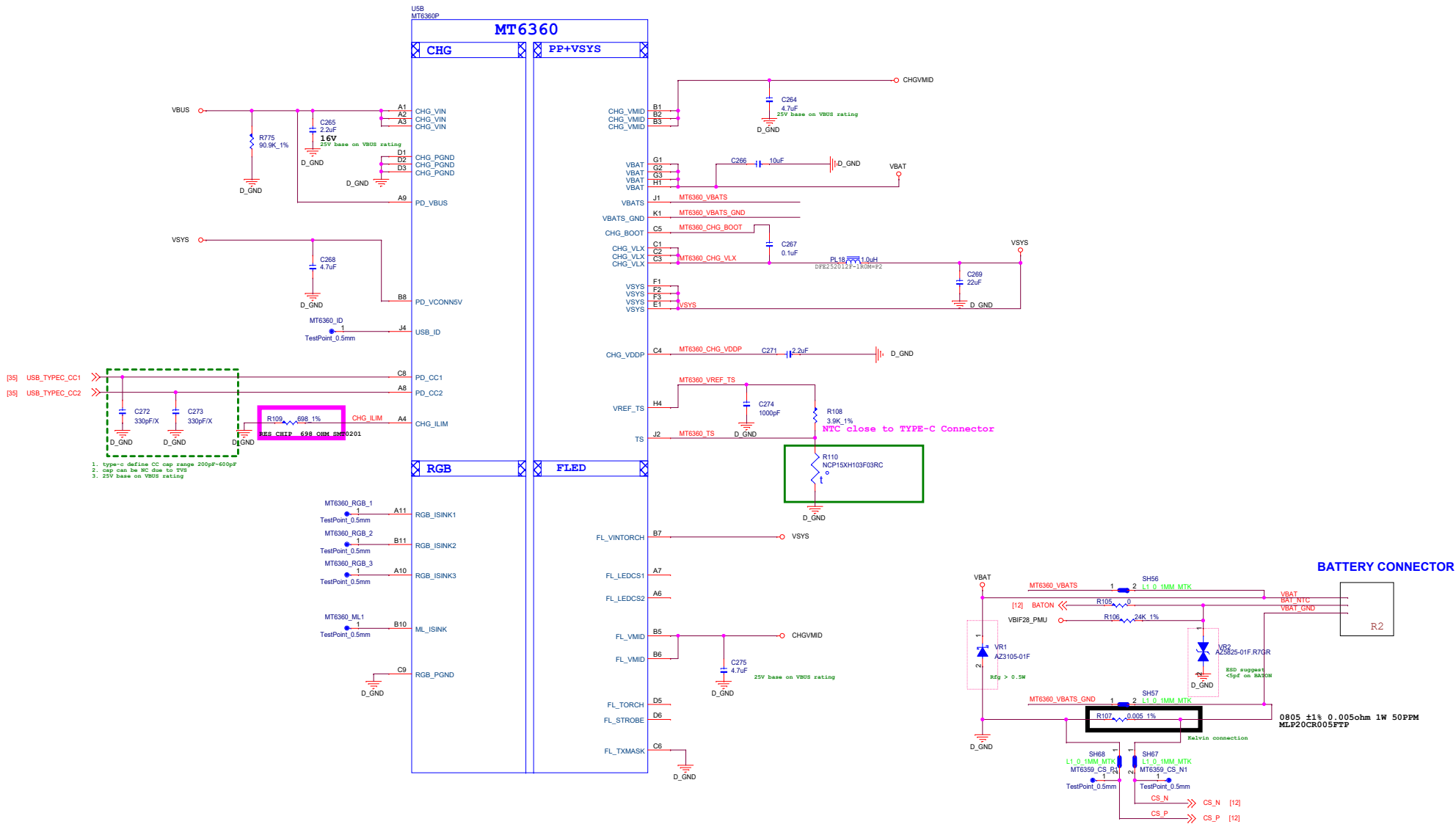
HW TRAPPING R (G) to GND  
 000 Short to VDDA  
 001 1.8M  
 010 430K  
 011 100K  
 100 28K  
 101 7.9K  
 110 1.6K  
 111 422R



Ball connect to cap. firstly, then SHORT the net.

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<b>VIA</b>		VIA TECHNOLOGIES INC.	
Title: <b>MT6360 General</b>			
Size: C	Document Number: <b>SOM-9X12</b>	Rev: A	
Date: Wednesday, December 14, 2022 Sheet 18 of 35			



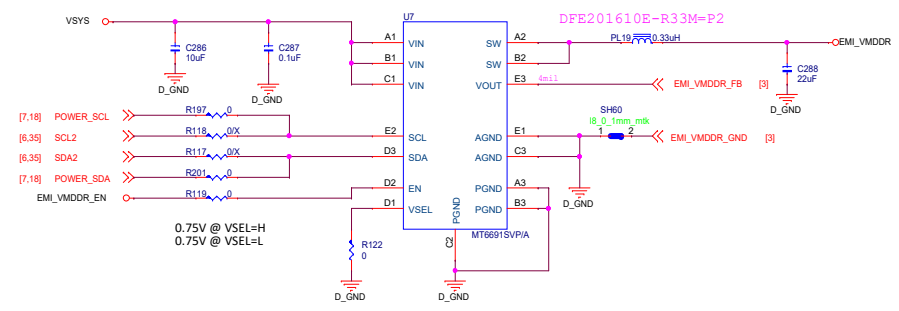
**Schematic design notice of "28\_POWER\_MT6360\_Charger" page.**

Note 28-1: For better ESD & surge performance we need choose suitable device for system protection. Please refer to the latest version of [Surge device selection guide] provided by MTK.

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VIA TECHNOLOGIES INC.	
Title	MT6360
Size	Document Number
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### LP4X DRAM: VMDDR(0.75V)

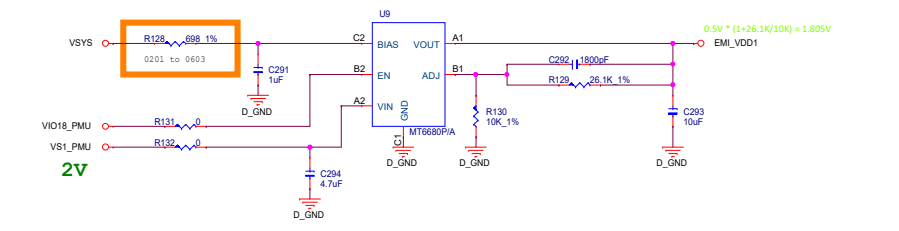


### Bypass/Boost for VSYS@LV (Reserve)

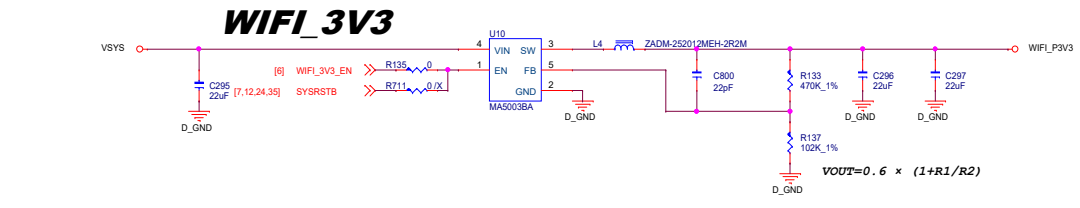
RT4803WSC I2C address: 0X75 (Write:0xEA, Read:0xEB)



### LP4X DRAM: VDD1 (1.8V)

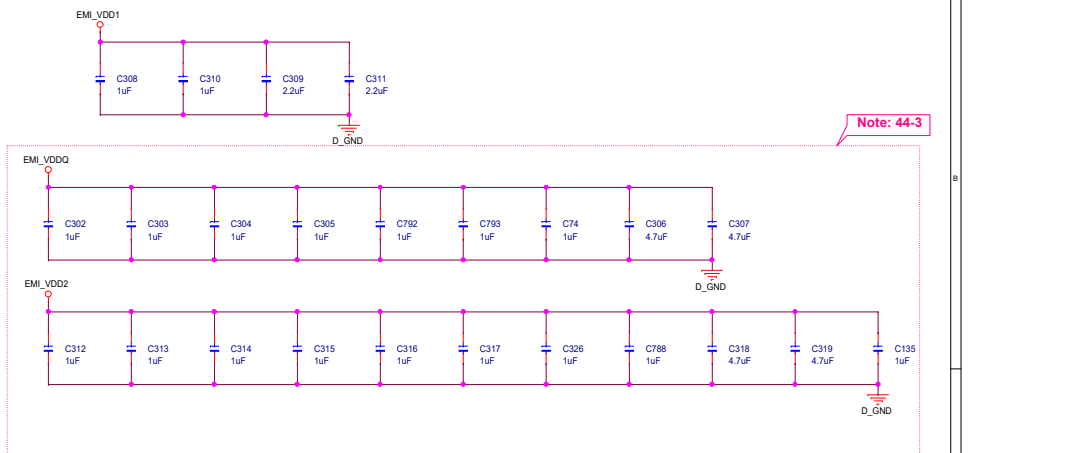
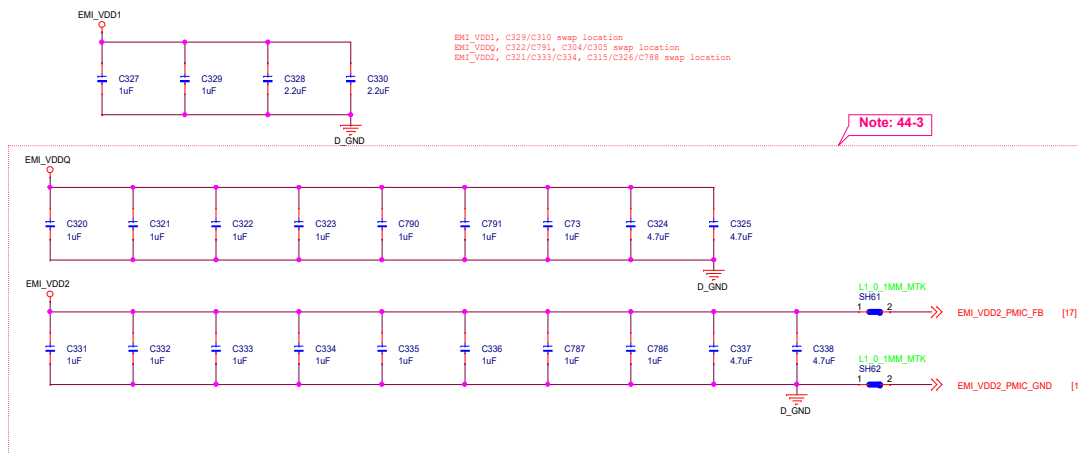
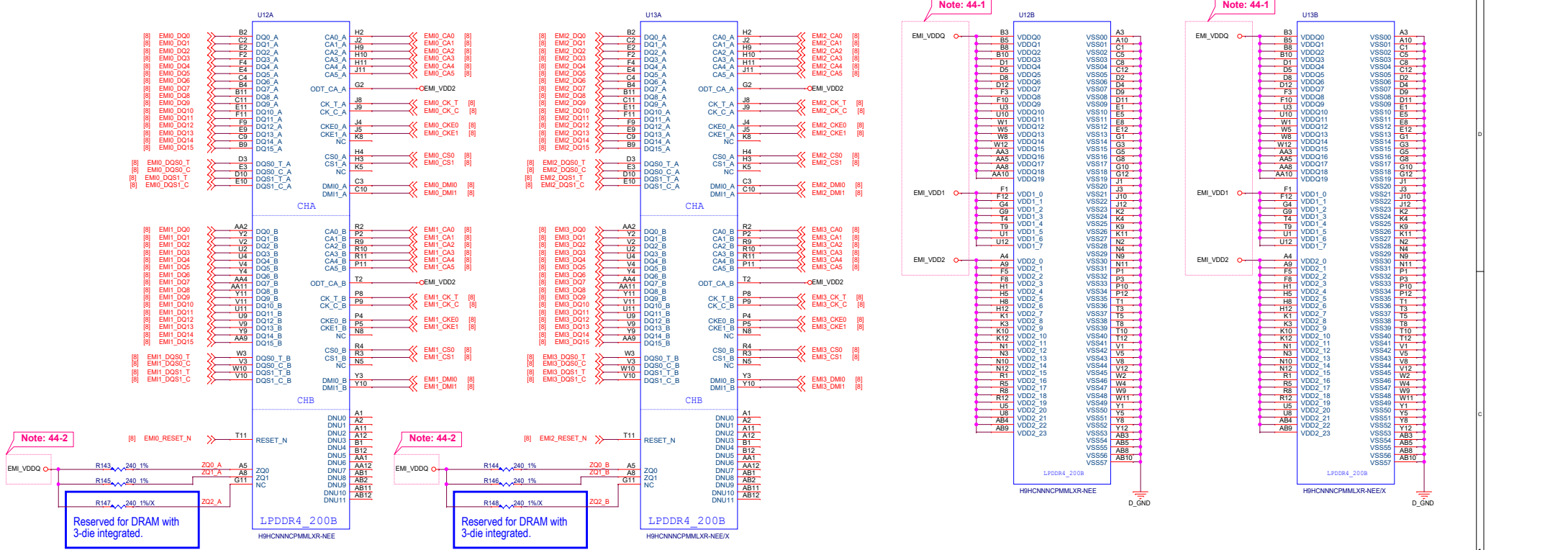


### WIFI\_3V3 2A



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		VIA TECHNOLOGIES INC.	
Title			
AC POWER IN & 3rd Party Powers			
Size C	Document Number <b>SOM-9X12</b>	Date Wednesday, December 14, 2022	Rev A
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## Schematic design notice of "44\_Memory\_eMMC\_LPDDR4X"

**Note 44-1:** Please refer to power supply related page select LDO7\_VOUT / BUCK1\_LX output voltage properly for LPDDR4X

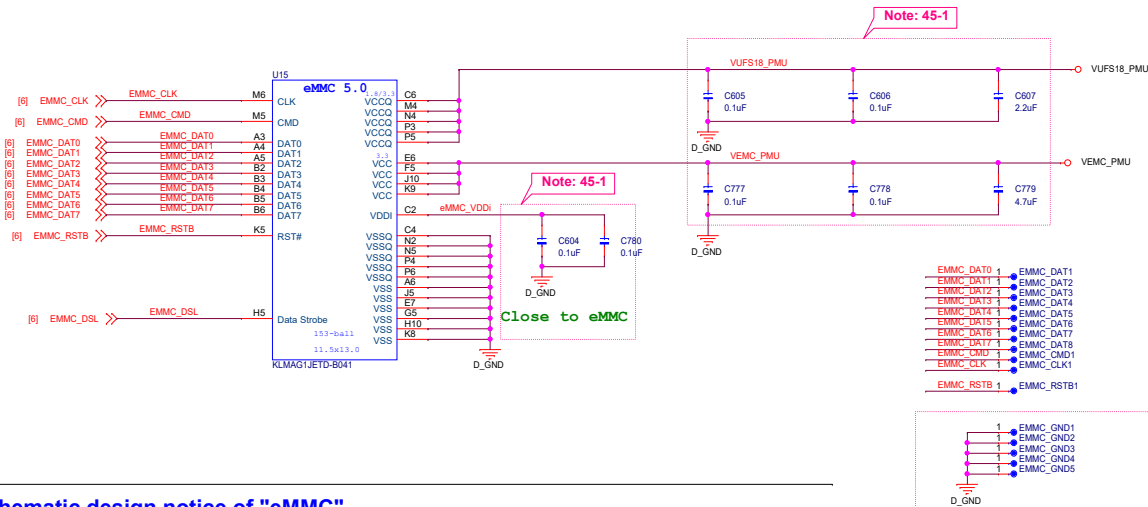
**Note 44-2:** DRAM ZQx resistor = 240ohm (1%) that must be connected to VDDQ,

**Note 44-3:** For other cap for PMIC >10uF, at PMIC page; please also refer to MMD and layout guide for placement.

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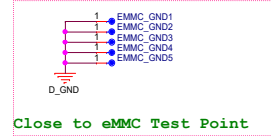
Title		Memory LPDDR4X	
Size	Document Number	SOM-9X12	
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Note: 45-1

Note: 45-1

- EMMC\_DAT0 1 EMMC\_DAT1
- EMMC\_DAT11 1 EMMC\_DAT2
- EMMC\_DAT12 1 EMMC\_DAT3
- EMMC\_DAT13 1 EMMC\_DAT4
- EMMC\_DAT14 1 EMMC\_DAT5
- EMMC\_DAT15 1 EMMC\_DAT6
- EMMC\_DAT16 1 EMMC\_DAT7
- EMMC\_DAT17 1 EMMC\_DAT8
- EMMC\_CMD 1 EMMC\_CMD1
- EMMC\_CLK 1 EMMC\_CLK1
- EMMC\_RSTB 1 EMMC\_RSTB1



### Schematic design notice of "eMMC"

Note 45-1: Please refer to eMMC vendor's datasheet or MTK common design notice to get the recommendation bypass cap. value for VCC/VCCQ/VDDI power domains of eMMC.

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<b>VIA TECHNOLOGIES INC.</b>	
Title: <b>eMMC</b>	
Size: C	Document Number: <b>SOM-9X12</b>
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		VIA TECHNOLOGIES INC.	
Title		reserved	
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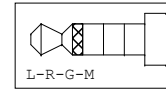
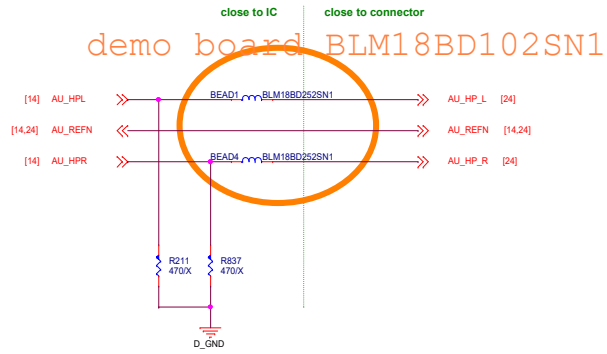
4

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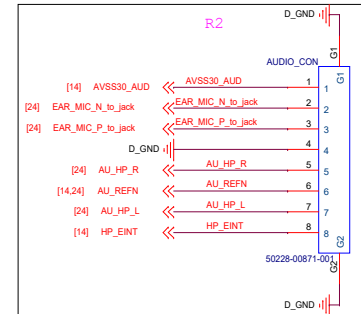
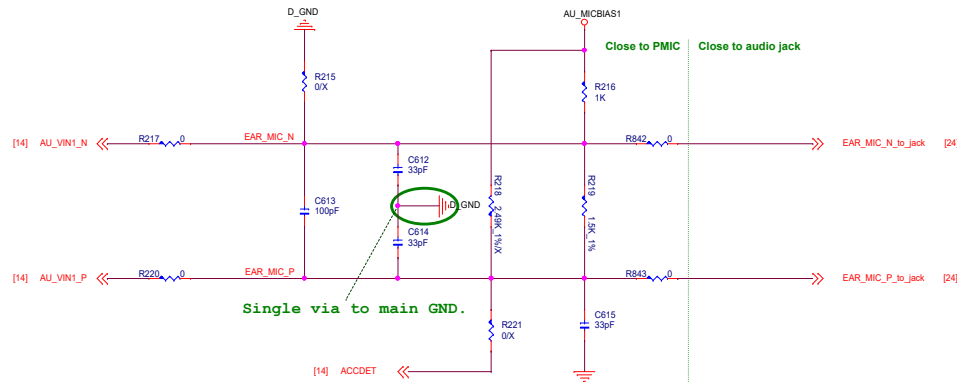
2

1

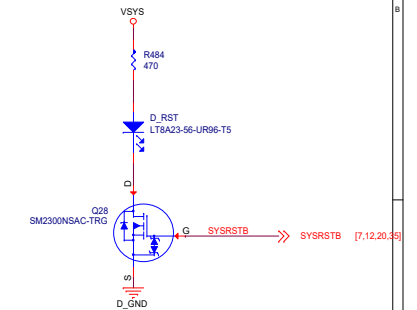
## Earphone Audio (PMIC)



## Earphone Microphone (PMIC)



## Reset LED



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VIA TECHNOLOGIES INC.	
Title: Earphone	
Size: C	Document Number: SOM-9X12
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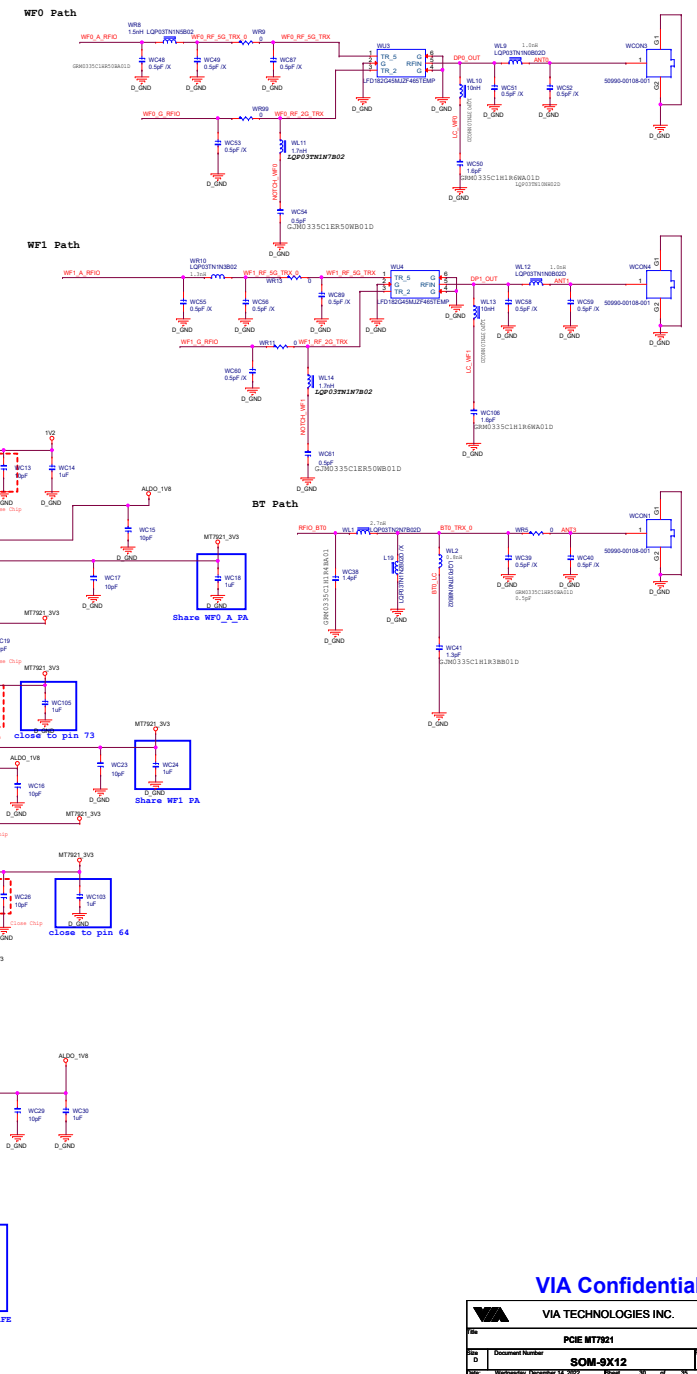
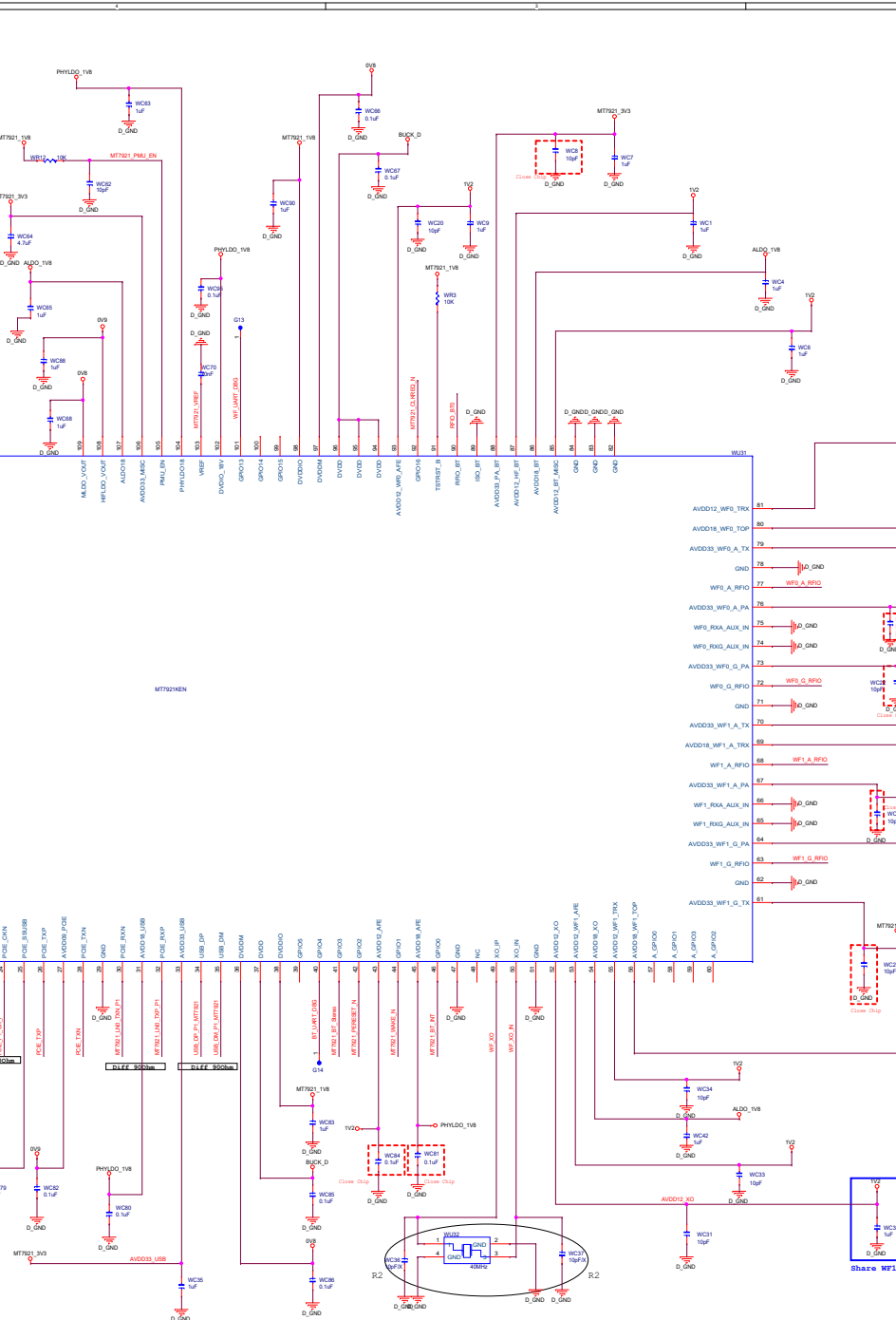
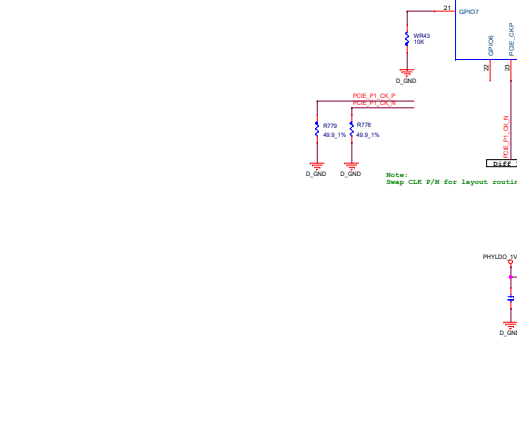
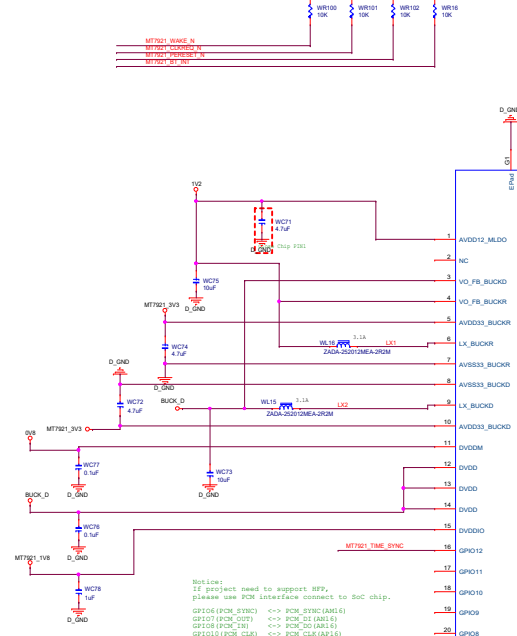
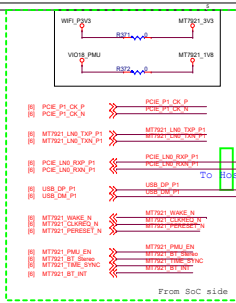
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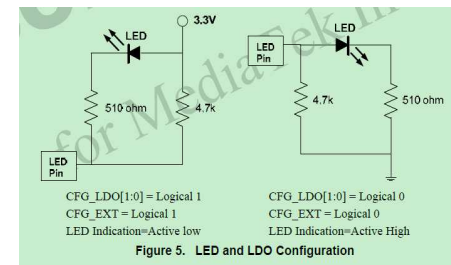
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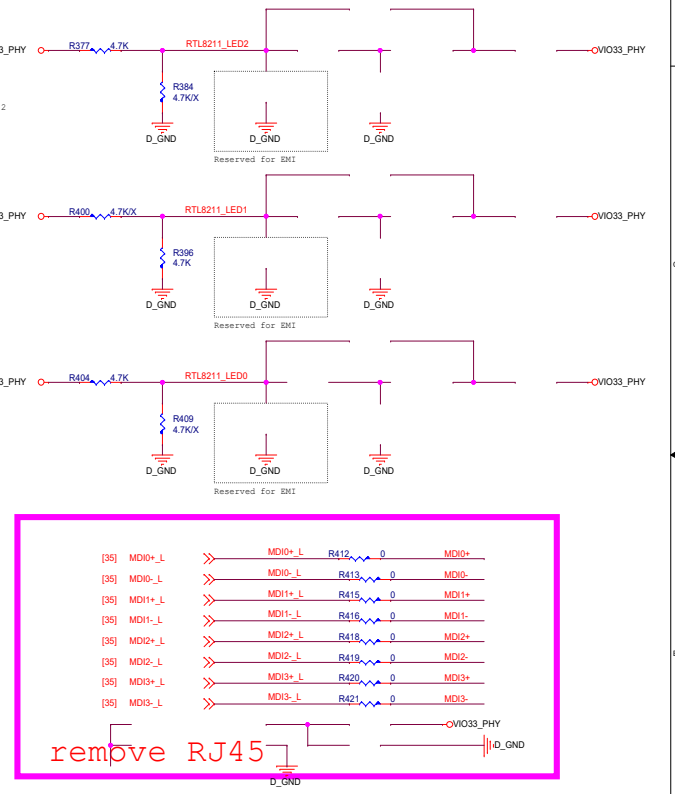
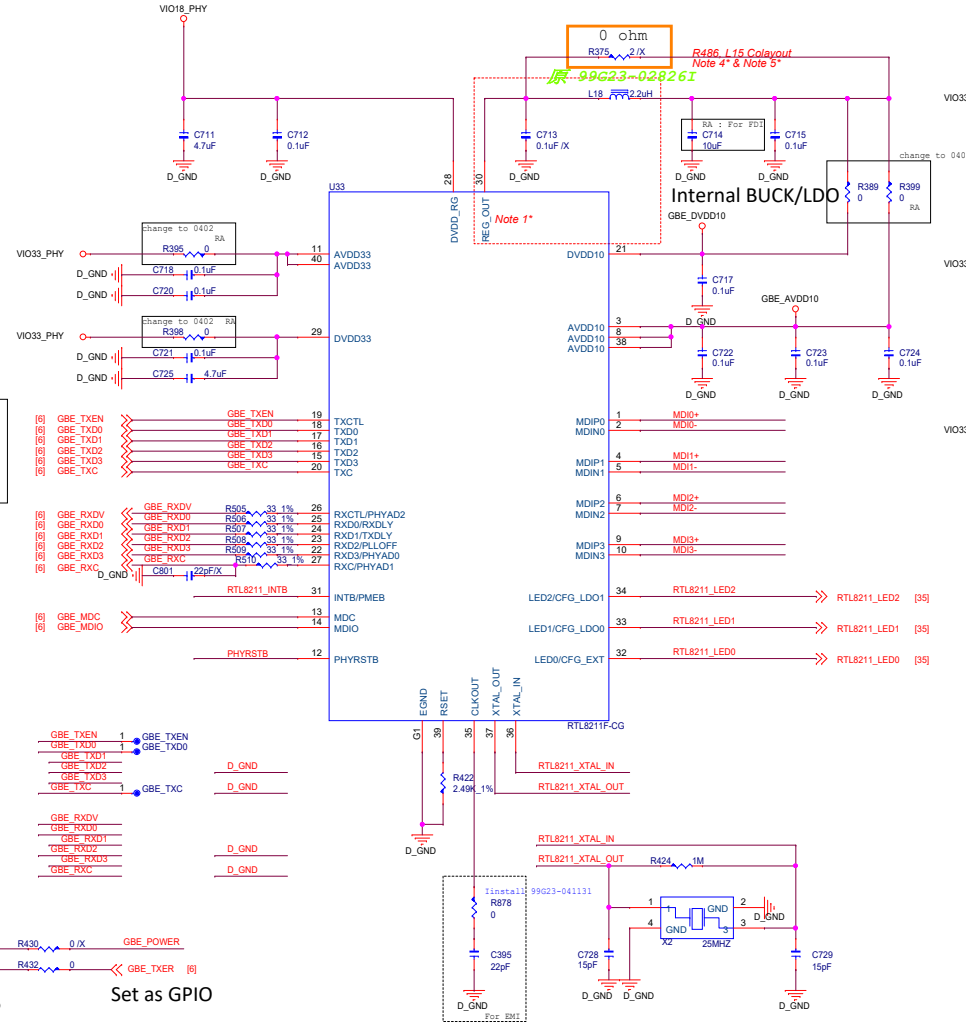
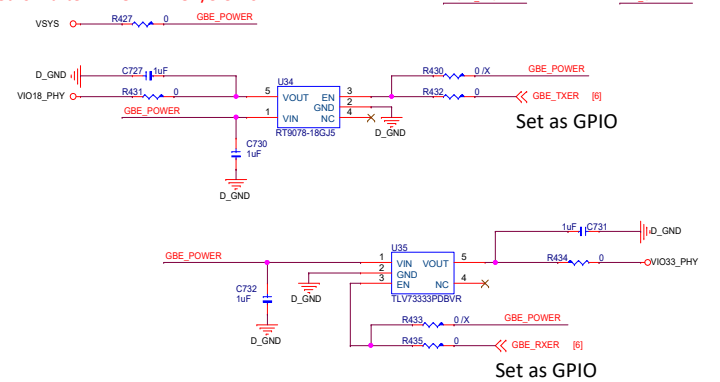
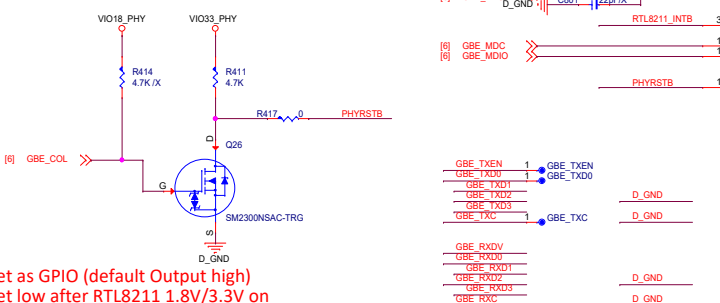
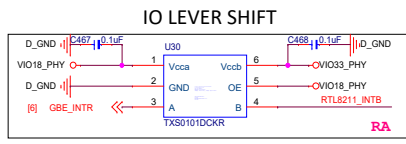
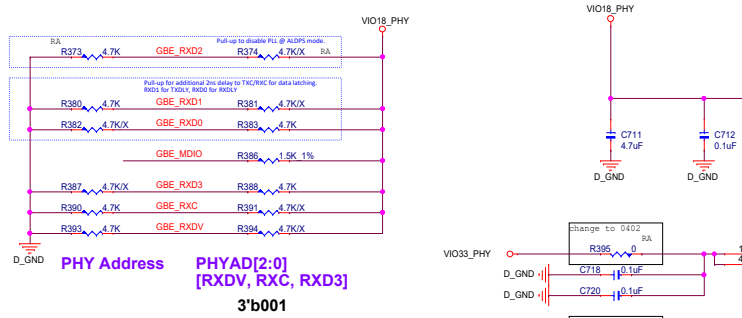
Note 1: The Trace length between L and PHY Pin 30 must be within 0.5 cm, 4.7uF and 0.1uF to L must be within 0.5cm.  
 Note 2: Bypass CAPs close to PHY DVDD10/AVDD10 power pins.  
 Note 3: Any inductance or bead except L1 is not allowed on the path from REGOUT to DVDD10/AVDD10.  
 Note 4: 0/NC is reserved to change the DVDD10/AVDD10 supply source to LDO mode (RTL8211FD).  
 Note 5: No design change of PCB model is needed if 0/NC is reserved. If only RTL8211FD used for particular PCB model, directly short REGOUT to DVDD10/AVDD10.

### POWER SWITCH TABLE

RGMII Power Source	CFG_EXT LED0	CFG_LDO[1:0] (LED2-LED1)
External 3.3V	1'b1	2'b00
External 2.5V	1'b1	2'b01
External 1.8V(default)	1'b1	2'b10
External 1.5V	1'b1	2'b11
Internal 2.5V	1'b0	2'b01
Internal 1.8V	1'b0	2'b10
Internal 1.5V	1'b0	2'b11



### RGMII PHY



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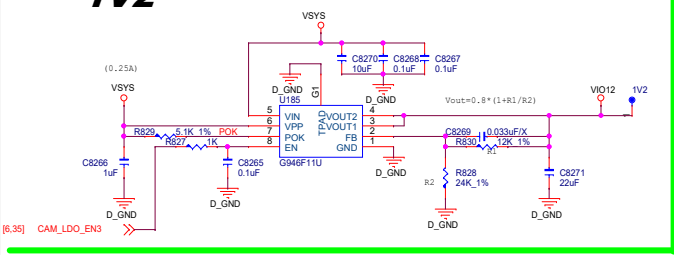
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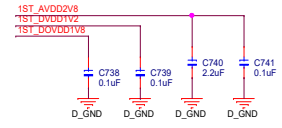


**CAMERA PWR (VCAMA\_D)**  
**Buck for VCAMD LDO input**

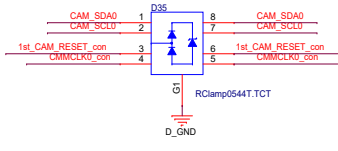
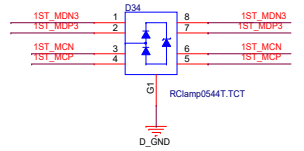
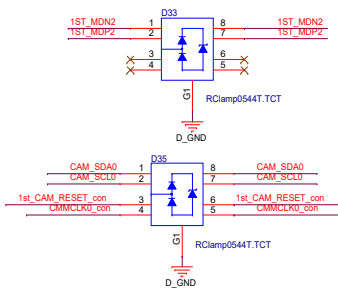
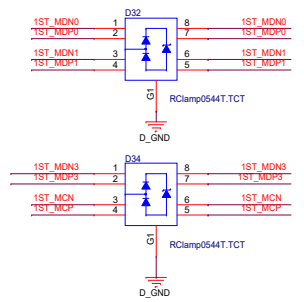
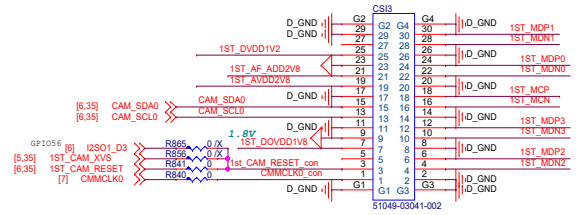
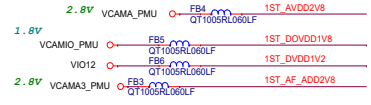
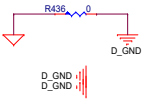
**1V2**



**SOC CAMERA1**



- [7] CS10B\_L0N >> EQWS201212M900 3 1ST\_MDN1
- [7] CS10B\_L0P >> 1 L35 2 1ST\_MDP1
- [7] CS10A\_L2N >> EQWS201212M900 3 1ST\_MCN
- [7] CS10A\_L2P >> 1 L34 2 1ST\_MCP
- [7] CS10A\_L1N >> EQWS201212M900 3 1ST\_MDN0
- [7] CS10A\_L1P >> 1 L33 2 1ST\_MDP0
- [7] CS10A\_L0P >> 1 L36 2 1ST\_MDP2
- [7] CS10A\_L0N >> 4 EOWS201212M900 3 1ST\_MDN2
- [7] CS10B\_L1P >> 1 L37 2 1ST\_MDP3
- [7] CS10B\_L1N >> 4 EOWS201212M900 3 1ST\_MDN3



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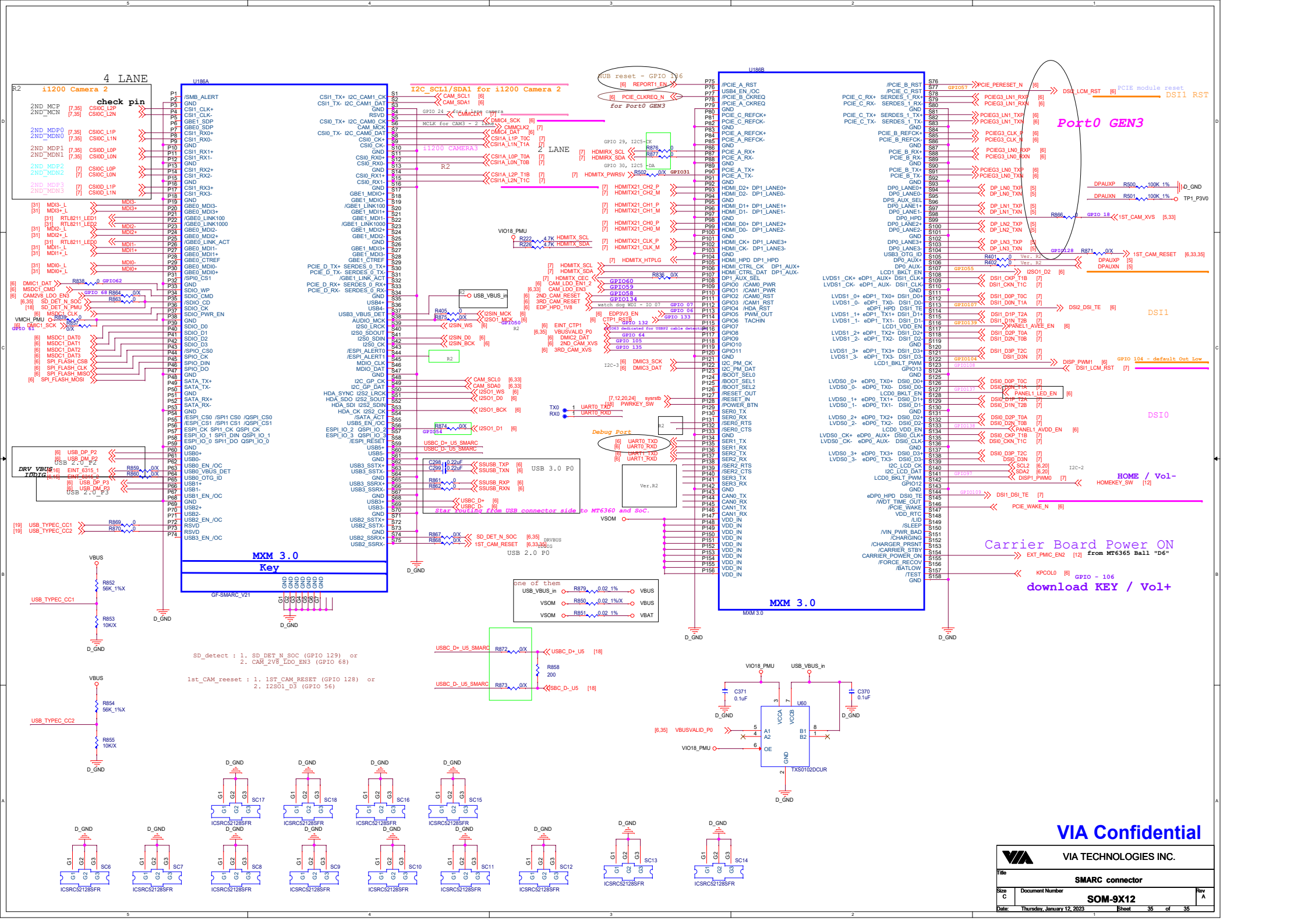
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Port0 GEN3

Carrier Board Power ON  
 KPC0L0 GPIO - 106  
 Download KEY / Vol+

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