EXHIBIT D

BLOCKDIAGRAMS SUBPARTS

SECTION I: SERVICE GUIDE:

CHAPTER 1: DESCRIPTIONS

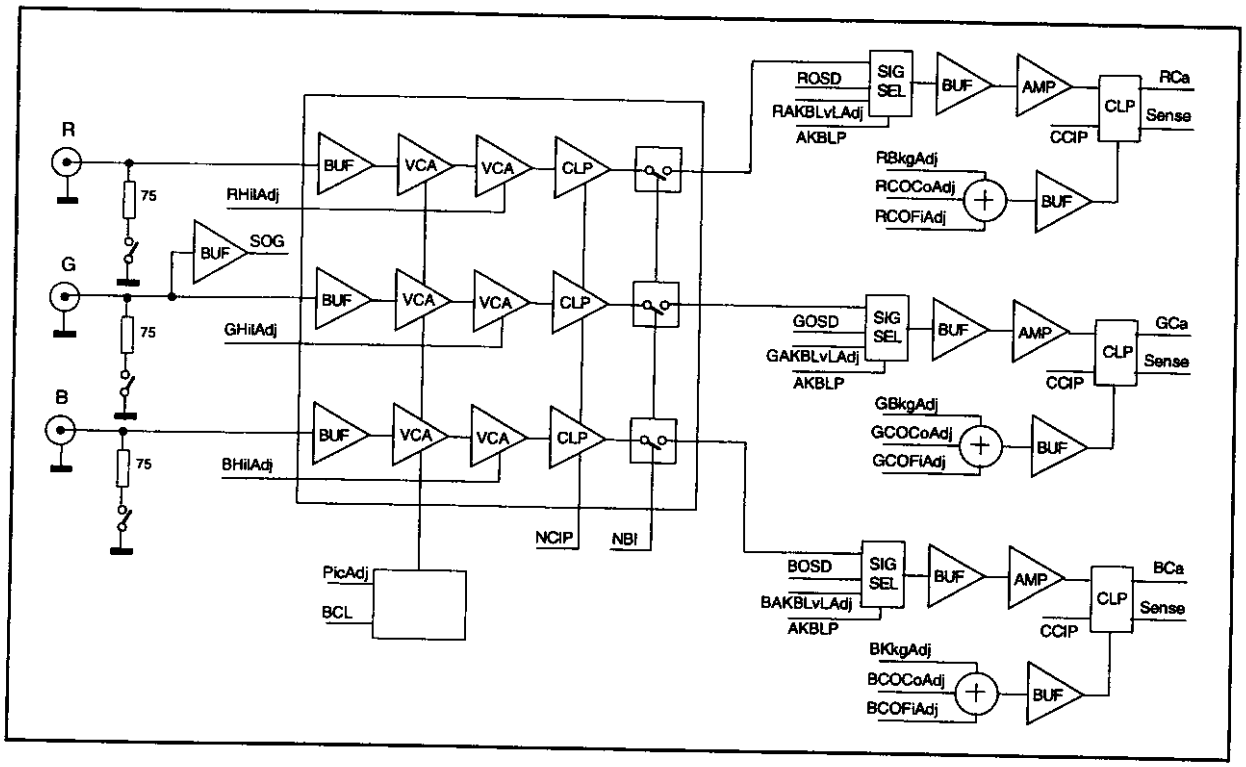
1.1 SIGNAL BOARD

1.1.1 RGB

General
The video section of the Signal board contains the following steps:
- Video inputs
- Preamplifier
- Addition of OSD and AKB pulses
- Power amplifier
- dc restorer

Moreover the circuit contains DACs for adjust voltages, the AKB measurement circuit, blanking, G1 and pulse generation, sync inputs and supplies.

Because the processing of the three video signals is done in a similar way, we consider only one of them, the Green channel, in this description.



Video inputs (diagram 1/3)
The G video signal is present at the BNC connector. The input can be terminated by means of a switch S1 that terminates the three video inputs at the same time. If not terminated, the input impedance is higher than 10kΩ.

The video signal is buffered internally in the preamplifier U4. The G video signal is additionally buffered by Q2, that leads the video signal to the SOG detection circuit.

Preamplifier (diagram 1/3)
The video signal is ac-coupled to U4, where it is internally buffered.

The PicAdj adjust voltage (from DAC U6) is connected to U4 through R2. It determines the contrast adjustment in U4, by determining the gain of the three video signals equally. The BCL_F signal can decrease the PicAdj voltage in case the beam current through the picture tube is too high.

The highlights adjust voltage GHilAdj is connected to U4 through resistor division (R337 and R338). This adjust voltage determines the gain of the G channel, independent from the other video signals.

An internal clamper clamps the video signal to 2V, which is externally determined by R5 and R6. The clamping is done when the NClp signal goes low.

After the clamping the video signal is blanked in case the NBl signal is low. This is done during the AKB interval and when the OSD is displayed. In those cases the output signal of U4 is blanked, and pin 20 (GOut) is in a quasi-high-impedance state.

OSD and AKB pulse (diagram 1/3)
The OSD information from U507 is added by Q300. The fast blanking signal (FBI) is fed to U4 through U13. At the moment that the OSD information comes from U507, FBI goes high and NBI goes low. The video signal disappears from the output of U4, which becomes quasi-high-impedant. As a result D301 and Q300 start conducting, and the OSD signal is presented at the output stage.
R300 and R339 create a dc-offset in the OSD signal, through which its black level is a little bit lower than the one from the video signal.

The AKB pulse is added by U1 and Q301. During an AKB pulse, AKBLP goes high and NBI goes low. The video signal from U4 is blanked, and the OSD buffer Q300 is blocked by the AKBLP through Q1. At the same time AKBLP blocks D302 and the dc-voltage GAKBLvlAdj is connected to the non-inverting input pin 10 of U1 as long as the AKBLP pulse is high. In that way an AKB measurement pulse is created, and presented at the output stage by Q301 and D301.

Power amplifier (diagram 1/3)
Because the output of U4 can only drive a small capacitive load, the output signal is buffered. And as the buffer should be capable of supplying high currents to the power amplifier, it is designed as a two-stage push-pull buffer. Q302 and Q303 have a low input capacity, Q304 and Q305 deliver the necessary current.

The CR6627, U3, is a three-channel amplifier where gain and pulse response are determined by external components. R331 determines the gain, C302 (high frequencies), C303 and R332 (low frequencies) determine the pulse response. C304 and R314 act as smearing compensation circuit, and R333 creates a dc-offset. D303 takes care of flash protection.

DC restorer (diagram 1/3)
The video signal is connected to the cathode by C306, C307 and Q306. The dc-level at the cathode is set by means of a clamp circuit. The dc-level is determined by the background, cut-off coarse and cut-off fine adjustments. The cathode is clamped to this dc-level during the CCIP pulse.
Clamp capacitor C306 is continuously charged by the base current of Q306, which is always present because current source Q307 delivers a continuous emitter current for Q306. The charge of C306 creates a rising base voltage at Q306.
During the CCIP Q309 acts as a current source that discharges C306 to the level where the base voltage at Q306 is equal to the emitter voltage of Q308. When this happens, both diodes of D306 conduct, and the base of Q306 is connected to the emitter of Q308. As a result the cathode is clamped to the voltage at the emitter of Q308.
This clamp voltage is created by U2, amplifier with voltage feedback. Its output voltage is determined by the background (GBkgAdj), cut-off course (GCoCoAdj) and cut-off fine (GCoFiAdj) adjust voltage.

DACs (diagram 1/3)
The DACs U5 and U6 generate 18 dc-adjust voltages and 4 digital control lines. All voltages can vary from 0 to 4V. The data enter the DACs through I2C, and are clocked out by the LdRGB pulse.

AKB measurement (diagram 2/3)
The measurement current from the G cathode (Sense) is added to the other measurement currents and connected to the inverting input of U7, pin 2. The resulting current is transformed into voltage, and amplified and buffered by Q3 and Q4.
A sample-and-hold integrator, controlled by VFlybP_F eliminates the measurement of quiescent beam current.
The measurement voltage charges a sample-and-hold capacitor C19 during the AKBMeasP. This is accomplished by switch U8 (1, 2, 10, 15). The voltage on C19 is buffered by U7 (12, 13, 14) and fed to ADC U9. The microcontroller measures the AKB voltage through I2C.

Blanking circuit (diagram 2/3)
The horizontal and vertical blanking are generated in the circuit around comparator U10 and D-Flipflop U11.

The horizontal blanking pulse appears at the output pin 5 of U11. It starts at the rising edge of the HFlybP_F, that triggers the flipflop. Q5 blocks and C23 is charged through R30. As soon as the voltage on C23 tends to exceed the voltage at the non-inverting input of U10, U11 is reset and the horizontal blanking ends. This moment is determined by HBlAdj.

The vertical blanking is generated in an identical way. Horizontal and vertical blanking pulses are added and form the composite blanking signal, CBI.
The inverse blanking pulses, NHBI and NVBI are used in the generation of the OSD.

G1 control (diagram 2/3)
This circuit consists of a blanking circuit (Q10 and Q11) and spot suppression (Q8 and Q9). During the active video, Q10 conducts because MxdBlNAKBBI is low. This TTL signal is shifted down in dc by C33 and D16. So during active video the gate of Q10 is at approx. -5V. So Q10 conducts, while Q11 is blocked. So G1 is at 0V. During blanking, Q10 blocks as the voltage at its gate becomes 0.2V because MxdBlNAKBBI becomes high. Q11 starts conducting, and G1 is connected to -50V. The CRT is blanked. During the AKB interval, MxdBlNAKBBI becomes low again, through which G1 is again connected to 0V. During that time the AKB pulses are 'written', after which G1 is connected to -50V again.

Spot protection: during the operation of the monitor, ACOK_F is high, Q8 is conducting and Q9 is blocked. C32 is charged to +170V. When the monitor is switched off, ACOK_F drops very quickly, through which Q8 blocks and Q9 starts to conduct, clamping the pos. side of C32 to 0V. As a result, the neg. side drops to -170V, which is connected to G1 through D15.
To prevent that Q10 would start to conduct, MxdBlNAKBBI is held high by U12.

Pulse generation (diagram 2/3)
This circuit generates the necessary control pulses for the clamping circuits (NCIP and CCIP), G1 control (MxdBlNAKBBI), AKB circuit (AKBMeasP, AKBLP, NBI and FocEn_F). NBI blanks the output of the video preamplifier during the AKB interval and FocEn_F interrupts the dynamic focus signal on the Frame board during the AKB interval.

Sync inputs (diagram 3/3)
The sync switch U506 switches between external H & V sync, external composite sync, and Sync on Green (SOG).
The SOG from the video input is directly connected to pin 5 of the switch.

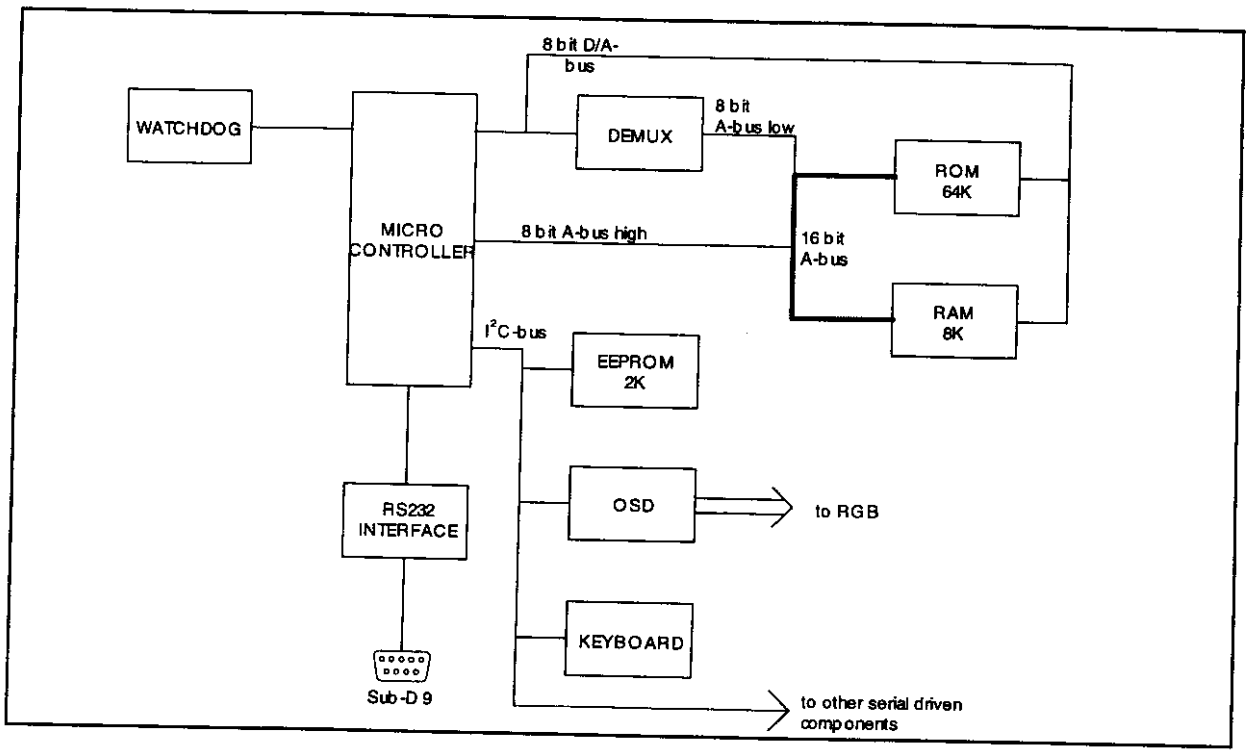
The external hor. or composite sync is clamped to ground by D520, buffered by Q504, and fed to the sync switch.
Comparator U509 transforms the signal to TTL level. The analog sync is connected to the non-inverting input, the slicing level voltage to the inverting input. This voltage is achieved by taking half of the peak level of the signal (R529 and R530). As a result the slicing level changes as the sync amplitude changes.

The external vertical sync is handled in an identical way.

1.1.2 Controller part

General

The controller part of the signal board is built around the 80c32 microcontroller, a latch to demultiplex the multiplexed AD-bus, the 27c512 EPROM for program memory, the 24C16 nonvolatile RAM and the 8k*8 external RAM. This group of components can be seen as the heart of the system.
The address range of the ROM is 64K, the external RAM is 8K, the internal RAM is 256 bytes, the NVM is 2K.
The demultiplexer separates the lower half of the 16-bit address bus from the multiplexed D/A-bus. The higher half of the 16-bit address bus is directly available on the microcontroller. This 16-bit address bus is connected to ROM and RAM. Some handshake lines directly available on the microcontroller take care of the address decoding.
An I²C bus interface generated by the firmware is used to communicate with the non volatile RAM, the OSD, the keyboard, and some other components on the signal board and the frame board.
The controller part is locally controlled via a keypad of 9 buttons, with an I²C bus interface and an interrupt output.
The controller part is remote-controlled via RS232 on a SUBD9.
The other half of the man-machine interface is the OSD (On-Screen Display).
A watchdog timer circuit prevents out-of-range operation.



Power supply

The entire control part is powered by one supply voltage only (+5VPwrOff_F) because this part of the monitor must keep on working in power off mode (highest power save mode).
This power supply is monitored by a watchdog timer MB3773 (U501), that has two jobs to do:

1. Monitor the power supply. If it drops below 4.8 V, the watchdog constantly resets the microcontroller. (RESET output pin 2 of the MB3773 is connected to the reset input of the microcontroller, pin 9). The 4.8 V sense voltage is controlled by R500.
2. Monitor the software that runs on the microcontroller. Under software control, at regular time intervals the CK input of the watchdog timer must be altered. If not, the watchdog timer gives reset pulses to the microcontroller.
   The time interval for watchdog refresh is set to 220 ms by C503. The duration of the reset pulse is also controlled by the capacitor (2 s). Jumper BR500 is normally in the run mode (R). Only in case of test or repair, it can be placed in position T.

Clock oscillator
The microcontroller (U502) has all the required circuitry inside for clock generation. All we need to add is the Xtal (Y500) and two C's (C505 and C506). The Xtal frequency is 11.059 MHz so that baud rates for the remote control can be derived perfectly.

Micro controller
The 80c32 (U502) is an 8-bit microcontroller from the 8051 family.
The microcontroller has an 8-bit multiplexed D/A-bus: DA0 - DA7 and an 8-bit address bus: A8 - A15. The 8-bit D/A-bus is demultiplexed by using the external Latch U503 which is clocked by the ALE signal provided by the microcontroller (pin 30). This results in the 8-bit Databus D0-D7 and the 16-bit Addressbus A0-A15.
These two busses are used to communicate with the 64K EPROM and the 8K RAM. There is no special address decoding required to separate the RAM from the ROM, since the microcontroller provides the PSEN signal (pin 29) to enable the EPROM and the RD* (pin 17) and WR* (pin 18) to communicate with the external RAM.
The nonvolatile RAM is controlled through the I²C-bus, so we do not need any address decoding for this memory block.

There is a simple way to check whether the heart of the system is running or not, in the sequence here described:
- The supply voltage must be between 4.8V and 5.25V.
- The Xtal must be oscillating as shown in the oscillogram that is added to the schematic diagram (signal 32 and 33).
- The reset pin (pin 9) must get a high pulse at power up and remain low for the rest of the time.
- Now the microcontroller should be able to communicate with the EPROM using the two handshake lines ALE and PSEN. Those lines are 1 MHz pulse trains as shown in the oscillogram that is added to the schematic diagram (signal 30 and 31).

The I²C bus is connected to pin 2 (SCL clock line) and pin 3 (SDA data line) of the microcontroller. The microcontroller is always the master of the bus.

The I²C clock and data lines are also used for another bus protocol, the 3-wire bus. This protocol is used to send data to the DACs.

There are 4 DAC components to be driven. Two of them are placed on the signal board itself to control the RGB part, and two others are placed on the Frame board. They are used to drive the deflection circuit.
The DACs are connected two by two in cascade, so only two handshake lines are required. The handshake is the third line of the 3-wire bus.
- Handshake RGB DACs is driven by pin 14 of the microcontroller (named LdRGB).
- Handshake Deflection DACs is driven by pin 4 of the microcontroller (named LdDat_F).

The vertical blanking pulse (NVBI) is fed to pin 1 of the microcontroller. It is used by the firmware to synchronize some actions to the vertical blanking. These actions are:
- AKB measurement
- Degauss action
- Refresh of the vertical size DAC
- Refresh of the vertical position DAC

The ACOK_F signal is connected to pin 5 of the microcontroller to inform the firmware that a software reset has to take place whenever AC is not OK.
The diode D511, together with the internal pull-up of pin 5 prevents the voltage at that pin to get higher than +5VPwrOff_F.

The main power supply is controlled by the firmware. It can be switched off by setting the line PwrOff_F high (pin 7 of the microcontroller). This is done in case of the highest DPMS mode (Power Off).

Communication with the 8k*8 RAM (U505) is controlled by two handshake lines of the microcontroller: WR (pin 16) and RD (pin 17). These control lines are directly connected to the external RAM.

OSD
The menu system through which the monitor is controlled and adjusted is displayed on-screen. The OSD chip is the STV9424 (U507). This component is controlled through the I²C bus. It provides the R, G an B output signals for OSD generation. Those three signals are mixed with the normal video in the RGB part of the signal board. A fourth pin, FBLK, is the fast blanking output. This signal is active whenever there is OSD video on one of the other 3 lines. It is used to blank the normal video information on the picture tube where OSD information must be displayed.

The OSD chip is reset under firmware control through the signal OSDRst, which is an output of one of the DACs in the RGB part of the signal board (pin 19 of U6).
The OSD chip runs with an external clock signal. The clock is the same as the one used for the microcontroller itself. Therefore the clock output XTAL2 (pin 18 of the microcontroller) is connected to the clock input of the OSD (pin 8).
Because the OSD chip is supplied from the main power supply, we must take special precautions to prevent the OSD chip from pulling down the clock signal when the main power supply is not running. This is prevented by D514 and C532.
The OSD automatically locks to the horizontal and vertical blanking signals. Therefore NVBI is connected to pin 2 and NHBI is connected to pin 3. Those signals are present whenever the main power supply is running, also when no sync is applied to the monitor (freerun).

Frequency measurement
For scan recognition, OSD parameter adjustment and DPMS, the microcontroller must have frequency information, such as:
- Frequency of horizontal clamp pulses.
- Vertical frequency on which the deflection controller runs.
- Presence of separate horizontal pulses.
- Presence and polarity of separate vertical pulses.

All this information is gathered through pin 12 (INT0) and pin 15 (T1) of the microcontroller.
There are four sources of information and only two inputs to the microcontroller, so an external sync switch (U506) is provided. The microcontroller controls the switch by its pin 6. As a result, the information on pins 14 and 15 of U506 is multiplexed in time.

Remote control
At the rear of the monitor there is a D-sub 9-pins connector. This is the remote control input connector. The protocol that can be used to control the monitor via this input is RS232 only, and must be according to the BARCO Interconnection Protocol.
Standard RS232 levels are -12V to + 12V. The microcontroller can only accept levels from 0V to +5V. A simple level shifting IC (U508) is used to connect the RS232 data lines to the microcontroller.
Protection and filtering, necessary because those lines are connected to the outside world of the monitor, are provided by:
- overvoltage protection diodes D501, D502, D503, D504
- capacitors C518, C519
- series resistors R512, R513, R514, R515

This remote connector is also used to connect a Thoma colour analyser to the monitor for automatic calibration of the color temperature. The colour analyser is supplied by the +15V from the main power supply at pin 6.
Here again, some protection is provided:
- multifuse F500 0.3 A
- overvoltage protection diodes D512, D513
- EMI filtering with F501 and C520

1.2 KEYBOARD

The keyboard has 9 keys. They are divided in two blocks:
- The block on the left has 5 keys, used to navigate through the OSD menu.
- The block on the right (4 keys) are direct access keys: Contrast, Brightness, Degauss and manual Power off.

The keys are arranged in a matrix: 3 by 3. There are 3 drive lines and 3 scan lines. Those six lines are connected to an I²C latch (U1) on the control panel.
Per default, the drive lines are low and the scan lines are high.
When a key is pressed, the dominant low of a drive line is connected to a scan line, which consequently becomes low too. This change in level at a pin is detected by U1 and the interrupt output (pin 13) becomes low. This interrupt line is directly connected to the microcontroller interrupt input INT1 (pin 13).
In this way the microcontroller is informed that a key is pressed. Now the firmware will start scanning the keyboard (through I²C) to determine which key or keys was/were pressed.

The interrupt line is reset (high) automatically when the key is released, or when I²C communication with U1 takes place.

There are two leds on the control panel. A green one and a red one. Both connected to an I/O line of U1. The leds are driven by firmware. A high level at the I/O pin puts the led out. A low level will illuminate the led.

The contrast DAC output on the RGB part of the signal board, can be driven automatically (when ALC is switched on by the user). In that case the ALC (Ambient Light Control) sensor (D3) is used. D3 is a current source. The current is converted into a voltage by C2 and R3.
This voltage can be measured with the ADC on the RGB part of the signal board. The contrast output is adjusted accordingly.
There is a connector provided for a second ALC circuit, similar to the one described above. This however is an option.

1.3 Frame board

1.3.1 Deflection

Principle (Blockdiagram on the next page)
The heart of the deflection part is the TDA4855, an Autosync Deflection Controller. Together with the 24 adjust voltages, generated by 2 DACs, this IC makes it possible that almost every adjustment can be made by software.
If the TDA4855 is driven by correct sync pulses, it will synchronise. The IC generates 2 vertical drive signals (VOUT1 and VOUT2), and the horizontal drive pulse HDRV.

The vertical deflection circuit transforms this voltage into a deflection current. To eliminate the disturbing influence of moiré patterns, the circuit contains a moiré canceller. This circuit modulates the vertical position at half of the vertical frequency.

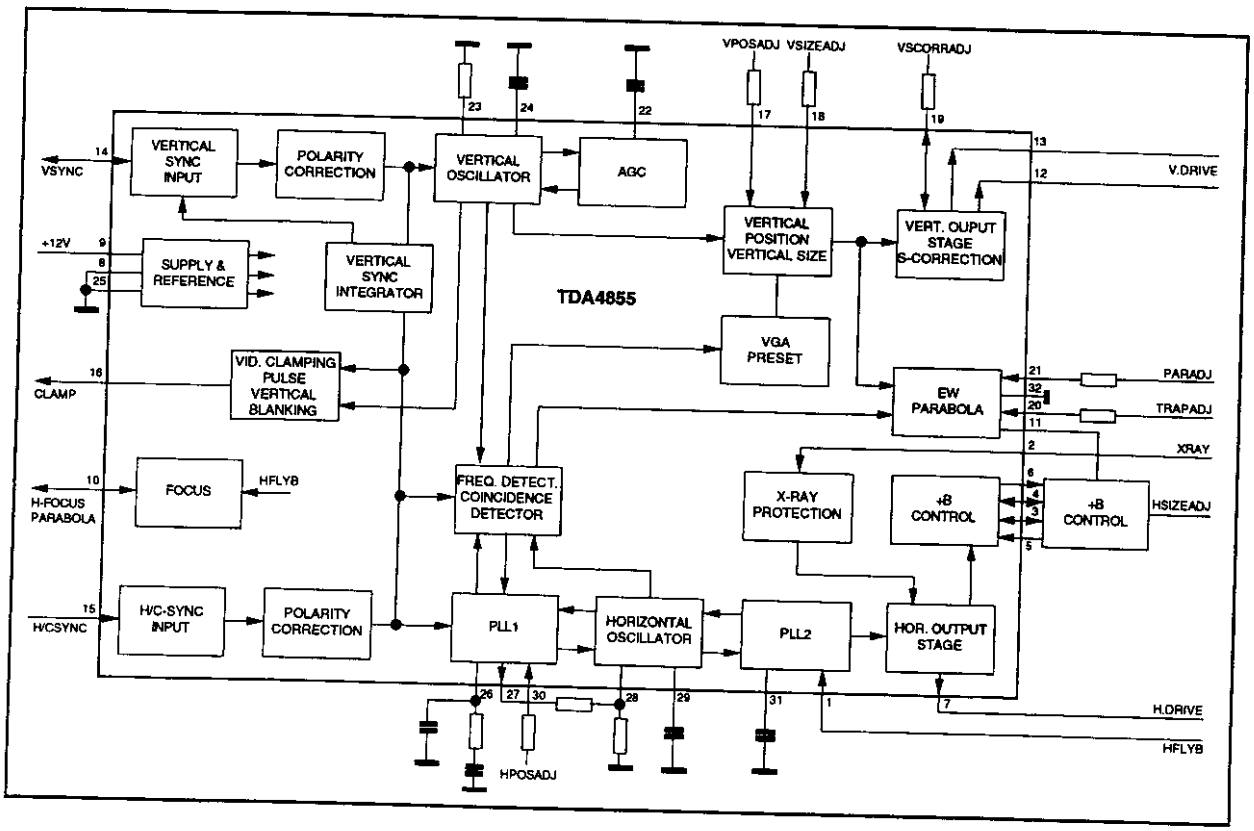
The horizontal drive pulses are connected to the horizontal drive circuit that drives the output stage. The horizontal size is controlled by the +B modulator, that drives the horizontal Pulse Width Modulator through BDRV.
The S-correction and horizontal linearity can be controlled through the serial bus.

The deflection circuit generates horizontal and vertical flyback pulses (HFlybP & VFlybP), and the EHTDwn signal from the safeguard circuit.

The TDA4855 is surrounded by a number of discrete circuits for additional corrections: skewing, bowing, corner corrections, and the dynamic focus drive signal.

At last the circuit contains the dynamic focus amplifier.

Deflection controller TDA4855



The TDA4855 contains the following blocks:
Horizontal and vertical input
The vertical sync signal enters at pin 14. It can have positive as well as negative polarity. The horizontal or composite sync enters at pin 15.

An internal vertical sync integrator extracts the vertical signal when composite sync is connected. In that case pin 14 becomes the output for the integrated vertical sync pulse. This pulse is used for frequency measurement and Power Management.

Clamping pulse
The clamping pulses are generated by the IC. They are present at pin 16. They are triggered by the trailing edge of the sync and have a width between 0.6µs and 0.8µs.

Vertical oscillator
R48, C28 and C29 determine the vertical free-running frequency of somewhat below 50 Hz. The vertical frequency range of the TDA4855 is 1:2.5, which means we could never achieve frequencies up to 150 Hz. Therefore for vertical frequencies higher than 100 Hz, C28 is switched off by the DAC output voltage VFHi through Q18, increasing the free-running frequency.
C30 at pin 22 takes care for a constant amplitude, independent from the vertical frequency.

Vertical amplitude, shift and S-correction
Vertical amplitude, shift and S-correction are controlled by the dc-adjust voltages from the DAC U2. They enter the TDA4855 at pins 17, 18 and 19. These pins are current inputs, at a voltage of approx. 5V.
The vertical S-correction is internally tracked by the amplitude and shift corrections: apart from the correction, achieved by the DAC output, the S-correction is automatically corrected inside the IC when vertical size or position are changed.
At pin 19 appears a small vertical sawtooth, superposed on the input current, that is used in the skewing correction circuit.

Horizontal oscillator and frequency-locked loop
The frequency-locked loop is able of locking the horizontal oscillator in a large range. This is achieved by a combination of search and PLL. The frequency range, with a ratio of 1:3.5, is determined by R45 and R46. Both resistors, together with C26, determine the horizontal free-running frequency.
An internal coincidence detector compares the horizontal sync with the oscillator frequency. At a difference of 4%, the control current of PLL1 is switched off, and the frequency detector starts a search operation, tuning the oscillator. When the coincidence is restored, the search mode is slowly replaced by the normal PLL operation, where a soft tuning is guaranteed and fast horizontal changes are avoided.

PLL1 phase detector
PLL1 compares the horizontal sync with the output of the horizontal oscillator.

PLL2 phase detector
PLL2 compares the horizontal flyback at pin 1 with the horizontal oscillator output. Its function is to compensate for the delay in the external horizontal deflection circuit and to adjust the phase of the horizontal drive pulse.
When pin 31 is pulled low, the horizontal and vertical outputs, as well as the +B control drive are internally disconnected, through which the pins 6, 7, 12 and 13 become floating and pin 16 (CLBL) generates blanking. This is used for one of the Power Save modes (Suspend). The Suspend signal switches pin 31 to ground. When pin 31 is released again, a soft start is generated because of C35 that is slowly charged. In the beginning, the horizontal drive pulses are narrow. They get broader as the voltage at pin 31 rises.

Horizontal position, parabola and trapezium correction
These adjustments are also achieved by dc adjust voltages of DAC U2. They are fed to the TDA4855 by means of resistors. Moreover the parabola and trapezium corrections are internally tracked by the vertical amplitude and position adjustments.
At pin 20 (trapezium adjustment input) the IC superposes a small vertical parabola on top of the input current. It is used for bowing and corner adjustments.

Bowing, skewing and corner correction
Bowing: Q4, Q5, Q12 and Q13 form a multiplier. One input is the vertical parabola current from pin 20 of the TDA4855, another is a reference voltage, derived from the VPos pin of the TDA4855. The gain is controlled by the BowAdj adjust voltage. The output of the circuit, the collectors of Q4 and Q13, modulates the HPos input, pin 30 of the TDA4855.
In a similar way, Skewing (Q2, Q3, Q10 and Q11) and Corner (Q6, Q7, Q14 and Q15) adjustments are performed.

Vertical deflection
The vertical deflection output is built around the deflection amplifier TDA8351 (U8). The symmetrical drive signals VOUT1 and VOUT2 are transformed into voltage by R60, and fed to pins 1 and 2 of U8. This IC amplifies the sawtooth, which is connected to the vertical deflection yoke. The feedback is done through R96 and R97 to pin 4 of U8.
At pin 6 we find the +V_Flyb voltage of approx. 52V, generated by T1, rectified by D18 and smoothened by C11. This voltage is used to get a shorter vertical flyback.

The flyback pulse appears at pin 8. It is buffered and transformed to TTL for further use in the circuit.

Moiré canceller
A so-called scan moiré pattern appears when there is interference between the CRT pitch, the line frequency and the vertical size. This phenomenon can more or less be hidden by applying a small vertical shift, frame after frame. Flip-flop U4, part 1 divides the vertical flyback pulse by two. At the Q output, pin 5, appears a square wave at half of the vertical frequency. Its amplitude is adjusted by the adjust voltage MreAdj, together with D10, R72 and R74. The adjusted pulse is fed to the deflection amplifier.

Horizontal drive circuit
The horizontal drive pulses from the TDA4855 (pin 7) are buffered by Q27, Q25 and Q26. The buffered signal is EHTDrv. It is the drive signal for the EHT circuit on the one hand, and is coupled by C55 to the horizontal driver on the other hand.
The drive pulses are transformed into drive current for the deflection transistor by auto transformer T3.
The amplitude of the base current of Q38 depends on the charge at C60. For small horizontal amplitudes this charge voltage is limited by R100. To increase the horizontal size of the image, the adjust voltage HSizeAdj must decrease. As a result, Q20 and Q28 draw more current, resulting in a higher voltage at C60, and a higher base current at Q38.

Horizontal output
The basic deflection circuit consists of deflection transistor Q38, recovery diode D43, flyback capacitor C84//C85, S-correction capacitor C83, choke coil T1, and the horizontal deflection yoke.
For correct S-correction over the frequency range, 5 programmable S-capacitors are switched in parallel to C83.
For linearity corrections, a controllable linearity coil T2 is added in the circuit.
The deflection transistor is protected by an overvoltage circuit D42, C88 and R154.
To correct for tolerances in the raster centering, a horizontal shift circuit is provided: L4, D38, D41 and P2. When P2 is adjusted out of its center position, a dc-current flows through the deflection yoke in one or the other sense.

Supply: the supply for the deflection must depend on the horizontal frequency and picture width. It is derived from the +B (180V) by means of a step-down convertor with Q32 as switch, controlled from the TDA4855. D26 acts as freewheel diode and T1 as coil. The period that Q32 conducts determines the eventual supply voltage for the deflection circuit.
Q32 is controlled through a high-side FET driver U11, by the voltage BDrv from pin 6 of the TDA4855. This voltage is inverted by Q21 before being fed to U11.

Horizontal S-correction and linearity
S-correction: the total value of the S-capacitor must depend on the horizontal frequency. Therefore 5 capacitors can be switched separately in the circuit by means of MOSFETs. The capacitors C57, C68, C72, C74 and C78 are switched by the outputs HSCorr1...5 of the DAC U1. When one of the outputs of the DAC is low, the corresponding FET is saturated, and the corresponding S-capacitor is switched on. The microcontroller determines which S-capacitors have to be switched. Its decision is based on the horizontal frequency and a possible offset given by the user in the adjust menus on-screen. The higher the horizontal frequency, the lower the value of the S-capacitance should be.
Quad comparator U5 prevents the occurance of failures due to the situation where the total S-capacitance would be too small. The outputs of the comparator depend on the horizontal VCO output voltage (U7 pin 27) and the voltage over R65, that is a measure of the number of capacitors that are switched on. When pin 2 of U5 is low, C72 is switched on, when pin 1 is low, C74 is switched on.
Linearity: is accomplished by means of a dc-controllable coil in series with the deflection yoke. By changing the current through the coil, the value of the coil impedance changes.
The linearity coil is T2. The deflection current flows through winding 1-2, the winding 3-5 is the control winding through which the dc-current flows. R141 and D34 form an anti-ringing circuit.
The control winding, together with D32 and switching transistor Q24 act as step-down converter from the +12V. The on-time of Q24 will determine the current through the control winding. This time depends on the output of U9, pin 3. This is a monostable multivibrator, triggered by HFlybP, and with a time determined by the adjust voltage HLinAdj.

Safe guard circuit
Comparator U3 (1, 2, 3) compares the +V_Flyb voltage with a voltage resulting from the detection of the VFlybP pulse.

The +V_Flyb voltage is derived from the horizontal flyback pulses (by T1), and VFlybP is the result of the vertical deflection.
When the horizontal deflection fails, +V_Flyb will be absent, and pin 3 of U3 will be lower than pin 2. As a result the output is low, switching off the EHT.
When the vertical deflection fails, VFlybP is absent, and is not detected by D8/C8. As a result, pin 2 rises to +12V, so pin 2 becomes higher than pin 3, and the output becomes low, switching off the EHT.

Dynamic focus
At pin 10 of U7 (TDA4855) appears a horizontal focus parabola, which will also be present on the collector of Q16. Its amplitude there depends on the HFocAdj adjust voltage from DAC U2.
The pulse FocEn switches off the horizontal focus parabola during the AKB measurement to prevent influence on the measurement.
The parabola is fed to the power amplifier by Q39, C92 and R159.

At pin 20 of U7 appears a small vertical parabola on top of the trapezium correction input current. The parabola is fed by R50 to transistor pair Q1 and Q9. It is also present on the collector of Q9, with an amplitude depending on P1, the vertical focus adjustment. The vertical focus parabola is buffered by Q17 and fed by C49 and R102 to the amplifier.

The power amplifier is a cascode amplifier with active load (Q36 and Q37). It is supplied with the +HT voltage of approx. 850V. It amplifies the horizontal parabola to 400V and the vertical one to 150V. Its feedback is done by R124, R131 and R133.
The output is coupled to the focus potentiometer by R140 and C81, and protected against flashes by SG1.

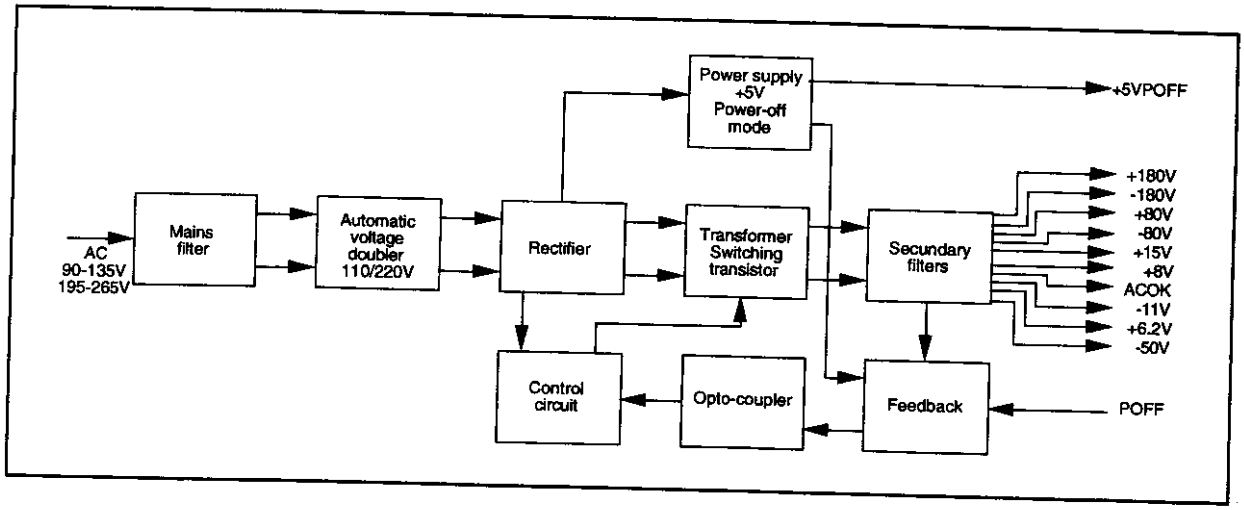
Raster rotation
The dc-adjust voltage RotAdj from DAC U1 is fed to LF amplifier U204 (diagram sheet 2/4), that supplies the necessary current through the rotation coil. The dc-current through the coil can be either positive or negative between 0 and 120mA.

1.3.2 Switched Mode Power Supply

General

The switched mode power supply (SMPS) has a mains input range from 90 Vac to 135 Vac and from 195 to 265 Vac.
It contains an additional +5V power supply for the microcontroller and a main power supply for the other supplies.
The secundary voltages from the main power supply are:

+180V	horizontal deflection, EHT
+170V(R) (G) (B)	RGB board
+80V	RGB power amplifiers
-80V	quick degauss
-50V	RGB board
+15V	vertical deflection, quick degauss, 12V supplies
-11V	-5V supplies, EHT drive, quick degauss
+8V	+5V supplies
+6.2V	filament voltage



Mains input

The mains voltage enters via the mains filter on the monitor chassis, and is fed to the filter in the SMPS circuit: C256, L206, C258 and C257. The mains capacitors are charged through NTCs R231 and R232 that limit the in-rush current. Automatic voltage selector U205 detects the type of mains voltage. In case of 220 Vac, triac TH200 is switched off, and the mains capacitors are charged by the full-wave rectifier bridge D216, D217, D218 and D219. In case of 110Vac, U205 switches on TH200, and the mains capacitors are charged by two half-wave rectifiers (voltage doubler) D216 and D219. D215, R255 and C237 take care for the supply for the IC. R246 and R247 form a resistive division that is a measure for the mains voltage. R245 and C238 determine the trigger frequency for the triac. Pin 5 triggers the gate of TH200 through R229.

5V power off

This separate supply is self-oscillating. When the current through R259 reaches a certain level, Q204 is switched off by D221 and D222. The energy charged in the transformer will charge C255 through D223.

The 5V supply is stabilised by zener diode D224.
R257 and R258 take care for the switching of Q204 when the monitor is started up. R264 and C253 deliver the base current for Q204 in normal operation.

Control circuit TDA8380 (U206)

The control circuit operates on a fixed frequency (28.5 kHz), with duty cycle control. During startup of the monitor, the supply for U206 is generated by charging C234 through Q204 (5V power off supply), which acts as a current source. After startup, D211 and R222 take over and C234 is supplied from T200, winding 7-8.
R234 and C247 at pin 10 determine the switching frequency.
R238 and R251 divide the feedback of the secundary voltage. If the voltage at pin 7 becomes higher than 3.1V, the over voltage protection becomes active. The SMPS is switched off and starts again with a slow start. C242 takes care for the slow start sequence, generating a duty cycle that starts from 0 and increases towards a normal regime. R239 determines the maximum duty cycle.

Pin 13 is the over current protection input to protect the transformer T200 and switching transistor Q202 against a primary current that is too high. Sense resistors R219 and R236 sense the current and feed it to pin 13. C241 makes pin 13 insensitive to spikes. If the voltage at pin 13 falls to 200mV, Q202 is switched off for one period. When the voltage drops to 0V, the SMPS is switched off completely and the slow start procedure begins.

Switching transistor and drive

The base current to switch on Q202 is delivered by a transistor inside U206. R228 and R233 determine the amplitude of the base current. To reduce switching loss of Q202, a snubber circuit (D207, R210 and C206) is provided. A peak voltage clamp (D206, R206 and C205) protects Q202 against a harmful peak voltage at its collector.

Secundary outputs and feedback

The secundary voltages are produced by rectifying the flyback voltages at the secundary windings of the transformer.
The -80V supply is stabilised by the circuit around Q200. The filament voltage (+6.2V) is stabilised by the circuit around Q201. The +12V is generated from +15V and stabilised by U203.
The +5V is generated from +8V and stabilised by U202.
OpAmp 1 of U208 (1, 2, 3) creates the signal ACOK, that drops from 6V to 0V when the secundary voltages tend to drop. This signal is used for spot suppression on the signal board.

The feedback is done by sensing the +80V supply. The 80V is divided by R224, R242, R243 and P200. It is connected to pin 6 of OpAmp U208. There it is compared to a reference voltage of 6.2V at pin 5 (reference zener D214). The output of U208 drives the diode in opto-coupler U207. At the primary side, the transistor in U207 drives Q203, that influences the duty cycle pin 9 of U206.
In case the secundary voltage tends to rise, the voltage at pin 9 of U206 decreases. This results in a smaller duty cycle of the switching signal of Q202, which results in a decrease (thus correction) of the secundary voltage.
The main SMPS can be switched off by pulling pin 2 of U207 to ground. In this case a large current flows through the diode of the opto-coupler, which is detected at the primary side as an over voltage occurance. This is accomplished by making PwrOff high, through which Q205 conducts.

1.3.3 Quick degauss

Principle:
Two FETs (switches) alternatively connect the degauss coils to +80V and -80V. This creates a triangular alternating current through the coils. As the switching time of the FETs decreases in time, the amplitude of the degauss current also decreases. The end of the cycle is formed by an oscillation in the coils and a parallel capacitor.

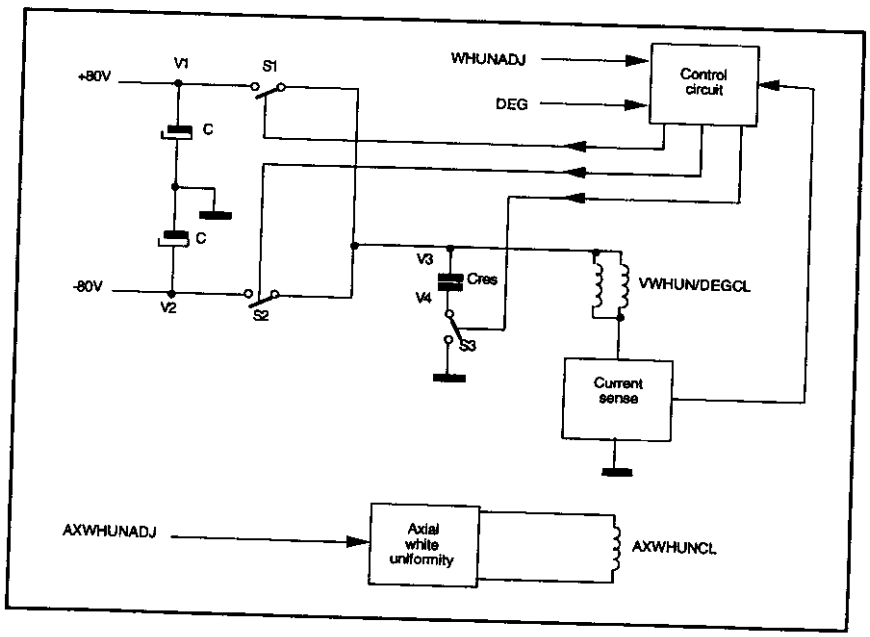
Q306 switches on: Deg makes pin 1 of U301 go low. Q303 blocks, its collector goes from -11 to +15V. This is differentiated by R302 & C304. Result: Set input of U300a is triggered. Output pin 1 goes high. Q304 & Q306 switch on. The degauss current rises.

Q306 switches off: Voltage over C316 decreases due to pin 1 of U301. Voltage over R338 increases due to degauss current. Both voltages are compared in U302 (8,9,14). When they get equal, pin 14 of U302 switches, giving a Reset at U300. Its output goes low, and Q306 switches off. The degauss current falls.

Q307 switches on: When degauss current reaches zero, voltage over R338 is 0. The output of U302 (2,4,5) will also be 0. Q302 blocks and its collector goes from low to high. This is also the clock-input of U300 (8-13). So output pin 13 goes high. Q305 & Q307 switch on. The degauss current goes negative.

Q307 switches off: Negative voltage over R338 is fed to Q308. This circuit acts as a voltage-depending resistor, depending on the VWhUnAdj voltage. The output is compared inU302 (10,11,13) to the ever decreasing voltage over C316. When they match, pin 13 of U302 resets U300 (8-13). Its output switches off. Q305 & Q307 switch off. The negative current rises again.

End: The voltage over C316 has almost reached 0. Pin 1 of U302 switches to low. Both parts of U300 are disabled. Q306 & Q307 are blocked. The degauss current is an oscillation Ldegauss-C301.



Vertical white uniformity
As explained above, the VWhUnAdj adjust voltage influences the degauss current. It actually generates a dc-offset in the current, so that there remains a magnetic field after degaussing. This magnetic field must compensate for the influence of the earth magnetic field.
It should be clear that this adjustment is only effective after degaussing.

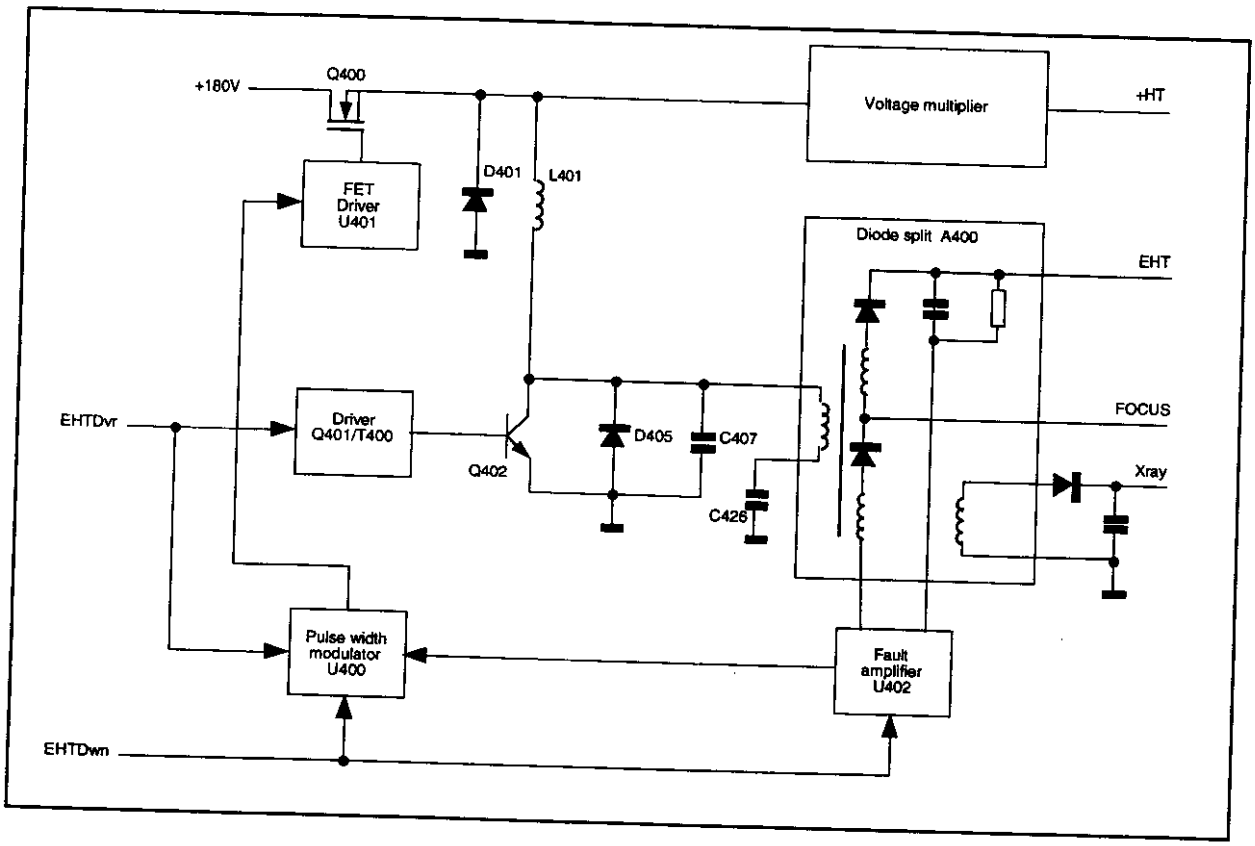
Axial white uniformity
The AxWhUnAdj adjust voltage is connected to amplifier Q312 & Q311 that drives the compensation current through the separate axial uniformity coil.

1.3.4 EHT

General

The EHT generator produces a stabilised high tension of 27 kV and a focus voltage of about 13.5 kV. Additionally it produces the +HT voltage of about 850 V. This is the supply voltage for the dynamic focus amplifier.

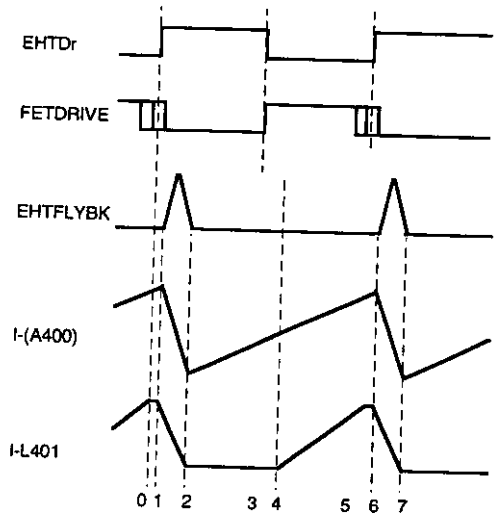
The circuit acts as a flyback generator with diode split transformer A400. The EHT generator is synchronised with the horizontal deflection by the signal EHTDrv. It contains an EHT limit protection, an EHT Down control line, and Beam Current Limiting.



Principle

The EHT is generated by a flyback generator and diode split transformer. The switching transistor Q402 is continuously switched on and off at the rate of horizontal frequency. Q401 and T400 take care for the appropriate drive.
While Q400 is conducting, the diode split transformer is filled with energy. When Q402 then blocks, this energy is transferred to the resonance circuit with C407. As a result, the primary side of the diode split transformer gets a flyback voltage. At its secondary side, it generates a dc voltage.
The amount of energy depends on the on-time of Q400, which is determined by pulse width modulator U400.

The following figure shows the most important currents and voltages in this circuit:



Diode split transformer

The diode split transformer generates the high tension. It consists of a primary winding and a secondary section that is split in different sections. Between the split sections there are high voltage diodes. This explains the name: diode split transformer.

The voltage, generated in each of the secondary sections is rectified and added on top of the rectified voltage of the previous section. On top we find the EHT.

Q402 driver circuit

The EHTDrv signal comes from the horizontal PLL (TDA4855) and drives low power FET Q401. This FET is connected to a driver transformer at its drain. R407 and C410 filter the +15 V supply, and C423/R421 form a damping circuit over the transformer. The voltage at the transformer's secondary side delivers the necessary base current for Q402 through R405/R406/D413.

Q400 driver circuit

Q400 is connected in the +180V supply line. It switches at horizontal frequency, with an on-time determined by U400.

The gate of Q400 is driven by high-side driver U401. We can consider two situations:

- Q400 is not driven, thus is blocked. The source voltage is almost 0. Pin 7 of U401 is low. The voltage at pin 8 of U401 is approximately 12 V.
- Q400 is driven and conducting. A positive pulse at pin 2 of U401 makes pin 7 become positive. The gate of Q400 becomes more positive than its source, so Q400 conducts. As a result the voltage at the source becomes 180 V, just like the voltage at pin 8 of U401. As a consequence D417 blocks immediately, isolating the 180 V from the 12 V. C417 now is charged with enough energy to keep Q400 conducting until the start of a new cycle.

Control circuit

EHT stabilisation and adjustment: U400 determines the on-time of Q400 through driver chip U401. U400 acts as voltage driven monostable multivibrator. It is triggered by the falling edges of the EHTDrv pulses. The output pulse width depends on the time constant of C416, R410 and R431, and the voltage at control pin 5. This voltage is the result of error amplifier U402 (output pin 6). The error amplifier compares the reference voltage at D420 with the divided high tension, divided by R426 and P402 (EHTAdj). This potentiometer influences the division, and thus the EHT.

BCL: The base current of Q403 is the difference between the current through R423 and that through the diode split transformer. When the transformer current reaches a certain value, the base current of Q403 will tend to reach 0. At this point, Q403 blocks and the EHT decreases. In this way a beam current limiting is obtained. The voltage at pin 8 of the transformer, influenced by P403, is a measure of the beam current. This voltage controls the switching of Q404, that gives the BCLInfo signal to the RGB amplifier.

EHT limit protection: The voltage from winding 4-5 is rectified by D412. A portion (Xray), adjustable by P401 (EHTLimAdj) is fed back to U7 in the deflection part. If the Xray voltage exceeds a certain value, U7 suppresses the EHTDrv pulses as long as the supply voltage remains.

EHT down: When the EHTDwn line is low, it switches off the EHT. This is the case when one of the deflections is down.

Voltage multiplier

The voltage multiplier creates the +HT voltage, supply for the dynamic focus amplifier.

The voltage at the source of Q400 is a square voltage between 0 and 180 V. This voltage is multiplied by 4 successive stages that each add 180 V. The resulting +HT voltage is about 850V.

CHAPTER 2: UNIT AND BOARD LOCATION

The following figure shows the location of the units and the boards in the MWD 321. One can find a swapping description in CHAPTER 3: "MAINTENANCE".

WARNING

Never remove boards or units while the display is connected to the mains

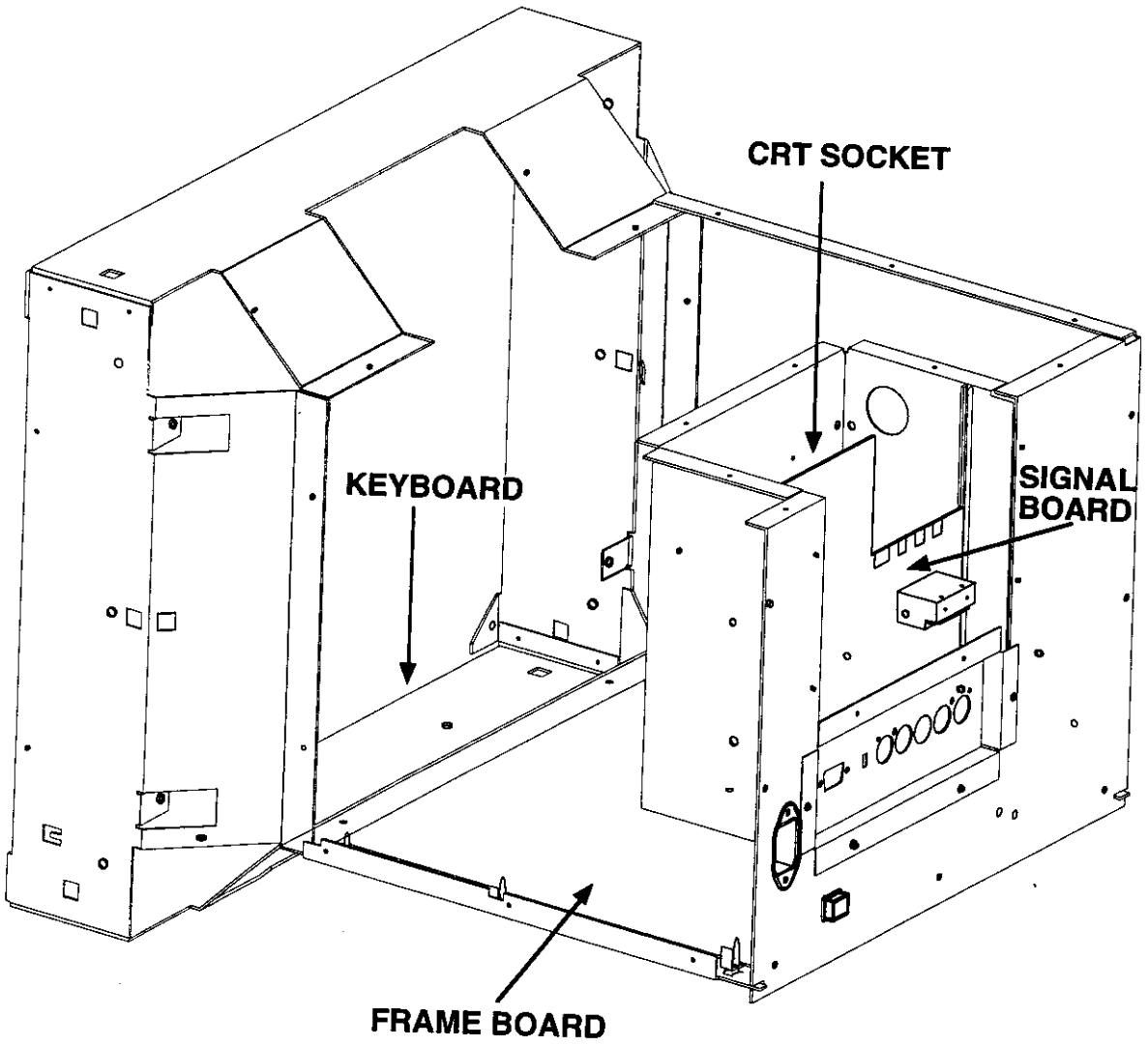


EXHIBIT E

DESCRIPTION OATS KTL

For practical reasons, an other OATS which is owned by 'KTL Arnhem' (previously called 'Telefication") was used to collect the final radiated emission results.

The KTL OATS is not a 'listed facility'.

A copy of our request to use this facility to the FCC and the response from the FCC is enclosed in this exhibit.

Address: KTL Arnhem
Utrechtseweg 310
6812 AR Arnhem
+31 26 3780780
contact person mr. P. Suringa
The Netherlands

The OATS is built on the roof of building H21 located at the premises of KEMA at Arnhem. A streetmap and relevant photographs are enclosed in this exhibit.

The metallic groundplane, dimensions 20 m * 10 m, is consisting of a 30mm*30mm*30mm galvanized grid.

A top-view of the OATS (constructing drawing) is presented in this exhibit.

All structures, including the dome, above the metal groundplane are made of synthetic material.

The control room is located inside building H21. The DUT is placed on the turntable and is transported to the OATS by means of an elevator.

The DUT and the antennas are observed, in the control room, by means of two cameras. The measurement receiver and the antenna- and turntable controller are operated at the control room.

The antenna-polarisation (horizontal and vertical) and the antenna-height (1-4 m) are controlled at the control room.

Some relevant specifications regarding the turntable and antenna mast are included in this exhibit.

Since the 3 meter antenna-mast was not operational at the time of the measurements the measurements were performed at an increased measurement of 10 meters.

Extra plots concerning the 3 meter pre-scan results carried out in the (listed) Anechoic Chamber are enclosed in the measurement report to indicate the (radiated emission) performance from the DUT at 3 meter.

The NSA results at 10 meter according to CISPR 16-1 (1993) are enclosed. The presented NSA measurements were carried out by P. Suringa at October 14th 1998.

Except for the biconilog antenna, all used equipment was filed to the commission. The calibration certificate (unfortunately written in Dutch) of the biconilog antenna is enclosed in this exhibit.

E-Mail Time 20:21:51 Date 24-02-99

From: TPHILLIP@fcc.gov
To: H.T. Jonker
Date Posted: Friday 15 January 1999 21:48:09

Subject: new OATS KEMA -Reply

Dear Mr. Jonker,

For this case only, we will accept your proposal provided that you submit a complete description of the test site with the application. Also include a copy of your request and our response.

>>> <H.T.Jonker@kema.nl> 01/15/99 10:19am >>>

Dear mr. Phillips, mr. Fabina,

Please your attention for my following practical problem.

We are constructing a new (10 and 3 meters) OATS at a different location than
the one we used and which was filed to the FCC as a listed facility.

It was plannned that the new OATS was operational in December 1998(!),
nowever we have a lot of delay due to the bad weather conditions in the Netherlands. It is expected that the new OATS will be operational within 2 or
3 weeks.

We have planned FCC measurements for a customer next week. We are dealing
with a computer monitor, which is considered to be a class B digital device
and should be certified. Our client needs the FCC identifier urgently.

Unfortunately our 'old' and listed OATS is not operational anymore.

Fortunately we have an other OATS available here in Arnhem which is owned by
KTL (Telification)-Arnhem'. They are dealing with the radio- and telecom equirements in the Netherlands and the EU. This OATS is not filed to the CC
nd can only be used for 10 meter measurements.

y proposal: we will perform the OATS measurements at a easurement distance
f 10 meters at the KTL-OATS. I already have the NSA results of this ATS
vailable. I will send the measurement facility description as requisted by he FCC rules (including the NSA results) together with the application eport and forms of the device to the FCC using the normal procedure.

he NSA measurements of our new OATS are scheduled within three eeks. I will
le our new OATS as soon as possible.

hope this proposal is acceptable for the FCC, can you please confirm is?

e measurements are scheduled next Tuesday, I hope you can give me ur
onest response!

Thank you and best regards,

Hermen Jonker

KEMA Registered Quality B.V.
****
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