APPLICATION FOR

TYPE ACCEPTANCE

Sierra Wireless Inc.

FCC ID: N7NACRD2

MODEL: AIRCARD 2

Prepared by:
Sierra Wireless Inc.

#260 - 13151 Vanier Place
Richmond, B.C.
V6V 2J2

Sept 23, 1998

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Letter of Submittal and Compliance

SIERRA WIRELESS
HEART OF THE WIRELESS MACHINE™

Sept 11, 1998

Federal Communications Commission
Authorization and Standards Division
7435 Oakland Mills Rd.
Columbia, M.D. 21046

Gentlemen:

Sierra Wireless Incorporated has tested this transmitter in accordance with the requirements contained in the appropriate Commission Regulations. To the best of my knowledge, these tests were performed using measurement procedures consistent with the Industry or Commission standards and demonstrates that the equipment complies with the published standard. We are unable to warrant against unpublished changes in requirements. The applicable rules are listed in the following test report.

The Open Area Test Site used for these measurements is located at Fluke Park, Mulkilteo, Washington. Site information required by Public Notice 24541 in accordance with ANSI C634-1992 was filed with the FCC Authorization and Evaluation Division Sampling and Measurements Branch in July 1994.

Sincerely

Trent McKeen
RF Engineer

Applicant Introduction

Sierra Wireless, Inc, located in Richmond, B.C., Canada, designs and manufactures wireless data modems for use on Cellular networks. The company was incorporated in May of 1993 around a core engineering staff with special expertise in development of products for use in commercial mobile data systems. The ACE, is a wireless CDPD (cellular digital packet data) data modem.

General Equipment Information

Receiver:

Frequency Range:	869 to 894 Mhz
No. of Channels:	833
Tunable Bands:	1
Designated Reception Mode and Bandwidth:	FM, 30 Khz
Intermediate Frequencies:	45.0 Mhz, 450 Khz
Local Oscillator Frequencies:	914.01 to 938.97 Mhz first LO 44.55 Mhz second LO
Input Impedance:	50 ohms
Output Impedance:	< 1 ohm
Audio Power Output:	0.125 W max.
Crystal Frequencies:	14.85 Mhz

Transmitter:

Frequency Range:	824 to 849 Mhz
No. of Channels:	833
Bandwidth:	30 Khz channel bandwidth
Type of Emission:	Frequency Modulation *
Output Impedance:	50 ohms
Crystal Frequencies:	14.85 Mhz 90 MHz
Power Output:	28 dBm max, variable to 8 dBm

* The transmitter sends computer data using modulation types that vary depending on mode of operation. Two modes are available, analog cellular (or AMPS) and CDPD (Cellular Digital Packet Data).

Description of Operational Modes

CDPD
The modem is only capable of comunicating using CDPD signalling. The modulation used in this case is GMSK at a single data rate of 19.2 Kbps. Deviation in this mode is factory adjusted to 4.8 Khz peak +/- 5%. Test results for all of these modulation types are included in this report.

Expository Statement (2.983)

Logic

A block diagram of the logic section is given below in Figure 1. The logic can be roughly separated into five different subsystems: PCMCIA Interface, FPGA, DSP, Radio Interface, and Battery Interface.

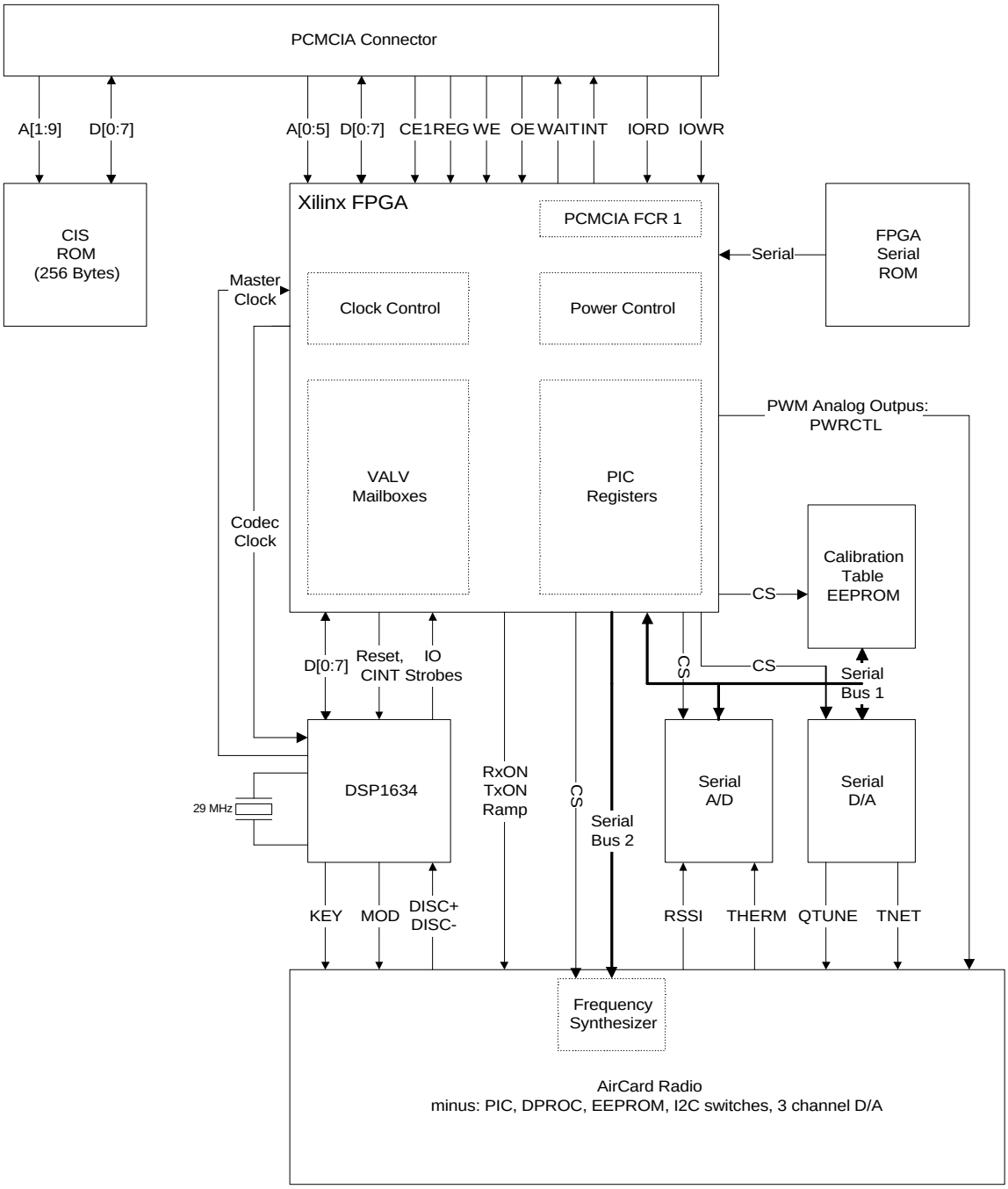


Figure 1: ACE Logic Block Diagram

PCMCIA Interface

The AirCard CE modem board is a PCMCIA IO device. The IO registers used for host communication are located inside the FPGA. The Card Information Structure (CIS) is located in an EEPROM.

68 Pin Connector

The 68 pin PC Card connector is a standard 0.042" offset type. The following signals are supported:

- VCC1 and VCC2: nominally +5.0V is used to power the CIS ROM, FPGA, and optionally the DSP and Radio. This power rail is filtered by ferrite bead L30 and capacitors C9 and C10. The allowable range on this pin is +4.5V up to +5.25V (-10%, +5%).
- GND1 - GND4: connected directly to digital ground and to analog ground through short S1 (inserted only to separate the schematic nets).
- ~CD1 and ~CD2: Card Detect pins connected directly to ground.
- Data[7:0]: bi-directional data bus is connected to the CIS ROM and to the FPGA.
- Address[11:0]: address bus is connected to the CIS ROM and to the FPGA. Within the FPGA, only Address[5:0] are used for IO register mapping (i.e., an IO space of 64 bytes).
- ~CE1 and ~CE2: inputs to the FPGA acting as chip enables.
- ~WE: Write Enable strobe is connected to the FPGA and to the CIS ROM. This signal is required when writing to Attribute Memory (e.g., writing to the CIS or to the Function Configuration Register).
- ~OE: Output Enable strobe is connected to the FPGA and to the CIS ROM. This signal is required when the host reads from Attribute Memory (e.g., reading the CIS on powerup).
- ~REG: selects between Attribute and Common memory: used as an additional chip select to the FPGA.
- ~IREQ: interrupt request output from the FPGA. Can be used to interrupt the host when the DSP reads or writes from/to the FPGA. On startup, when the card is a memory device, this line is RDY/~BSY and is held low by the FPGA (using Q8 and R36) until configuration has completed – the PROM_DONE signal is low during configuration, and is automatically pulled high when the FPGA is loaded and running.
- ~INPACK: input acknowledge output from the FPGA when the card is mapped as an IO device (logical OR of ~CE, ~REG, and ~IORD).
- ~IORD: IO Read strobe is connected to the FPGA and is used to clock out (active low) the contents of the IO register at address[5:0] to the data bus.
- ~IOWR: IO Write strobe is connected to the FPGA and is used to clock in the contents (rising edge) of the data bus to the IO register at address[5:0].
- RESET: Hard reset – used to force a reconfiguration of the FPGA, and subsequent power off of the DSP and radio.
- ~WAIT: Card output pulled high through R1– used to delay a clock cycle, but not required at this time.
- ~IOIS16: Card output pulled high through R2 – used to select between 8 bit (when high) and 16 bit (when low) IO space.
- ~SCHG: Status change card output pulled high through R3 – not used at this time.
- ~SPKR: Speaker output used to (optionally) drive the host's PC speaker. See section 1.1.4 below.

CIS ROM

The data and address busses of the CIS ROM (U2) are connected directly to the PCMCIA connector. This memory holds the Card Information Structure that allows the host to recognize the card immediately after insertion. Currently, the ROM is 2kx8 in size, but only the bottom 256 bytes are actually used: the reason for designing in a larger than necessary memory is because the 2kx8 size is actually less expensive. The

ROM's read and write strobes are connected directly to PCMCIA ~OE. The chip select, however, is gated through the FPGA, for one reason:

1. The Function Configuration Register (FCR) is located at attribute memory location 0x100. The host writes to this register to configure the card as an IO device from its power-on default memory configuration. This location must be located within the FPGA so that the value is not stored over a power reset. By gating the ROM chip select, the FPGA can decode the address and decide whether the host attribute memory access is targeted towards the CIS (and therefore enable the ROM) or the FCR (leave the ROM disabled).

Capacitor C2 is for power supply decoupling.

Power Switch

As stated above, the +5V rail supplied over the PCMCIA connector is used to power the FPGA and CIS ROM. The circuit composed of R10, R35, R48, Q7 and Q10 allows the same voltage rail to supply power to the DSP and radio. By pulling ~PC_5 low, the PNP transistor Q10 is turned on, connecting the +5V net to VBAT. By pulling ~PC_5 high, the switch is turned off. By default (and at powerup) the switch is open (i.e., no current flows through Q10). The PNP pass transistor used is a Zetex FMMT717, a low loss power transistor with a Vce(sat) rating of < 100mV at 1 Amp. The slow down the transistor's turn-on time, C39 was added.

DISC Buffer

To aid development and debugging, it is often necessary to externally monitor the radio discriminator output, DISC. The op-amp U28 brings the DISC signal to the PCMCIA connector (pin 62) where it can be hooked up to an oscilloscope or test set. For an IO device, pin 62 is the digital ~SPKR signal which drives the host PC's speaker (XORed with system SPKR). The SPKR_DISC control line is used to turn the DISC buffer on and off: when low (by default at reset), the circuit formed by Q9, R4, and R41 pulls the ~SPKR line high (effectively shutting off the speaker). R40 is inserted to prevent Q9 from driving back into the output of the op-amp when SPKR_DISC is low.

FPGA

The FPGA (Field Programmable Gate Array) at the heart of the ACE digital design is primarily an interface chip that allows communication between the host and the DSP via the PCMCIA bus. This document focuses on the hardware design of the *circuit*: for a description of the inner workings of the chip, see reference 1 and/or reference 2, the FPGA schematic).

XC-5204

The FPGA is a Xilinx XC-5206 in a 100-VQFP package (U1). The current plan is to replace the FPGA with a custom gate array (~$10 savings) when the design is completely verified and the quantities justify the extra NRE associated with a custom chip. For this document, the term FPGA applies equally to the Xilinx part as well as its eventual replacement.

The host interface (PCMCIA) is made up of the Address and Data busses, as well as the various chip enables and write strobes (~CE1, ~CE2, ~WE, ~OE, ~REG, ~INPACK, ~IORD, and ~IOWR). The CIS ROM chip enable (~CIS_CE) is generated within the FPGA by gating the card enable with the valid CIS address range.

The DSP interface consists of the multiplexed address/data bus (PB[7:0]), read and write strobes (PIDS and PODS), chip selects (I2PSEL2 and PSEL1), and an interrupt line (CINT) designed to let the DSP know when the host has written or read another piece of data. In addition, the FPGA controls the DSP reset line (~DSP_RST), and divides down the DSP master clock (DSP_CLK, nominally 29.4912 MHz) to a codec clock (CODEC_CLK, nominally 4.9152 MHz or 1.8432 MHz depending if the card is operating in CDPD or AMPS mode). The DSP clock is also used internally by the FPGA as a master clock for its serial ports, PWM, and various counters.

Capacitors C3 and C5-8 are for power supply decoupling and are distributed around the various power/ground pins of the device.

Configuration PROM

Because the XC-5204 is an SRAM based FPGA, it loses its configuration whenever power is removed. The Configuration PROM (U4) reloads the FPGA on power up and after a hard reset. The device is a one-time-programmable (OTP) serial ROM chip that can reload the FPGA in less than 100ms. One of the programming lines, ~PROM_INIT, is an open collector output and therefore requires a pull-up resistor, R9. Three additional resistors are necessary during startup: R11-13 are pulldowns on the FPGA Mode pins (M0-2) to force the FPGA to reads its configuration from the serial PROM.
During development, it is often necessary to reprogram the FPGA many times. In this instance, the PROM must be removed (as well as R11-13), and the three configuration signals (PROM_CLK, PROM_DONE, and PROM_DIN) can be connected to a PC serial port through a special 'Xchecker' cable.

Capacitor C4 is for power supply decoupling.

When the Xilinx part is replaced by a custom gate array, the serial PROM is no longer necessary.

Reset Buffer

As stated in section 1.1.1, the PCMCIA RESET signal forces the FPGA to reconfigure itself (i.e., forces a hard reset, as opposed to the soft reset accomplished by writing to the RESET bit of the FPGA). The circuit formed by Q1, R5, R7, R8, and C1 inverts the sense of the RESET signal (active high from PCMCIA, but active low into the FPGA). It also puts in a measure of glitch protection through the RC filter composed of R8 (1k) and C1 (33nF) – the values were chosen for maximum filtering, while still allowing a reset pulse of 10us (PCMCIA spec).

PWM Buffer

The internal PWM driver of the FPGA runs at 100 kHz and outputs a digital signal of varying pulse width. The circuit formed by Q3, R22, R28, R33, and C28 perform 2 functions. First, it references full scale to a known analog voltage (VDDA) rather than the unknown PCMCIA digital voltage (which may be anywhere from 4.5V to 5.25V). Second, it transforms the digital waveform to a DC level. Because the PWM buffer has a high output impedance, op-amp U28B in the non-inverting unity gain configuration is inserted to ensure an even higher impedance load.

LED Driver

D9 and R27 form a simple LED driver. The FPGA can sink up to 8mA, which should result in a bright enough light. If 8mA is not enough, the custom gate array can be designed to sink an extra amount of current through that pin.

DSP

The third major component of the ACE digital design is the DSP. This subsystem is composed primarily of a single IC, along with some analog support circuitry. The data pump design is similar to other products (e.g., AirCard or MP200), with the one major difference that the FPGA replaces the VALV Interface ASIC that is used in all the other products. The FPGA is not a complete replacement (does not allow V34 operation), but does emulate enough of the VALV functions to allow CDPD operation.

DSP16345-AC

The DSP IC is a Lucent DSP16345, with built-in V34 ROM code (AC version of the ROM) and a small amount of built-in RAM. The DSP communicates with the FPGA through a bi-directional address/data bus labeled PB[7:0]. The DSP is the bus master in all transactions (controls the read and write strobes as well as the chip enables), but the FPGA has the ability to reset and interrupt the DSP. See also section 1.2.1.

Resistors R14-18 are pull-ups/pulldowns necessary to configure the DSP properly at startup. R57 is inserted to workaround a known bug in the chip – several rising edges must appear at this pin before the DSP is taken out of reset to allow the internal JTAG port to reset properly. Capacitors C19-24 (0.33uF) are required for analog biasing within the DSP. Resistors R38-39 and R43-44 are used to tie down the inputs of the DSP's internal op amps.

Capacitors C13-15 are for digital power supply decoupling.

29.4912MHz Crystal

The DSP master clock is generated by a 29.4912MHz crystal (X1) using a clock buffer internal to the DSP. Capacitors C11 and C12 supply the requisite load capacitance.

+5V Analog Regulator

A +4.5V linear regulator (U9) is used to generate the analog voltage supply. C33 and C30 act as input and output capacitors, respectively, while C34 is a noise decoupler. The input voltage is +5V. The analog supply is used by the DSP for its codec and op-amp operations as well as by the FPGA for its PWM reference and the serial A/D and D/A for their reference voltages.

Before feeding to the DSP, the analog supply is RC filtered through R20, C16 and C18.

Radio Interface

The radio interface is a collection of otherwise unrelated circuits that allow the host to control and monitor the radio transceiver.

Serial A/D

Four analog levels within the radio card must be monitored by the host: Received Signal Strength Indicator (RSSI), internal temperature (THERM), the +5V socket voltage, and the battery cell voltage. This is accomplished by a 2-channel, serial, 8-bit A/D converter, U7. This IC is programmed and polled by the host through the FPGA. Full-scale is equal to the VCC supply pin (the analog voltage supply rail). For detailed programming information, consult reference 1.

RSSI originates within the radio and is connected directly to channel 1. Thermistor readings are directly coupled to channel 0.

Capacitor C26 provides power supply rail filtering.

Serial D/A

Three analog levels are needed by the radio transceiver for proper calibration and tuning. One of these levels, PWR_CTL, is provided by the FPGA PWM output. The other two, QTUNE and TNET, are provided by a 2-channel, serial, 8-bit D/A. Again, full scale is the analog supply rail, and the converter is programmed by the host through the FPGA. For detailed programming information, consult reference 1.

Capacitor C25 provides power supply rail filtering.

Voltage Inverter

A single chip voltage inverter, U10, produces a -5V bias from the radio/DSP digital supply rail, VBAT. Three switching capacitors are needed: C35-37 are all 10uF ceramics. Note that no shutdown circuit exists for this switcher – whenever voltage is applied to the DSP and radio, this chip will be on. Because switching IC's generate a great deal of noise, a filter comprised of L29 and C32 is inserted before the negative bias is fed to the radio.

Calibration EEPROM

The radio calibration parameters are stored in a serial EEPROM, U8. This IC communicates with the FPGA using the same serial port as the D/A and the A/D. The memory size is 512 bytes, of which half is occupied by the radio calibration table, and half is taken by various CDPD data (e.g., NEI's and network authentication information).

Capacitor C17 provides power supply rail filtering.

Feed-thru Capacitors

The digital and radio portions of the radio card are separated by a metal shield. All signals passing through this interface are filtered using feed-thru capacitors. C48-50 each filter six signals, while C51 filters the higher current supply rail and C53 filters the ground. Resistors R45-47 prevent current leakage from the FPGA to the radio synthesizer through the second serial port.

Battery Interface

The usual power source for the ACE card is an external battery pack. The connection is an 8-pin 'connector' which on the PC Card side is simply exposed traces at one end which fit into an 8 position FPC connector on the battery pack.

8 Pin Connector

The following signals appear at the 8 pin battery connector:

- VBAT (2 traces to accommodate up to 1 Amp): Zener diode D1 provides some overvoltage and transient protection.
- Ground (2 traces to accommodate up to 1 Amp)
- CHGR_ON (battery input): when high, allows the battery to be recharged by the PCMCIA socket. If the external adapter is plugged in, this pin toggles between slow and fast charge (the battery always charges if the external adapter is present). Zener diode D3 provides some overvoltage and transient protection.
- BATT_ON (battery input): when high, allows the battery to discharge into the radio card, providing a stable +5.0V rail on VBAT. When low, the battery is disconnected and leakage current is < 100uA. Zener diode D5 provides some overvoltage and transient protection.
- ADAPTER (battery output): indicates the presence of the external DC adapter when high. Zener diode D2 provides some overvoltage and transient protection.
- RAW_BATT (battery output): the raw lithium cell battery voltage which can be monitored by the host to determine approximate cell charge and warn against low battery conditions. Zener diode D6 provides some overvoltage and transient protection. This analog level is monitored by the serial A/D (see section 1.5.2 below).

Aircard CE Radio

RF Circuit, Cellular Transceiver

The transceiver is a narrow band FM Full duplex transceiver designed for operation in the AMPS (Advanced Mobile Phone System) frequency range of 824 MHz to 894 MHz. Channel spacing is 30 KHz and frequency generation for the transmitter and receiver is synthesized using conventional Phased Locked Loop technology. Transmitter output power is 600 mW (max) with a duty cycle of 100%. The transceiver is only suitable for CDPD packet operation with extremely fast transmitter on/ off times.

Specifications

Aircard CE will comply with the requirements of CDPD 1.1 as detailed in section 409 of the CDPD specification.

General

Table 1: Power Supply

DC Power Supply	5V +/- 5% in series with a source impedance of 0.5 ohms (minimum of 4.6V under load)

Table 2: Aircard CE Power Consumption on 5V supply

		Power Source	
		Battery	HPC Socket
CDPD	Sleep	< .1 mA	< 5mA
	Receive	80 mA	30 mA
	Transmit	600 mA	30 mA

2.2 Specifications Cont…

Table 3: Transceiver Specifications

Transmit Frequency	824 to 848 MHz
Receive Frequency	869 to 893 MHz
Channel Spacing	30 KHz
Modes	Receive, Full Duplex Transmit
Modulation	Direct FM, max deviation +/- 14 KHz
Performance Bandwidth	25 MHz
Frequency Stability	+/- 2.5 ppm
Transmitter	
Transmit Output Power (conducted)	600 mW (28 dBm), adjustable to 8 dBm @ 4.6VDC, +2/ -4 dB from set points of 8, 12, 16, 20 , 24 and 28 dBm
Transmitter Spurious Outputs	Per FCC Part 22
Tx Ramp Up/ Down	Per CDPD 1.1
Receiver	
Sensitivity (conducted) CDPD Voice	 -111 dBm for 5% BLER -117 dBm for 12 dB SINAD (C message weighted)
Adjacent Channel Selectivity CDPD Method AMPS Method	 16 dB @ +/- 30 KHz 60 dB @ +/- 60 KHz
Intermodulation Distortion CDPD Method AMPS Method	 57 dB @ +/- 120/240 KHz 65 dB @ +/- 12-/240 KHz
Rx Channel scan time	60 mSec. Band edge to band edge
Spurious Emissions	Per FCC Part 15

Table 4: Environmental Specifications

The product must, as a minimum, meet all PCMCIA specifications (release 2.01, section 3.6) except for operating temperatures as shown below:

Operation Temperature	-20 to +65 deg. C
Humidity	95% non-condensing
Vibration	Per PCMCIA spec 15G peak, 10-2000 Hz (non-operating)
ESD	Per PCMCIA spec
Shock	Per PCMCIA spec
Drop	30 in. onto non-cushioning vinyl covered concrete

Physical Specifications

Aircard CE will be a type II PCMCIA card with minimal (<15mm) or no extension other than the antenna.

Antenna Specifications

The antenna is a removable flip-up telescopic antenna that is capable of withstanding a drop onto vinyl from 30 inches (per PCMCIA spec) while in any extended position without damage (while out of slot). The antenna, when not in use, will fold down or rotate. The RF output of the Aircard CE will have a 50 ohm coaxial connection to support remotely mounted antennas and test connections.

The gain of the antenna will be in the range of –2 to –4 dBd.

Architecture

A block diagram of the radio section is given below in Figure 2. The Aircard CE wireless modem consists of two main sections, i.e. the Control Logic Circuits and the Radio Transceiver Circuits. The Field Programmable Gate Array (FPGA) in the logic section controls all functions in the transceiver. It is responsible for programming the synthesizer, RF power selection, enabling and disabling the transmitter and receiver sections, and performing electronically tuned adjustment.

The transceiver uses a single synthesizer for both the transmitter and receiver. The operation of the synthesizer is described in section 2.4, Frequency Generation Unit. The synthesizer produces a frequency that is 45 MHz above the desired receive frequency (our Rx first LO), and 90 MHz above the desired transmit frequency (our Tx LO to the upconverter). The transmitter and receiver are described in more detail in the appropriate sections.

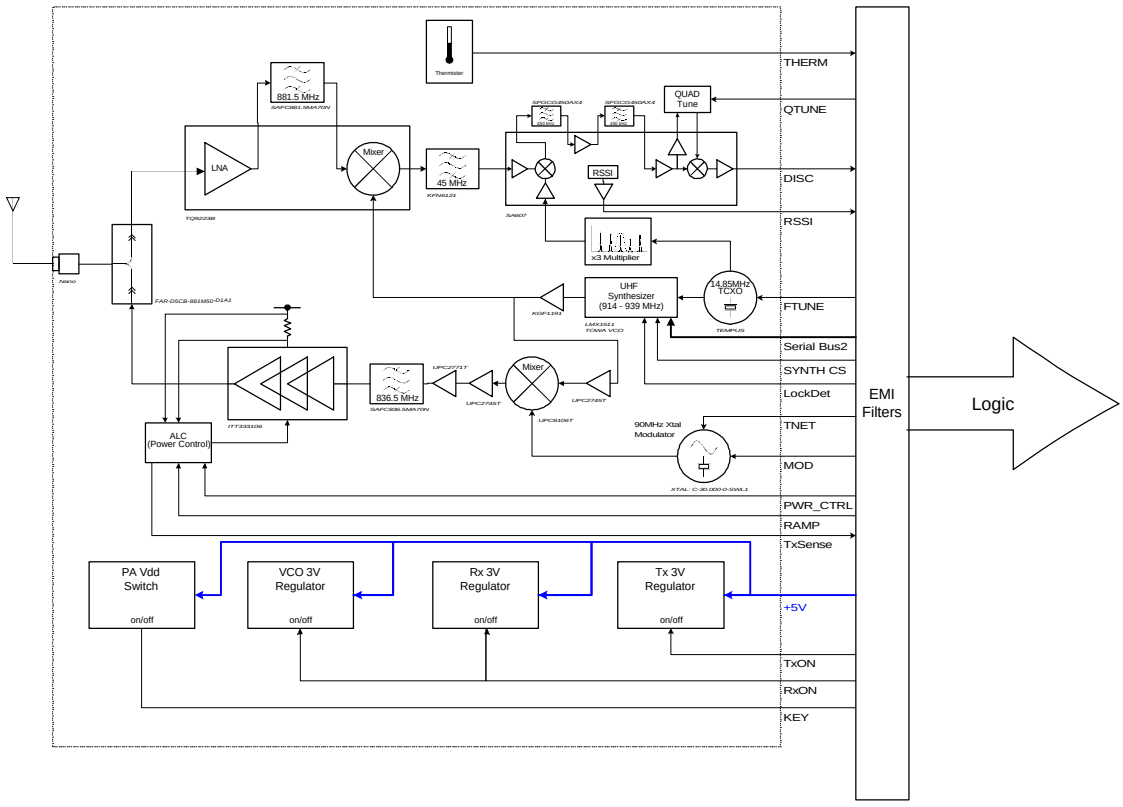


Figure 2. Radio Block Diagram

Frequency Generation Unit

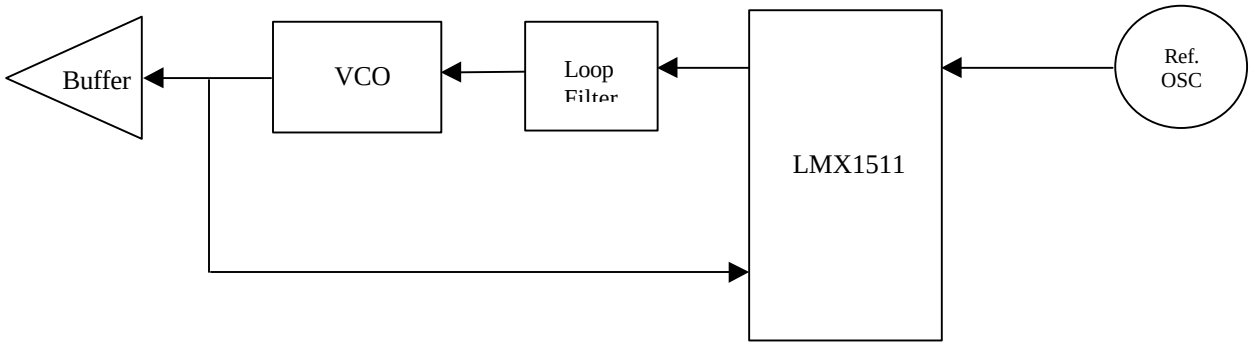
The frequency generation unit (FGU) generates the local oscillator signals for the receiver and the transmitter. It consists of a phased locked loop system that produces a synthesized signal in the frequency range of 914 to 939 MHz. The desired frequency is programmed by the FPGA.

This LO signal is routed to the transmitter where it is downconverted by mixing with a 90 MHz modulated signal to produce our transmit carrier frequency. It is also routed to the receiver mixer where it downconverts receive signals into the first IF of 45 MHz. The FGU also supplies a reference frequency of 14.85 MHz to the receiver's FM subsystem where it is tripled providing our second LO.

FGU Description and Block Diagram

The FGU uses a 1.1 GHz frequency synthesizer integrated circuit, LMX1511 to provide us with our desired frequencies. The Phase Locked Loop circuitry consists of a 14.85 MHz reference oscillator, a LMX1511 frequency synthesizer IC, loop filters a voltage controlled oscillator (VCO), and a buffer amplifier. A block diagram of the Frequency Generation Unit is illustrated below in figure 3.

Figure 3: FGU Block Diagram.



14.85 MHz Reference Oscillator

The Reference Oscillator produces a 14.85 MHz output sine wave signal. It has digital temperature compensation that provides frequency stability of +/- 1.5 ppm over the temperature range of 0 deg. C. to +60 deg. C. Total frequency stability over temperature, voltage and load variation is +/1 2 ppm. The reference oscillator feeds both the LMX1511 synthesizer chip and to the receiver's IF subsystem via a frequency trippler.

LMX1511 PLL

The output of the reference oscillator is directed to the LMX1511, frequency synthesizer chip. This chip includes the components necessary to build a phase lock loop system. Features include dual modulus prescalers which can select either 64/65 or a 128/129 divide ratio at input frequencies of up to 1.1 GHz. Using a proprietary digital phase locked loop technique, the LMX1511's linear phase detector characteristics can generate very stable, low noise local oscillator signals.

Loop Filter

The output of the phase detector in the LMX1511 is fed into the loop filter. The loop filter controls the loop dynamics of the phase locked loop system, i.e. how fast the loop locks and its transient response also helps to suppress the phase detector frequency pulses from modulating the VCO.

Voltage Controlled Oscillator

The output of the loop filter is connected to the Voltage Controlled Oscillator (VCO). This DC voltage controls the output frequency of the VCO in a fashion that always maintains a locked condition.

Buffer Amplifier

The output of the VCO is amplified by a buffer amplifier to increase its output level and providing isolation to the VCO. This amplified output is then routed to the receiver and transmitter sections where it serves as the local oscillator for downconversions and upconversions respectively.

Transmitter

The transmitter produces an output frequency in the range of 824 to 849 MHz, with channel assignments as per the AMPS frequency allocation specifications. The transmitter consists of a 90MHz modulator, an upconverter, buffer preamplifiers, power amplifier, automatic level control circuit, and a duplexer. The output of the FGU is mixed with the output of the modulator to produce our desired transmit carrier. It is further processed by filtering and amplification before being applied to the duplexer and then to the antenna.

90 MHz Modulator

The modulator consists of a voltage controlled, 30 MHz crystal oscillator/ trippler. Baseband data signals serve as the data source for the transmitter. Baseband processing is described in the appropriate section(s). The 90 MHz component of the oscillator/ trippler, bandpass filtered to attenuate adjacent upper and lower sidebands, is then connected to the upconverting stage.

Tx Upconverter

The 90 MHz modulated RF signal is then upconverted to the desired transmit frequency in the transmitter upconverter stage. The transmit signal is produced by mixing the 90 MHz signal with the output of the FGU, which serves as our local oscillator.

PA Preamplifiers and Filters

The signal from the output of the mixer undergoes amplification (to provide adequate drive level, then filtering (to remove any undesired mixed products) before being applied to the power amplifier.

Power Amplifier

The PA amplifies the transmit signal to produce 1.2W of RF power before being applied to the duplexer. RF output level is controlled by the field programmable gate array (FPGA).

Automatic level control and Tx Key

RF power is controlled by adjusting the negative supply voltage to the –Vgg pin of the PA. The FPGA supplies a positive analog voltage which is fed to a difference amplifier, the resultant –ve DC level output from the amplifier is used as our control signal to the PA. The negative rail of the difference amplifier is produce via a switching regulator operating at approximately 100 KHz. Automatic level control functions by monitoring the supply current to the PA and thereby adjusting –Vgg to sustain this current.

The FPGA controls the key function of our transmitter.

Duplexer

The RF output of the PA is fed to the duplexer, which combines the transmitter and receiver sections to use one antenna port. The duplexer also provides additional bandpass filtering for the transmitter and receiver.

Receiver

The receiver is a dual conversion super heterodyne type, with a first IF of 45 MHz and a second IF of 450 KHz. Receive signals coupled into the antenna passes through the duplexer to a SAW bandpass filter, then to the LNA. The output of the LNA is filtered by an additional SAW bandpass filter and then fed to the first mixer.

The receive signal is downconverted to the first IF of 45 MHz in the first mixer. The local oscillator for this mixer is provided by the FGU. The downconverted signal is bandpass filtered by a 45 MHz crystal filter and then fed into the IF subsystem IC. This IC first mixes our 45 MHz IF signal with a second LO of 44.55 MHz (generated by tripling the 14.85 MHz FGU reference signal) giving us our second IF of 450 KHz. This signal further undergoes a series of amplifiers and limiters before being applied to the quadrature detector (tuning is achieved via a DC level applied to our detector provided by the FPGA). The end result, a demodulated baseband signal and RSSI (Receiver Signal Strength Indicator) information to our DSP.

Baseband Audio Processing –Transmitter and Receiver

Baseband data signals to the radio are buffered, amplified and level shifted before being applied to the transmit modulator.
Transversely, a demodulated receive signal is fed to the digital signal processor for decoding.

Tuning Functions

All tuning functions in the transceiver are performed electronically. The tuning voltages are controlled by the field programmable gate array and an on-board digital-to-analog converter. The radio's tuning functions are described below.

QTUNE

QTUNE provides tuning of the receiver's quadrature detector for our baseband signal.

MOD

Centering of the transmitter's 90 MHz modulator is achieved by adjusting its DC bias (via the FPGA, MOD) to the crystal.

TNET

TNET provides netting of the frequency generation unit.

PWRCTL

PWRCTL controls the RF power at the output of the device.

Power Supply

The ACE radio draws its power from the host computer through the PCMCIA interface.

VBAT, +5.0Vdc is filtered directly out of the PCMCIA connector and then used to supply power to the transmitter and receiver. VBAT is further regulated down to +3.0Vdc using three separate integrated circuit regulators to provide RX3V, VCO3V, and TX3V, which in turn powers the receiver, FGU, and part of the transmitter respectively. Each regulator has its own individual control pin so it can be turned on and off independently.

Battery

A block diagram of the battery pack is given below in Figure 4. The battery can be roughly separated into three different subsystems: charger, 5V DC-DC converter, and the lithium cell itself.

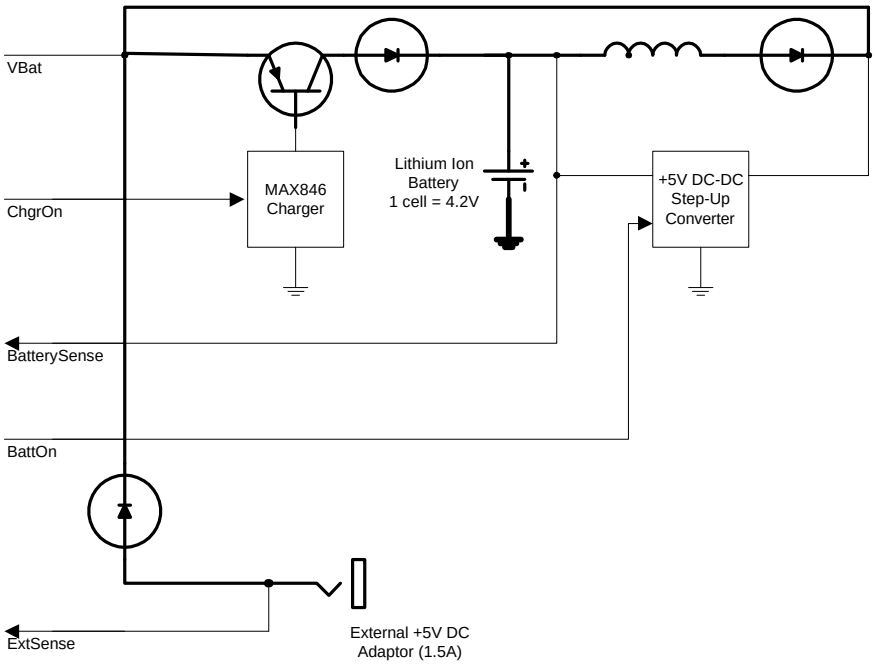


Figure 4. Aircard Battery Pack Block Diagram

Charger

The charging circuit regulates the voltage and current going to the battery cell. A lithium ion cell must be charged very carefully, and a dedicated IC is used to perform this function. The MAX846, U1, implements the lithium-ion charging algorithm. The primary current path is through power PNP transistor, Q2 -- the IC controls the base voltage/current and therefore controls the voltage/current going to the cell. Schottky diode, D1, prevents leakage from the cell back into the charging IC.

The charge current can come from one of two sources:

- from the PCMCIA socket through the 8 pin connector J3.
- from an external DC adapter plugged into J2. The DC adapter must be rated at +5.0V, +/- 5% and be capable of sourcing 1.5 Amps.

The charger is turned on when the 'CHGR_ON' net goes high. This happens when the host activates the 'HST_CHGR_ON' signal on pin 1 of J3 (through D3), or when the external 5V DC adapter is plugged in (through D5).

If an external DC adapter is plugged in, the battery will automatically charge without any control necessary from the host. Additionally, current will be supplied from the adapter to the card through the 8 pin connector J3. For this reason, some signal conditioning is necessary. Ferrite beads FB1-2 and

capacitors C12-13 provide some filtering. A schottky diode, D2, protects against reverse bias. An alternate circuit comprised of Q3, Q7, R26, and R27 can be used in place of the diode, but is currently not populated (the transistor circuit results in less voltage drop, but is more expensive).

When the cell is below ~75% full, it must be charged at a constant current. For ACE, this current is either 600mA (when an external DC adapter is plugged and the modem is otherwise off) or 200mA (when charging from the socket or when an external DC adapter is plugged in and the modem is on). The selection between 200mA and 600mA is accomplished by transistors Q5 and Q6. When both are on (i.e., when the adapter is plugged in *and* the CHGR_ON control signal is high) a 10k resistor, R29, is switched in parallel with the 20k resistor, R3 -- this resistance (between the ISET pin of U1 and ground) sets the charging current. The current is sensed through parallel resistors R1 and R24.

As the cell is charged, its terminal voltage increases. When the cell voltage reaches 4.2V, the MAX846 IC stops charging at a constant current and begins charging at a constant voltage. The voltage threshold is set internally, and is accurate to within +/- 1%.

When the charger is on (regardless of whether in fast or slow charge, or whether the battery is empty or full), the LED D4 will be turned on through the transistor switch composed of Q4, R11, and R12.

5V DC-DC Converter

In order to provide a regulated +5.0V output, the raw battery voltage must be 'switched' up from a nominal 3.6V to 5.0V. A switching IC, U5, is used. This IC has a built in power FET, and therefore only requires an inductor, L1, a diode, D6, and input and output capacitors, C20 and C21-22, to 'pump' up the voltage to +5.0V. Typical efficiency is 85%, up to 90% at certain load levels. The output voltage is set by the resistor combination of R15-18.

Because there is the possibility of leakage from the cell through the diode, D6, a shutdown transistor circuit was added. This circuit reduces the off-state leakage of the cell to below 100uA. When the DC-DC converter is switched off (the 'BATT_ON' net is driven low), the PNP transistor Q1 is also shut off by the transistor switch circuit made up by Q6, R7, R8, R10, and R25.

Resistors R19-23 are all used to configure the switching IC, and C17 and C18 are used as reference capacitors.

Lithium Cell

The actual battery cell is rechargeable lithium-ion with a nominal capacity of 900 mA-hours. Typical cell voltage is 3.6V: maximum is 4.2V (e.g., when charging), and minimum (when empty) is 3.0V – responsibility for detecting when the cell is near empty and shutting off the power lies with the host software.

Currently, the type of lithium cell used is a lithium-manganese (made by Moli Energy). This type of chemistry is safer than most other types of cells and requires minimum protection circuitry. A thermal fuse and PTC is included within the cell, and is all the protection required.

An alternate chemistry is lithium-cobalt (made by a variety of possible second source manufacturers). Lithium-cobalt typically gives increased capacity for a given volume, but requires more protection circuitry. Usually, manufacturers require that the cell be fitted with a small PCB containing additional protection – this PCB is generally attached to the cell and included by the cell manufacturers.

The battery connects to the charger PCB through J1 – this 'connector' will ultimately be a simple solder connection from the battery leads to the PCB, but for the initial production run (i.e., Pilot) a keyed connector may be used to prevent the cell from being connected in reverse bias.

Calculation of Necessary Bandwidth for FCC ID: N7NACRD2

For CDPD 19.2Kbps Transmission (emission type FXW)

The data rate is 19200 bits per second.

Necessary Bandwidth = 2M + 2DK

M = 10 kHz
D = 4.8 kHz
K = 1.2

So necessary bandwidth = $2 \times 10 + 2 \times 4.8 \times 1.2 = 31.5$ kHz

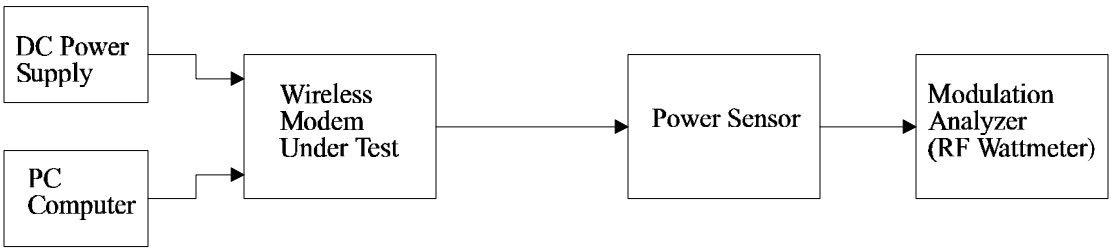
Performance Test Data

RF Output Power (2.985)

Name of Test:	RF Power Output
FCC ID:	N7NACRD2
Grantee:	Sierra Wireless
Serial No.:	CE000221
Manufacturing Rating:	0.00631 to 0.631 Watt +8dBm to +28dBm in 4 dB steps (Controlled by Cell Base Station)
Equipment Authorization Procedure:	Para. 2.985(a)
Test Equipment:	HP8901A Modulation Analyzer HP8481H Power Sensor Astron VS20M DC power supply Zegna 486 PC Computer
Duty Cycle:	Portable (intermittent)

Block Diagram of Test Set-up

The computer is used to select the channel and key the transmitter.



Final Radio Frequency Amplifying Device

MC5951 NEC PA Module

	LOW POWER	**HIGH POWER**
Drain Current, (I_C) =	50 mA	365 mA
Drain Voltage, (V_C)=	5.0 V	5.0 V
Total Transmitter Load	70 mA	395 mA
DC Input Voltage	5.0 V	5.0 V
Power Input = (I_C)(V_C) = P_{in} =	0.35 W	1.98 W
Measured Power Output = P_{out} =	7.95 dBm	27.66 dBm
Rated Power Output	8.0 dBm	28.0 dBm

Modulation Characteristics (2.987)

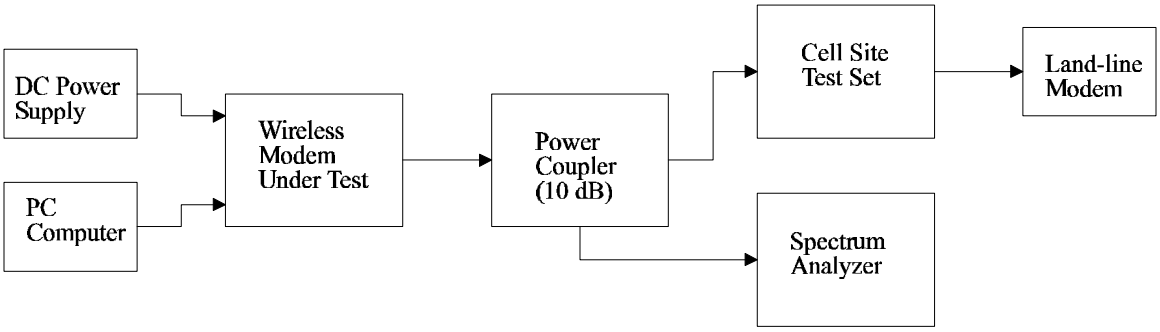
Name of Test:	Modulation Characteristics
FCC ID:	N7NACRD2
Grantee:	Sierra Wireless
Serial No.:	CE000221
Minimum Standard Specified	Para. 22.907 (a)
Test Results	N/A
Equipment Authorization Procedure	Para 2.987 (a) and (b)
Test Equipment:	HP8921A Cell Site Test Set HP35665A Dynamic Signal Analyser Astron VS20M DC power supply Zegna 486 PC Computer

Note: These tests are not applicable as the device is not capable of voice transmission.

Occupied Bandwidth (2.989)

Name of Test:	Occupied Bandwidth
FCC ID:	N7NACRD2
Grantee:	Sierra Wireless
Serial No.:	CE000221
Minimum Standard Specified	Para. 22.907 (b) and (d)
Test Results	Equipment is Compliant with Standard
Equipment Authorization Procedure	Para 2.989 (c)(1)
Test Equipment:	HP8594E Spectrum Analyzer HP8921A Cell Site Test Set Astron VS20M DC Power Supply Zegna 486 PC Computer Mini-Circuits splitter, model ZA3PD-1.5 Land-line modem: shop built (unit # 1) RF attenuators, model PE7016-30, and CAT-3

Test Setup Block Diagram



Measurement Data

Spectrum Analyzer: Hewlett Packard 8594E

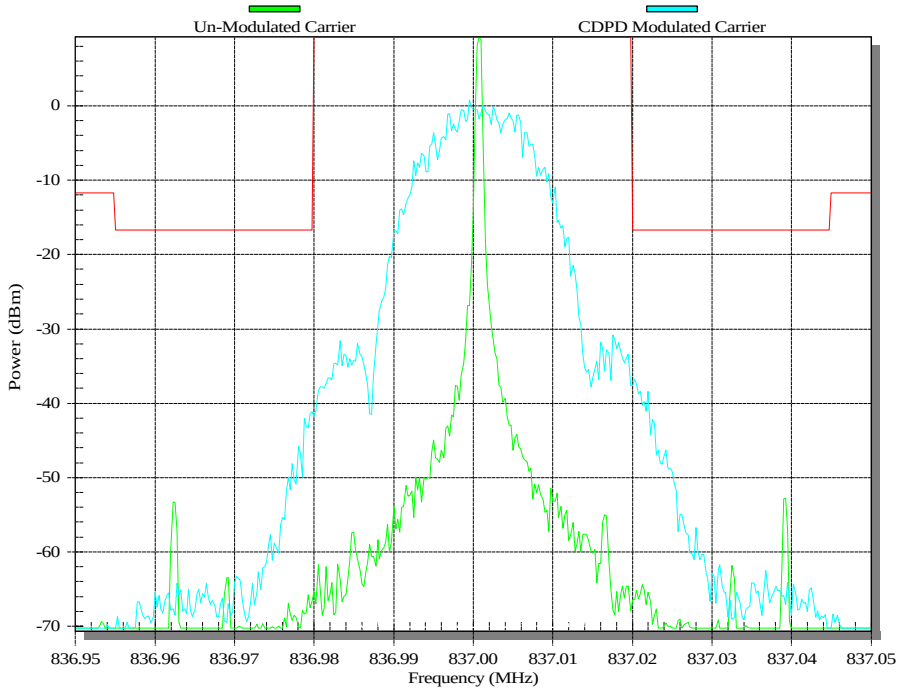
Settings:

Resolution Bandwidth	300 Hz
Video Filter	300 Hz
Scan Time	3.33 sec
Scan Width	100 kHz
Center Frequency	836.43 MHz

Data Or Signaling Type	**Tx Deviation**	**Emission Designator**
1) CDPD, Cellular Digital Packet Data (19.2 kbaud)	4.8 kHz	31K5FXW

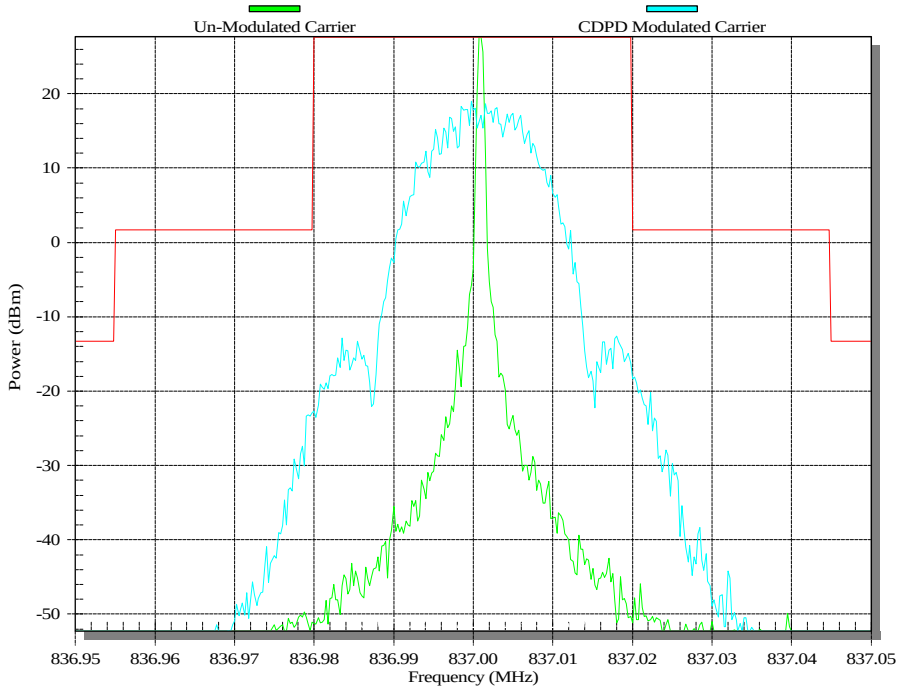
CDPD (FXW) Occupied Spectrum - 2.989

09/29/98 CE000221 19.2kbps, 4.8kHz Deviation, 8dBm Output Power



CDPD (FXW) Occupied Spectrum - 2.989

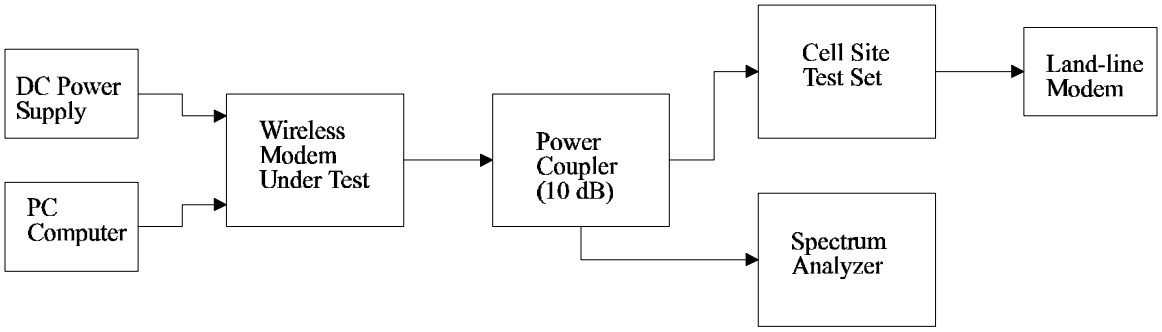
09/29/98 CE000221 19.2kbps, 4.8kHz Deviation, 28dBm Output Power



Spurious Emissions at Antenna Terminals (2.991)

Name of Test:	Spurious Emissions at Antenna Terminals
FCC ID:	N7NACRD2
Grantee:	Sierra Wireless
Serial No.:	CE000221
Minimum Standard Specified	Para. 22.106
Test Results	Equipment Compliant with Standard
Equipment Authorization Procedure	Para. 2.993
Frequency Range Observed	0 to 9 GHz
Operating Frequency	837.000 MHz
Crystal Frequency	14.85 MHz TCXO
Power Output	0.00631 to 4.0 Watt (8 to 36 dBm) in 4 dB steps
Spurious Limit = 43dB + 10Log$_{10}$ (P_O) =	-21 to -41 dBm

Test Setup Block Diagram



Measurement Data

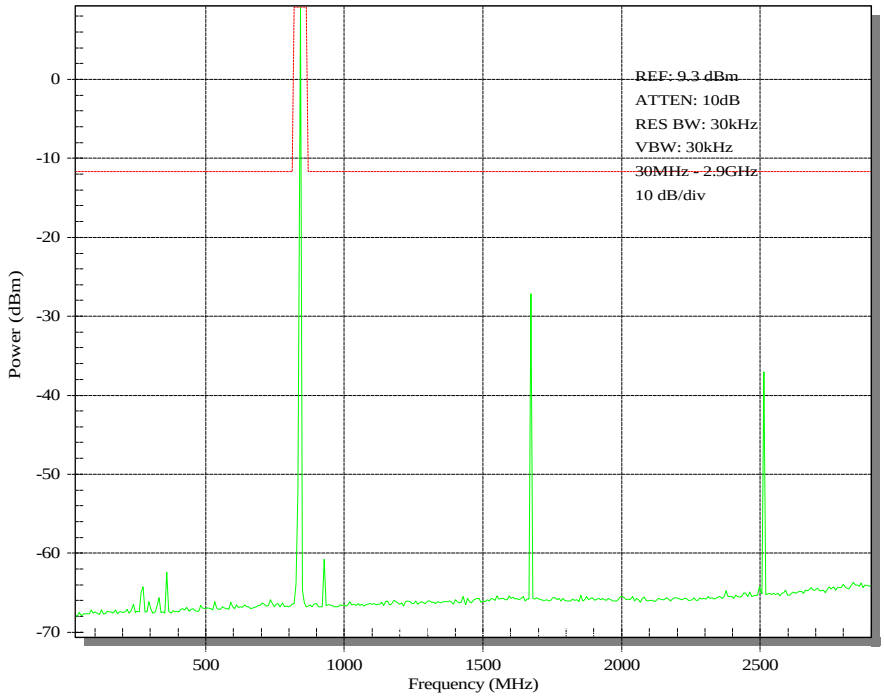
Formula	Frequency (MHz)	Level (dB below carrier)	
		Low Power	High Power
f_o	837.0	- 0 -	- 0 -
$2f_o$	1647.0	-36 dB	-44 dB
$3f_o$	2511.0	-46 dB	-62 dB
$4f_o$	3348.0	-	-57 dB
$7f_o$	5859.0	-	-60 dB
$8f_o$	6696.0	-	-58 dB

Note: All other emissions were greater than 20dB below the spurious limit. Plots of the spurs reported in the table can be seen on the following 2 pages.

Low Power (8dBm Nominal)

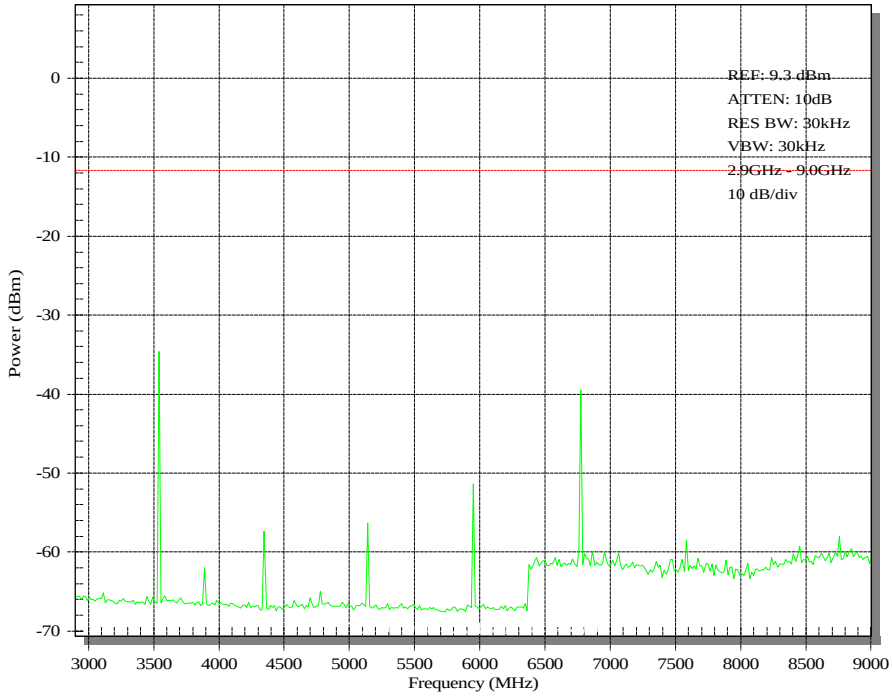
Spurious Emissions at Antenna Terminals - 2.991

09/29/98 CE000221 19.2kbps, 4.8kHz Deviation, 8dBm Output Power



Spurious Emissions at Antenna Terminals - 2.991

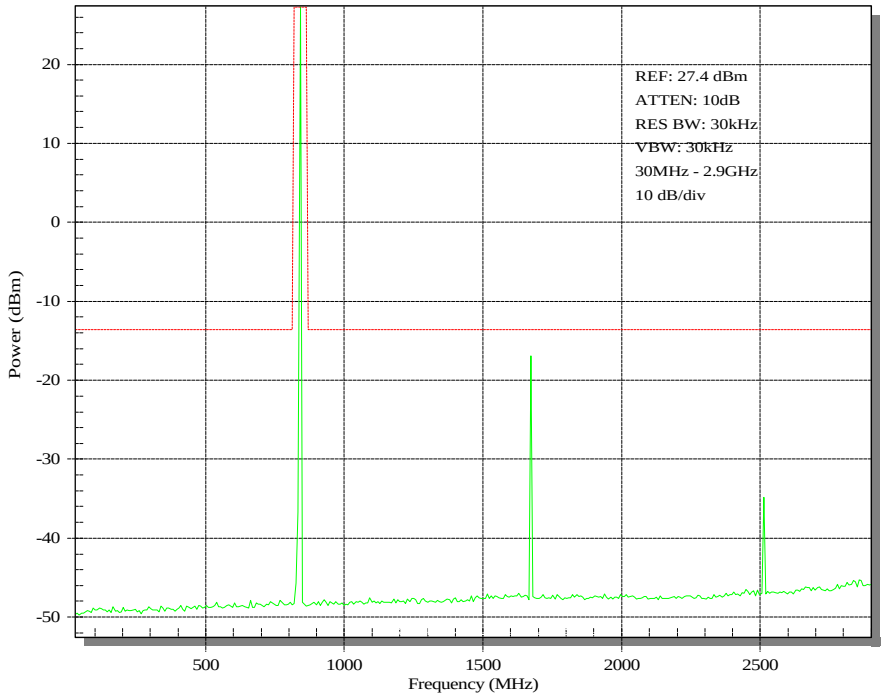
09/29/98 CE000221 19.2kbps, 4.8kHz Deviation, 8dBm Output Power



High Power (28dBm Nominal)

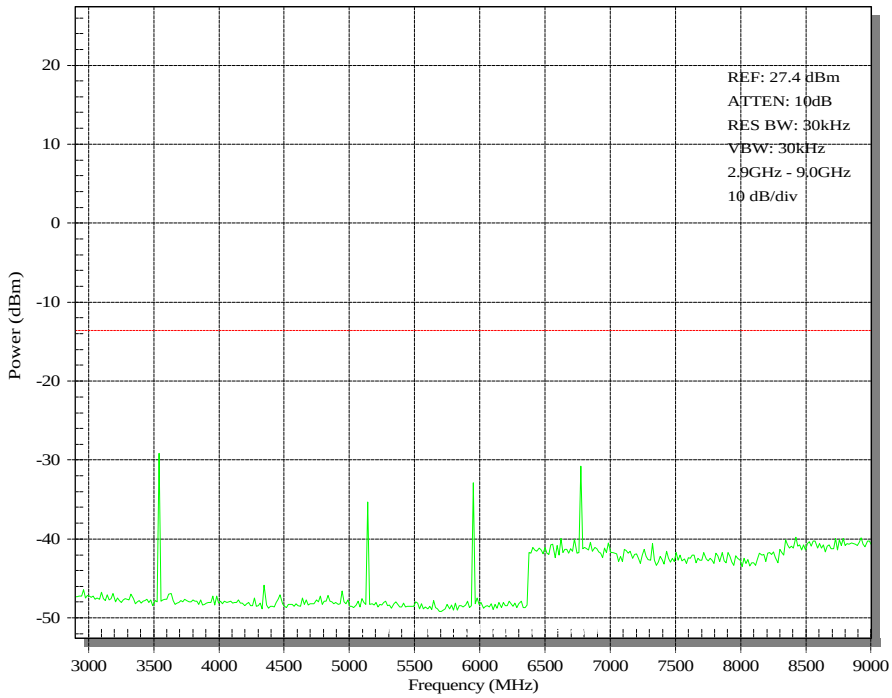
Spurious Emissions at Antenna Terminals - 2.991

09/29/98 CE000221 19.2kbps, 4.8kHz Deviation, 28dBm Output Power



Spurious Emissions at Antenna Terminals - 2.991

09/29/98 CE000221 19.2kbps, 4.8kHz Deviation, 28dBm Output Power



Field Intensity Measurements of Spurious Radiation (2.993)

Name of Test:	Field Intensity Measurements of Spurious Radiation
FCC ID:	N7NACRD2
Grantee:	Sierra Wireless
Serial No.:	CE000221
Minimum Standard Specified	Para. 22.106
Test Results	Equipment is Compliant with Standard
Equipment Authorization Procedure	Para. 2.993
Frequency Range Observed	0 MHz to 9 GHz
Spurious Limit = 43dB + 10Log$_{10}$ P$_O$=	-21 to -49 dB

Note: This test was performed at:
Spectrum Technologies Inc.
209 Dayton St., Suite 205
Edmonds, WA 98020

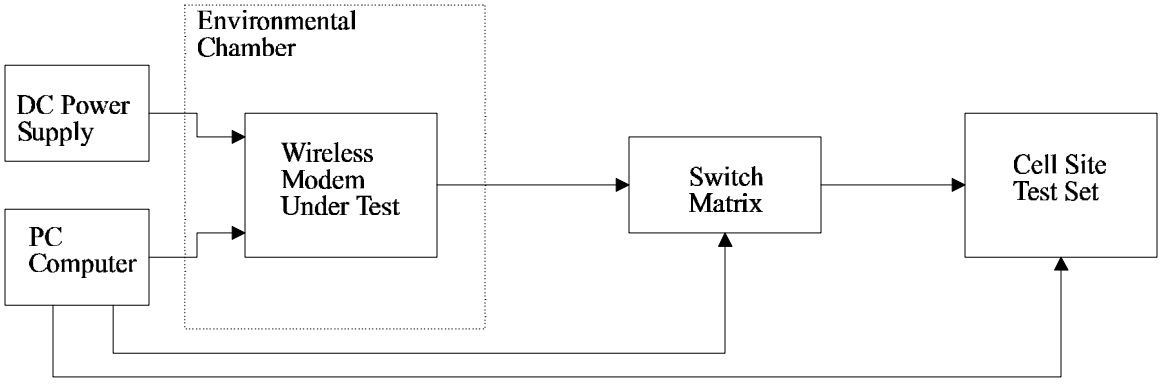
Operation Stability Performance (2.995)

Name of Test:	Operational Stability Performance
FCC ID:	N7NACRD2
Grantee:	Sierra Wireless
Serial No.:	CE000221
Minimum Standard Specified	Para. 22.101 (a)
Equipment Authorization Procedure	Para. 2.995
Test Results	Equipment is Compliant with Standard
Test Equipment	HP8921A Cell Site Test Set Tenney Jr environmental chamber Astron VS20M DC power supply Zegna 486 PC Computer
Standard Test Frequency	837.0 MHz

Notes : Tolerance =+/- 2091 Hz or 2.5 ppm

Block Diagram of Test Set-up

Measurements were performed using an automated test facility which includes a switch matrix to route transmitter power to the test set. Path loss is accounted for automatically in our test software.



EUT set up in test chamber with temperature probe located adjacent to EUT in chamber center to observe ambient.

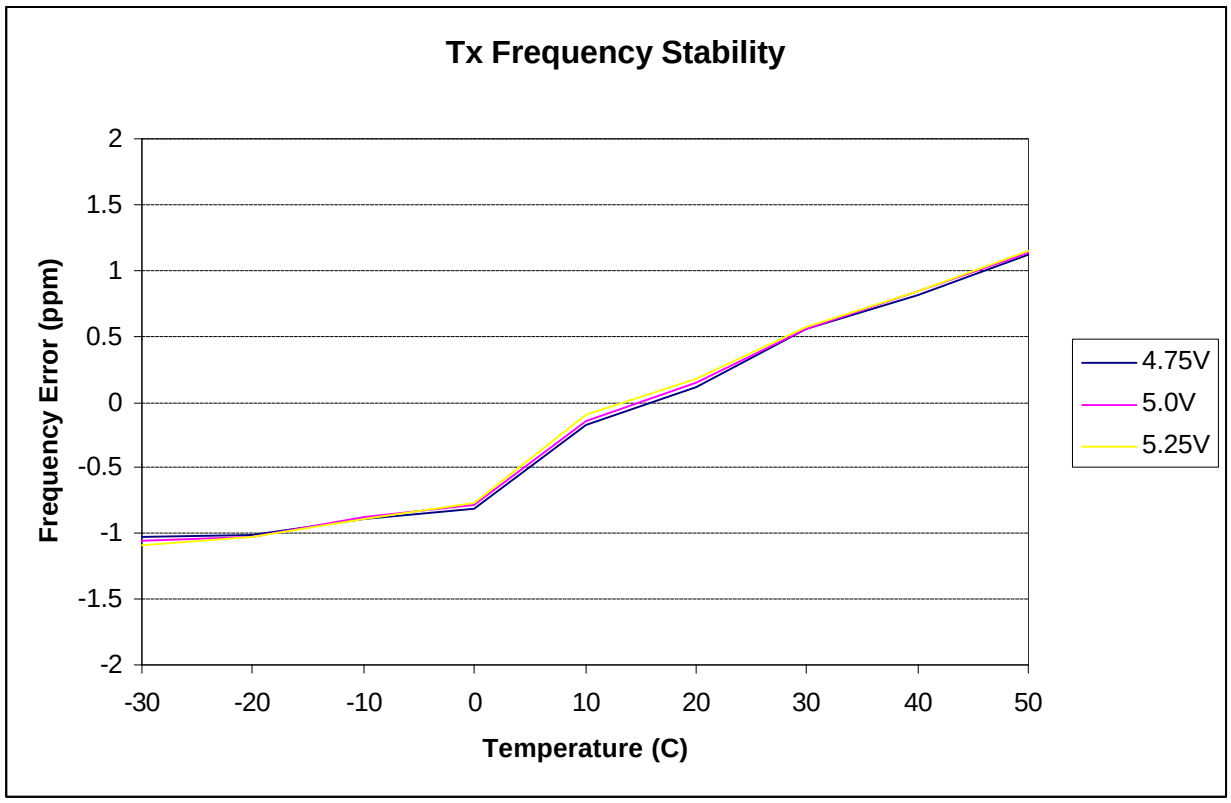
NOTE: The EUT has an internal voltage detector which disables the modem if power supply deviates more the 0.25V from nominal. Testing was therefore performed at nominal voltage (5.0V) and the upper and lower threshold of operability permitted by the voltage supervisor, 5.25V and 4.75V respectively.

Measurement Data

Table 1: Tx Stability Varying +5V Supply

Temp (°C)	Freq. Stability (rated voltage 5.0V) (ppm)	Freq. Stability (max voltage 5.25V) (ppm)	Freq. Stability (min. voltage 4.75V) (ppm)	Worst Case Relative to Rated Freq. Stability (ppm)
-30	-1.03	-1.06	-1.09	-1.09
-20	-1.01	-1.02	-1.03	-1.03
-10	-0.89	-0.88	-0.89	-0.89
0	-0.81	-0.78	-0.77	-0.81
10	-0.17	-0.14	-0.10	-0.17
20	0.12	0.14	0.17	0.17
30	0.55	0.55	0.56	0.56
40	0.81	0.84	0.84	0.84
50	1.11	1.14	1.15	1.15

Worst case frequency error found was 1.15 ppm which falls within the minimum standard of +/- 2.5 ppm.



Test Equipment List

Sierra Wireless, Inc.

Type	Manufacturer and Model No.	Serial no.	Accuracy
Spectrum Analyzer	Hewlett Packard HP8562A	08562-60062	
Pre-Amp	Hewlett-Packard 83006A	3104A00167	
Amplifier 9 kHz-1300MHz	Hewlett Packard 8447F OPT H64	2727A02208	
Service Monitor	IFR FM/AM 500A	4103	0.2PPM
Oscilloscope	Kikusui C055060	6132295	
Power Supply	Astron VS35	8601266	
Voltmeter	Fluke 8020A	N2420658	DCV +/- 0.1%
Multimeter	Fluke 25	3710310	DCV +/- 0.1%
Wattmeter	Bird 43	56227	+/-5%FS
RF Termination	Bird 8135	10004	1.1 VSWR
Dual Phase LISN 50 ohm/50 uH	STI per MP-4	O2	
Dual Phase LISN 50 ohm/50 uH	Compliance Design	9=8012-50R-24-BNC	
Audio Generator	Hewlett-Packard 205-AG	8689	
Attenuators	Texscan FP45-20 Texscan FP45-10 Weinshel 40-10-33 Mini-Circuits CAT30 Pomona 4108-10	 CZ682 8419 01	 +/-1% to 1.5 GHz
Thermometer	Fluke 52	3965185	+/-(0.1% reading +/-0.7 deg C)
Test Line Simulator	Teltone TLS-2	none	
Turn Table, RC	EMCO 1060-2M	8912-1415	
Antenna Mast, RC	Compliance Design, Inc.	M100	
Antennas	Singer/Empire Devices		

Two Di-Pole Sets	Models: DM-105-T1, T2, T3	STI Modified w/Roberts Balums
Bi-Conical	STI per Mil. Spec. 461	BCSTI-201
Bi-Conical	EMCO 3104	3763
Bi-Conical	EMCO 3104 C	9401-4635
Log-Periodic	EMCO 3146	1754
Active Loop	EMCO 6502	9107-2645
Dual Ridged Guide Horn	Electro-Metrics	EM-6961/RGA-60
Pyramidal Feed/	EmpireDevices AT-112	none
Para. Dish	LPA-112, HF-112	
RGA-60	Electro-Metrics	6225

FCC Sample Label

Finished Product Label:

See the photos accompanying this report for the layout and positioning of the FCC label.

Finished Product Label Location:

See the photos accompanying this report for the layout and positioning of the FCC label.