DESCRIPTION OF CIRCUIT FUNCTION

CIRCUIT DESCRIPTION

1. RECEIVER CIRCUITS

1.1 ANTENNA CIRCUIT

Received signal are passed through the low-pass filter (L202, L203, C206, C204, C279)). The filtered signals are applied to the antenna circuit. Its impedance becomes very high while D203 is turned ON. The passed signals are then applied to the RF amplifier circuit.

1.2 RF CIRCUIT

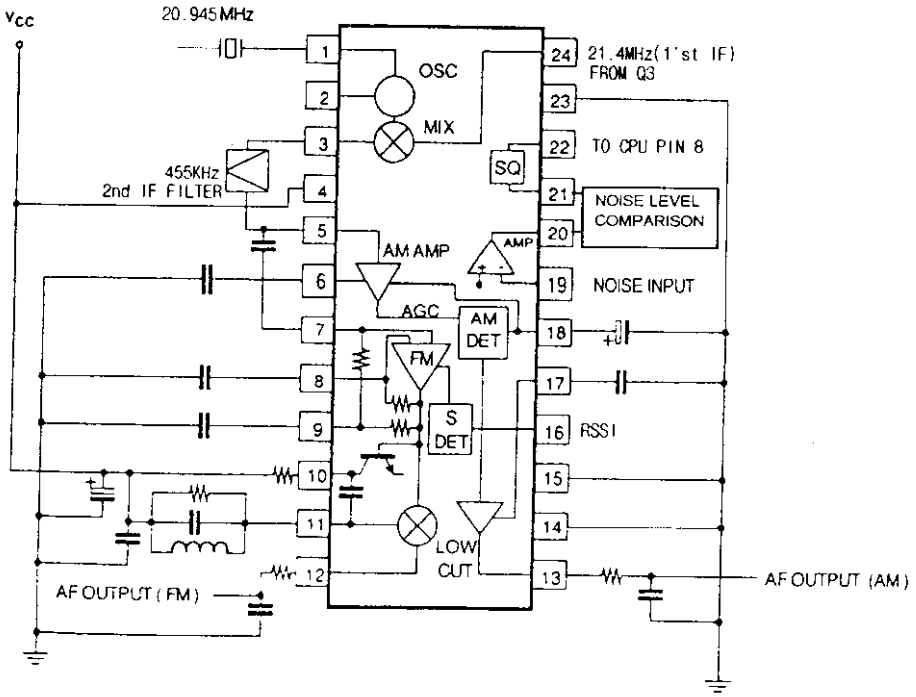
The RF circuit amplifies signals within the range of frequency coverage and filters D212, D207, L208, C280, C207 out-of-band signals. The signals from the antenna circuit are amplified at the RF amplifier (Q1, Q2) after passing through the tunable bandpass filter (L206, L207, D205, D206, C209, C217, C222). The amplified signals are applied to the 1st mixer circuit (Q4) after out-of-band signals are suppressed at the tunable bandpass filter.

1.3 1ST MIXER AND 1ST IF CIRCUITS

The 1st mixer circuit converts the received signal to a fixed frequency of the 1st IF signal with a VCO output frequency. By changing the VCO frequency, only the desired frequency will be passed through a crystal filter at the next stage of the 1st mixer. The signals from the RF circuit are mixed at the 1st mixer (Q4) with a 1st local signal coming from the VCO circuit to produce a 21.4 MHz 1st IF signal. The 1st IF signal is applied to a pair of crystal filter (XF201, XF202) to suppress out-of-band signals. The filtered 1st IF signal is applied to the IF amplifier (Q3), then applied to the 2nd mixer circuit (IC203, pin24).

1.4 2ND IF AND DEMODULATOR CIRCUITS

The 2nd mixer circuit converts the 1st IF signal to a 2nd IF signal. A double conversion superheterodyne system (which converts receive signals twice) improves the image rejection ratio and obtains stable receiver gain. The 1st IF signal from the IF amplifier is applied to the 2nd mixer section of the AM, FM IF IC (IC203, pin24), and is mixed with the 2nd LO signal to be converted to a 455 kHz 2nd IF signal. The AM, FM IF IC contains the 2nd mixer, limiter amplifier, quadrature detector and active filter circuits. A 21.4 MHz 2nd local signal is produced at the VCO circuit by dividing it's reference frequency. The 2nd IF signal from the 2nd mixer (IC203, pin3) passes through a ceramic filter (CF201) to remove unwanted heterodyned frequencies. It is then amplified at the limiter amplifier (IC203, pin5) and applied to the quadrature detector (IC 203, pins10, 11) to demodulate the 2nd IF signal into AF signals.



1.5 RECEIVER LOCAL OSCILLATOR OUTPUTS

1st mixer : The output signals of Q19 is injected to the sources of 1st mixer Q4 in the 1st if mixer section.
2hd mixer : The output of 20.945 MHz oscillator circuit with XF201, XF202 is injected into the IC201. Incoming if signal and 20.945 MHz signal are mixed inside the if IC to extract 2nd if signal 455 KHz.
AM, FM signals are recovered with envelope detector.

1.6 SQUELCH CIRCUIT

A squelch circuit cuts out AF signals when no RF signals are received. By detecting noise components in the AF signals, the squelch switches the AF mute switch.
A portion of the AF signals from the AM, FM IF IC (IC203, pin 12) are applied to the active filter section (pin 19) where noise components are amplified and detected with an internal noise detector. The squelch level adjustment port (VR201A) is connected in parallel to the active filter input (pin 19) to control the input noise level.

1.7 AM AUDIO OUTPUT

IF IC (PIN 13) detected AUDIO signal is fed through IC204, VR201B to low frequency AUDIO amp (IC202) for driving speaker.

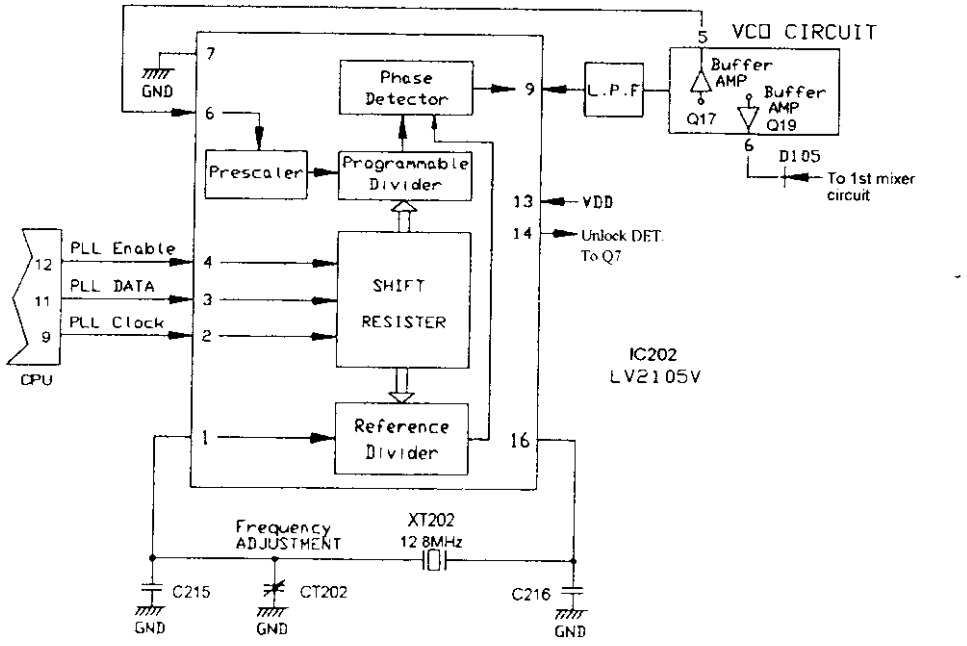
1.8 FM AUDIO OUTPUT

IF IC (PIN 12) detected AUDIO signal is fed through IC204, VR201B to low frequency AUDIO amp (IC202) for driving speaker.

2. PLL CIRCUIT AND VCO CIRCUITS

2.1 PLL CIRCUIT

A PLL circuit provides stable oscillation of the transmit frequency and receive 1st local frequency. The PLL output compares the phase of the divided VCO frequency to the reference frequency. The PLL output frequency is controlled by the divided ratio (N-data) of a programmable divider. The PLL circuit contains the VCO circuit. The oscillated signal is amplified at the buffer-amplifiers (Q17) and then applied to the PLL IC (IC201, pin6). The PLL IC contains a prescaler, programmable counter, programmable divider, phase detector and charge pump, etc. The entered signal is divided at the prescaler and programmable counter section by the N-data ratio from the CPU. The divided signal is detected on phase at the phase detector using the reference frequency.
Reference frequency is the crystal, XT202 (12.80 MHz) and other components at the pin1 and 16 of IC202 can make a reference frequency oscillator with internal amplifier.



2.2 PROGRAMMBLE DIVIDER AND ITS CONTROL

The programmable inputs for each channels are setted ic inside. Each input signal to control the PLL IC202 is done with the provided (CPU IC1) key matrix input pins -pin32 to pin33 and for each key matrix input, an internal code convert eprom provides the appropriate binary control to the IC202 for that channel.
The programmable divider to PLL IC102.
The IC202 output is fed to the phase detector for comparing with the 25 kHz reference frequency inside.

2.3 PHASE DETECTOR AND VCO CONTROL

The phase detector is a digital phase comparator which compares the phase of the reference signal with programmable divider output square waves and develops a series of pulses whose DC level depends on the phase error of each signal.
The phase detector pulse output is fed to an active low pass filter, and fed to varicap D202 control the VCO frequency.
If the oscillated signal drifts, its phase changes from that of the reference frequency, causing a lock voltage change to compensate for the drift in the oscillated frequency.

2.4 VCO

The Q15, Q16 and surrounding parts are consisting a clapp oscillator works as a VCO of IC202 with appropriate control voltage on D202, the VCO can be oscillate over the required range of 129.400 MHz to 184.675 MHz.