CIRCUIT DESCRIPTION

1.RECEIVER CIRCUITS

1.1 ANTENNA SWITCHING CIRCUIT

Received signal are passed through the low-pass filter (LT12,LT11,LT14,CT26~CT31,CT50,CT51). The filtered signals are applied to the antenna switching circuit. The antenna switching circuit functions as a low-pass filter while transmitting. However, its impedance becomes very high while DT1,QT9 is turned ON. Thus transmit signals are blocked from entering the receiver circuits. The passed signals are then applied to the RF amplifier circuit.

1.2 RF CIRCUIT

The RF circuit amplifies signals within the range of frequency coverage and filters out-of-band signals. The signals from the antenna switching circuit are amplified at the RF amplifier (QF2,QF3) after passing through the tunable bandpass filter (LF2~LF5,DF1~DF4) which the tuning frequency range were controlled by PLL tuning voltage and buffer circuit (QP4,QP3,QP2,QP5). The amplified signals are applied to the 1st mixer circuit (QT4) after out-of-band signals are suppressed at the tunable bandpass filter (CF21,LF1).

1.3 1ST MIXER AND 1ST IF CIRCUITS

The 1st mixer circuit converts the received signal to a fixed frequency of the 1st IF signal with a VCO output frequency. By changing the VCO frequency, only the desired frequency will be passed through a crystal filter at the next stage of the 1st mixer. The signals from the RF circuit are mixed at the 1st mixer (QF4) with a 1st local signal coming from the VCO circuit to produce a 21.4MHz 1st IF signal. The 1st IF signal is applied to a pair of crystal filter (XF1,XF2) to suppress out-of-band signals. The filtered 1st IF signal is applied to the IF amplifier (QA16), then applied to the 2nd mixer circuit (IC1, pin20).

1.4 2ND IF AND DEMODULATOR CIRCUITS

The 2nd mixer circuit converts the 1st IF signal to a 2nd IF signal. A double conversion superheterodyne system (which converts receive signals twice) improves the image rejection ratio and obtains stable receiver gain. The 1st IF signal from the IF amplifier is applied to the 2nd mixer section of the FM IF IC (IC1, pin20), and is mixed with the 2nd LO signal to be converted to a 455 kHz 2nd IF signal. The FM IF IC contains the 2nd mixer. Limiter amplifier, quadrature detector and active filter circuits. A

20.945MHz 2nd local signal is produced at the IF IC (IC1, pin1, pin2). The 2nd IF signal from the 2nd mixer (IC1, pin4) passes through a ceramic filter (FA1) to remove unwanted heterodyned frequencies. It is then amplified at the limiter amplifier (IC1,pin6) and applied to the quadrature detector (IC1,pin9,10) to demodulate the 2nd IF signal into AF signals .

1.5 RECEIVER LOCAL OSCILLATOR OUTPUTS

1st mixer: The output signals of QT2 are injected to the sources of 1st mixer QF4 in the 1st IF mixer section. 2nd mixer: 2nd local oscillating frequency is the crystal, XA1 (20.945MHz).

1.6 SQUELCH CIRCUIT

A squelch circuit cuts out AF signals when no RF signals are received. By detecting noise components in the AF signals the squelch switches the AF mute switch.
A portion of the AF signals from the FM IF IC (IC1, pin11) is applied to the active filter section (IC1, pin13) where noise components are amplified and detected with an internal noise detector. The squelch level adjustment pot (RA24) is connected in parallel to the active filter output (pin14) to control the output noise level.

2.TRANSMITTER CIRCUITS

2.1 MODULATION CIRCUIT

The modulation circuit modulates the VCO oscillating signal (RF signal) using the audio signal. The audio signals change the reactance of a diode (QV3) to modulate an oscillated signal at the VCO circuit (QV1, QV2). The oscillated signal is amplified at the buffer-amplifiers (QV6, QT2), and then applied to the T/R switching circuit (QT4).

2.2 DRIVE/POWER AMPLIFIER CIRCUITS

The signal from the VCO circuit passes through the T/R switching circuit (QT4) and is amplified at the buffer (QT5), pre-drive (QT10), drive (QT7) and power amplifier (QT8) to obtain 5W of RF power (at 12.5V DC). The amplified signal passes through the antenna switching circuit (DT1, QT9), and low-pass filter (L11, L13, L14, CT26~CT31, CT50, CT51) and is then applied to the antenna connector (J1).

2.3 CIRCUIT FOR SUPPRESSION OF SPURIOUS RADIATION

The tuning circuit between the output of final amp QT8 and antenna, 4-stage "PHI type" network LT8, CT23, LT10, CT51, LT14, CT50, CT26, LT11, CT29, CT31,

LT12, CT28, CT30) server as a spurious radiation suppressor. This network also serves to match the impedance between TX power amp QT8 and the antenna.

3.PLL CIRCUIT AND VCO CIRCUITS

3.1 PLL CIRCUIT

A PLL circuit provides stable oscillation of the transmit frequency and receive 1st local frequency. The PLL output compares the phase of the divided VCO frequency to the reference frequency. The PLL output frequency is controlled by the divided ratio (N-data) of a programmable divider. The PLL circuit contains the VCO circuit. The oscillated signal is amplified at the buffer-amplifiers (QT1) and then applied to the PLL IC (IC6, pin8). The PLL IC contains a prescaler, programmable counter, programmable divider, phase detector and charge pump, etc. The entered signal is divided at the prescaler and programmable counter section by the N-data ration from the CPU. The divided signal is detected on phase at the phase detector using the reference frequency. Reference frequency is the crystal; XF1 (12.80MHz) and other components at the pin1 and 2 of IC6 can make a reference frequency oscillator with internal amplifier. The DC 12V tuning voltage was provided by IC5 network, there is connect to the PLL IC (IC6) pin3.

3.2 PROGRAMMBLE DIVIDER AND ITS CONTROL

The programmable inputs for each channel are set IC inside. Each input signal to control the PLL IC6 is done with the cpu's PLL STB, Data, and clock 3 controlled pins. An internal code convert eprom provides the appropriate binary control to the IC6 for than channel. Since the binary number necessary to change during transmit and receive, an additional bit is required at the pin7 of CPU IC (unlock pin) is low under transmit mode. The IC6 output is fed to the phase detector for comparing with the 6.25KHz or 5KHz reference frequency inside.

3.3 PHASE DETECTOR AND VCO CONTROL

The phase detector is a digital phase comparator which compares the phase of the reference signal with programmable divider output square waves and develops a series of pulses whose DC level depends on the phase error of each signal. The phase detector pulse output is fed to an active low pass filter, and fed to varicap QV1, QV2, QV3 control the VCO frequency. If the oscillated signal drifts, its phase changes from that of the reference frequency, causing a lock voltage change to compensate for the drift in the oscillated frequency. A portion of the VCO signal is amplified at the buffer-amplifier (QV6, QT2) and is then applied to the receive 1st mixer or transmit

buffer-amplifier circuit via the T/R switching diode (QT4).

3.4 VCO

The QV5 and surrounding parts are consisting a clapp oscillator works as a VCO of IC6 with appropriate control voltage on QV1, QV2, QV4, and the Audio Input JV02 is from MIC Amp IC7 to get the FM modulation for TX mode

SYSTEM DC POWER AND CONTROLLED CIRCUIT.

The main of the system controlled is DC 4V, which provide by IC4, the CPU power supply is DC 5V, there is provided by Q1, Q4, D5, which controlled by the DC 4V, and the radio's command are come from shift IC (IC2, IC3) through the CPU controlled pin clk, 40494STB, Data (U7 pin4~6).