TELEFIELD LTD.
CIRCUIT DESCRIPTION

Model :FF2125B **Date: 01/ 24 / 2002**

CCT Ref :

FF2125B is answering machine with 900M cordless .Following content is TAD part circuit description.

1. Function Blocks

The answering part of FF2125B consists of the following functional circuit blocks:-

1.1 Power Supply & Low Battery Detection
1.2 Telephone Line Interface
1.3 Surge Protection
1.4 Branch Phone Reset
1.5 Ring Detection
1.6 CPU & CPU Interface
1.7 Voice Recording / Reproducing ASIC & Interface
1.8 Pre _amplifier &ALC
1.9 Audio Amplifier
1.10 Day / Time Stamp
1.11 RF release answering

2. Circuit Block Description

2.1 Power Supply & Low Battery Detection

The power is supplied from an AC/AC adaptor which gives 9VAC from the 120VAC mains, the AC from the adapter is then coupled to bridge-rectify(D21-24)which transform AC to DC, the DC pass the C11 filter then coupled to the voltage regulator Q3 (8050)&DZ2 (7.5V),which regulates the voltage to 6.8VDC, this voltage supplies power to all the audio circuitry of the circuit. The DC power pass rectifier D11(IN4004) and the voltage is regulated to around 5.0V by Q4(8050) & DZ1(5.6V, Zener), this voltage supplies power to all the digital circuitry of the circuit.

The circuit is backed up by one 9V alkaline battery, the battery is disconnected from the supply rail when the AC mains is presented by D10(IN4004), When there is a power failure, D1 is turned on and the 9V is regulated down to about 5.0V by Q4 (8050) & DZ1 (5.6V, Zener) which together form a voltage regulator. The back up voltage will only supplied to the digital part circuit which will back up all messages stored in the ARAM.

Low Battery is detected by voltage comparison U3A(LM339) ,then CPU (#39) checks U3A(LM339 #1) level to adjudge battery state.

2.2 Telephone Line Interface

The telephone line input (Tip/Ring) and line is controlled to relay RL1A by CPU (U6 #51) and RF_REL, then the parallel connection is fed to transformer(TRA1)&R68, line is segregated and coupled to balance net(RF part BQ10& BQ9 etc).. The line seizure is performed by relay RL1B, when Q5 is turned on by the CPU(U6,#51).RL1B is on and the line is seized,

2.3 Surge Protection

Surge protection is performed by R70(10 Ohm,1/2W).

2.4 Branch Phone Reset

The circuit will release the answering machine from the telephone line when a parallel phone goes OFF HOOK. Line pass bridge rectifiers formed by D3-6 (IN4004) which act as a polarity guard for the circuitry.C4(22uF) is constantly charged and discharged and cause Q8(2N3906) IC1(PC817) &Q1(2N3906) to turn on/off. CPU(U6 #35) checks Q1.E level change for adjudging if parallel phone has seized the line.

2.5 Ring Detection

Ring signal is coupled from L1, L2, F1, R1, C1, Z1(33V), Z2(33V)to IC1(PCB817) which forms for ring voltage threshold level adjustment. The wave shaped ring signal is then passed to the CPU U6 #36

2.6 CPU & CPU Interface

The heart of this circuit block is a CPU and the voice chip — U6 (SV9601–B).

It's function is as followings:-

---- Low Battery Detection (see section 2.1)
---- Telephone Line Seizure and Disconnect (see section 2.2)
---- Branch Phone Detection (see section 2.4)
---- Ring Signal Detection (see section 2.5)
---- Voice Recording/Reproduce Interface (see section 2.7)
---- Line in/out path, record/play path control (see section 2.6.1)
---- Function Key Interface (see section 2.6.2)
---- 7 Segment Display Interface (see section 2.6.3)
---- VOX Detection (see section2.6.4)
---- DTMF Decode (see section 2.6.5)

2.6.1 Paths Control

The CPU will provide control for the following paths through suitable control (namely

The CPU will provide control for the following paths through suitable control (namely the MIC. enable U6 #98, speaker enable U6 #97, line in enable U6 #99 and line out enable U6 #83) to the desired analogue switches for the corresponding paths. The control can be divided into the following areas:-

---- OGM recording

The microphone MIC. is enabled, the speaker / line in / line out is disable.

---- OGM / ICM play back

Speaker / line out enable, line in / MIC. disable.

---- ICM recording

Speaker / line in enable, MIC / line out disable.

2.6.2 Function Key Interface

The CPU will accept input and perform corresponding functions from the following function keys:-

---- Answer ON/OFF (SW9)

This key input will inform the CPU to turn the unit into or out of the Answer Ready mode.

---- GREETING (SW12)

This key input will inform the CPU to record OGM or play OGM.

---- STOP (SW11)

The CPU will perform the stop function when this particular key input is sensed.

---- PLAY (SW5)

This key will inform the CPU to play the ICM message and MOME.

---- SKIP (SW6)

When this key input is sensed, the CPU will skip the message being played.

---- REPEAT (SW1)

When this key input is sensed, the CPU will repeat the message being played.

---- ERASE (SW4)

When this key input is sensed, the CPU will erase the current message being played

----UP(SW8)

When this key input is sensed, the CPU will adjust the Speaker volume to be higher.

----DOWN(SW10)

When this key input is sensed, the CPU will adjust the Speaker volume to be lower.

----2,4 &TS (SW17)

Ring selection switch.

2.6.3 Segment Display interface

The 7-segment display is controlled by CPU #63-70. The 7-segment display will

display the following:-

----Message received after the first incoming message, the display will change from 0 to indicate 1 and so on.

---- Battery Low

The 7-segment display will flash rapidly to indicate that the battery is low.

---- RAM FULL

The 7-segment will show "F", the display will be flash if new message is received

2.6.4 VOX Detection

The voice signal is passed to the VOX comparator U3B(LM339) from the pre_ amplifier U5(KA22130), The comparator will take the reference voltage as derived using the potential divider R52 & R53 (150k &3.3k respectively), If signal level is lower than this level, the comparator will output a high signal to CPU #37, conversely, it will output a low signal to CPU #37, The CPU will use this signal to determine when to drop the line.

2.6.5 DTMF Decode

DTMF signal is fed from RF BALANCE NET&Q6 to decode circuit main formed by U2(8870) and then decode DATE passing to CPU(U6 #52-56) for subsequent remote detection.

2.7 Voice Recording / Reproducing Interface

The OGM / ICM message is stored in the ARAM(U7, S4004SB1 4M x 4) via the voice chip(U6, SV9601-B). The voice signal is input to the ADI terminal of the voltage comparator (U3D, #9 LM339), the voice chip U6 will always try to generate a signal equal to the signal present at ADI. The voice chip constantly check the O/P of the comparator (U3D, #14) to know the signal information.

The ARAM interface is also performed by the Voice chip (U6) with its internal refresh counter providing refresh cycles to the ARAM.

2.8 Automatic Level Control, SIGNAL AMPLIFER& SP POWER

The heart of the block is U5(KA22130) which include PRE_AMP ALC POWER_AMP ROPPLE_FILTER. It is used to process difference analogue signals.

2.9 VOL_SP

D/A signal volume is controlled by digit volume control circuit (R86_89 etc),then the signal passes from the analogue switch U4C (4066) is passed (by CPU #96) to the input terminal (U5 #13),the amplified signal is coupled to the speaker through C38(100uF).

2.10 Day / Time Stamp

The voice of the seven days and the 24 hours are presented in the EPROM U5(UM23C1101). The current day/time clock can be manually set through [<<],[ON/OFF] and [PLAY] key. The time of ICM message will be stamped and it can be played associated with the ICM messages. Thus, the EPROM's interface is also performed by the Voice chip U7(9601) with its internal refresh counter providing refresh cycles to it.

2.11 RF release answering

while the unit is answering ,if it shall establish RF communication ,because CPU (U6 #42) checks HI level ,casing to must stop answering.

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2125 RF Circuit Description

1. Introduction

The model 2125 RF is a 40 channel (902.125 - 927.100Mhz) cordless telephone. The whole unit is divided into two main parts as follow :

a. A remote Handset.
b. A Base unit.

2. Functional Blocks of the Remote Handset

2.1 Keyboard matrix and function LED
2.2 MCU and MCU interface
2.3 Antenna and RF module
2.4 Compander
2.5 Data shaper
2.6 Charge detector
2.7 Low battery detector
2.8 Buzzer amplifier

3. Circuit Block Description

3.1 Keyboard matrix and function LED

Pin 4 to pin7, pin 10 to pin 11 and pin 25 of the U2 ACT15H MCU form a keyboard, and the talk LED is controlled by the pin 12 of the MCU.

3.2 MCU and MCU interface

The handset and the base is link up by the pins(9,24 in HS and 21,24 in Base). Besides, the PLL of the RF Module is controlled by the pins 15,17 and 18 of the MCU.

3.3 Antenna and RF module

ANT is the common point for transmitting and receiving through antenna. MD1 is a RF module which consists of Duplexer, Power amplifier, Mixer & IF, RXVCO, TXVCO, VCC & TXVCC control, Synthesizer and DEMO Audio Output circuits.

3.4 Compander

A compander U3 is used for improving the S/N of the transmit and receive audio signal.

3.5 Data shaper

The information which sending from base unit, is recovered by the amplifier Q1 and Q2.

3.6 Charge detector

ZD1, D4, D5, D6, D7, D8, R53, C29 form a charge detector to direct the charging signal to the MCU pin 26.

3.7 Low battery detector

A battery low detector is built-in by Q3 and Q4 which detects the battery dropping and sends a signal to pin 19 of MCU.

3.8 Buzzer amplifier

Q11 is a buzzer amplifier driven directly by the MCU pin 23.

4. Functional Blocks of the Base unit

4.1 Power supply
4.2 MCU and MCU interface
4.3 Antenna and RF module
4.4 Compander
4.5 Data shaper
4.6 Charge detector
4.7 Ring detector
4.8 Led function board
4.9 Noise detector and carrier detector

5. Circuit Block Description

5.1 Power supply

BQ5 is regulate the input DC 9V to 5V which provides power to every part of the circuit.

5.2 MCU and MCU interface

The heart of the base is BU5 ACT81 MCU that communicates with the PLL of BMD1 through pins 5,6 and 7. Transmitter is controlled by the signal TX_DC which output from MCU via pin 20. MCU pins 6 to 11 consist of a resistor ladder for generating DTMF signal. The communication between Handset and Base is via the pin 24 and pin 26 through the RF link.

5.3 Antenna and RF modulator

ANT is antenna transmit and receive signal. BMD1 is a RF modulator which consist of Duplexer, Power amplifier, Mixer & IF, RXVCO, TXVCO, VCC & TXVCC control, Synthesizer and DEMO Audio Output circuits.

5.4 Compander

A compander BU1 is used for improving the S/N of the transmit and receive audio signal.

5.5 Data shaper

The information which sending from handset unit, is recovered by the amplifier BQ1 and BQ2.

5.6 Charge detector

BQ7 is a charge detector to direct the charging signal to the MCU pin 25.

5.7 Ring detector

BC41, BR69, BZD3, BZD2, BD8, BU4(K817P or LTV817) and BR44 form a ring detector which feed the signal through pin 26 of MCU.

5.8 LED function board

BLED1 is used for indicating "IN USE" OR "CHARGING" when handset is on cradle.

5.9 Carrier detector

The RF Module BMD1 pin 12 is an output pin of the carrier detector signal , it is sent to BU5 pin 23.When there is carrier, it is Low; when there is noise, it is High. BU5 finds the clear channel by this pin 23.

CORDLESS OPERATION

Channel frequencies FREQUENCY TABLE

CH.	BASE TX	H/S TX	CH.	BASE TX	HS/TX
1	902.125	926.125	21	902.625	926.625
2	902.150	926.150	22	902.650	926.650
3	902.175	926.175	23	902.675	926.675
4	902.200	926.200	24	902.700	926.700
5	902.225	926.225	25	902.725	926.725
6	902.250	926.250	26	902.750	926.750
7	902.275	926.275	27	902.775	926.775
8	902.300	926.300	28	902.800	926.800
9	902.325	926.325	29	902.825	926.825
10	902.350	926.350	30	902.850	926.850
11	902.375	926.375	31	902.875	926.875
12	902.400	926.400	32	902.900	926.900
13	902.425	926.425	33	902.925	926.925
14	902.450	926.450	34	902.950	926.950
15	902.475	926.475	35	902.975	926.975
16	902.500	926.500	36	903.000	927.000
17	902.525	926.525	37	903.025	927.025
18	902.550	926.550	38	903.050	927.050
19	902.575	926.575	39	903.075	927.075
20	902.600	926.600	40	903.100	927.100