1. Circuit Description

The following descriptions are included: (1) means for modulation limiting, (2) means for power limiting, (3) means for spurious radiation limiting, (4) means for frequency stabilization. (5) Tune-up procedure, (6) Defined adjustable power levels

1.1. Means for Modulation Limiting

Figure 1 illustrates the Adaptasite signal flow when functioning as a repeater between the mobile unit and the broadband RF transceiver (BTS). The GMSK modulated (uplink or downlinkl) RF signal is received at the DAS receive (RX) inputs and downconverted to baseband by RF and digital circuitry. Surface Acoustic Wave (SAW) filters in the receive chain limit the signal bandwidth to the desired frequency range. The analog baseband signal is converted to a digital signal and input to a digital downconverter (DDC). The DDC utilizes a cascaded - integrator – comb (CIC) filter and multiple programmable FIR filters (87 total taps used) to limit the signal bandwidth through the downconversion process. The output signal 3 dB bandwidth (baseband) is 100 kHz with 105 dB rejection at 150 kHz and 170 dB rejection at 400 kHz.

The digital signal from the DDC is routed to a digital upconverter (DUC) in preparation for re-broadcast over the uplink or downlink. Distributed filtering (FIR, halfband, and comb) is applied through the x48 interpolation process to maintain a 3 dB bandwidth of 250 kHz on a 10.7 MHz output signal. The TX RF applies additional ceramic filtering (removes clocks, alias, etc) to the 10.7 MHz signal and SAW filtering at the 2nd IF to control the transmitted bandwidth while the signal is upconverted to the appropriate GSM frequency band.

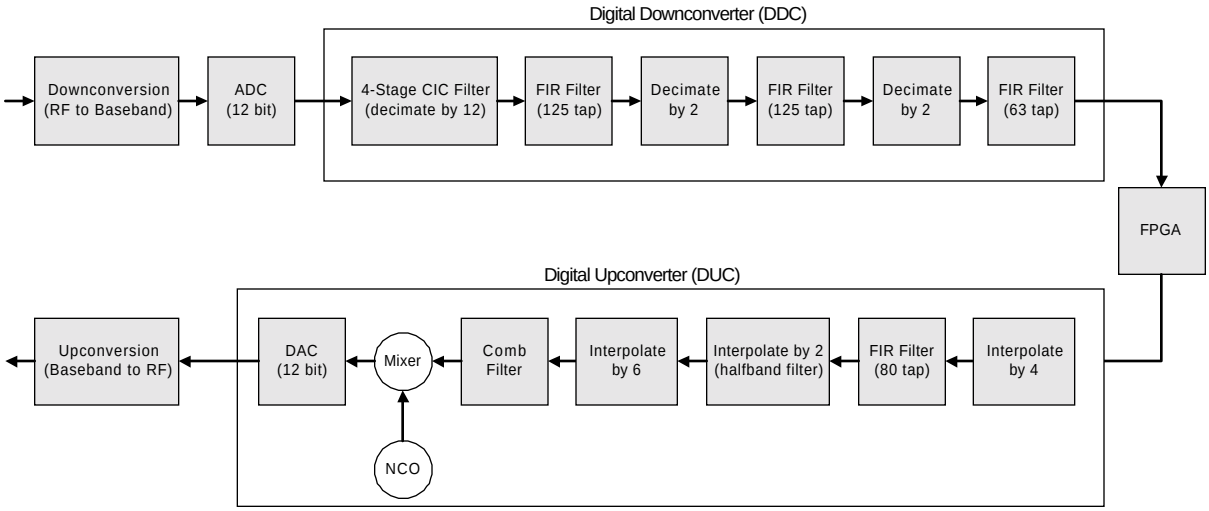

Figure 1: Modulated Signal Bandwidth Control

1.2. Means for Power Limiting

The Digital Adaptasite (DAS) receives and transmits both uplink and downlink signals between the mobile station (MS) and the broadband RF transceiver (BTS). The DAS provides no automatic RF power level control (ALC) on the uplink signal and only minimal ALC on the downlink BCCH signal to counter slow fading due to atmospheric conditions or component temperature variations.

Referring to Figure 2, the uplink from the MS is translated to IF, analog to digital converted (ADC), and digitally downconverted (DDC). The digital data is processed (DSP) to determine the received power level (RX_LEV) from the mobile. To maintain complete receive dynamic range, the RX_LEV is used to adjust a digital variable gain amplifier (DVGA) for full scale input to the ADC. The uplink signal is then upconverted to RF and transmitted over the backhaul link to the BRT. During system installation a test signal is used to set the maximum transmit level from the DAS to provide –70 dBm at the BTS (if possible) while remaining compliant with spectral specifications. The digital sine wave output amplitude (FPGA) required to set this –70 dBm level is stored in DAS memory for use during normal operation. The uplink output power of the DAS is **+30 dBm (1 watt) nominal**. The output amplifier will saturate to limit the antenna input power to **+31.5 dBm (1.4 watts) maximum**.

Signal flow through the downlink DAS is identical to the uplink except for the addition of a 56 watt high power amplifier at the output. In this case a sample of the transmit signal is detected and used for closed loop level control on the broadcast control channel (BCCH). The gain of the digital upconverter (DUC) is adjusted to maintain maximum output power of +46 dBm (40 watts) at the antenna input. Detector accuracy is +/- 1 dB over frequency and temperature and DUC gain resolution is < 1 dB . The downlink output power of the DAS is **+46 dBm (40 watt) nominal**. The output high power amplifier will saturate to limit the antenna input power to **+47.5 dBm (56 watts) maximum** if level control fails. The BTS controls traffic channel power relative to this maximum level.

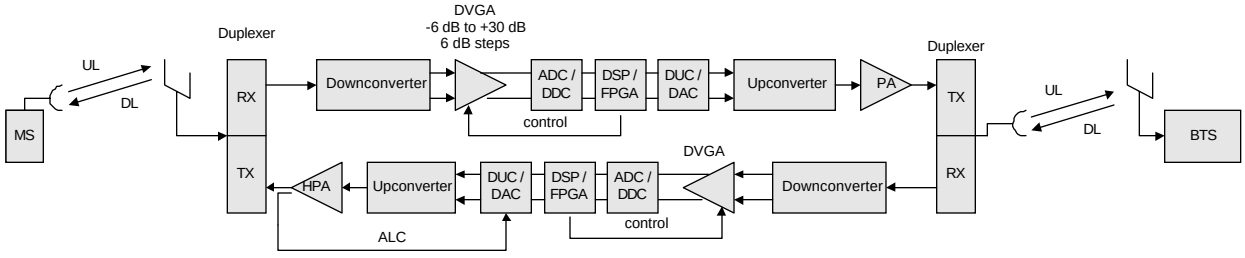

Figure 2: Simplified Danger Signal Flow Diagram

1.3. Means for Spurious Radiation Limiting

The Digital Adaptasite (DAS) is designed to minimize spurious emissions inside and outside of the selected modulation bandwidth. Careful frequency planning in the up conversion chain minimizes intermodulation (IM) products from the mixer stages. Multiple stages of filtering further attenuates out of band spurious signals generated by mixers and amplifiers. Figure 3 illustrates the DAT transmit (TX) frequency plan and filtering scheme.

A modulated 10.7 MHz TX signal is received from the DAT digital upconverter (DUC) and translated to a 125 MHz IF using a double balanced passive mixer and a low side LO at 114.3 MHz. Input bandwidth is constrained with digital filtering in the DUC and a ceramic filter in the RF circuit. The IF is filtered by a surface acoustic wave (SAW) bandpass filter centered at 125 MHz with a 800 kHz 3 dB bandwidth. Out of band rejection for the first SAW is greater than 55 dBc at 13 MHz offset from center out to 450 MHz. An LC image reject filter is also included prior to the second mixer. The signal is then translated to the uplink or downlink TX frequency range with a DB passive mixer and a high side LO from 1975 to 2115 MHz. A SAW filter following the mixer is selected for the proper link frequency. Both filters have a 60 MHz 3 dB bandwidth and greater than 25 dB out of band rejection at 50 MHz offset. Proper impedance control at each mixer port improves VSWR and reduces reflections back into the mixer which can cause additional spurious responses. A separate cavity filter after the DAT is block specific and limits the bandwidth to 5, 10, or 15 MHz depending on block. Greater than 73 dB harmonic and spurious rejection is achieved through second harmonic of selected center frequency. The combination of prudent frequency planning and multiple SAW / cavity filters specific to the desired band assure attenuation of spurious emissions within specification limits.

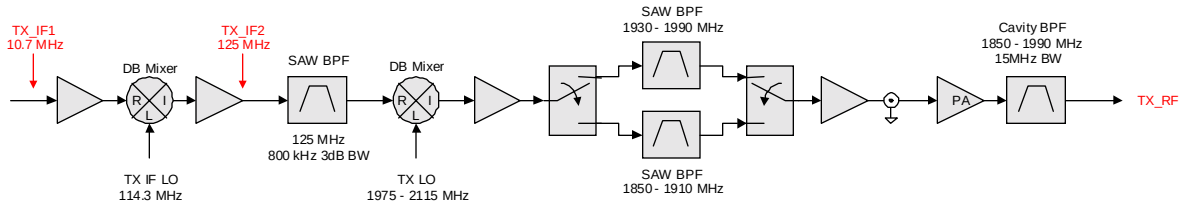

Figure 3: DAT TX Simplified Block Diagram

1.4. Means for Frequency Stabilization

Each DAS includes a 13 MHz temperature compensated voltage controlled crystal oscillator (TCVCXO) to discipline all on-card local oscillators used in the frequency translation process. This TCVCXO is specified for a **± 10 ppm** accuracy over temperature and a 10 year operational life. The 'master' Danger transceiver (DAT) TCVCXO is frequency locked to the BTS via a frequency correction channel (FCCH) on the downlink backhaul signal. The DAT averages multiple FCCH bursts, calculates the frequency error of the received signal (DSP), and generates a proportional control voltage to tune the TCVCXO to within **0.05 ppm**. The BTS corrected master DAT 13 MHz signal is applied to the DAS backplane. In multiple transceiver configurations, 'slave' DAT's are frequency locked to the 'master' DAT using the 13 MHz reference available from the DAS backplane and a double balanced mixer based phase lock loop (PLL). 'Slave" DAT's show no measurable frequency error relative to the 'master'.

The DAT transmit path uses a dual conversion scheme to translate the modulated baseband signal from 10.7 MHz to a 125 MHz IF and then to the desired GSM RF band. As shown in Figure 4, both the IF and RF local oscillator (LO) signals are synthesized with an LMX2330A PLL IC using the 13 MHz TCVCXO as reference. The 13 MHz reference is applied to the PLL IC and then split between the two synthesizers. For the IF synthesizer the reference is divided by 130 and a sample of the 114.3 MHz VCO output is divided by 1143 to yield a 100 kHz compare frequency at the phase / frequency detector. The PLL charge pump outputs an error current proportional to the phase difference between the reference and IF signals. The error signal is converted to voltage and low pass filtered with an active loop filter before application to the tuning port of the VCO. The RF synthesizer PLL works identically to the IF except that a 200 kHz comparison frequency is used and the VCO output divider is programmable between 9875 and 10575 to allow tuning of the RF output frequency**.** Therefore, the DAT output signal is phase locked to the 13 MHz reference (which is corrected by the BTS) to generate an extremely accurate and stable transmit frequency.

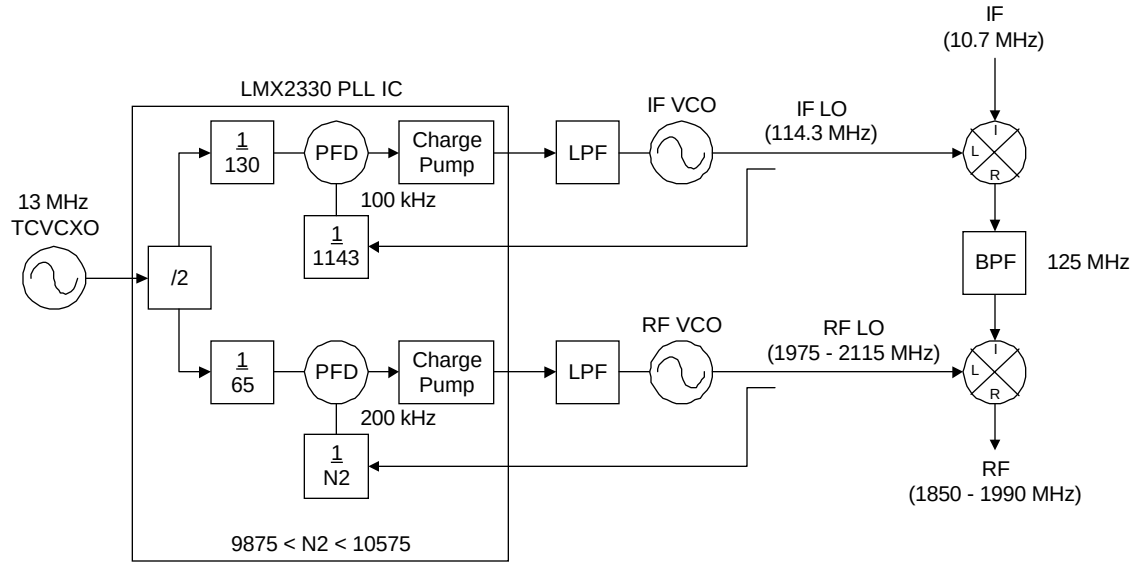

Figure 4: Transmit PLL Functional Block diagram

1.5 Power Tune-up Procedure

(Excerpt from AirSite FCC ID: MZKRE3010-1900)

1.5.A1 Frequency

The parameters for programming the uplink and downlink synthesizers are stored in flash memory on the AirSite Remote Radio microprocessor module. These parameters determine receive and transmit frequencies and their separation. The parameters are stored in the flash (non-volatile) during AirSite Remote Radio installation based on the frequency plan for that particular coverage area. The AirSite Remote Radio automatically tunes to these frequencies at power-up once the flash has been programmed. There is no user accessible way of re-tuning the AirSite Remote Radio.

1.5.A2 Output Power

The rated output powers that this application is written for (40-Watt downlink and 2-Watt uplink) are the maximum achievable output powers. To get this output level, the maximum signal level is input and the attenuators in the downlink and uplink ALC circuits (see Means for Limiting Power) are set to 0 dB. This gives the maximum gain through the uplink and downlink paths. Higher output powers are not realistically
achievable.
At installation, the installer (see installation manual) verifies that the correct ground and backhaul frequencies (per the RF plan) are programmed in the AirSite. Tests are then performed to ensure that the signal does indeed transmit and receive on the specified frequencies. He then insures that the highest receive signal level from the serving BTS does not exceed the rated input level. Then the ARR is brought into service. It relies on in-band signaling from the serving BTS to command it to activate and deactivate a channel.

1.6 Output Amplifier DC Voltage and Current

The Adaptasite is rated for full RF transmit power on a single GSM carrier of +30 dBm (1 watt) on the uplink and +46 dBm (40 watts) on the downlink.

To achieve the specified uplink transmit power, the DANGER transceiver module (DAT) must output +33 dBm (2 watts). Final amplification in the DAT is provided by a dual stage FET amplifier with active bias circuitry. Bias voltage is provided from a linear regulated **+10 VDC** supply. Bias current from the supply is **1.0 A** nominal yielding a total DC power of **10 W**.

To achieve the specified downlink transmit power, the DAT must output +47.5 dBm (56 watts). Final downlink amplification is provided by a single carrier power amplifier (SCPA) module. The SCPA is specified to operate from a **+12 VDC** supply and draw no greater than **15.5 A** in any frequency band at full operating RF output power. Maximum DC power is **186 W**.

1.7 Range of Operating RF Output Power Levels

The downlink transmit power for a DANGER system with a maximum power level of **40 Watts per carrier** has 6 static power levels (implemented via software) in steps of 2 dB is listed in Table 1.6-1.

Table 1.6-1: DANGER System Downlink Static Power Levels

Static Power Level	D/A Level (dBFS)	DAT-2 Power Level (dBm)	DAT-56 Power Level (dBm)	System Power Level (dBm)	System Power Level (Watts)
0	**-3**	+33 dBm	+47.5 dBm	+46 dBm	40.00
1	**-5**	+31 dBm	+45.5 dBm	+44 dBm	25.12
2	**-7**	+29 dBm	+43.5 dBm	+42 dBm	15.85
3	**-9**	+27 dBm	+41.5 dBm	+40 dBm	10.00
4	**-11**	+25 dBm	+39.5 dBm	+38 dBm	6.31
5	**-13**	+23 dBm	+37.5 dBm	+36 dBm	3.98
6	**-15**	+21 dBm	+35.5 dBm	+34 dBm	2.51