Operation Principles：

ATMEL AT76C510：A RISC CPU with IEEE802.11b MAC layer.

- ✍✍ Wireless interface following the IEEE 802.11b standard.
- ✍✍ Ethernet MAC unit interfaces with 10/100 Mbit Ethernet Physical through a standard MII port.
- ✍✍ Internetworking unit with integrated ARM7TDMI RSIC processor provides the bridging functions between Ethernet and wireless interfaces.
- ✍✍ WLAN MAC unit with a second ARM7TDMI RSIC processor.
- ✍✍ Supports data rat of 1Mbps, 2Mbps, 5.5 Mbps and 11Mbps, with automatic fallback.
- ✍✍ Supports Wire Equivalence Privacy (WEP) as in IEEE802.11.
- ✍✍ Digital interface with HFA3861B, the DSSS baseband processor.
- ✍✍ A 32MHz oscillator is used to provide main clock of the RISC CPU.

Flash ROM and SRAM：Memory resources of CPU.

- ✍✍ Flash ROM is nonvolatile memory. Firmware program is stored in flash ROM.
- ✍✍ SRAM is volatile memory resource for CPU operation.

REALTEK RTL8201L：Ethernet PHY.

- ✍✍ Single Chip 100Base-TX /10Base-T Physical Layer Solution.
- ✍✍ MII interface to Ethernet Controller.
- ✍✍ Using 25MHz crystal as clock source.
- ✍✍ 10 Base transmit function：The transmitted 4 bits nibble (TXD[0:3]) clocked in 2.5MHz(TXC) is first feed to parallel to serial converter, then put the 10MHz NRZ signal to Manchester coding. The Machester encoder converts the 10Mbps NRZ data into a Manchester Encoded data stream for the TP transmitter and adds a start of idle pulse (SOI) at the end of the packet as specified in IEEE802.3. Then, the encoded data stream is shaped by band-limited filter embedded in RTL8201 and then transmitted to TP line.
- ✍✍ 10 Base receive function：In 10Base receive mode, the Manchester decoder in RTL8201 converts the Manchester encoded data stream from

the TP receiver into NRZ data by decoding the data and stripping off the SOI pulse. The, the serial NRZ data stream is converted to parallel 4 bit nibble signal (RXD [0:3])

PI5L200：Precision Wide Bandwidth LanSwitch QUAD 2:1 MUX/DEMUX.

IM4A3-32： ispMACH 4A CPLD family. High performance E^2 CMOS. In-system programmable logic.

HFA3861B：DSSS baseband processor.

- Complete Direct Sequence Spread Spectrum (DSSS) baseband processor.
- Supporting Differential Binary Phase Shift Keying (DBPSK), Differential Quadrature Phase Shift Keying (DQPSK) and Complementary Code Keying (CCK).
- As a PHY layer in IEEE802.11b.

Data Rate (Mbps)	1	2	5.5	11
Modulation	DBPSK	DQPSK	CCK	CCK

- FCC compliant processing gain.
- On-chip A/D and D/A converters for I/Q data (6bit, 22MSPS), AGC, and Adaptive power control (7-bit).
- Supports short preamble acquisition and antenna diversity.

- Transmitter operation：Digital data form MAC layer is modulated to produce analog I/Q baseband signal for transmission. When MAC asserts begin of transmission, HFA3681B generate preamble and header itself. After combining with data sent from MAC, all of the data, depends on different data rate, are modulated by the modulation skim listed above. The modulated data pass through a digital LPF. At last, a on-chip D/A converter converts digital data to analog data and then outputs balanced differential analog signals TXI±, TXQ±

✍✍ Reception operation：Received analog I/Q baseband signal is demodulated into digital data and sent to MAC layer. Baseband spectrum occupies 0~11MHz, for any of the above modulation or data rate.

✍✍ Operating clock is provided by a 44MHz oscillator.

HFA3783：I/Q modulator/demodulator.

✍✍ Integrating all IF transmit and receive functions.
✍✍ Integrating IF transmission and reception AGC.
✍✍ Integrating a receiver DC offset calibration loop.

✍✍ Baseband I/Q signals are combined and converted to IF (Intermediate Frequency). IF center frequency is 374MHz, Bandwidth is 22MHz. IF signal are IF_TX± and IF_RX± and IF RX+. IF signals are sent to or from a SAW filter, and then up and down converted to RF by ISL3685. Baseband I/Q signals are TXI±, TXQ±, RXI± and RXQ±. Baseband I/Q signals are fed from or to the baseband processor, HFA3861B.

✍✍ An on chip frequency synthesizer cooperates with IF VCO is used to generate the 374MHz Local Oscillator frequency required by the up-down mixer. The 44MHz oscillator provides the reference frequency required by the frequency synthesizer.

✍✍**ISL3685**：RF to IF converter.

✍✍ A low noise, gain selectable amplifier (LNA) followed by a down-converter mixer is integrated.
✍✍ An up-converter mixer and a high performance preamplifier compose the transmit chain.
✍✍ Integrating a high frequency PLL synthesizer with a three wire programmable interface for LO applications.

✍✍ For receiver path, RF signal passes through a LNA with down-conversion mixer and then be converted to IF (374MHz) signal. For transmission path, signal from SAW filter is up converted to RF and amplified by preamplifier. The output is fed to MAX2242 power amplifier.

✍✍ An on chip frequency synthesizer is used to generate the Local Oscillator frequency, 2.038~2.110GHz, required by the mixer. An external VCO of 2.074GHz center frequency is used in the frequency synthesizer loop. The 44Mhz oscillator provides the reference frequency required by the frequency synthesizer.

✍✍**ISL3984**：power amplifier for transmission.

✍✍**T/R switch**：Transmission or reception multiplexing switch.

✍✍ Transmission/reception are half duplex.