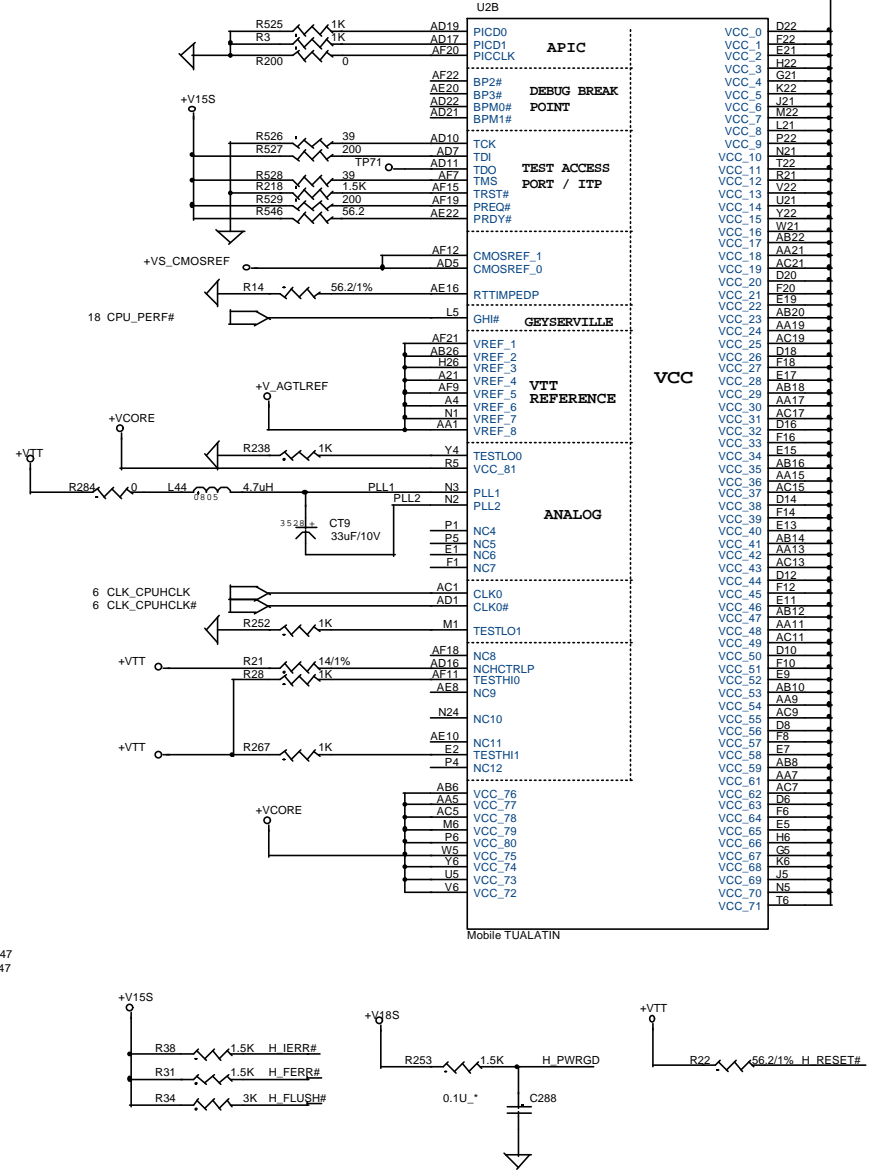
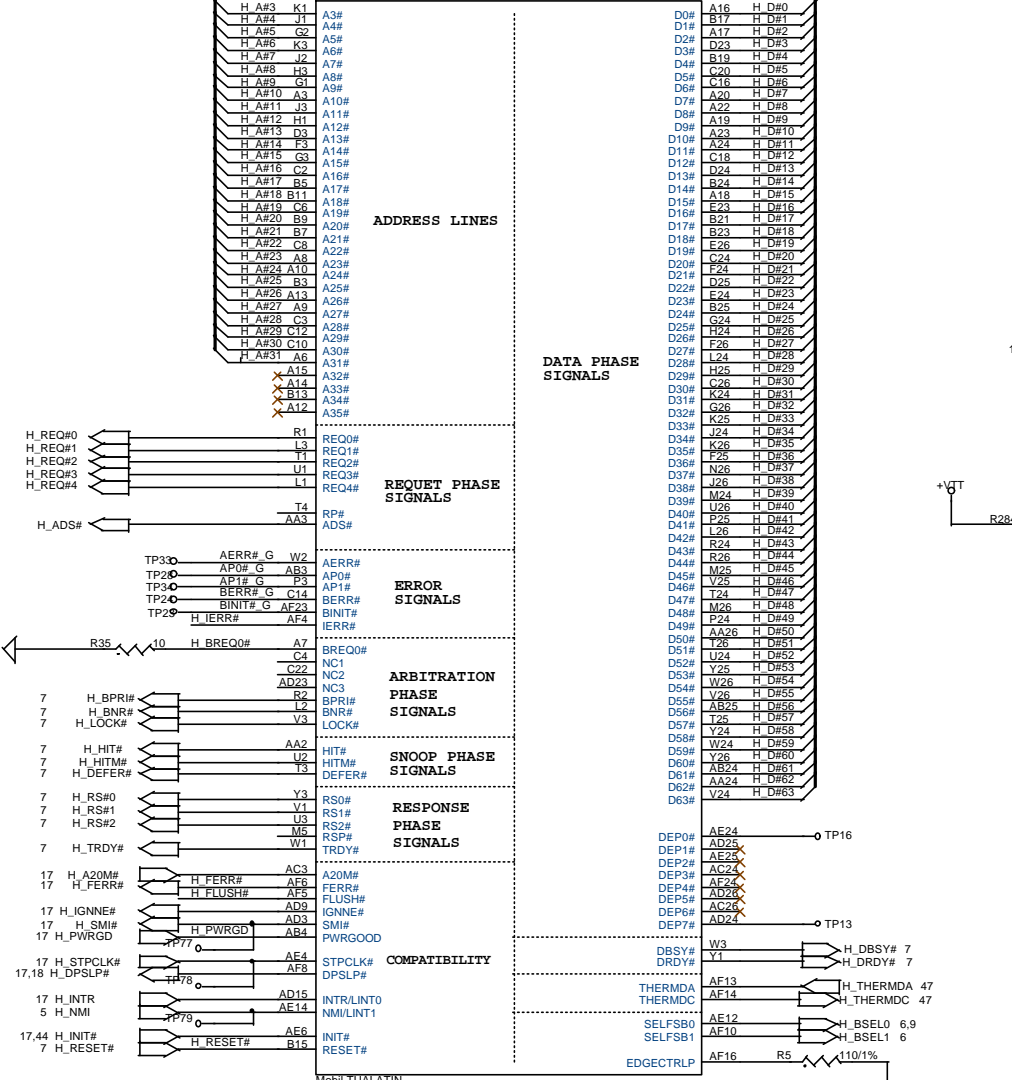
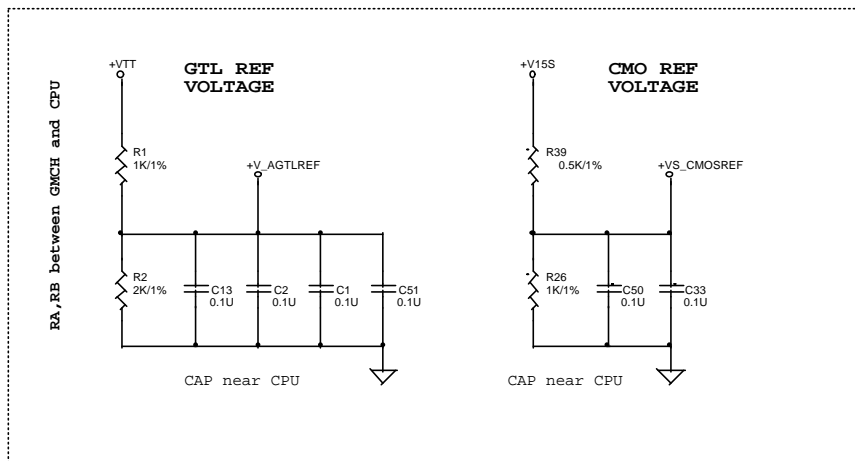
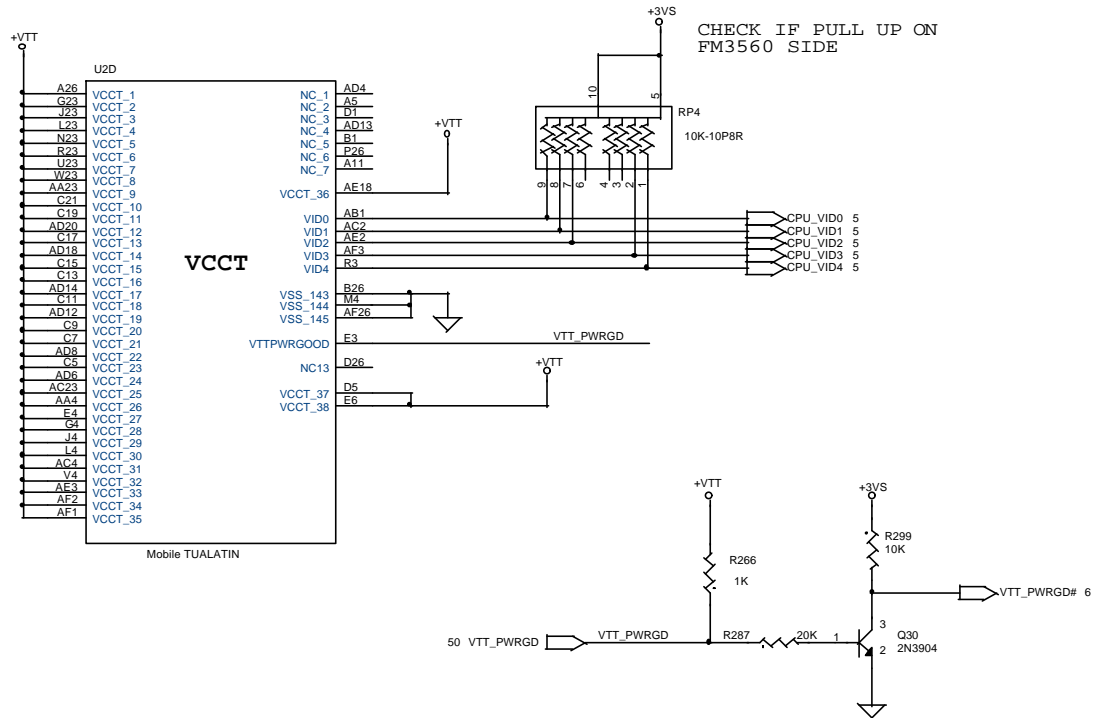
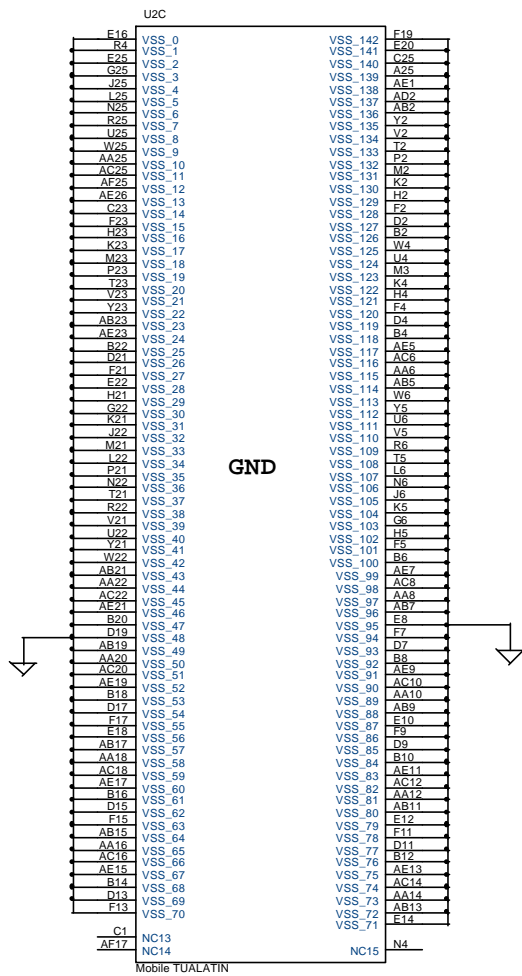
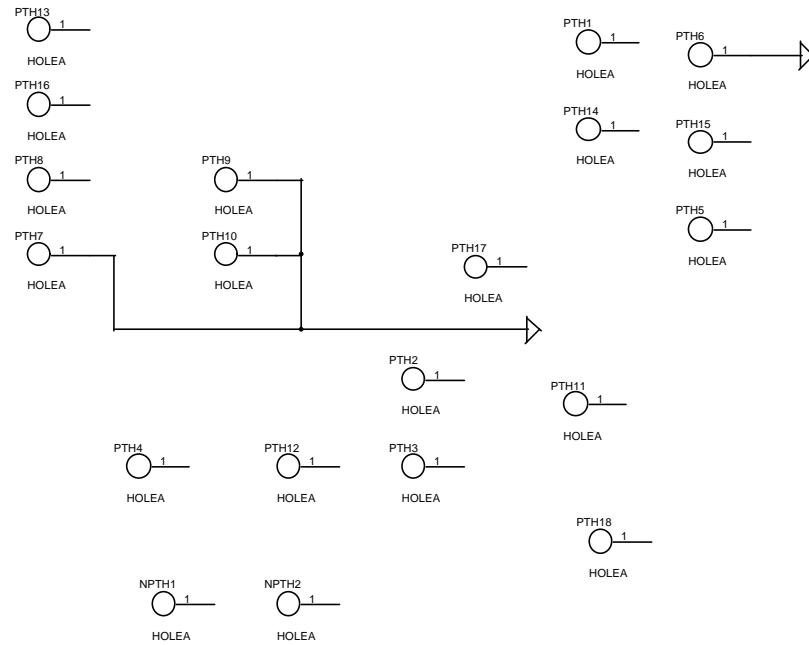
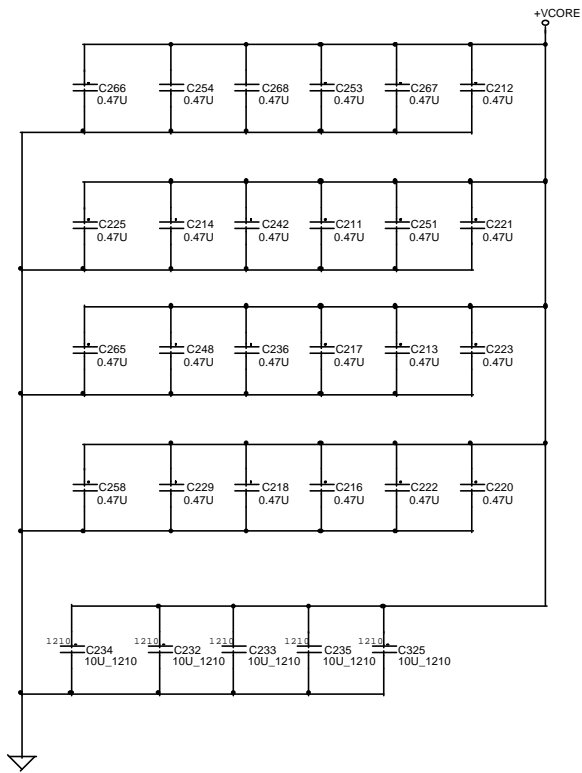
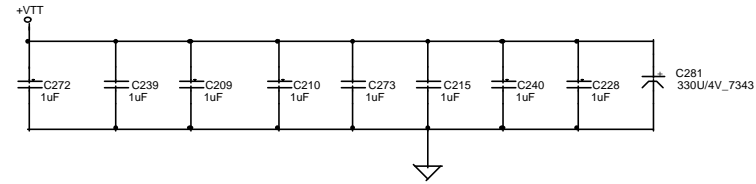
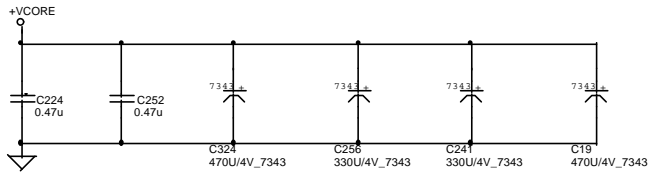
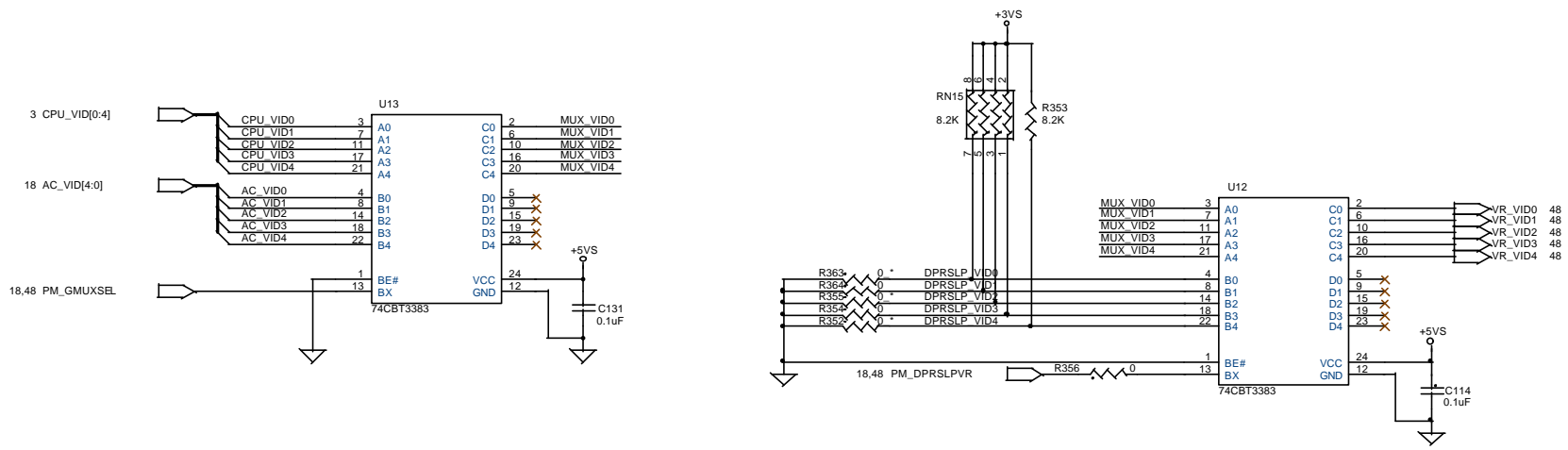


7 H_A#[3:31] ← H_A#[3:31] U2A H_D#[0:63] → H_D#[0:63] 7







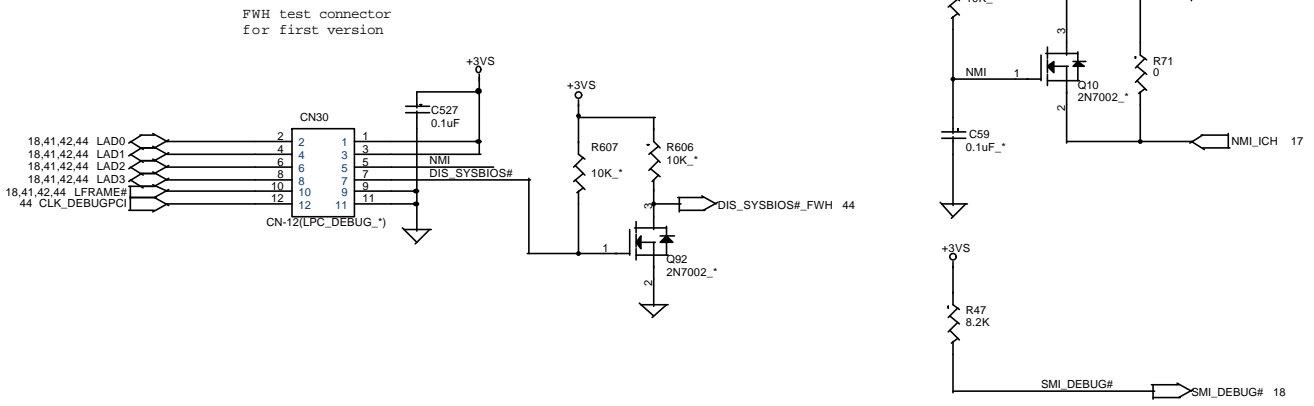


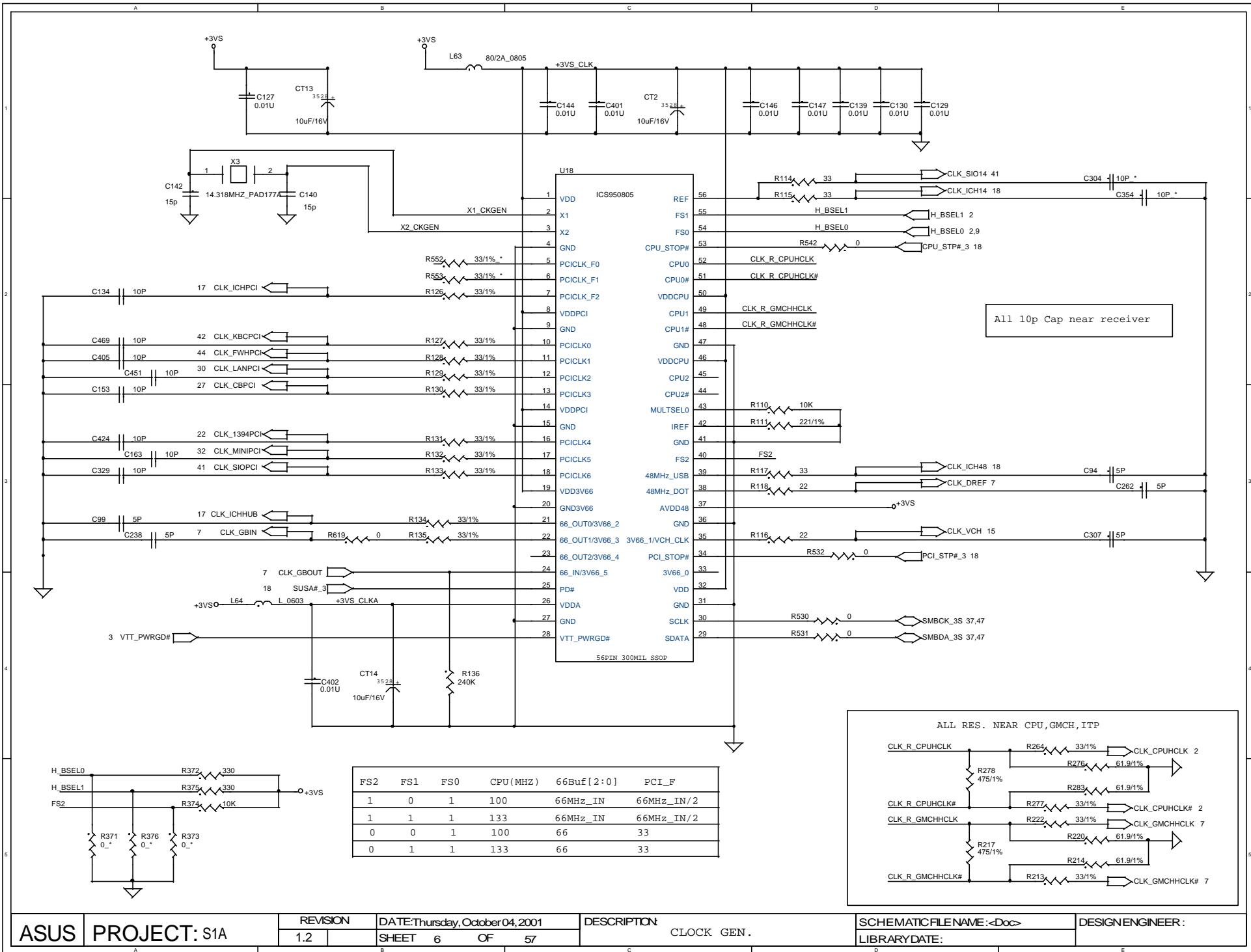
PM_GMUXSEL 0==> LOW VOLTAGE
 1==> HIGH VOLTAGE

PM_DPRSLPVR 1==>DEEPER SELLEEP MODE

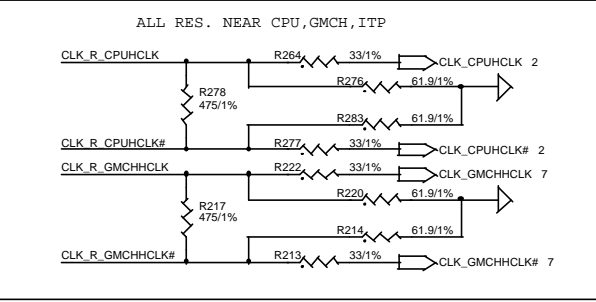
Mobile Tualatin VID values

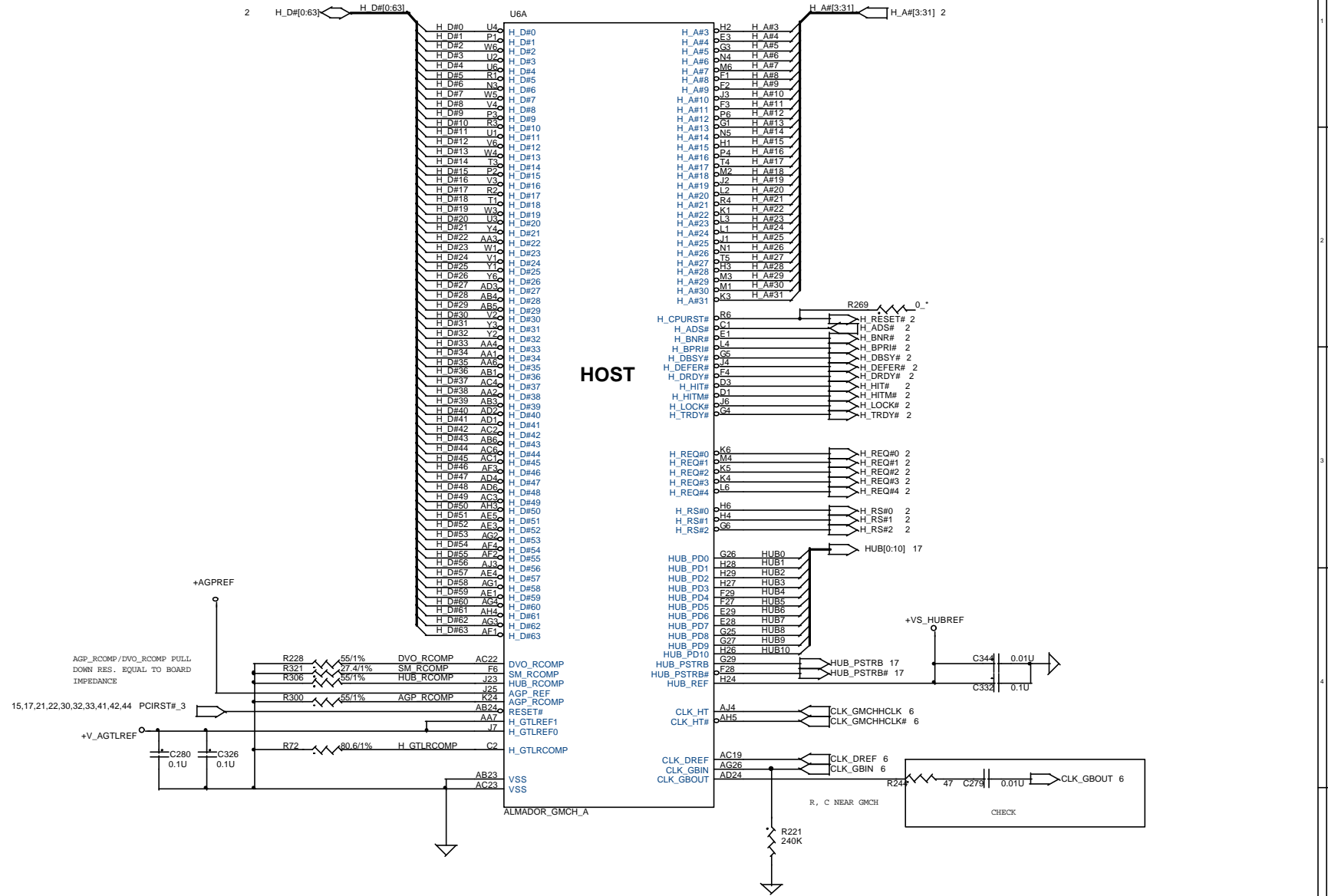
	VID0	VID1	VID2	VID3	VID4
1.30V	0	1	0	0	1
1.25V	0	1	0	1	0
1.20V	0	1	0	1	1
1.15V	0	1	1	0	0
1.10V	0	1	1	0	1
0.85V	1	0	1	0	1

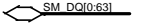
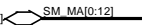


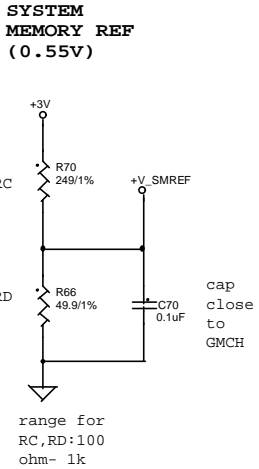
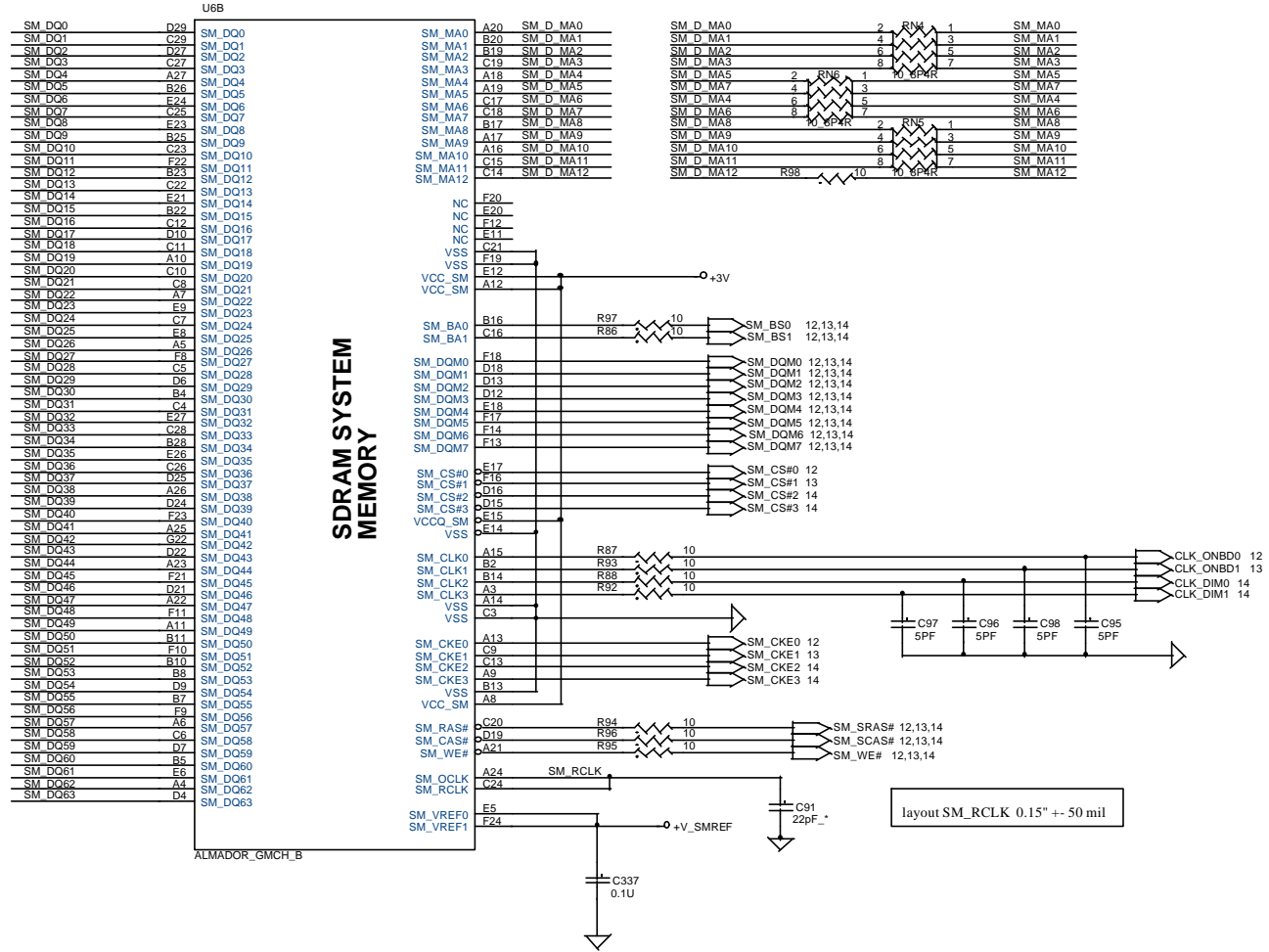


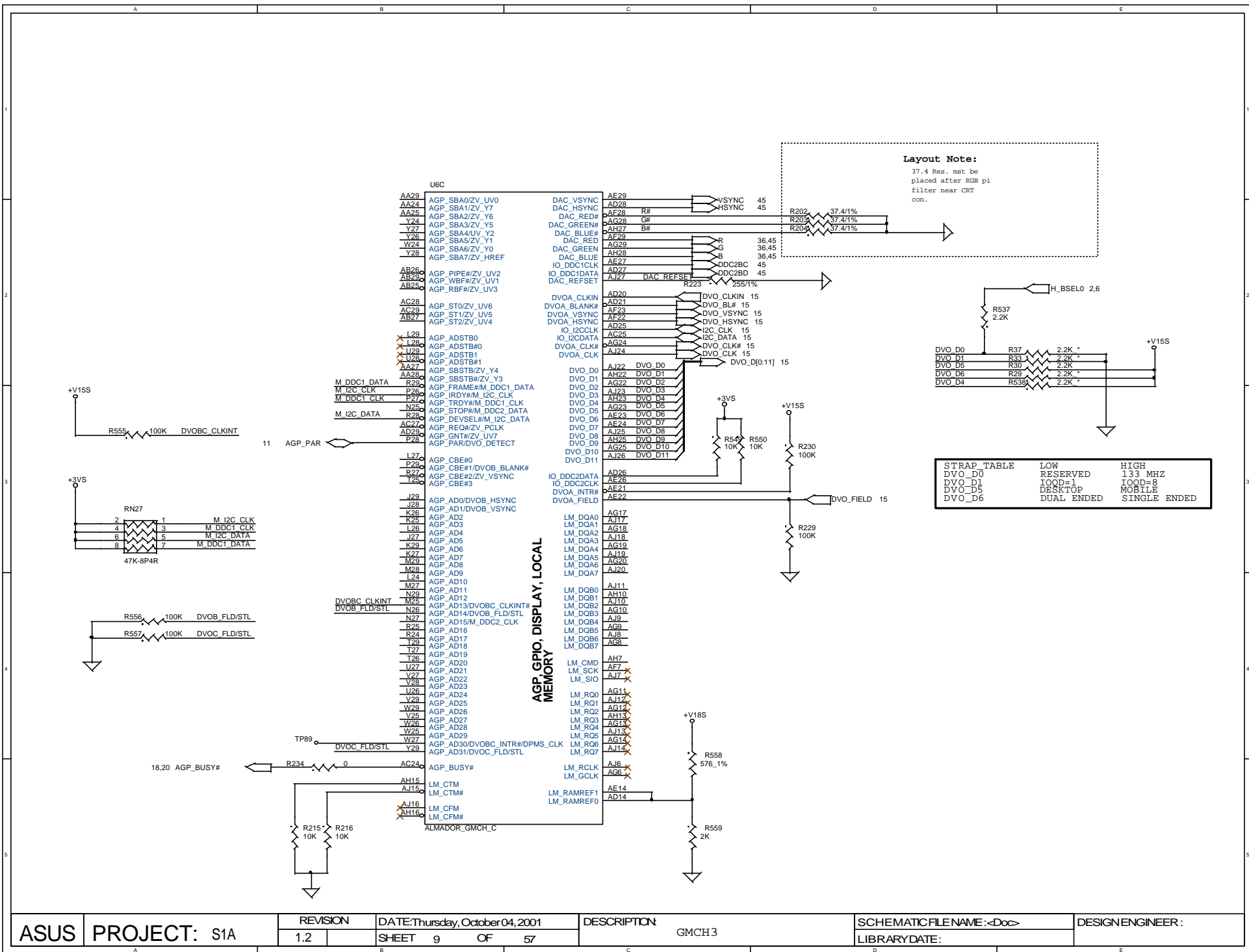
All 10p Cap near receiver

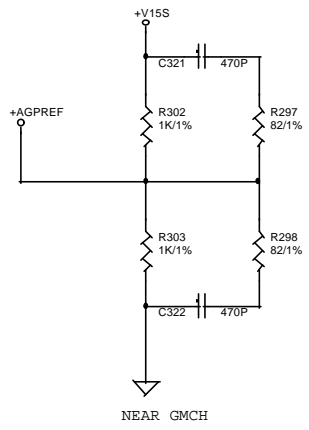
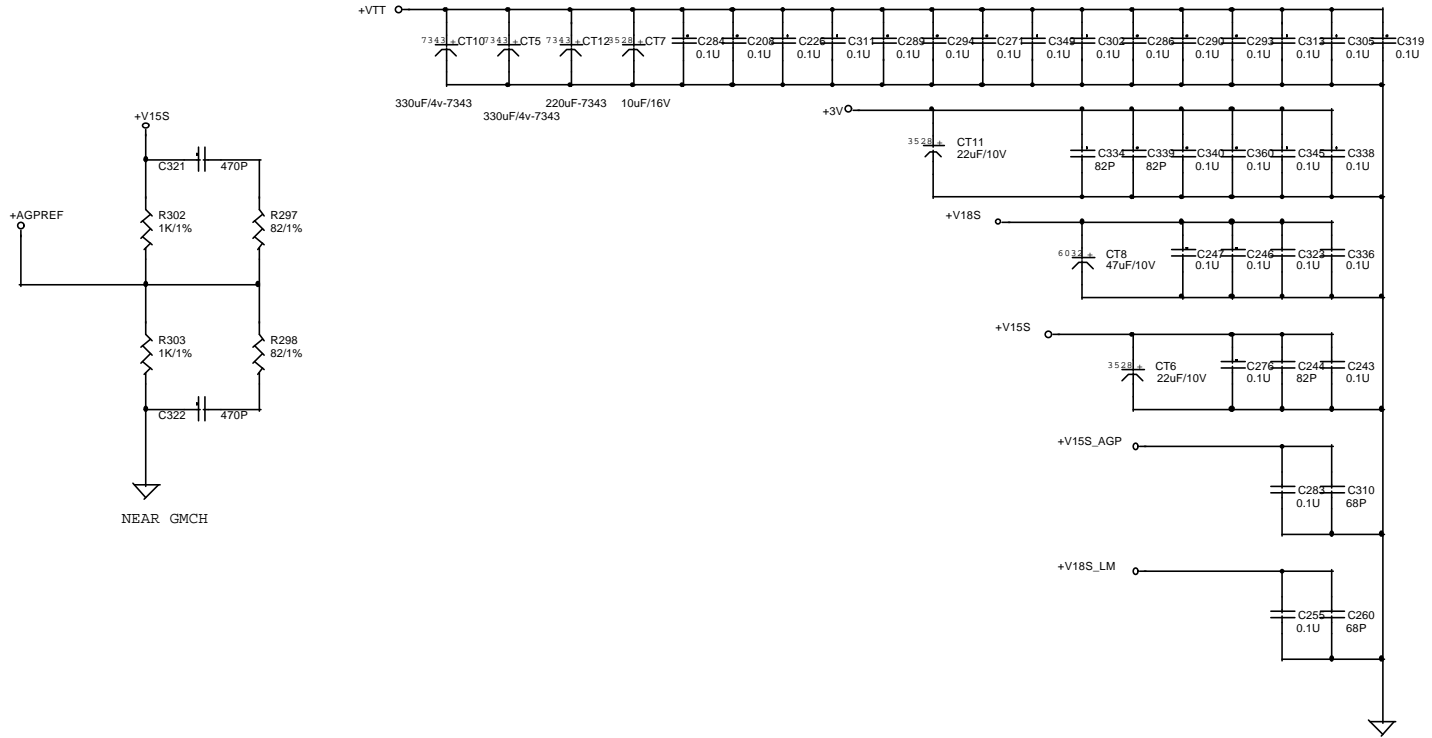




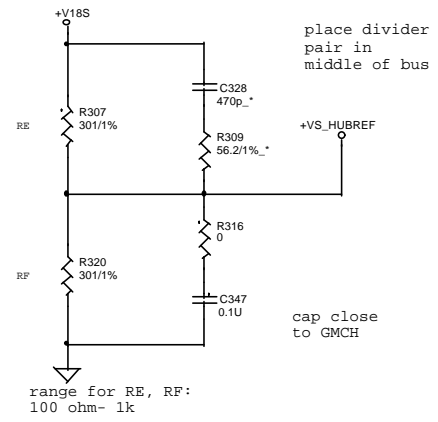
12.13.14 SM_DQ[0:63]  SM_DQ[0:63]
 12.13.14 SM_MA[0:12]  SM_MA[0:12]





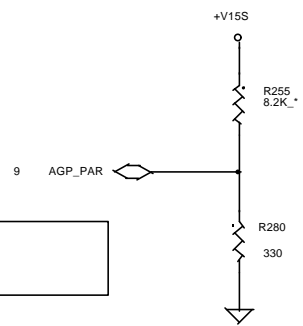


**HUB INT. REF.
(1/2 1.8V)**



range for RE, RF:
100 ohm- 1k

AGP_PAR
1 AGP
0 DVOB/C

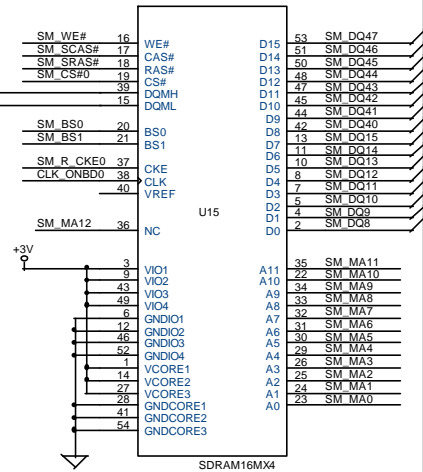
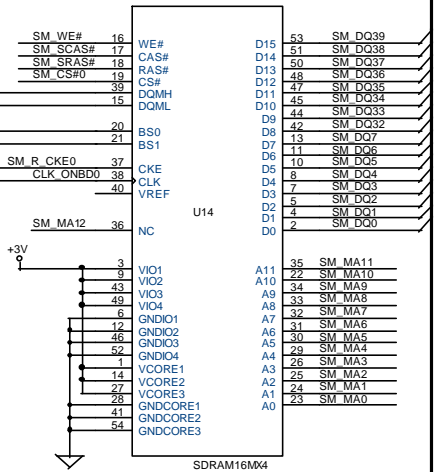


8,13,14 SM_DQM1
8,13,14 SM_DQM1

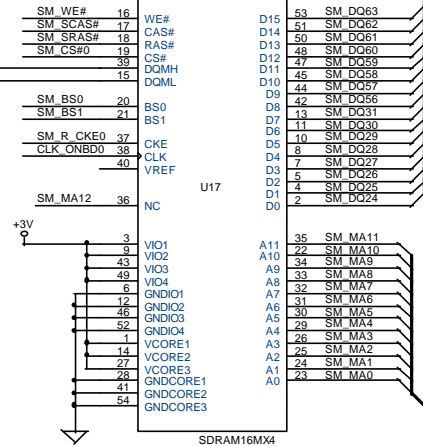
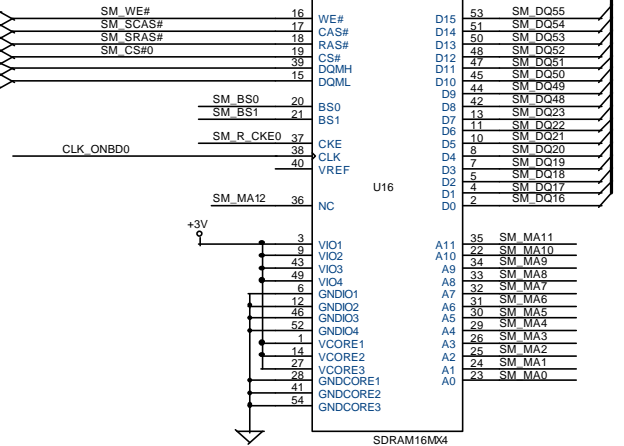
8,13,14 SM_DQM1
8,13,14 SM_DQM1

8,13,14 SM_BS0
8,13,14 SM_BS1

8 SM_CKE0
8 CLK_ONBD0



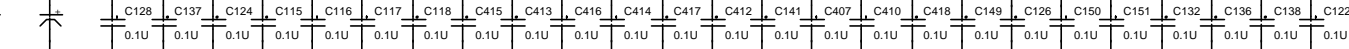
8,13,14 SM_WE#
8,13,14 SM_SCAS#
8,13,14 SM_SRAS#
8 SM_CS#0
8,13,14 SM_DQM6
8,13,14 SM_DQM2



8,13,14 SM_DQM1
8,13,14 SM_DQM1

+3V

C143
10U/16V_1210



C82
10U/16V_1210

SM_DQ[0:63]

SM_DQ[0:63] 8,13,14

SM_MAI0[12] SM_MAI[0:12] 8,13,14

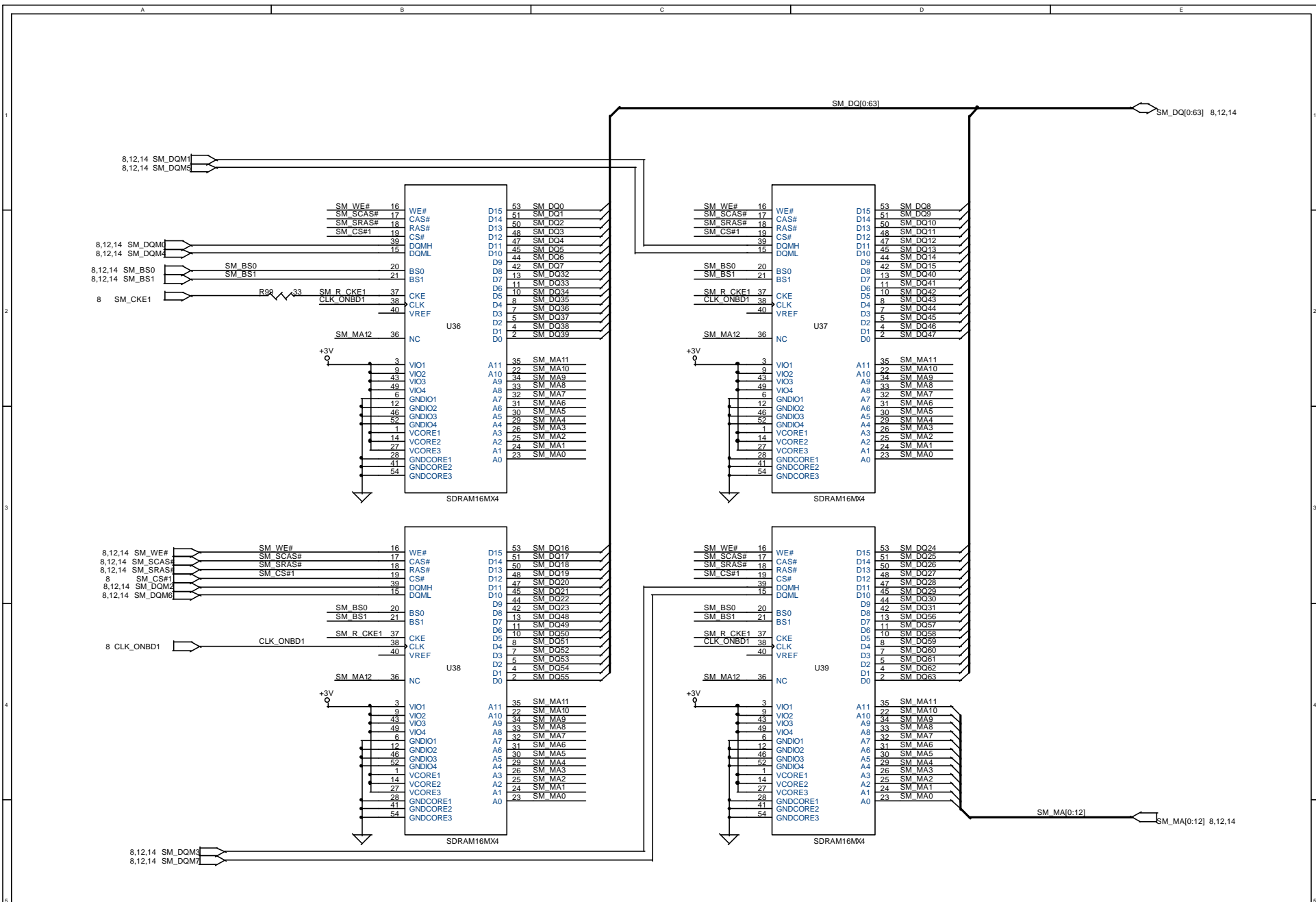
ASUS PROJECT: S1A

REVISION 1.2
DATE: Thursday, October 04, 2001
SHEET 12 OF 57

DESCRIPTION ON BOARD SDRAM

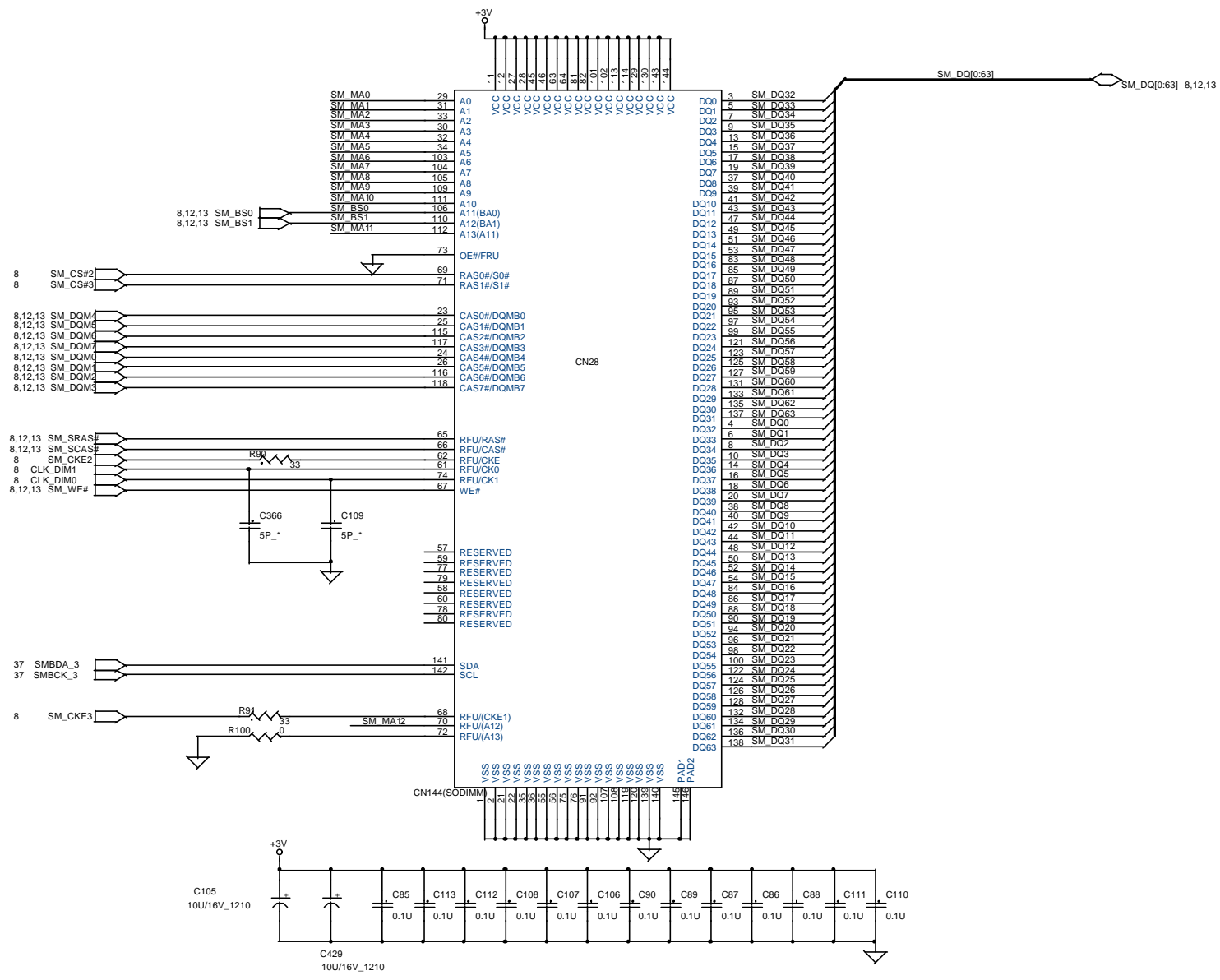
SCHEMATIC FILE NAME: <Doc>
LIBRARY DATE:

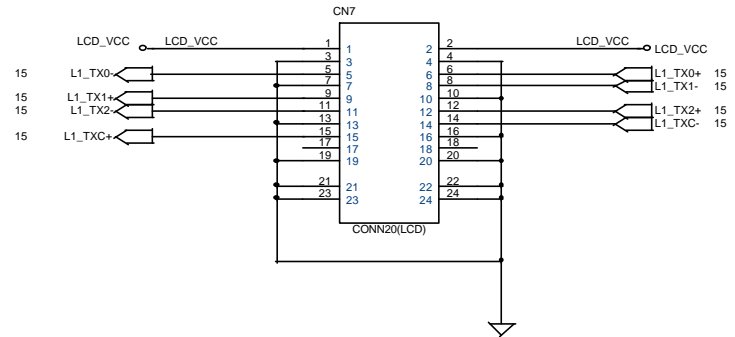
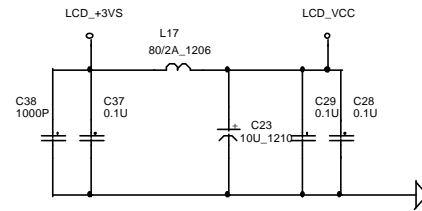
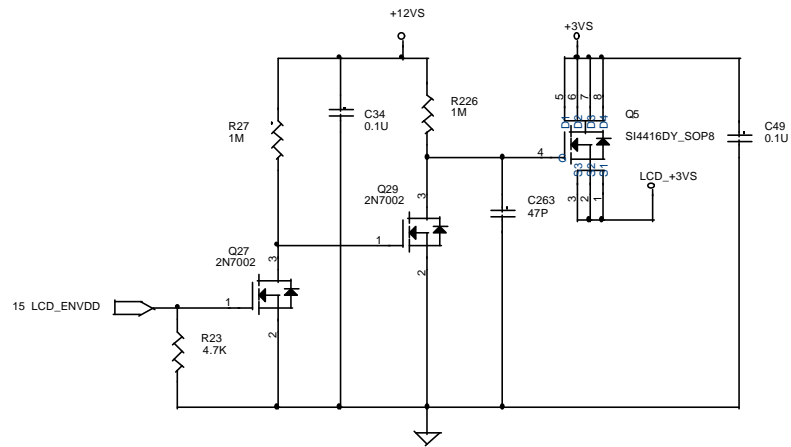
DESIGN ENGINEER:

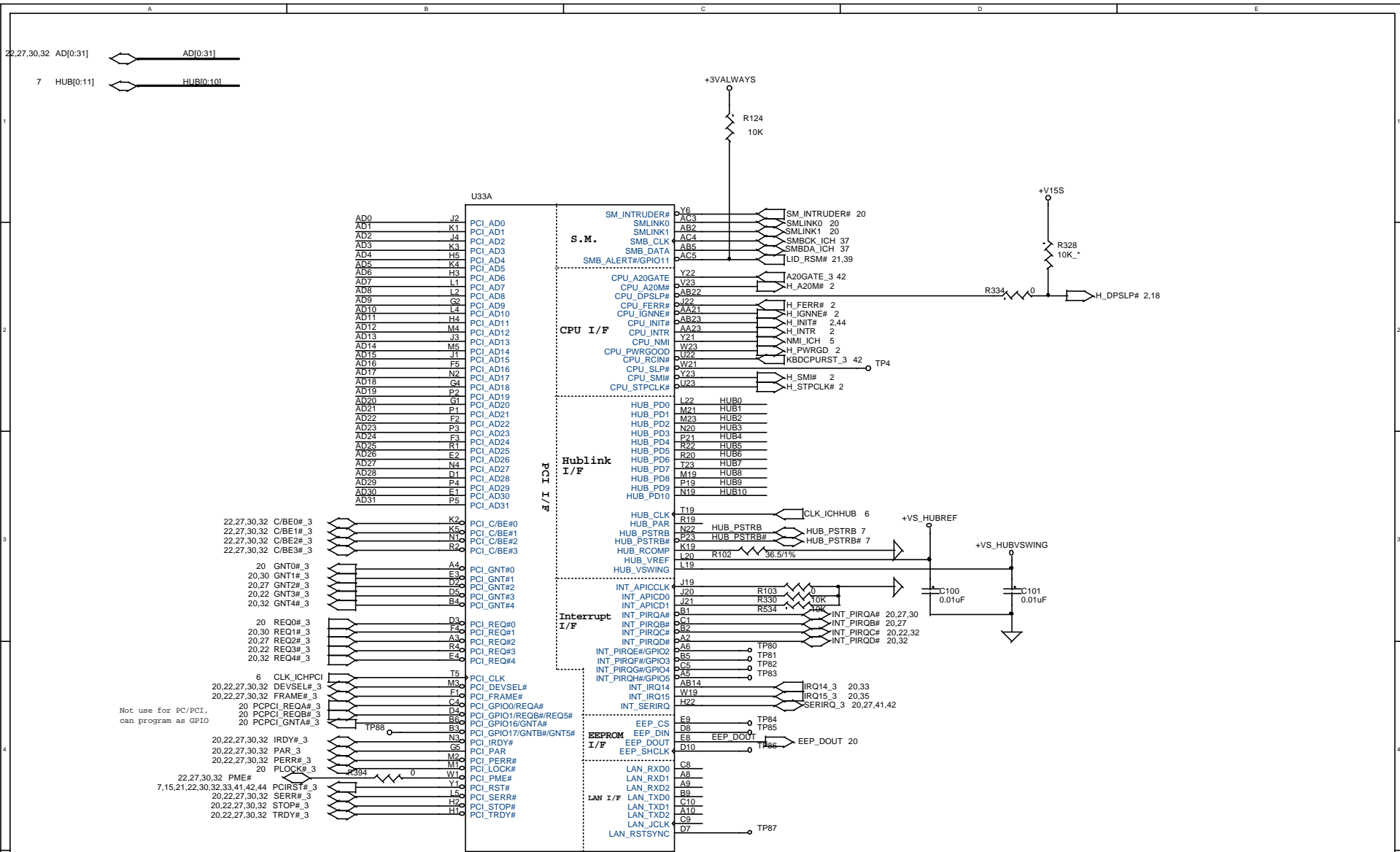


ASUS PROJECT: S1A	REVISION	DATE: Thursday, October 04, 2001	DESCRIPTION	SCHEMATIC FILE NAME: <Doc>	DESIGN ENGINEER:
	1.2	SHEET 13 OF 57	ON BOARD SDRAM2		

8,12,13 SM_MA[0:12] SM_MA[0:12]





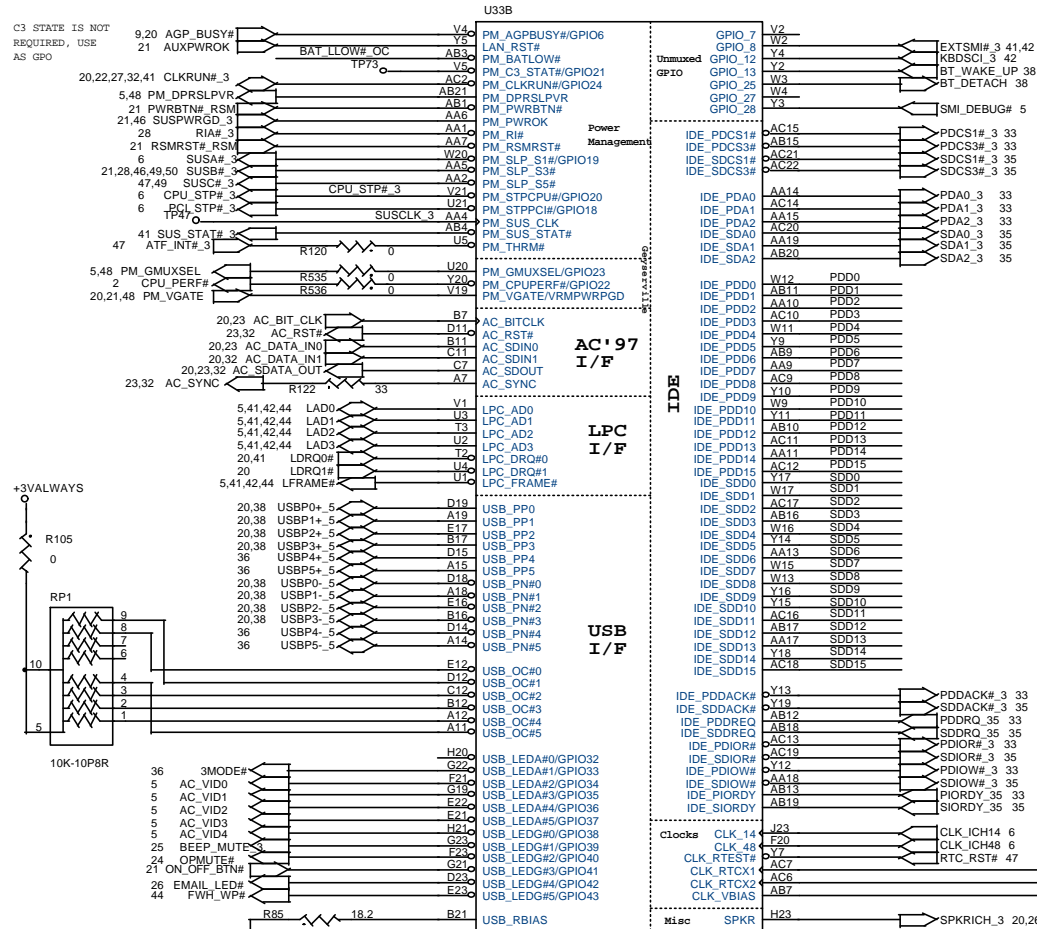


ICH3-M Part A

ASUS PROJECT: S1A	REVISION	DATE: Thursday, October 04, 2001	DESCRIPTION	SCHEMATIC FILE NAME: <Doc>	DESIGN ENGINEER:
	1.2	SHEET 17 OF 57	ICH2M 1	LIBRARY DATE:	

33 PDD[0:15] PDD[0:15]
 35 SDD[0:15] SDD[0:15]

24.51 BAT_LLOW#_OC R613 0_ BAT_LLOW#_OC_ICH 20



GPIO7 Fixed as input
 only, chk BIOS if need to
 change to another GPIO
 for KBDSCL

+3VALWAYS

R105

0

RP1

9

8

7

6

5

4

3

2

1

10K-10P8R

36

3MODE#

5 AC_VID0

5 AC_VID1

5 AC_VID2

5 AC_VID3

5 AC_VID4

25 BEEP_MUTE#

24 ON_OFF_BTN#

26 EMAIL_LED#

44 FWLH_WP#

R85

18.2

B21

ICH3-M Part B

CPU_STP# 3

R329

0

2,17 H_DPSLP#

R335

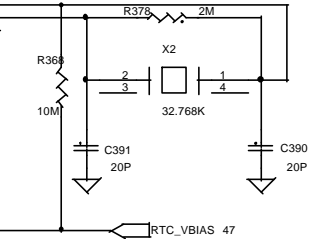
33.2K/1%

PM_DPSLP_PWR# 48

H23

SPKRICH_3 20,26

RTC_VBIAS 47



ASUS PROJECT: S1A

REVISION

1.2

DATE: Thursday, October 04, 2001

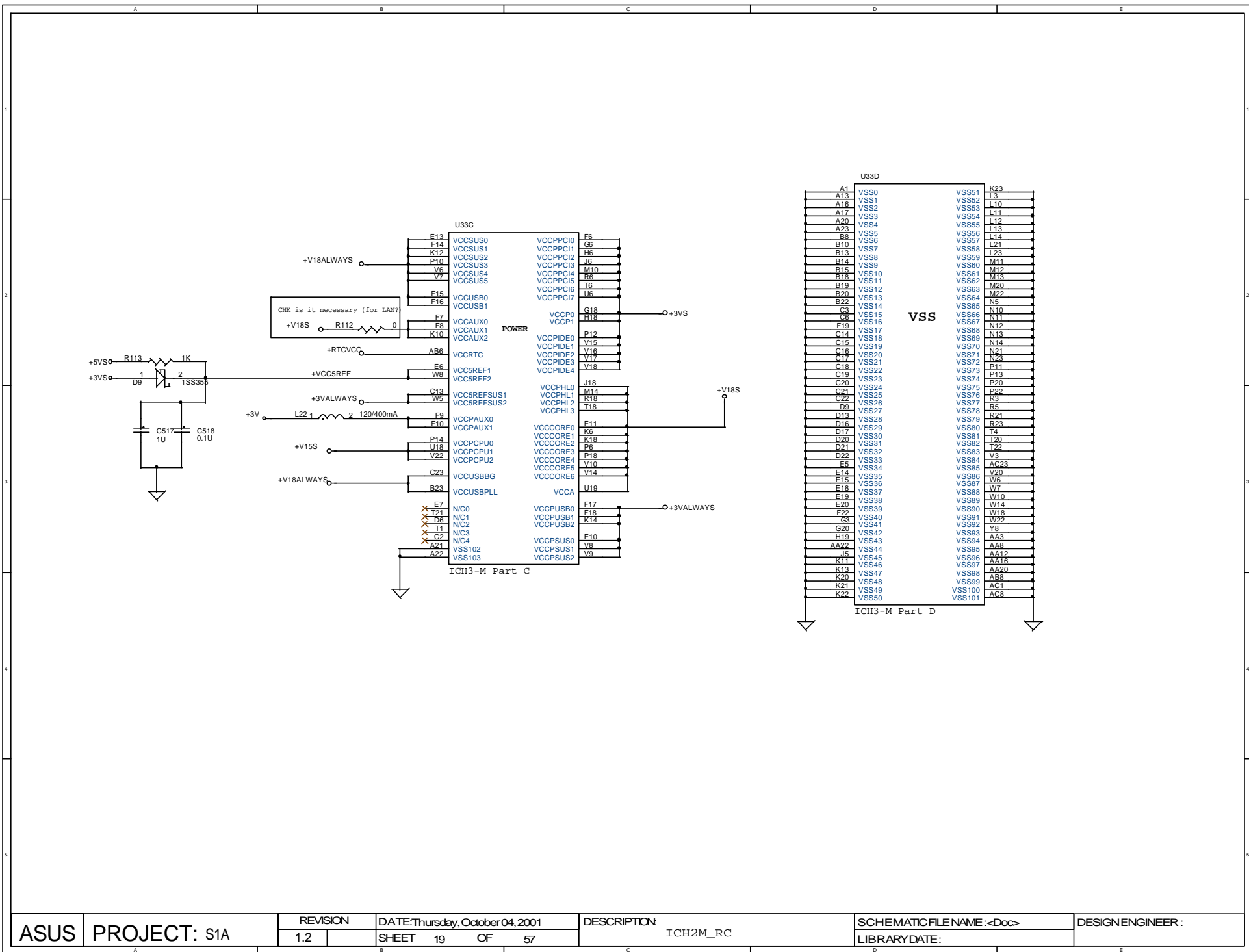
SHEET 18 OF 57

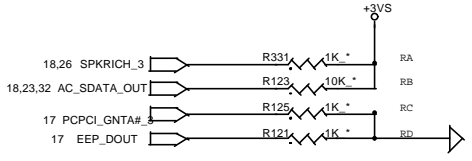
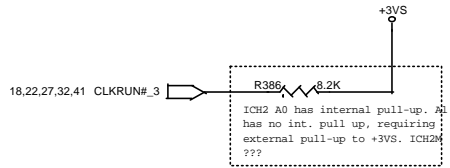
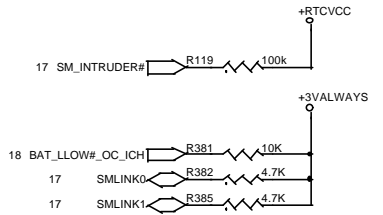
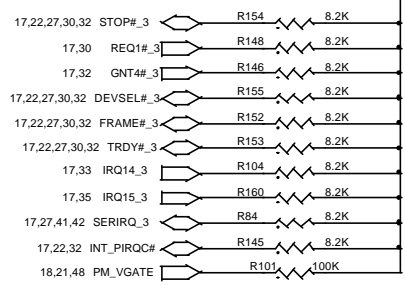
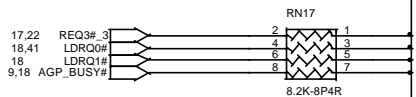
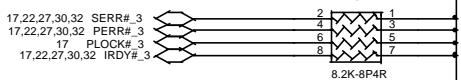
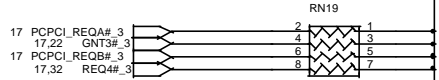
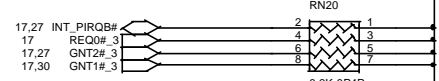
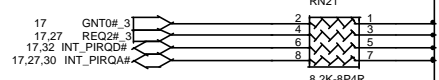
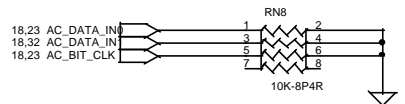
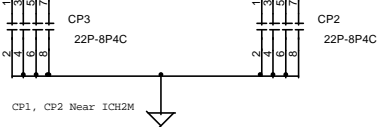
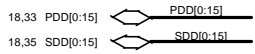
DESCRIPTION

SCHEMATIC FILE NAME: <Doc>

LIBRARY DATE:

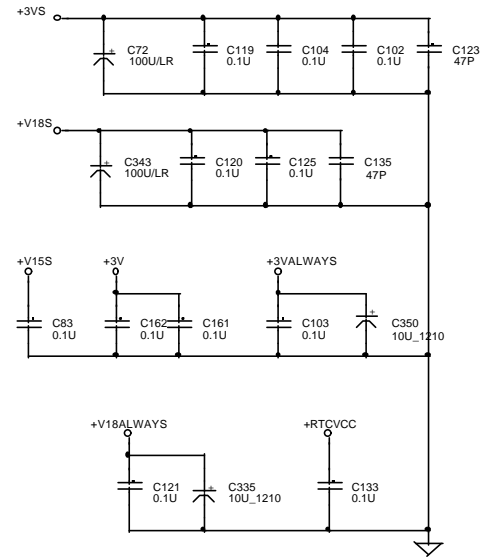
DESIGN ENGINEER:



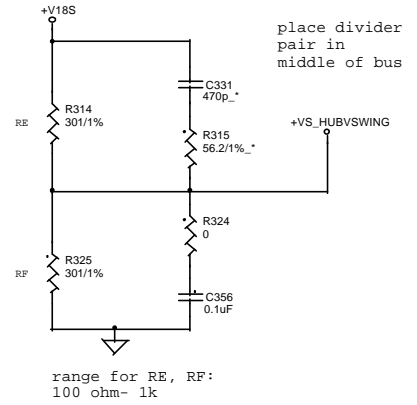


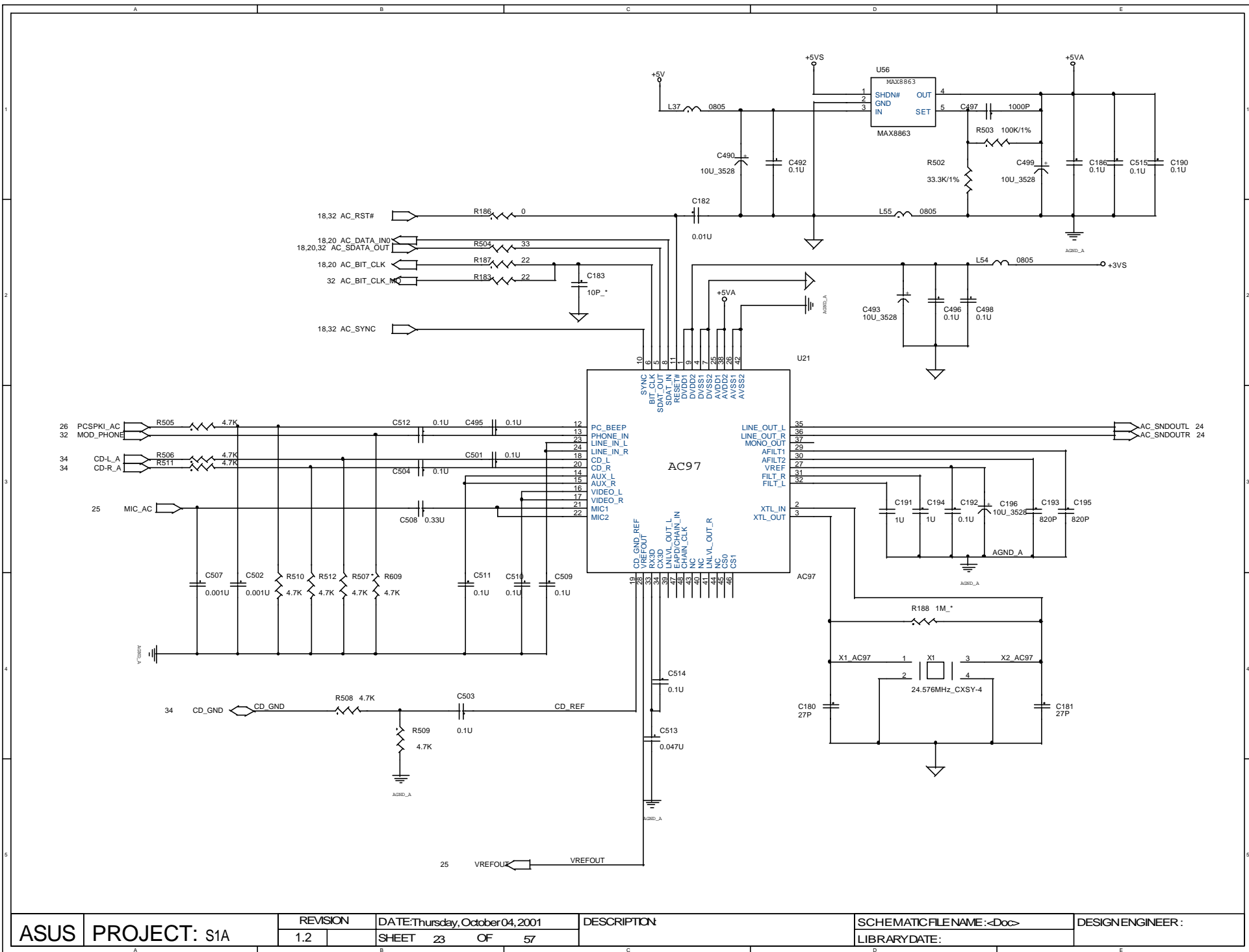
ICH3M STRAPPING OPTIONS

Function	Default	Optional Override
RA	No Reboot	No Stuff
RB	Safe Mode Boot	Stuff for safe mode
RC	Al6 swap override	Stuff for Al6 swap override
RD	Reserved	No Stuff

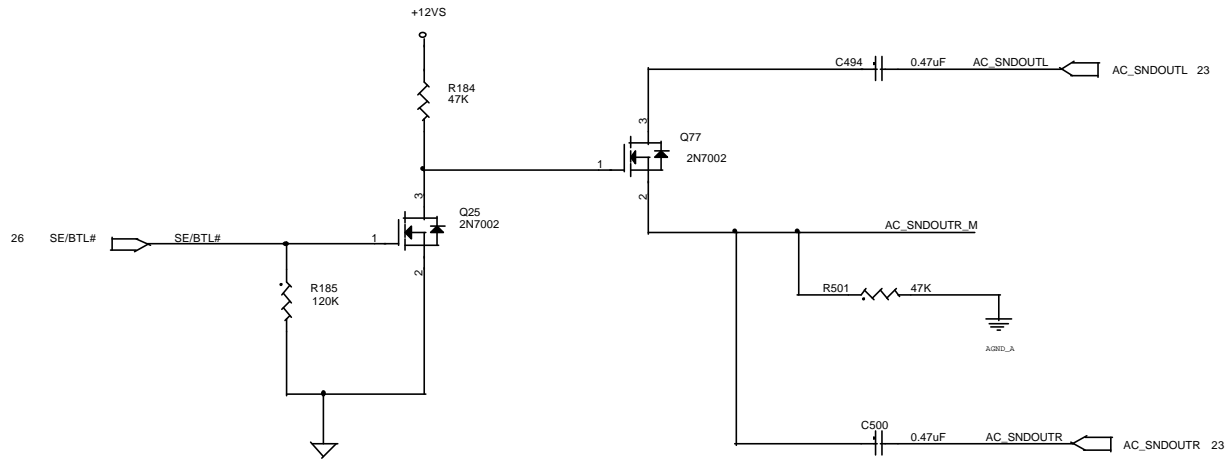
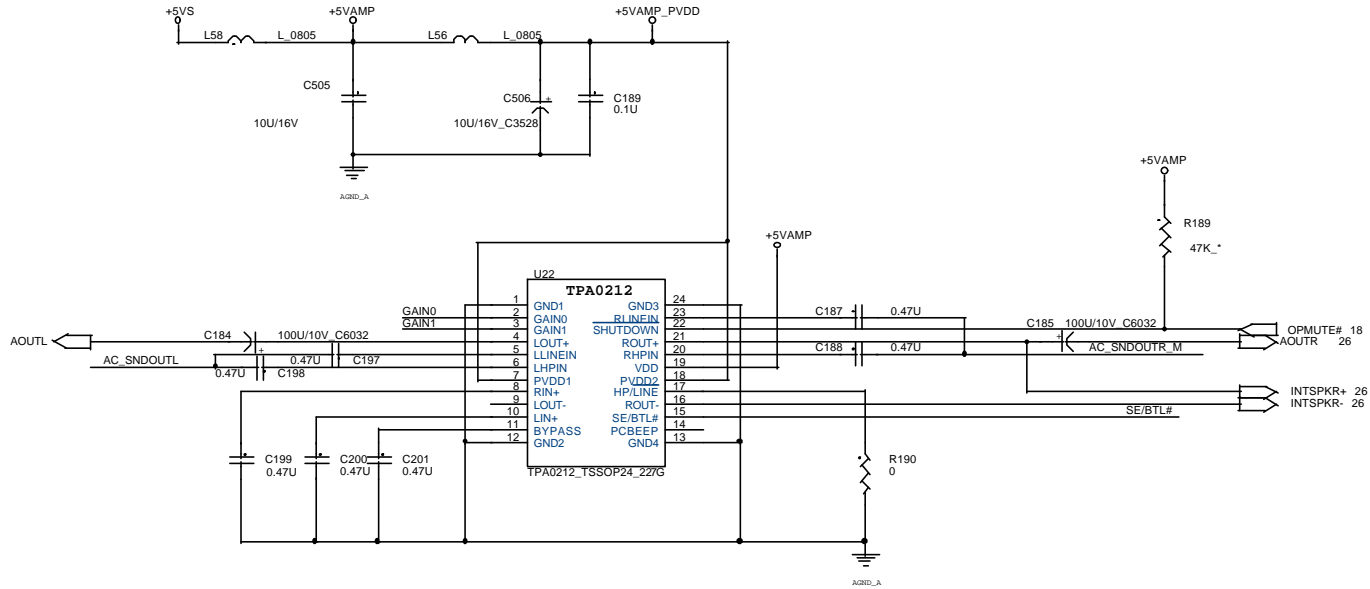
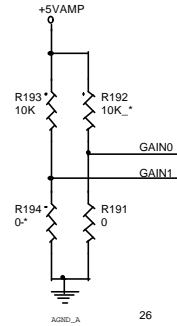


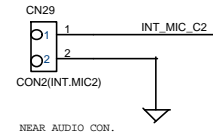
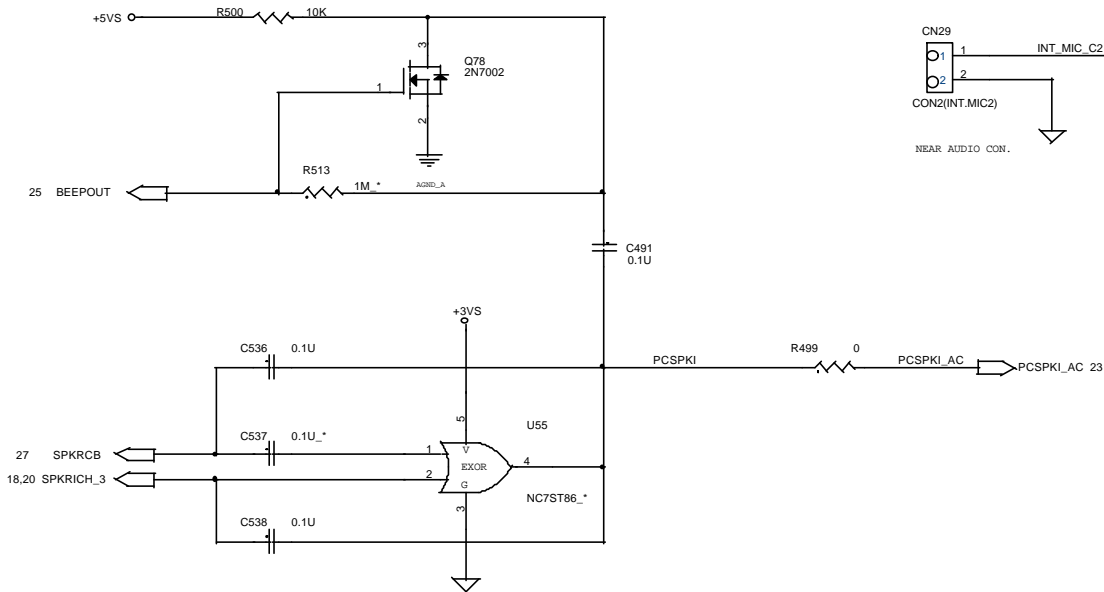
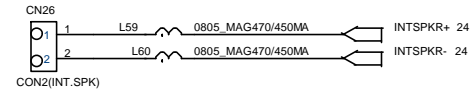
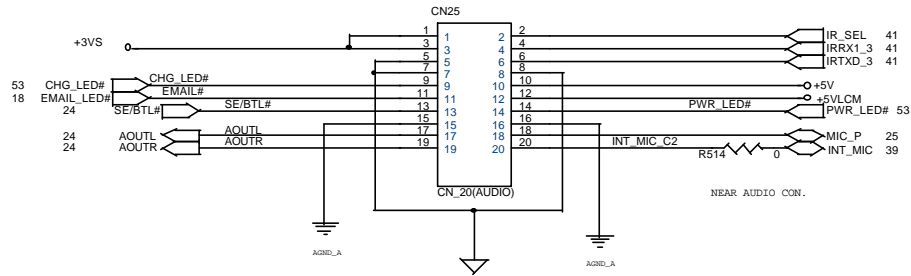
HUB INT. VSWING VOLTAGE (1/2 1.8V)

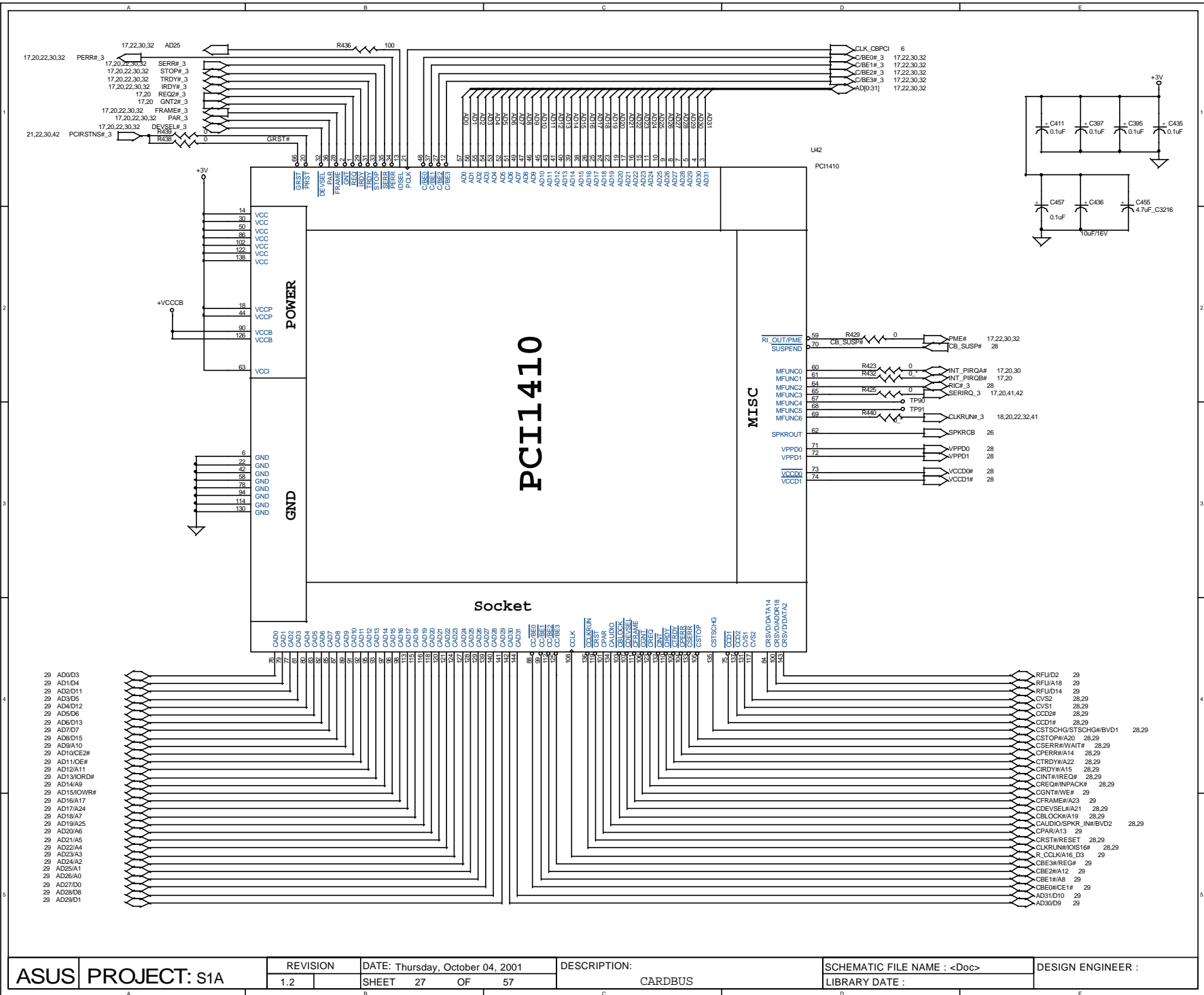




GAIN0	GAIN1	SE/BTL#	AV (V/V)
0	0	0	-2
0	1	0	-6
1	0	0	-12
1	1	0	-24
X	X	1	-1







ASUS PROJECT: S1A

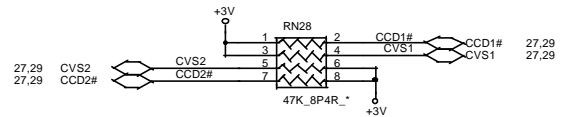
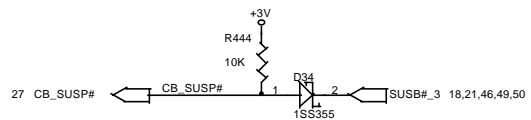
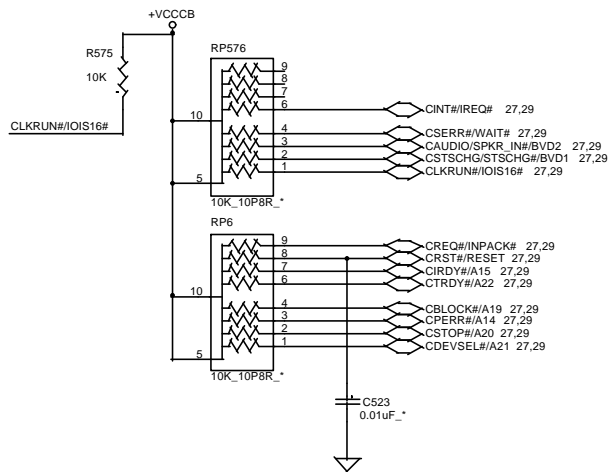
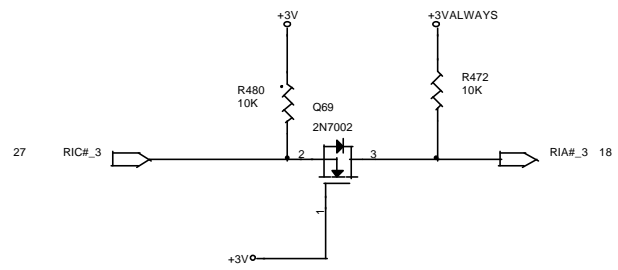
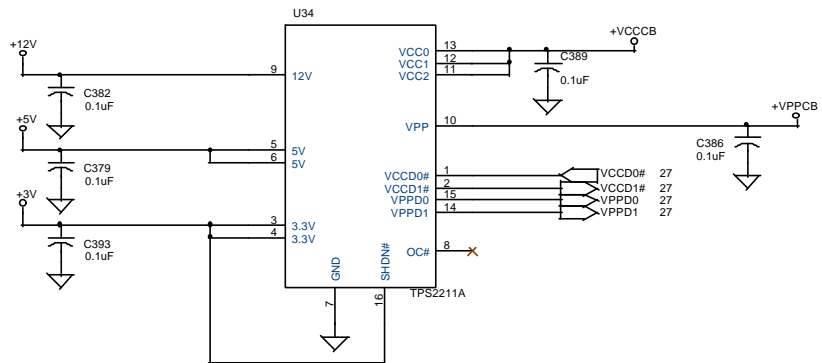
REVISION
1.2

DATE: Thursday, October 04, 2001
SHEET 27 OF 57

DESCRIPTION:
CARDBUS

SCHEMATIC FILE NAME : <Doc>
LIBRARY DATE :

DESIGN ENGINEER :



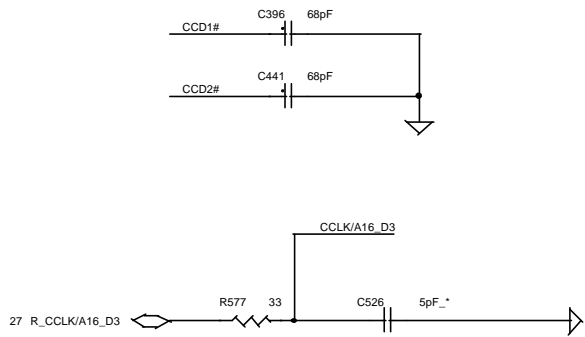
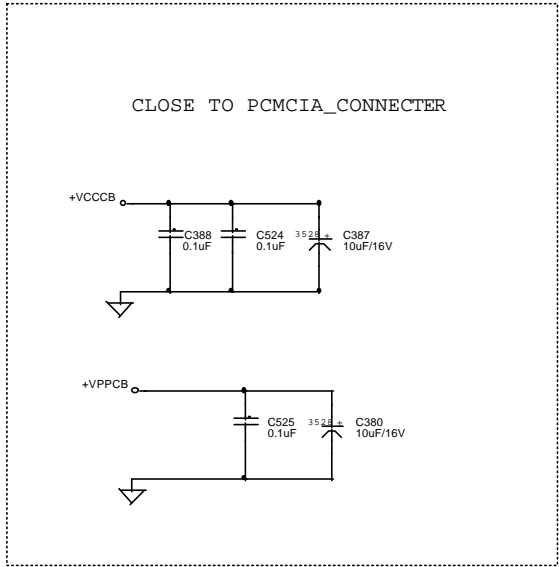
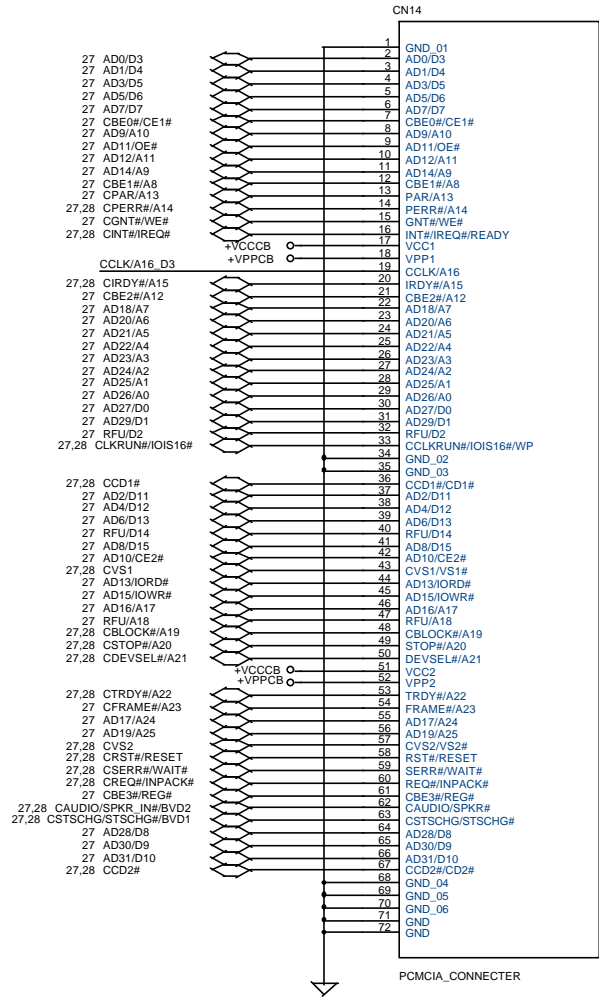
ASUS PROJECT: S1A

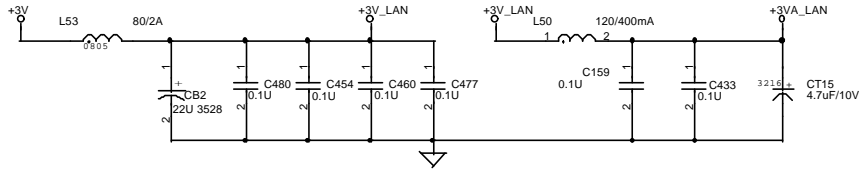
REVISION 1.2 DATE: Thursday, October 04, 2001 SHEET 28 OF 57

DESCRIPTION CARDBUS POWER SW.

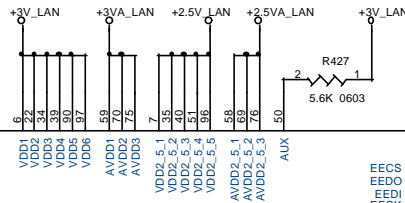
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DESIGN ENGINEER:



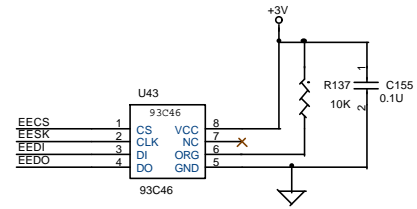


17.22.27.32 AD[0:31] AD[0:31]



AD0	45	AD0	45
AD1	44	AD1	44
AD2	42	AD2	42
AD3	41	AD3	41
AD4	39	AD4	39
AD5	37	AD5	37
AD6	36	AD6	36
AD7	33	AD7	33
AD8	30	AD8	30
AD9	29	AD9	29
AD10	28	AD10	28
AD11	27	AD11	27
AD12	26	AD12	26
AD13	25	AD13	25
AD14	24	AD14	24
AD15	23	AD15	23
AD16	10	AD16	10
AD17	9	AD17	9
AD18	8	AD18	8
AD19	5	AD19	5
AD20	4	AD20	4
AD21	3	AD21	3
AD22	1	AD22	1
AD23	100	AD23	100
AD24	95	AD24	95
AD25	94	AD25	94
AD26	93	AD26	93
AD27	92	AD27	92
AD28	91	AD28	91
AD29	89	AD29	89
AD30	87	AD30	87
AD31	86	AD31	86

RTL8100(L)



EECS	49	EECS	49
EEDO	46	EEDO	46
EEDI	47	EEDI	47
EESK	48	EESK	48

TXD+	72	TDP	31
TXD-	71	TDN	31
RXIN+	68	RDP	31
RXIN-	67	RDN	31

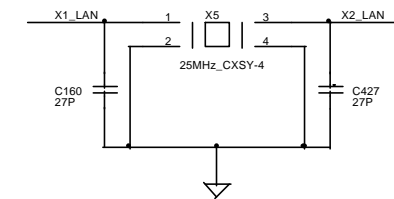
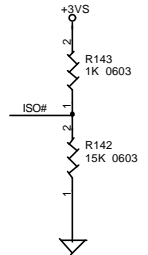
VCTRL	55	VCTRL	TP6
RTT3	63		
RTSET	65	RTSET	1

X1	61	X1 LAN	
X2	60	X2 LAN	

PME#	57	ISO#	17.22.27.32
ISOLATE#	74		
LWAKE	64		

LED0	80	TX/RX_LED#	31
LED1	79	LINK100_LED#	31
LED2	77		

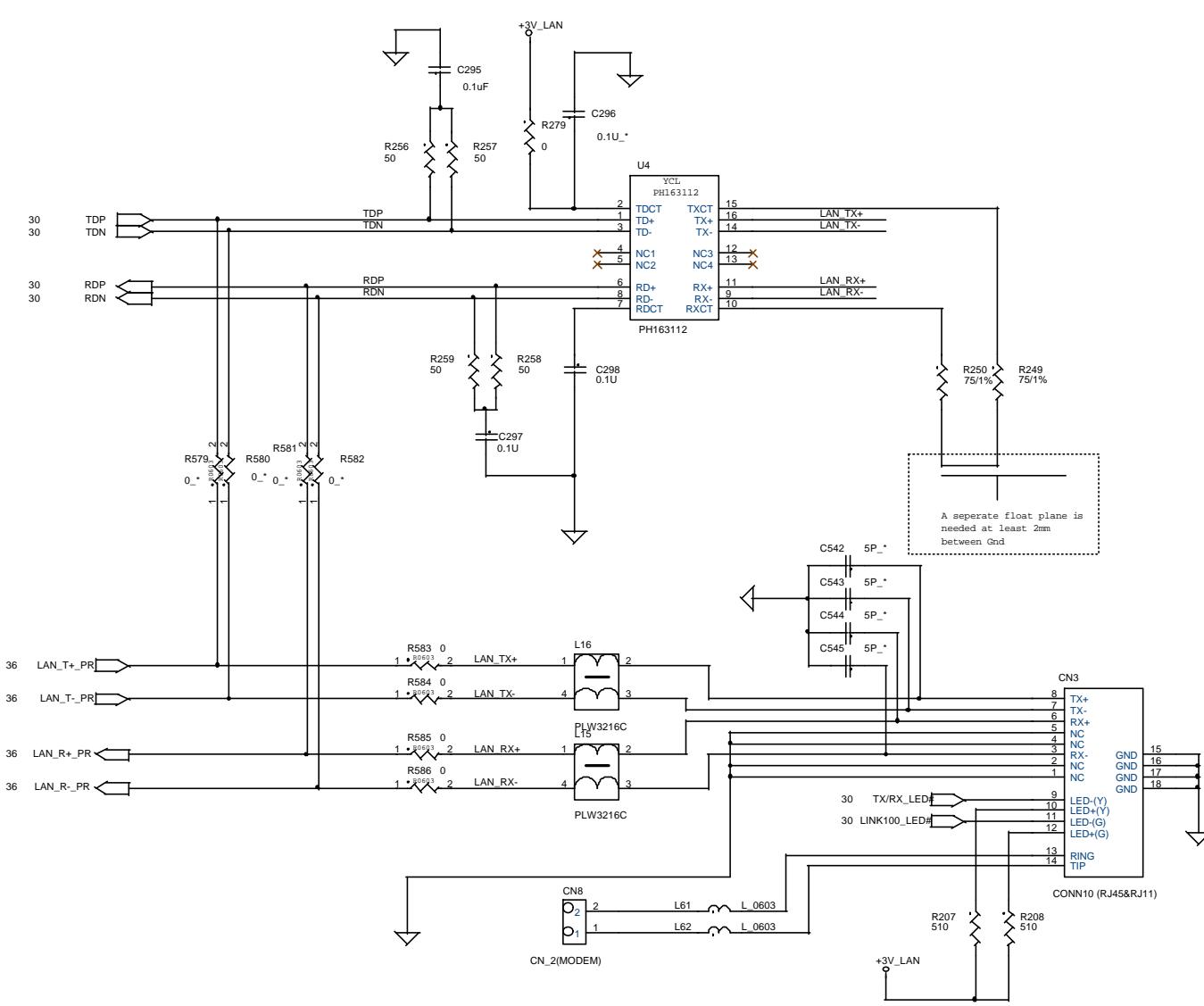
NC1	52		
NC2	53		
NC3	54		
NC4	78		




17.22.27.32	C/BE0#	3	32	C/BE0#	32
17.22.27.32	C/BE1#	3	21	C/BE1#	21
17.22.27.32	C/BE2#	3	11	C/BE2#	11
17.22.27.32	C/BE3#	3	98	C/BE3#	98

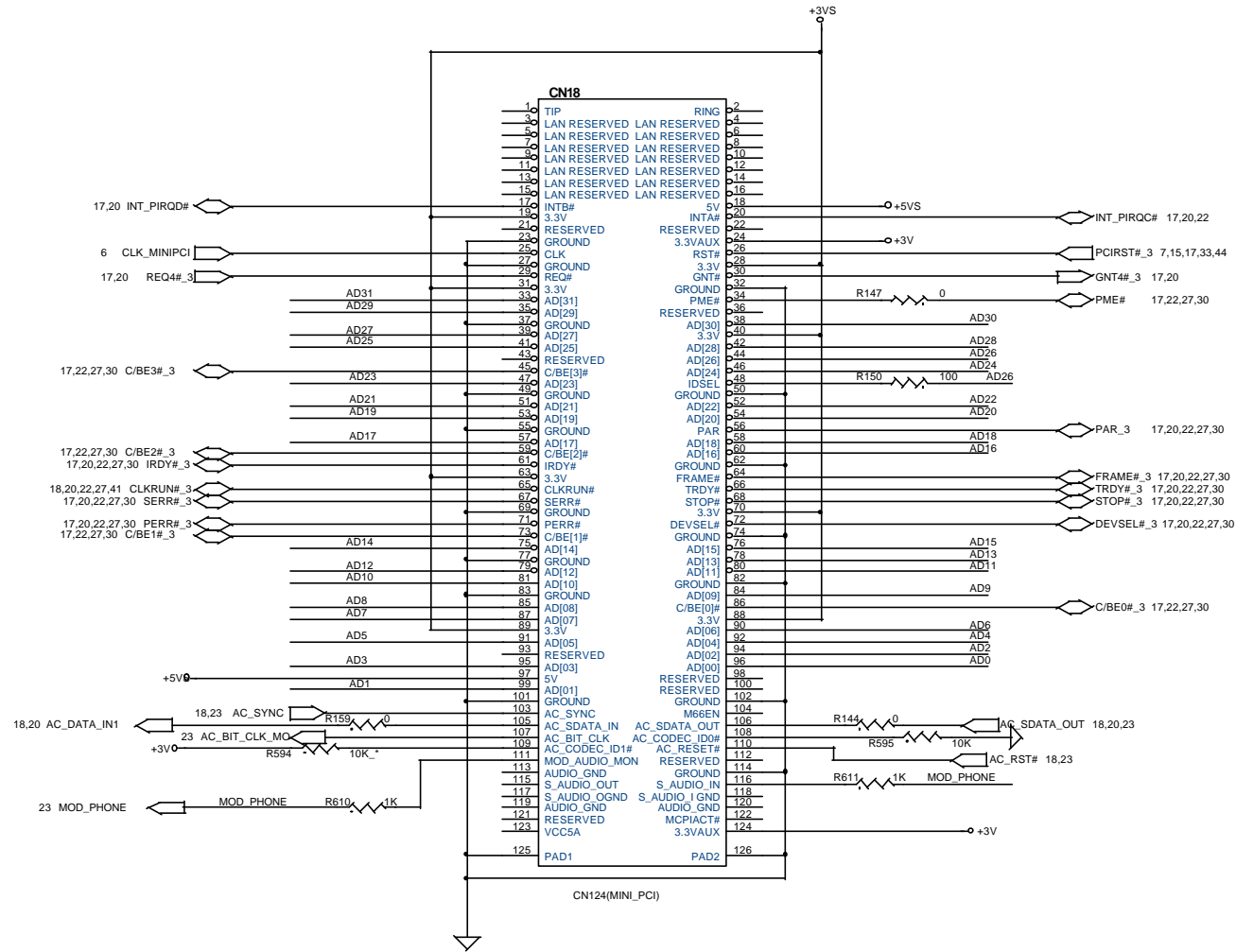
6	CLK_LANPCI		83	CLK	83
17.20.22.27.32	DEVSEL#	3	15	DEVSEL#	15
17.20.22.27.32	FRAME#	3	12	FRAME#	12
17.20	GNT1#	3	84	GNT#	84
AD28	REQ1#	3	85	REQ#	85
17.20	INT_PIRQA#		81	IDSEL	81
17.20.22.27.32	IRDY#	3	13	INTA#	13
17.20.22.27.32	TRDY#	3	14	IRDY#	14
17.20.22.27.32	PAR	3	20	TRDY#	14
17.20.22.27.32	PERR#	3	18	PAR	20
17.20.22.27.32	SERR#	3	19	PERR#	18
17.20.22.27.32	STOP#	3	17	SERR#	19
			82	STOP#	17

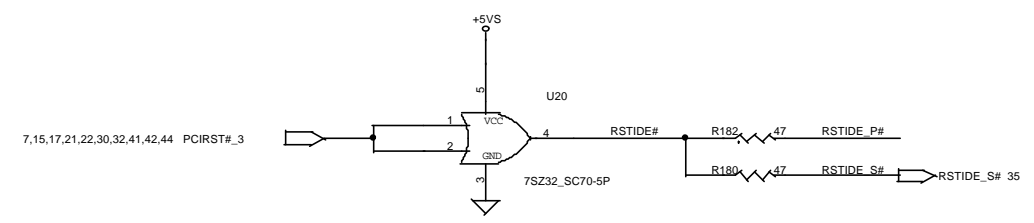
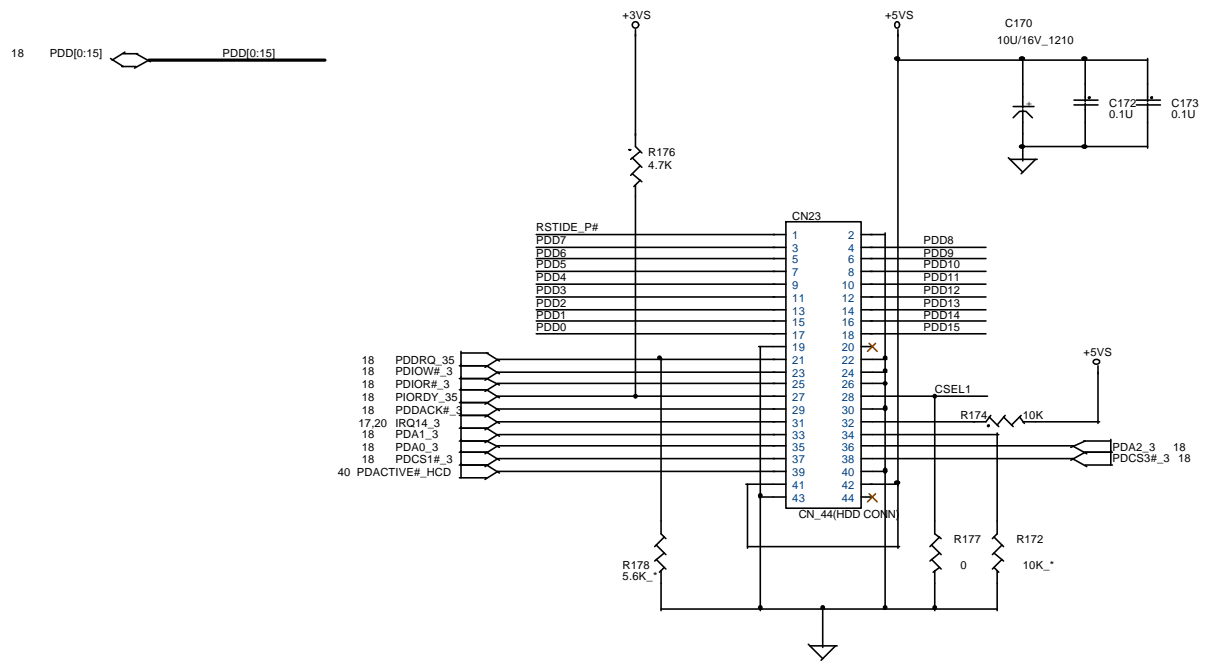
7.15,17.33,44	PCIRST#	3	0		
21.22.27.42	PCIRSTNS#	3	0		

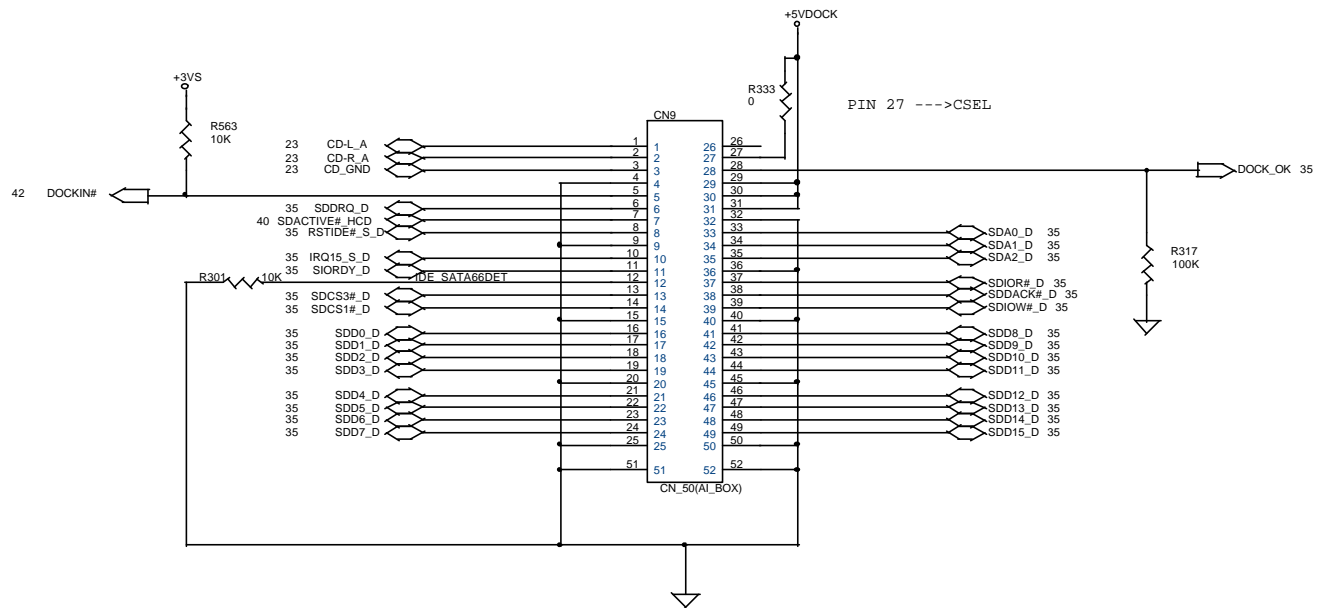
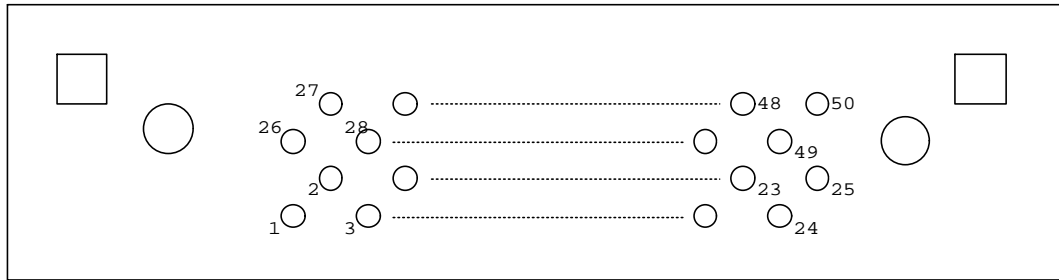
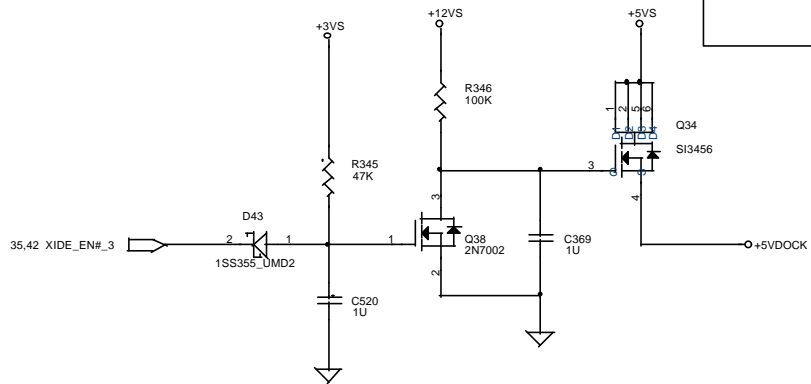


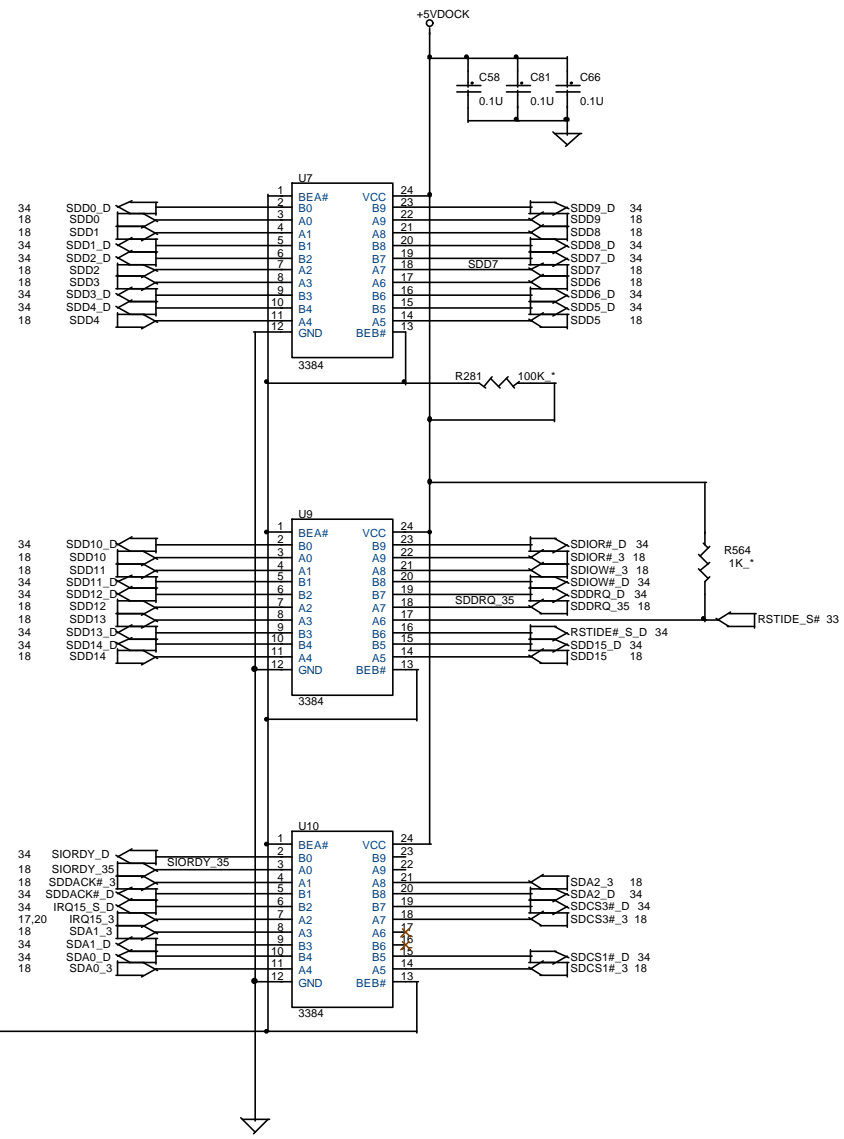
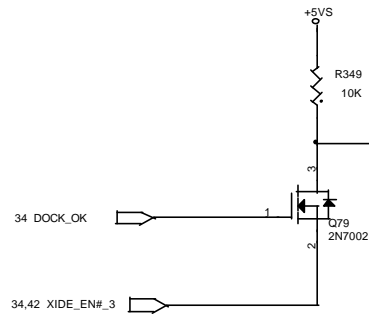
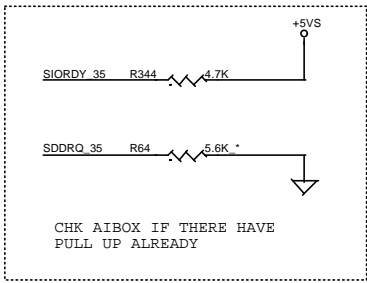
ASUS PROJECT: S1A	REVISION	DATE: Thursday, October 04, 2001	DESCRIPTION	SCHMATIC FILE NAME: <Doc>	DESIGN ENGINEER:
	1.2	SHEET 31 OF 57	LAN I/O	LIBRARY DATE:	

17,22,27,30 AD[0:31]  AD[0:31]







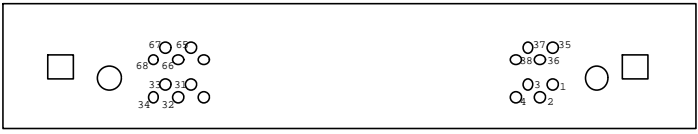


MTR0#_35 IS RESERVED,
NOT USE IN PORTDOCK

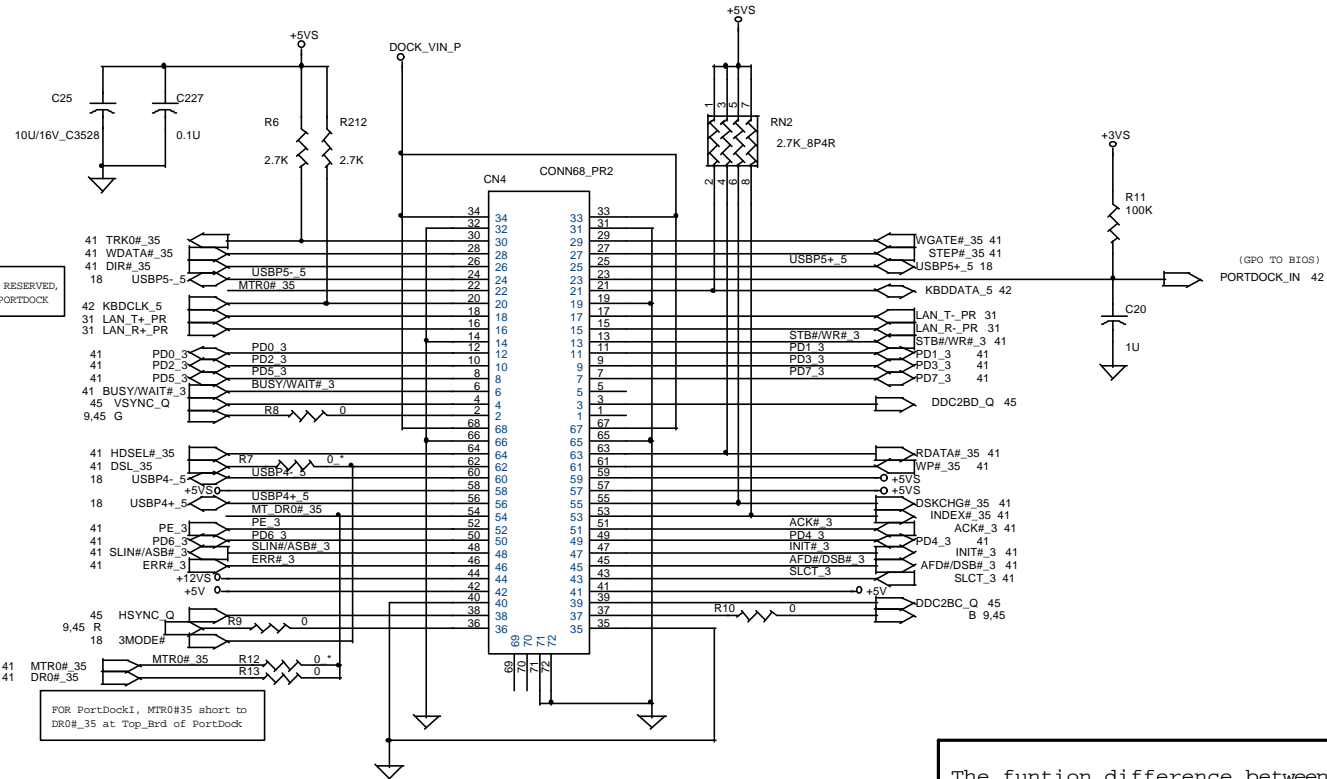
FOR PortDockI, MTR0#35 short to
DR0#_35 at Top_Brd of PortDock

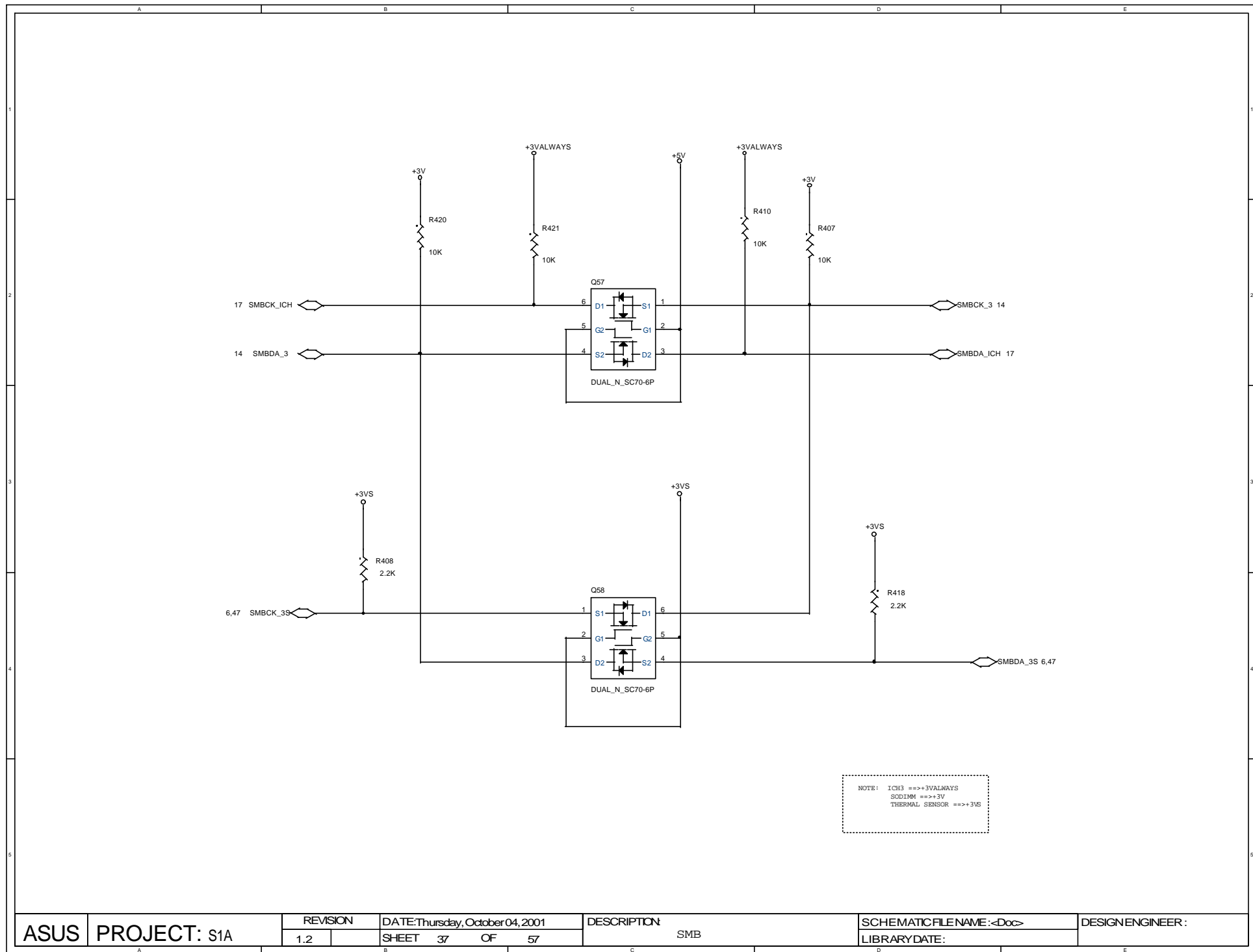
Note: pin 40, 35 reserve for AGND_V (VGA GND),
for S1A project, using GND only

The funtion difference between
Port-DockI / Port Dock II:
1. PDI w/ COM, 2xPS2, wo/ Lan
2. PDII w/ 2xUSB, Lan, 1xPS2



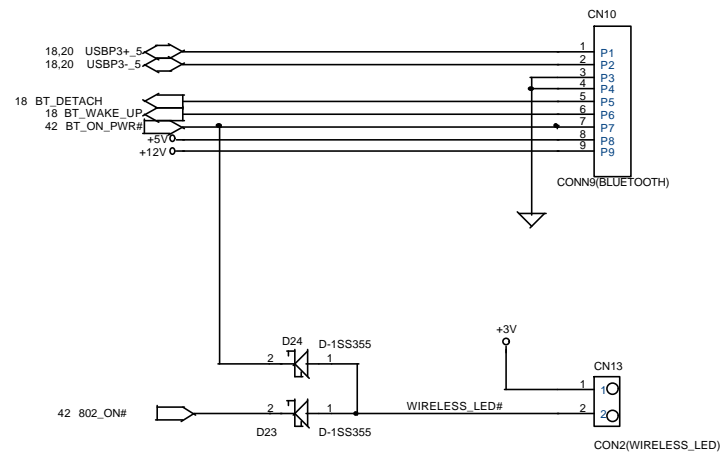
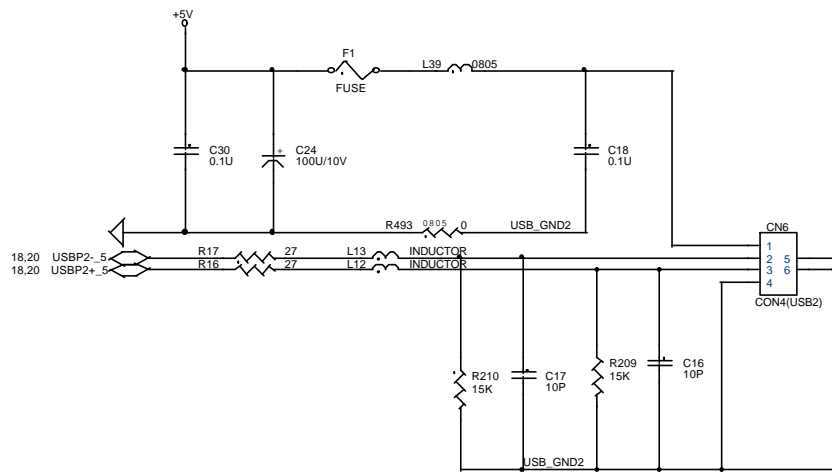
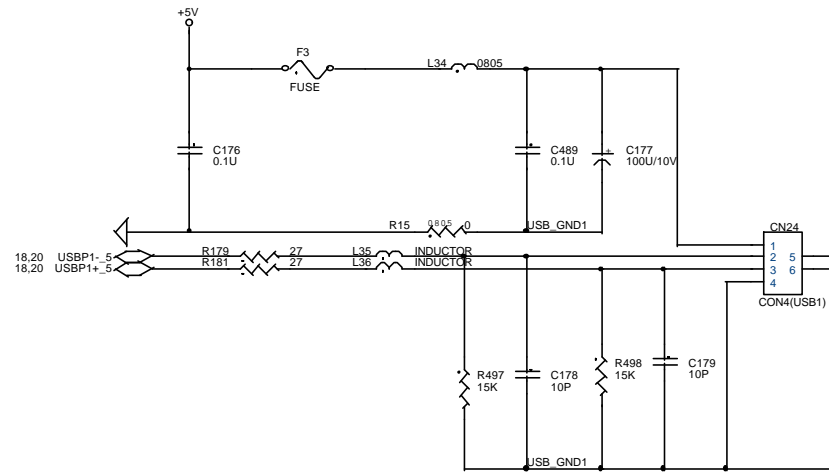
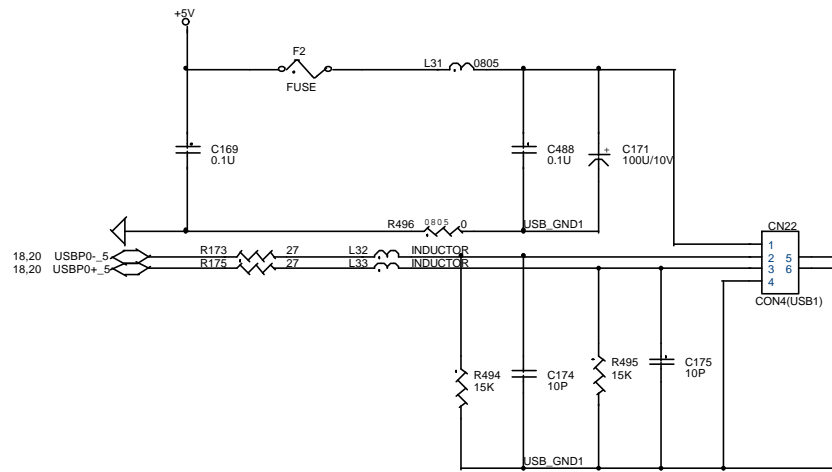
Top View

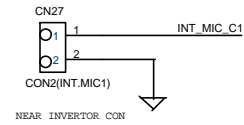
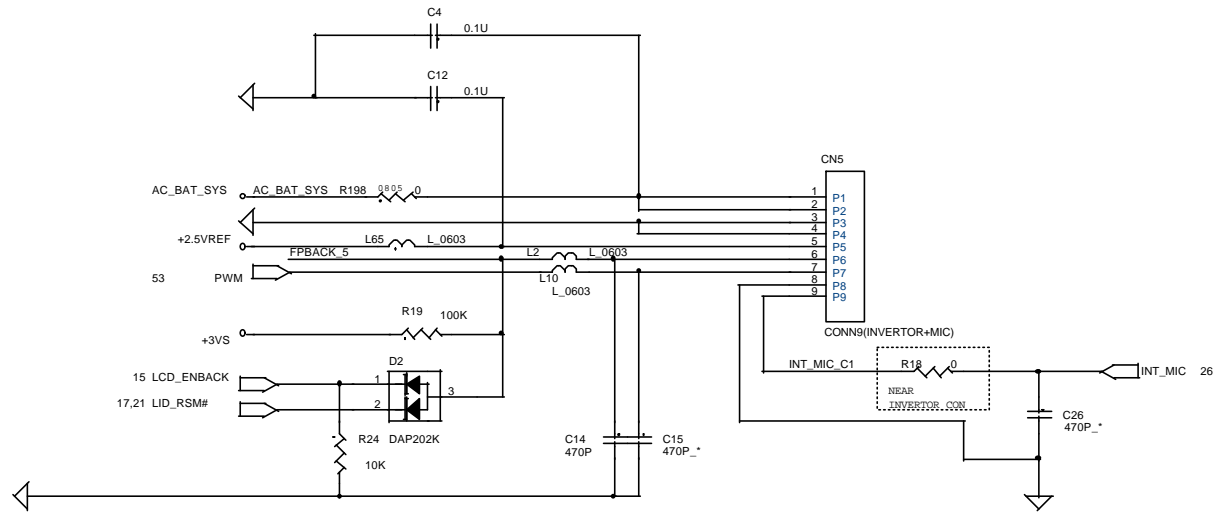


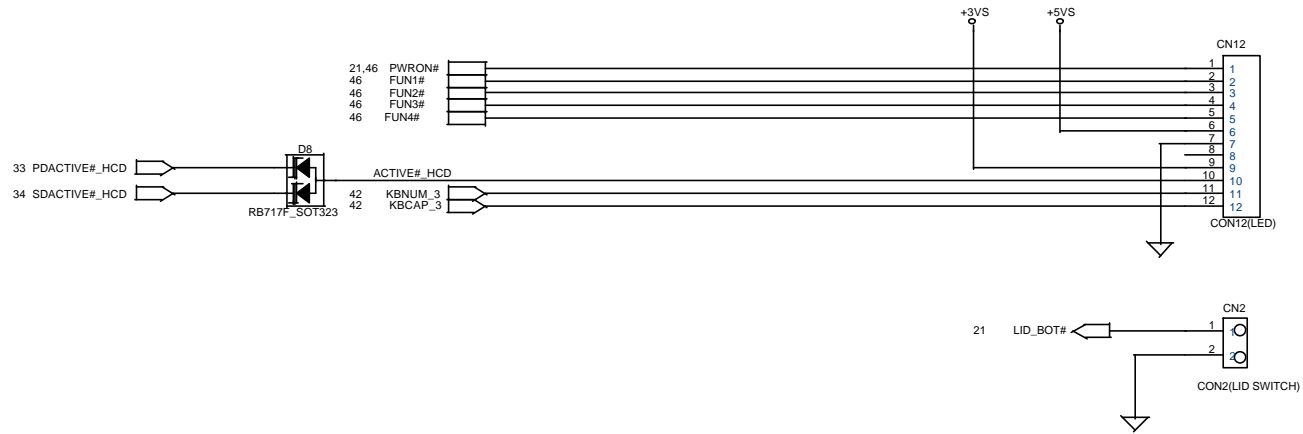
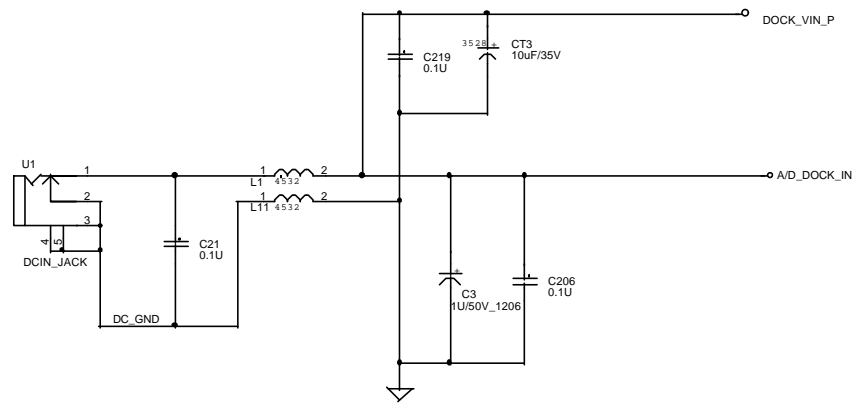


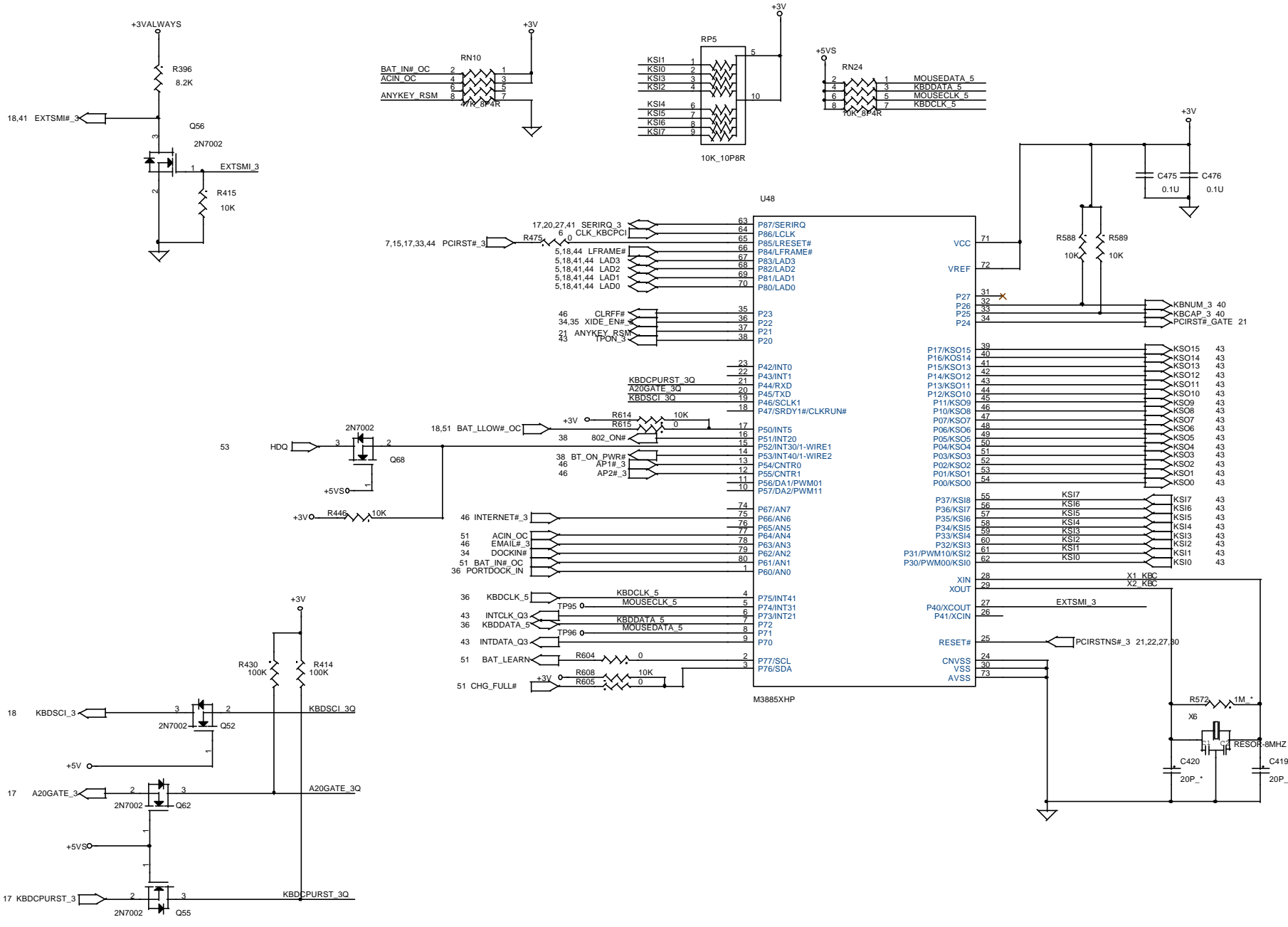
NOTE: ICH3 ==>+3VALWAYS
 SODIMM ==>+3V
 THERMAL SENSOR ==>+3VS

ASUS PROJECT: S1A	REVISION	DATE: Thursday, October 04, 2001	DESCRIPTION	SCHMATIC FILE NAME: <Doc>	DESIGN ENGINEER :
	1.2	SHEET 37 OF 57	SMB	LIBRARY DATE:	

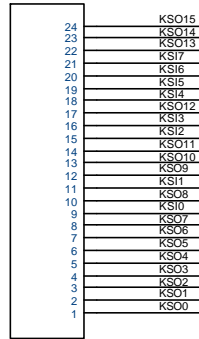




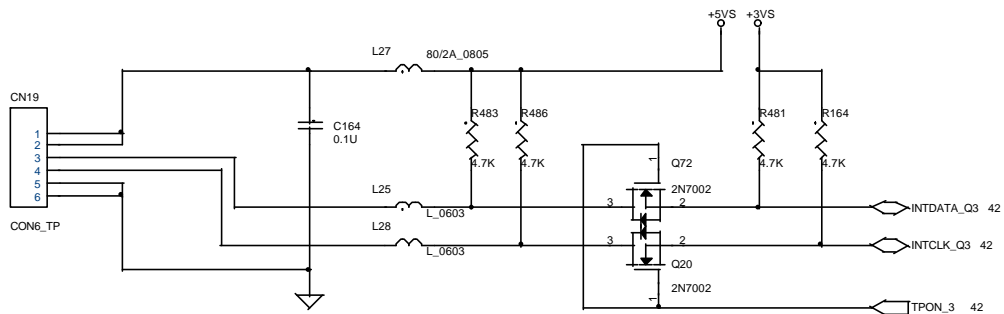
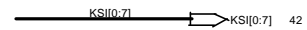
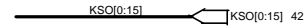


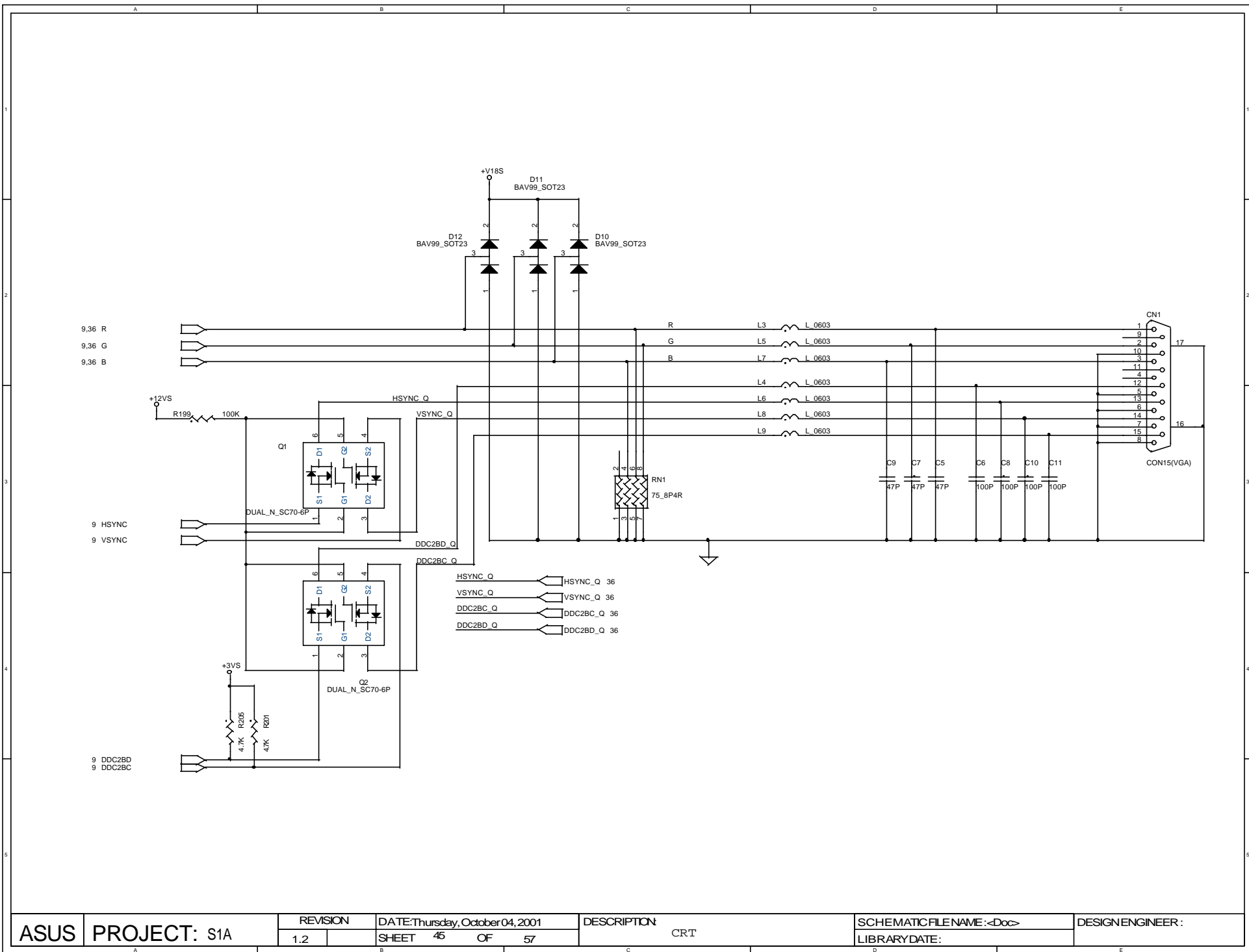


CN17



CN24(KEYBOARD)





ASUS PROJECT: S1A

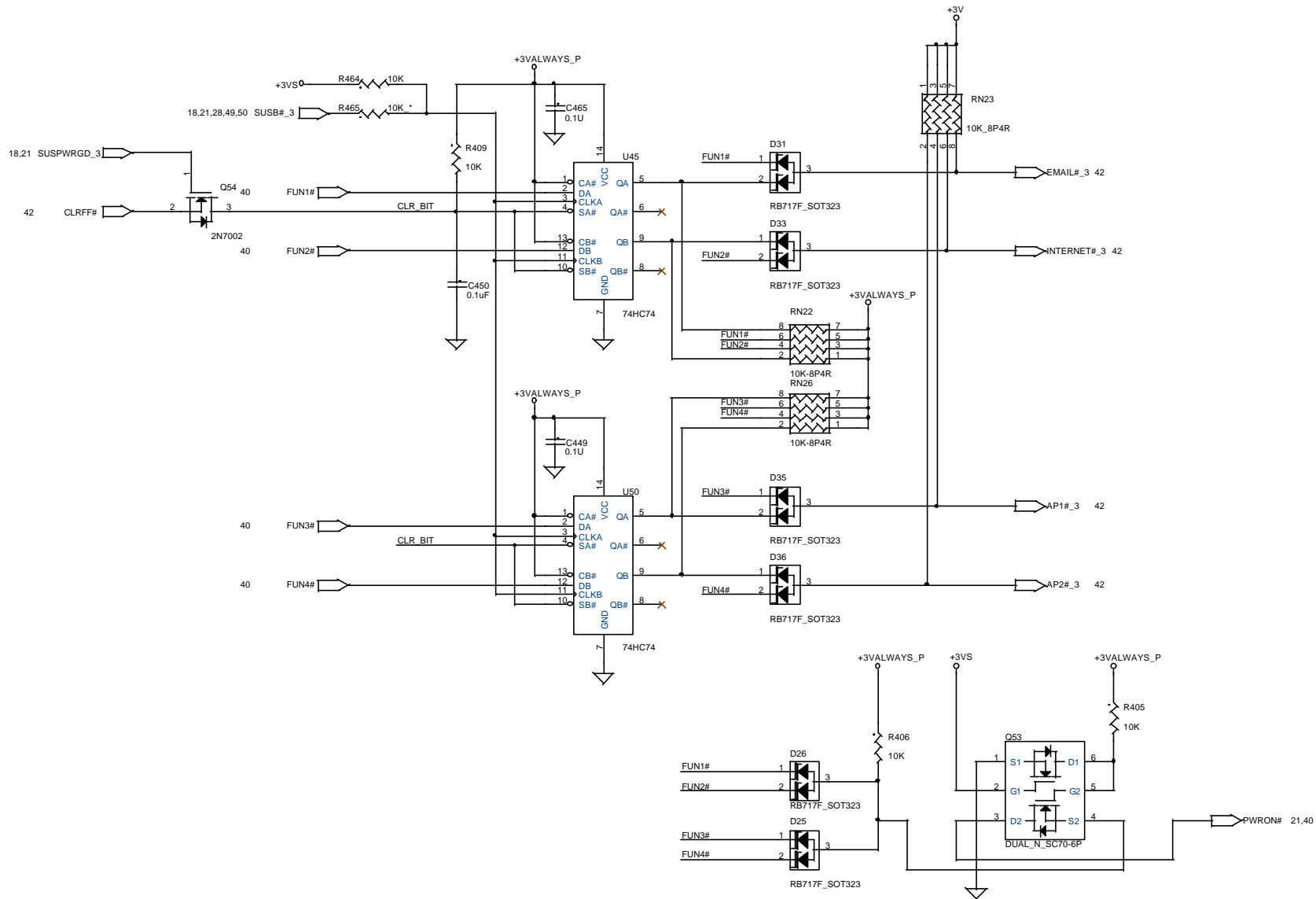
REVISION
1.2

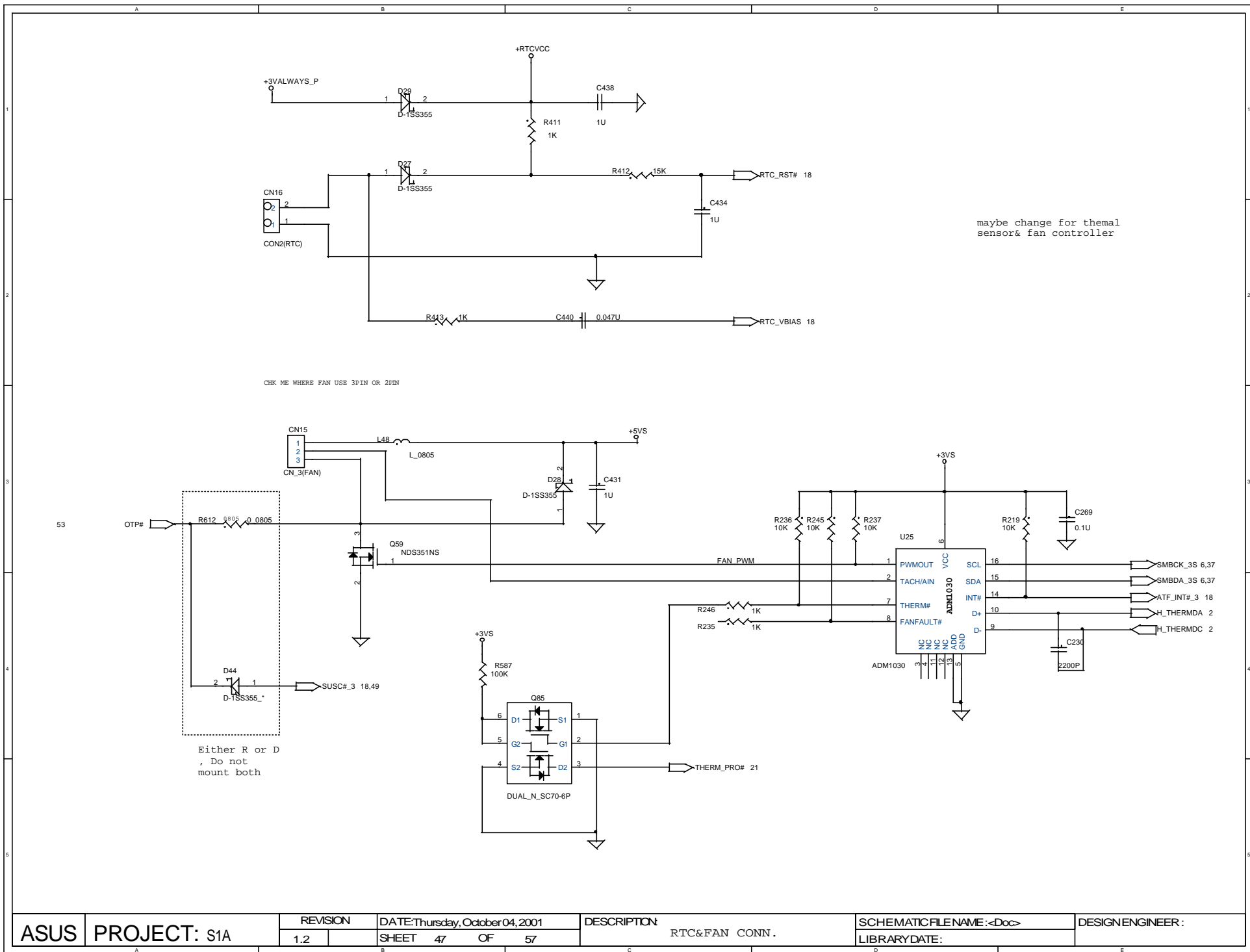
DATE: Thursday, October 04, 2001
SHEET 45 OF 57

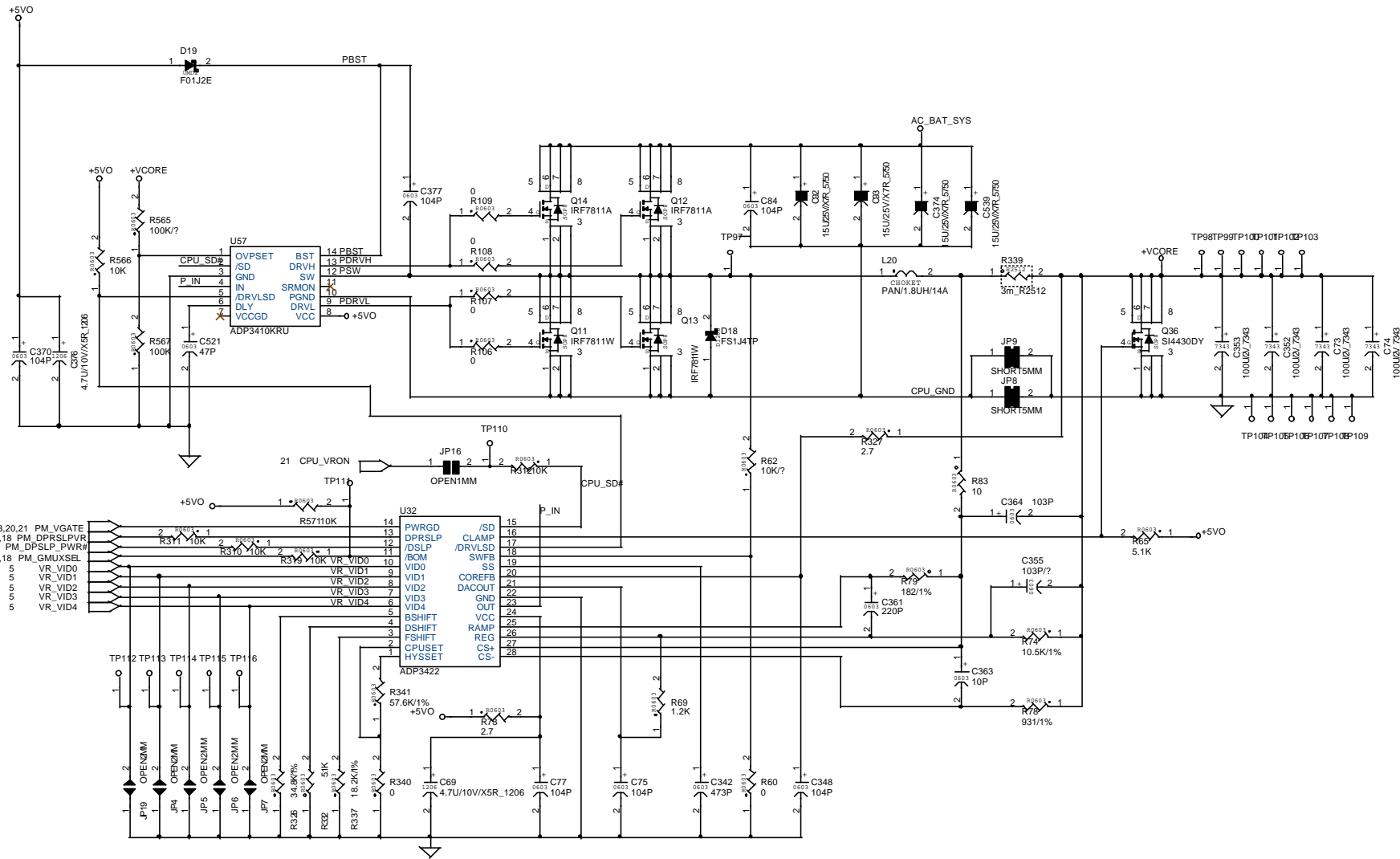
DESCRIPTION
CRT

SCHEMATIC FILE NAME: <Doc>
LIBRARY DATE:

DESIGN ENGINEER:







Deep sleep = $0.182 / 3.48K * 1.15V = 60.14mV$
 Battery modw = $0.182 / 34.8K * 1.15V = 6.01mV$



PROJECT: S1A

REVISION

2.0

DATE: Thursday, October 04, 2001

SHEET 48 OF 57

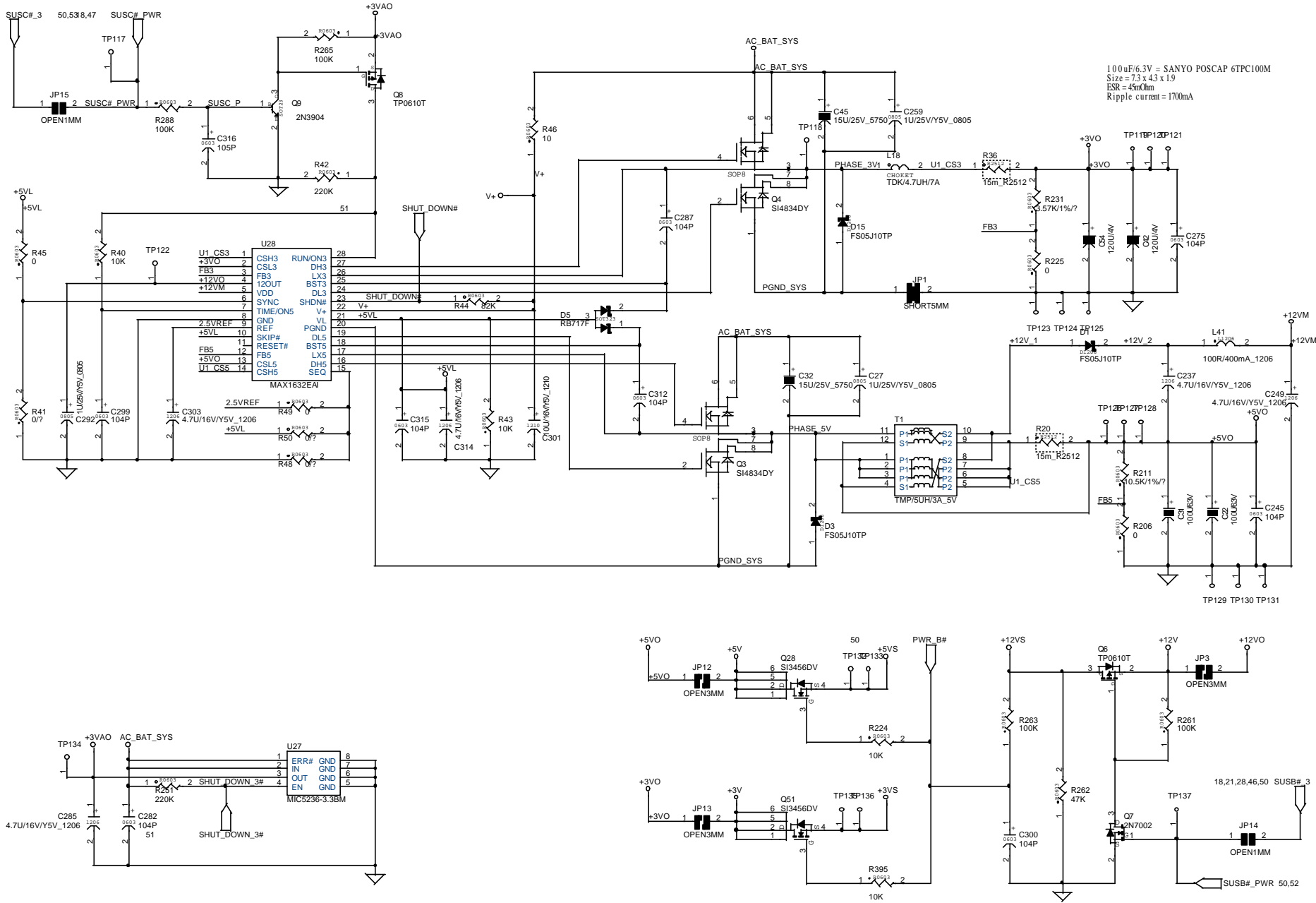
DESCRIPTION

POWER CPU Vcore ADP3422

SCHEMATIC FILENAME:

LIBRARY DATE:

DESIGN ENGINEER:



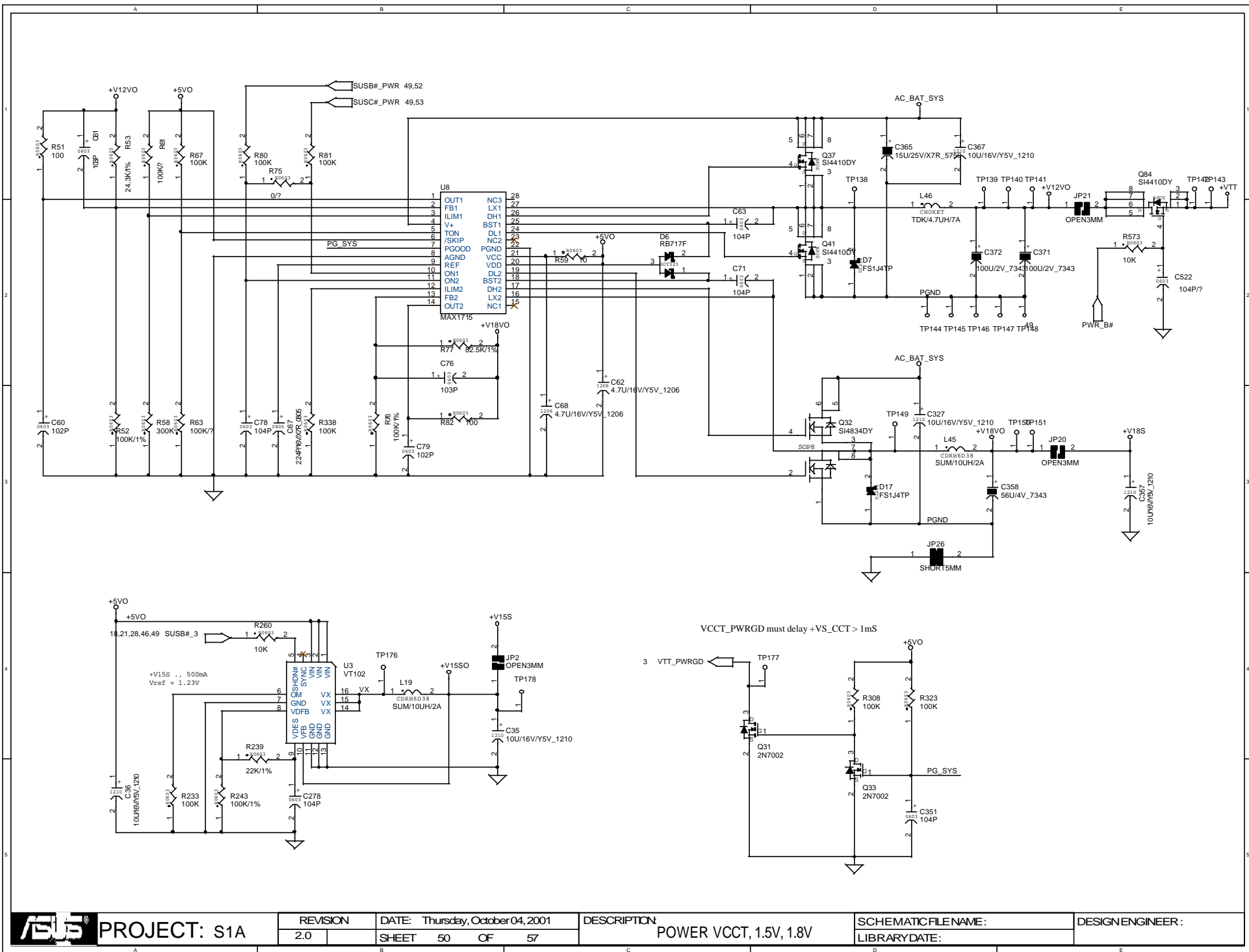
PROJECT: S1A

REVISION	DATE: Thursday, October 04, 2001
2.0	SHEET 49 OF 57

DESCRIPTION
 POWER 3.3V, 5V, 12V MAX1632

SCHEMATIC FILENAME:
 LIBRARY DATE:

DESIGN ENGINEER:



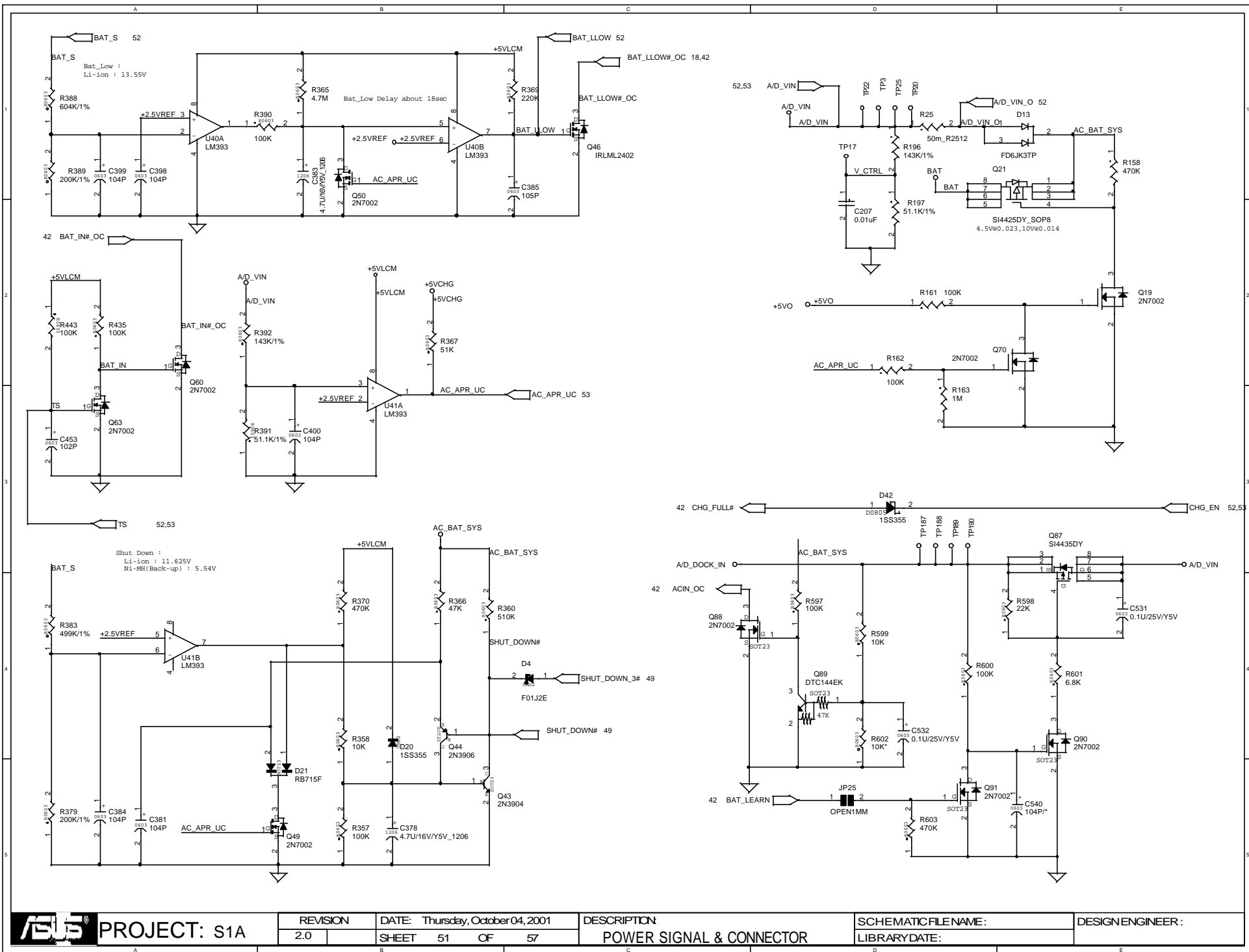
PROJECT: S1A

REVISION	DATE: Thursday, October 04, 2001
2.0	SHEET 50 OF 57

DESCRIPTION: POWER VCCT, 1.5V, 1.8V

SCHEMATIC FILENAME:
LIBRARY DATE:

DESIGN ENGINEER:



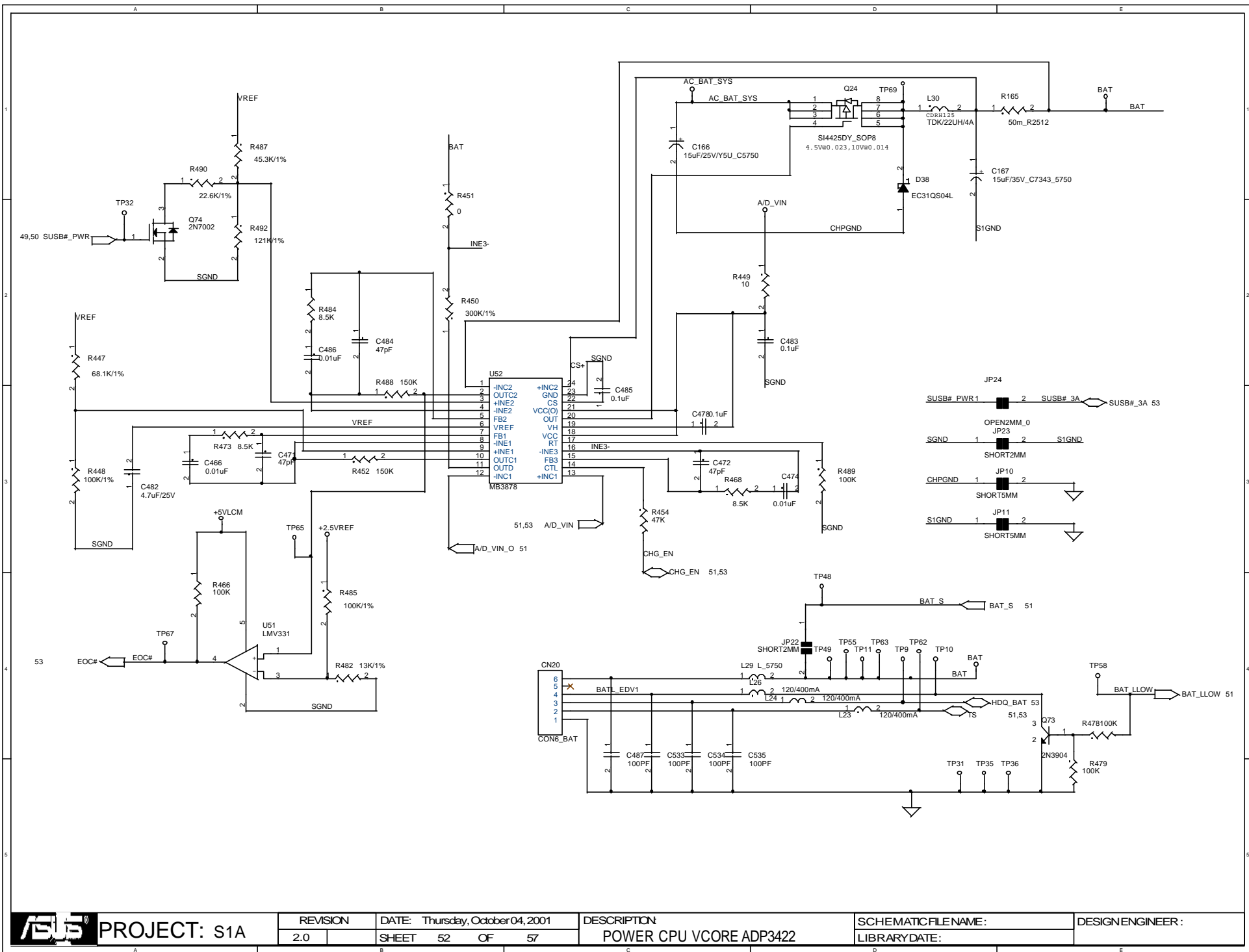
PROJECT: S1A

REVISION	DATE: Thursday, October 04, 2001
2.0	SHEET 51 OF 57

DESCRIPTION
POWER SIGNAL & CONNECTOR

SCHEMATIC FILE NAME:
LIBRARY DATE:

DESIGN ENGINEER:



PROJECT: S1A

REVISION	DATE: Thursday, October 04, 2001
2.0	SHEET 52 OF 57

DESCRIPTION
POWER CPU VCORE ADP3422

SCHEMATIC FILENAME:
LIBRARY DATE:

DESIGN ENGINEER:

ICH2M_GPIO	Use As	Signal Name
GPI2/PIRQE#	GPI	KBDSKI_3
GPI3/PIRQF#	Pull-Down	KBDSKI_3
GPI4/PIRQG#	Pull Up	KBDSKI_3
GPI5/PIRQH#	GPI	IDE_PATA66DET
GPI7	GPI	IDE_SATA66DET
GPI8	GPI	EXTSMI#_3
GPI12	GPI	BT_WAKE_UP
GPI13	GPI	ON_OFF_BTN#
GPO21/NOGO	Not_Use	
GPO25	Not_Use	
GPO27	Not_Use	
GPO28	GPO	FWH_WP#

PCI Device	IDSEL#	REQ/GNT#	Interrupts	PC/PCI
Chipset (Host to PCI)	(AD30 internal)	n/a		
AGP	(AD17 internal)			
LAN	AD28	1	A	
CardBus	AD25	2	A,B	
1394	AD27	1	A	
Mini_PCI	AD26	2	A,B	

OZ998_GPIO	Use As	Signal Name
GPI0	GPO	SMIEVENT
GPI01	GPI	BOOT_ST_CHK
GPI02	GPO	SMBALERT#
GPI03	GPO	EMAIL#
GPI04	Not_Use	
GPI05	Not_Use	
GPI06	Not_Use	
GPI07	GPO	BEEP_MUTE_3
GPI08	GPI	FUN1_BAN
GPI09	GPI	FUN2_BAN
GPI010	GPI	FUN3_BAN
GPI011	GPI	FUN4_BAN
GPI012	Pull_Down	
GPI013	Pull_Down	
GPI014	GPI	RIA#_3
GPI015	GPI	LID_RSM#

M38867_GPIO	Use As	Signal Name
P62/AN2	GPI	DOCKGD#_3
P64/AN4	GPI	ACIN_OC
P67/AN7	GPO	FWH_TBL#
P54	GPI	SMBALERT#
P21	GPI	ANYKEY_RSM
P22	GPO	BT_DETACH
P23	GPO	CD_DOCK
P40	GPO	EXTSMI#_3

PAGE	Content	Revision History
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1	BLOCK DIAGRAM	
2	TUALATIN CPU-1	
3	TUALATIN CPU-2	
4	CPU RES/CAP	
5	CPU VID / ITP	
6	CLOCK GEN. (ICS9250-38)	
7	ALMADOR_GMCH_A	
8	ALMADOR_GMCH_B	
9	ALMADOR_GMCH_C	
10	ALMADOR_GMCH_D	
11	ALMADOR RES/ CAP	
12	ON BOARD SDRAM-1	
13	ON BOARD SDRAM-2	
14	SODIMM	
15	VCH	
16	LCD VCC	
17	ICH3_A	
18	ICH3_B	
19	ICH3_C	
20	ICH3 RES/ CAP	
21	RESET	
22	1394 (TSB43AB22)	
23	AC97	
24	AUDIO AMP (TI-TPA0132)	
25	MIC PRE. AMP	
26	AUDIO CON/ INT. MIC	
27	CARDBUS SWITCH (TPS2214)	
28		
29	LPT	
30	SMBus	
31	CARDBus CONTROLLER TI4410	
32	CARDBus POWER & SLOT	
33	1394 PHY & 1 PORT	
34	INSTANT KEY	
35	RTC & FAN	
36	RESET CIRCUIT	
37	BATTARY LOW DETECT CIRCUIT	
38	CHARGER	
	SYSTEM POWER	