PERFECT WIRELESS EXPERIENCE

FIBOCOM FM101-GL

Hardware Guide

V1.0

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Change History

V1.0 (2021-09-22)	Draft version.

1 Foreword

1.1 Introduction

The document describes the electrical characteristics, RF performance, dimensions and application environment, etc. of FM101-GL (hereinafter referred to as FM101). With the assistance of the document and other instructions, the developers can quickly understand the hardware functions of FM101 modules and develop products.

1.2 Reference Standard

The design of the product complies with the following standards:

- 3GPP TS 34.121-1 V8.11.0: User Equipment (UE) conformance specification; Radio transmission and reception (FDD); Part 1: Conformance specification
- 3GPP TS 34.122 V11.13.0: Technical Specification Group Radio Access Network; Radio transmission and reception (TDD)
- 3GPP TS 36.521-1 V13.4.0: User Equipment (UE) conformance specification; Radio transmission and reception; Part 1: Conformance testing
- 3GPP TS 21.111 V10.0.0: USIM and IC card requirements
- 3GPP TS 51.011 V4.15.0: Specification of the Subscriber Identity Module -Mobile Equipment (SIM-ME) interface
- 3GPP TS 31.102 V10.11.0: Characteristics of the Universal Subscriber Identity Module (USIM) application
- 3GPP TS 31.11 V10.16.0: Universal Subscriber Identity Module (USIM) Application Toolkit (USAT)
- 3GPP TS 36.124 V10.3.0: Electro Magnetic Compatibility (EMC) requirements for mobile terminals and ancillary equipment
- 3GPP TS 27.007 V10.0.8: AT command set for User Equipment (UE)

- 3GPP TS 27.005 V10.0.1: Use of Data Terminal Equipment - Data Circuit terminating Equipment (DTE-DCE) interface for Short Message Service (SMS) and Cell Broadcast Service (CBS)
- PCI Express M.2 Specification Rev4.0

1.3 Related Documents

TBD

2 Overview

2.1 Introduction

FM101 is a highly integrated 4G WWAN module which uses M.2 form factor interface. It supports LTE FDD/LTE TDD/WCDMA systems and can be applied to most cellular networks of mobile carrier in the world.

2.2 Specification

2.2.1 RF Characteristic

FM101 RF characteristic is shown in Table 1:

Table 1. RF characteristic

Operating Band	
FDD-LTE	B1/2/3/4/5/7/8/12/13/14/17/18/19/20/25/26/28/29/30/66/71
TDD-LTE	B38/39[1)]/40[3)]/41/42[3)]/43[3)]/48[2)]
UMTS/HSPA+	B1/2/4/5/6/8/19
GNSS	GPS/GLONASS/Galileo/BDS
Data Throughput	
LTE Peak	DL 300Mbps (CAT6)/UL 50Mbps (CAT4)
UMTS/HSPA+ Peak	DL UMTS: 384 kbps/UL 384 kbps
	DL DC-HSPA+: 42 Mbps (CAT24)/UL 5.76 Mbps (CAT6[4)])
Modulation Characteristic	
LTE Modulation	3GPP Release 12

	Download 64 QAM
UMTS Modulation	3GPP Release 9
RF Characteristic	
HPUE[5)]	B41
MIMO	2x2 MIMO
Carrier Aggregation	
LTE	DL 2CA

1) Don't support B39 in Japan
2) Don't support B40/42/43 in FCC/IC
3) Don't support B48 in IC
4) CAT8 11.5Mbps under developing
5) Don't support HPUE in Japan

2.3 Key Features

Table 2. Key features

Specification	
CPU	Qualcomm SDX12, 14nm process, ARM Cortex-A7, up to 1.28 GHz
Memory	2Gb LPDDR2+2Gb NAND Flash
Supported OS	Windows 10/Chrome /Linux
Power Supply	DC 3.135V to 4.4V, typical 3.3V

Temperature	Normal operating temperature: –10°C to +55°C
	Extended operating temperature: –30°C to +75°C[1)]
	Storage temperature: –40°C to +85°C
Physical Characteristics	Interface: M.2 Key-B
	Dimension: 30 mm x 42 mm x 2.3 mm
	Weight: TBD
Interface	
Antenna Connector	WWAN Antenna x 2
	Support 2x2 MIMO
Function Interface	Dual SIM (one embedded eSIM), 1.8V/3V
	USB 2.0 (For debug)
	USB 3.0
	W_Disable#
	Bodysar
	LED
	Tunable antenna
	I2C (Reserved)
Software	
Protocol Stack	IPV4/IPV6
AT Commands	3GPP TS 27.007 and 27.005
Firmware Update	USB
Other Feature	Multiple carrier

	Windows MBIM support
	Windows update
	AGNSS

1) When temperature goes beyond normal operating temperature range of -10°C to +55°C, RF performance of module may be slightly off 3GPP specifications.

2.4 Application Block

The peripheral applications for FM101 module are shown in Figure 1:

2.5 Hardware Block Diagram

The hardware block diagram in Figure 2 shows the main hardware functions of FM101 module, including base band and RF functions.

Baseband contains:

- UMTS/LTE TDD/LTE FDD controller
- PMU
- MCP (NAND+ LPDDR2)
- Application interface

RF contains:

- RF Transceiver
- RF DCDC/PA
- RF Duplexer
- Antenna Connector

2.6 Antenna Configuration

FM101 module supports two antennas and the configuration is as below table:

Table 3. Antenna configuration

Antenna Connector	Function Description	Band Configuration (TX)	Band Configuration (RX)	Frequency Range (MHz)
ANT0 (M)	Main antenna port for TRX	WCDMA B1/2/4/5/6/8/19 LTE Band B1/2/3/4/5/7/8/12/13/14/17/18/19/20/25/26/28/30/66/71/38/39/40/41/42/43/48	WCDMA B1/2/4/5/6/8/19 LTE Band B1/2/3/4/5/7/8/12/13/14/17/18/19/20/25/26/28/29/30/66/71/38/39/40/41/42/43/48	617–3800
ANT1 (D/G)	Antenna port for RX		WCDMA B1/2/4/5/6/8/19 LTE Band B1/2/3/4/5/7/8/12/13/14/17/18/19/20/25/26/28/29/30/66/71/38/39/40/41/42/43/48 GNSS	617–3800

3 Application Interface

3.1 M.2 Interface

The FM101 module applies standard M.2 Key-B interface, with a total of 75 pins.

3.1.1 Pin Map

74	+3.3V	CONFIG_2	75
72	+3.3V	GND	73
70	+3.3V	GND	71
68	NC	CONFIG_1	69
66	SIM1_DETECT(1.8V)	RESET#(1.8V)	67
64	COEX_TXD(1.8V)	ANTCTL3(1.8V)	65
62	COEX_RXD(1.8V)	ANTCTL2(1.8V)	63
60	COEX3(1.8V)	ANTCTL1(1.8V)	61
58	RFE_RFFE_SDATA	ANTCTL0(1.8V)	59
56	RFE_RFFE_SCLK	GND	57
54	NC	NC	55
52	NC	NC	53
50	NC	GND	51
48	NC	NC	49
46	NC	NC	47
44	I2C_IRQ#(EINT)	GND	45
42	I2C_SDA(I2C Master)	NC	43
40	I2C_SCL(I2C Master)	NC	41
38	NC	GND	39
36	UIM1_PWR	USB3.0-Rx+	37
34	UIM1_DATA	USB3.0-Rx -	35
32	UIM1_CLK	GND	33
30	UIM1_RESET	USB3.0-Tx+	31
28	GPIO(I)	USB3.0-Tx -	29
26	W_DISABLE2#(3.3/1.8V)	GND	27
24	VIO_1.8V	DPR(3.3/1.8V)	25
22	GPIO(I)	WOWWAN#(1.8V)	23
20	GPIO(I)	CONFIG_0	21
	Notch	Notch	
	Notch	Notch	
	Notch	Notch	
	Notch	Notch	
10	LED1#(3.3V OD)	GND	11
8	W_DISABLE1#(3.3/1.8V)	USB D-(debug)	9
6	FULL_CARD_POWER_OFF#(3.3/1.8V)	USB D+(debug)	7
4	+3.3V	GND	5
2	+3.3V	GND	3
		CONFIG_3	1

Figure 1. Pin map

Pin “Notch” represents the gap of the gold fingers.

3.1.2 Pin Definition

IO Parameter definition is as below table.

Table 4. IO parameter definition

Type	Description
PI	Power Input
PO	Power Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input /Output
AI	Analog Input
AO	Analog Output
AIO	Analog Input /Output
OD	Open Drain
T	Tristate
PU	Internal pull up
PD	Internal pull down
Hi-Z	High impedance
NC	Not connected

The pin definition is as follows:

Table 5. Pin Definition

Pin	Pin Name	I/O	Reset Value	Pin Description	Type
1	CONFIG_3	O	GND	GND, FM101 M.2 module is configured as the WWAN – SSIC, USB 3.0 interface type	-
2	+3.3V	PI	-	Power input	Power Supply
3	GND	-	-	GND	Power Supply
4	+3.3V	PI	-	Power input	Power Supply
5	GND	-	-	GND	Power Supply
6	FULL_CARD_ POWER_OFF#	I	PU	Power enable, module power on input, internal pull up	3.3/1.8V
7	USB D+	I/O	-	USB data plus, only for debug	0.3---3V
8	W_DISABLE1#	I	PD	WWAN disable, default high, active low	3.3/1.8V
9	USB D-	I/O	-	USB data minus, only for debug	0.3---3V
10	LED1#	OD	T	System status LED, output open drain, CMOS 3.3V	3.3V
11	GND	-	-	GND	Power Supply
12	Notch			Notch	
13	Notch			Notch	

Pin	Pin Name	I/O	Reset Value	Pin Description	Type
14	Notch			Notch	
15	Notch			Notch	
16	Notch			Notch	
17	Notch			Notch	
18	Notch			Notch	
19	Notch			Notch	
20	GPIO	I	PD	GPIO(I), default low, reserved	1.8V
21	CONFIG_0	-	NC	NC, FM101 M.2 module is configured as the WWAN – SSIC, USB 3.0 interface type	-
22	GPIO	I	PD	GPIO(I), default low, reserved	1.8V
23	WOWWAN#	O	PD	Wake up host, default low, Reserved	1.8V
24	ANT_TUNER_1V8	PO	PD	1.8V output for ANT Tuner, reserved.	Power Supply /1.8V
25	DPR	I	PD	Dynamic power reduction detect, default high, active low	3.3/1.8V
26	W_DISABLE2#	I	PD	GNSS disable, default high, active low, reserved	3.3/1.8V
27	GND	-	-	GND	Power Supply
28	GPIO	I	PD	GPIO(I), default low, reserved	1.8V
29	USB 3.0_TX-	O	-	USB 3.0 transmit data minus	-

Pin	Pin Name	I/O	Reset Value	Pin Description	Type
30	UIM1_RESET	O	-	SIM reset signal	1.8V/3V
31	USB 3.0_TX+	O	-	USB 3.0 transmit data plus	-
32	UIM1_CLK	O	-	SIM clock signal	1.8V/3V
33	GND	-	-	GND	Power Supply
34	UIM1_DATA	I/O	-	SIM data input/output	1.8V/3V
35	USB 3.0_RX-	I	-	USB 3.0 receive data minus	-
36	UIM1_PWR	O	-	SIM power supply, 1.8V/3V	1.8V/3V
37	USB 3.0_RX+	I	-	USB 3.0 receive data plus	-
38	NC	-	-	NC	-
39	GND	-	-	GND	Power Supply
40	I2C_SCL	O	PU	I2C clock, master mode, default high, reserved	1.8V
41	NC	-	-	NC	-
42	I2C_SDA	I/O	PU	I2C data, master mode, default high, reserved	1.8V
43	NC	-	-	NC	-
44	I2C_IRQ#	I	PD	I2C interrupt, used for wake up I2C host, default high, reserved	1.8V
45	GND	-	-	GND	Power Supply

Pin	Pin Name	I/O	Reset Value	Pin Description	Type
46	NC	-	-	NC	-
47	NC	-	-	NC	-
48	NC	-	-	NC	-
49	NC	-	-	NC	-
50	NC	-	-	NC	-
51	GND	-	-	GND	Power Supply
52	NC	-	-	NC	-
53	NC	-	-	NC	-
54	NC	-	-	NC	-
55	NC	-	-	NC	-
56	RFFE_SCLK	O	PD	MIPI interface tunable ANT, RFFE clock	1.8V
57	GND	-	-	GND	Power Supply
58	RFFE_SDATA	I/O	PD	MIPI interface tunable ANT, RFFE data	1.8V
59	ANTCTL0	O	PD	Tunable ANT CTRL0, default low	1.8V
60	COEX3	I/O	PD	Wireless coexistence between WWAN and WIFI/BT modules, based on BT-SIG coexistence protocol. COEX_EXT_FTA, Reserved	1.8V
61	ANTCTL1	O	PD	Tunable ANT CTRL1, default low	1.8V

Pin	Pin Name	I/O	Reset Value	Pin Description	Type
62	COEX_RXD	I	PD	Wireless coexistence between WWAN and WIFI/BT modules, based on BT-SIG coexistence protocol. UART receive signal (WWAN module side), Reserved	1.8V
63	ANTCTL2	O	PD	Tunable ANT CTRL2, default low	1.8V
64	COEX_TXD	O	PD	Wireless coexistence between WWAN and WIFI/BT modules, based on BT-SIG coexistence protocol. UART transmit signal (WWAN module side), Reserved	1.8V
65	ANTCTL3	O	PD	Tunable ANT CTRL3, default low	1.8V
66	SIM1_DETECT	I	PD	SIM1 detect, internal pull up (390KΩ), active high	1.8V
67	RESET#	I	PU	WWAN reset input, internal pull up (22KΩ), active low	1.8V
68	NC	-	-	NC	-
69	CONFIG_1	O	GND	GND, FM101 M.2 module is configured as the WWAN – SSIC, USB 3.0 interface type	-
70	+3.3V	PI	-	Power input	Power Supply
71	GND	-	-	GND	Power Supply
72	+3.3V	PI	-	Power input	Power

Pin	Pin Name	I/O	Reset Value	Pin Description	Type
					Supply
73	GND	-	GND	GND	-
74	+3.3V	PI	-	Power input	Power Supply
75	CONFIG_2	O	GND	GND, FM101 M.2 module is configured as the WWAN – SSIC, USB 3.0 interface type	-

Reset value is the status while module reset, not the status in working. Digital IO pins cannot be connected to power directly. The unused pins can be left floating.

3.2 Power Supply

The power interface of FM101 module as shown in the following table:

Table 6. Power interface

Pin	Pin Name	I/O	Pin Description	DC Parameter (V)		
				Minimum Value	Typical Value	Maximum Value
2, 4, 70, 72, 74	+3.3V	PI	Power supply input	3.135	3.3	4.4
24	ANT_TUNER_1V8	PO	1.8V power output for antenna tuner	1.71	1.8	1.89
36	UIM1_PWR	PO	USIM power supply	-	1.8V/3V	-

The Power rating is shown in the following table:

Table 7. Power rating

Pin	Pin Name	I/O	Pin Description	Peak Current (mA)
2, 4, 70, 72, 74	+3.3V	PI	Power supply input	2500
24	ANT_TUNER_1V8	PO	1.8V power output for antenna tuner	200
36	UIM1_PWR	PO	USIM power supply	150

3.2.1 Power Supply

The FM101 module should be powered through the +3.3V pins, and the power supply design is shown in Figure:

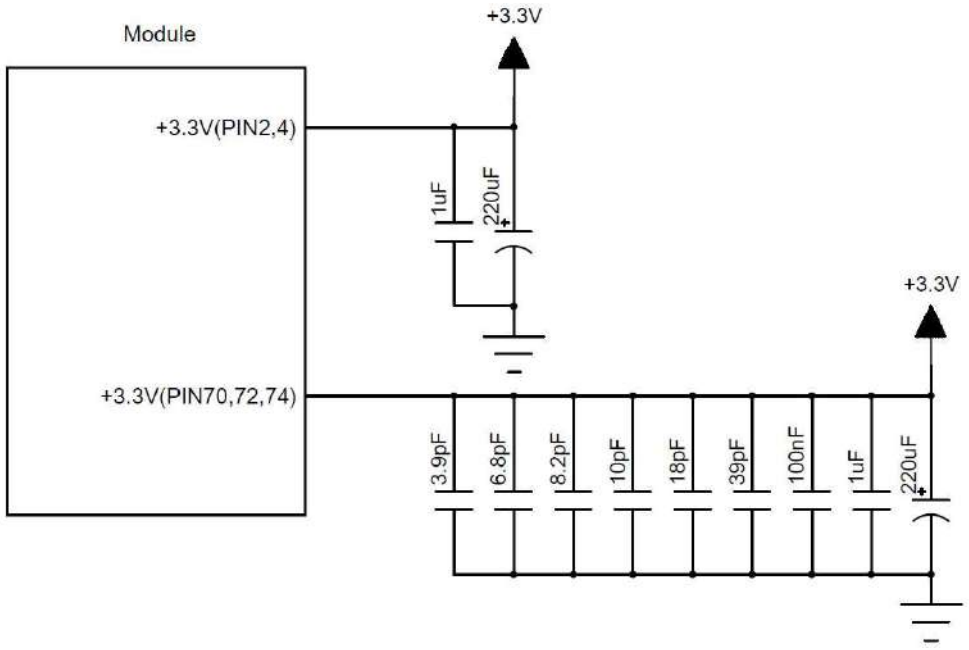

Figure 4. Power supply design

The filter capacitor design for power supply as shown in the following table:

Table 8. The filter capacitor design for power supply

Recommended capacitance	Application	Description
220uF x 2	Voltage-stabilizing capacitors	Reduce power fluctuations of the module in operation, requiring capacitors with low ESR. LDO or DC/DC power supply requires the capacitor with no less than 440uF in the power supply voltage range.
1uF, 100nF	Digital signal noise	Filter out the interference generated from the clock and digital signals
39pF, 33pF	700/800, 850/900 MHz frequency band	Filter out low frequency band RF interference
18pF, 10pF, 8.2pF, 6.8pF, 3.9pF	1500/1800, 2100/2300, 2600MHz, 3500/3600/3700MHz, 5GHz	Filter out medium/high frequency band RF interference

The stable power supply can ensure the normal operation of FM101 module; and the ripple of the power supply should be less than 300mVpp in design. When the module operates with the maximum emission power, the maximum operating current can reach 2.5A, so the power source should be not lower than 3.135V, or the module may shut down or reboot. The power supply limits are shown in Figure 5:

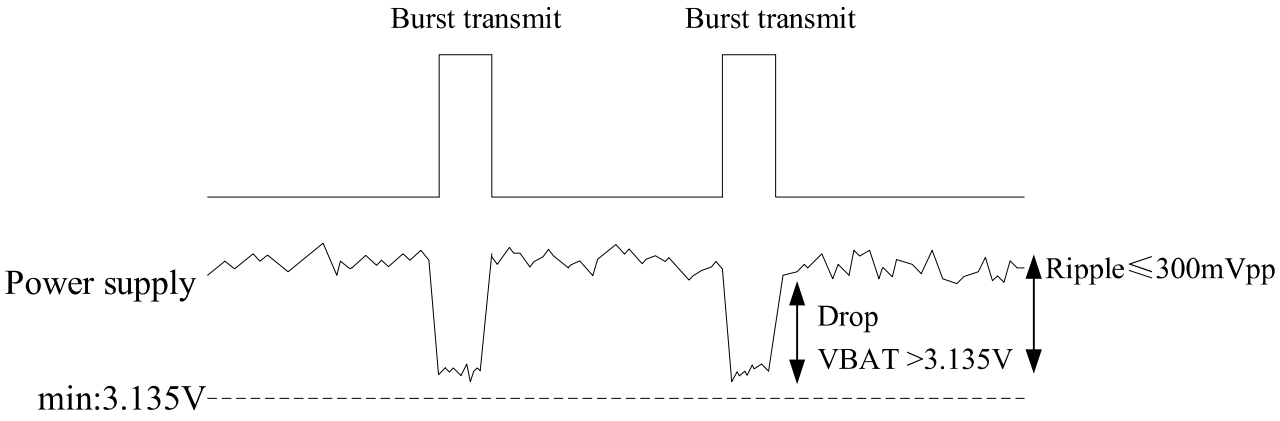

Figure 5. Power supply requirement

3.2.2 Logic Level

The FM101 module 1.8V logic level definition is shown in the following table:

Table 9. Module 1.8V logic level definition

Parameter	Minimum	Typical	Maximum	Unit
V_{OH}[1)]	1.71	1.8	1.89	V
V_{IH}[2)]	1.3	1.8	1.89	V
V_{IL}[3)]@1mA	-0.3	0	0.3	V

The FM101 module 3.3V logic level definition is shown in the following table:

Table 10. Module 3.3V logic level definition

Parameter	Minimum	Typical	Maximum	Unit
V_{IH}[2)]	2.3	3.3	3.465	V
V_{IL}[3)]@1mA	-0.3	0	0.3	V

1) V_{OH}: Output high level effective voltage.
2) V_{IH}: Input high level effective voltage.
3) V_{IL}: Input low level effective voltage.

3.2.3 Power Consumption

In the condition of 3.3V power supply, the FM101 power consumption is shown in the following table:

Table 11. Power consumption

Parameter	Mode	Condition	Typical Current (mA)
I_{off}	Power off	Power supply, module power off	TBD
I_{Sleep}	WCDMA	DRX=6	TBD
		DRX=8	TBD
		DRX=9	TBD
	LTE FDD	Paging cycle #128 frames (1.28s DRx cycle)	TBD
	LTE TDD	Paging cycle #128 frames (1.28s DRx cycle)	TBD
	Radio Off	AT+CFUN=4, flight mode	TBD
$I_{WCDMA-RMS}$	WCDMA	WCDMA Data call Band 1 @23.5dBm	TBD
		WCDMA Data call Band 2 @23.5dBm	TBD
		WCDMA Data call Band 4 @23.5dBm	TBD
		WCDMA Data call Band 5 @23.5dBm	TBD
		WCDMA Data call Band 6 @23.5dBm	TBD
		WCDMA Data call Band 8 @23.5dBm	TBD
		WCDMA Data call Band 19 @23.5dBm	TBD
$I_{LTE-RMS}$	LTE FDD	LTE FDD Data call Band 1 @23dBm	TBD

Parameter	Mode	Condition	Typical Current (mA)
		LTE FDD Data call Band 2 @23dBm	TBD
		LTE FDD Data call Band 3 @23dBm	TBD
		LTE FDD Data call Band 4 @23dBm	TBD
		LTE FDD Data call Band 5 @24dBm	TBD
		LTE FDD Data call Band 7 @23dBm	TBD
		LTE FDD Data call Band 8 @24dBm	TBD
		LTE FDD Data call Band 12 @24dBm	TBD
		LTE FDD Data call Band 13 @24dBm	TBD
		LTE FDD Data call Band 14 @24dBm	TBD
		LTE FDD Data call Band 17 @24dBm	TBD
		LTE FDD Data call Band 18 @24dBm	TBD
		LTE FDD Data call Band 19 @24dBm	TBD
		LTE FDD Data call Band 20 @24dBm	TBD
		LTE FDD Data call Band 25 @23dBm	TBD
		LTE FDD Data call Band 26 @24dBm	TBD
		LTE FDD Data call Band 28 @24dBm	TBD
		LTE FDD Data call Band 30 @22dBm	TBD
		LTE FDD Data call Band 66 @23dBm	TBD
		LTE FDD Data call Band 71 @24dBm	TBD
	LTE TDD	LTE TDD Data call Band 38 @23dBm	TBD

Parameter	Mode	Condition	Typical Current (mA)
		LTE TDD Data call Band 39 @23dBm	TBD
		LTE TDD Data call Band 40 @23dBm	TBD
		LTE TDD Data call Band 41 @23dBm	TBD
		LTE TDD Data call Band 41 @26dBm	TBD
		LTE TDD Data call Band 42 @23dBm	TBD
		LTE TDD Data call Band 43 @23dBm	TBD
		LTE TDD Data call Band 48 @21dBm	TBD

The above data is the average value obtained by testing the sample for high/medium/low channels in room temperature(ambient 25℃). LTE TDD test is under the uplink downlink configuration 1 condition.

3.3 Control Signal

The FM101 module provides two control signals for power on/off and reset operations. The pin is defined in the following table:

Table 12. Control signal

Pin	Pin Name	I/O	Reset Value	Function	Level
6	FULL_CARD_POWER_OFF#	DI	PU	Module power on/off input, internal pull up (22KΩ) Power on: High/Floating Power off: Low	3.3/1.8V
67	RESET#	DI	PU	WWAN reset input, active low, internal pull up (22KΩ)	1.8V

RESET# needs to be controlled by independent GPIO, and not shared with other devices on the host. RESET# is sensitive signal, so it should be kept away from RF interference and protected by ground. It should be neither near PCB edge nor route on surface layer to avoid being reset abnormally caused by ESD.

3.3.1 Module Start-Up

3.3.1.1 Start-up Circuit

The FCPO# (FULL_CARD_POWER_OFF #) pin needs an external 3.3V or 1.8V pull up for booting up. AP (Application Processor) controls the module start-up. The recommended design is using a default PD port to control FCPO#. It also should reserve a 100KΩ(NC) pull down resistor on AP side. The circuit design is shown in Figure:

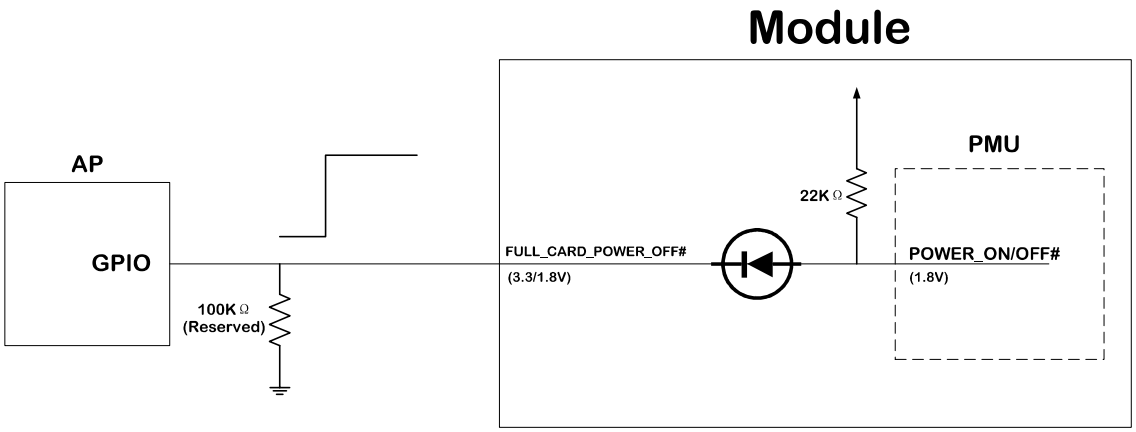

Figure 6. Circuit for module start-up controlled by AP

3.3.1.2 Start-up Timing Sequence

When power supply is ready, the PMU of module will power on and start initialization process by pulling high FCPO# signal. After about TBDs, module will complete initialization process. The start-up timing is shown in Figure:

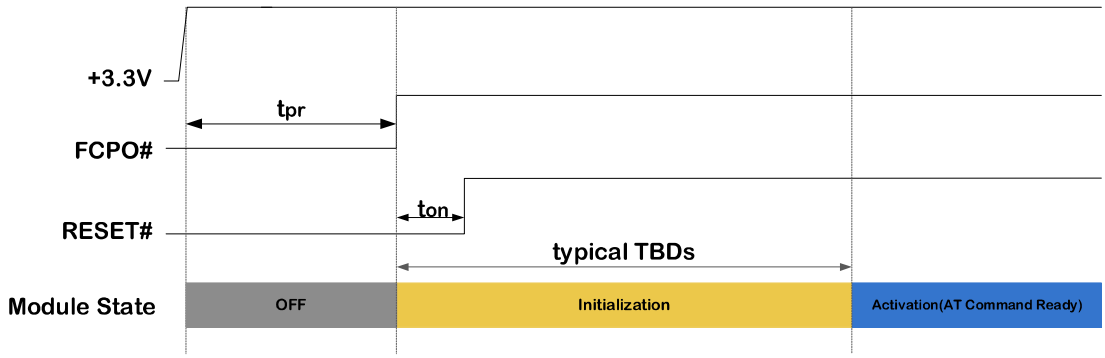

Figure 7. Timing control for start-up

Index	Min.	Recommended	Max.	Comment
t_{pr}	0ms	-	-	The delay time of power supply rising from 0V up to 3.135 V stably. If power supply always ready, it can be ignored.
t_{on}	8ms	20ms	-	The time from FCPO# high to RESET# high.

3.3.2 Module Shutdown

The module can be shut down by the following controls:

Shutdown Control	Action	Condition
Software (Recommend)	Sending AT+CPWROFF command, and then pull down RESET# and FCPO# pin	Normal operation status.
Hardware	Pull down RESET# and FCPO# pin	No response after sent the AT+CPWROFF

The module can be shut down by sending AT+CPWROFF command. When the module receives the software shutdown command, the module will start the finalization process (the reverse process of initialization), and it will be completed after tsd time (tsd is the waiting time from AP send AT+CPWROFF to AP receive OK, the max tsd is 5s). The control timing is shown in Figure 8:

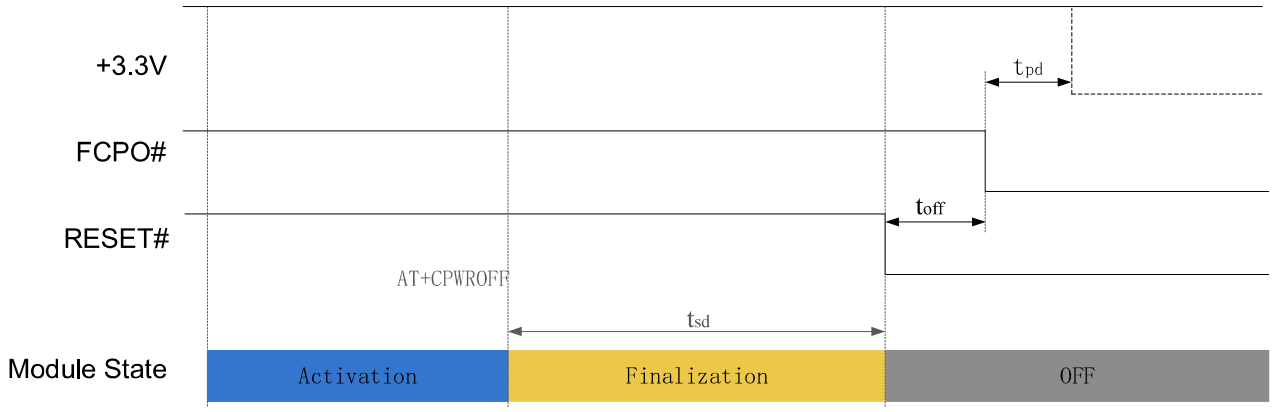

Figure 8. Recommend control power off timing

Index	Min.	Recommended	Max.	Comment
t_{pd}	10ms	100ms	-	The time for +3.3V delay time of shutdown. If + 3.3V keeps constant supply, the delay time can be ignored.
t_{off}	20ms	20ms	-	The time difference between the RESET # signal and the FULL_CARD_POWER_OFF # signal.
t_{sd}	0	-	5s	Waiting time from AP send AT+CPWROFF to AP receive OK

3.3.3 Module Reset

The FM101 module can reset to its initial status by pulling down the RESET# signal for more than

20ms, and module will restart after RESET# signal is released. When customer executes RESET# function, the PMU power will be turned off. The recommended circuit design is shown in the Figure 9:

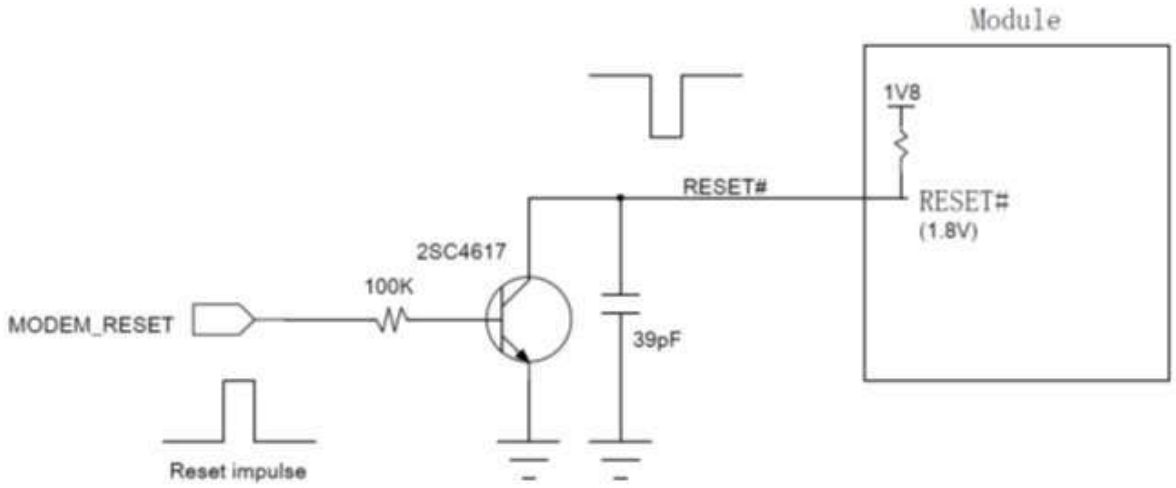

Figure 9. Recommended design for reset circuit

There are two reset control timings as below:

- Reset timing 1st in Figure 10, PMU of module internal always on in reset sequence, recommend using in FW upgrade and module recovery;
- Reset timing 2nd in Figure 11, PMU of module internal will be off in reset sequence (including whole power off and power on sequence, t_{sd} can refer section 3.3.2), recommend using in system warm boot.

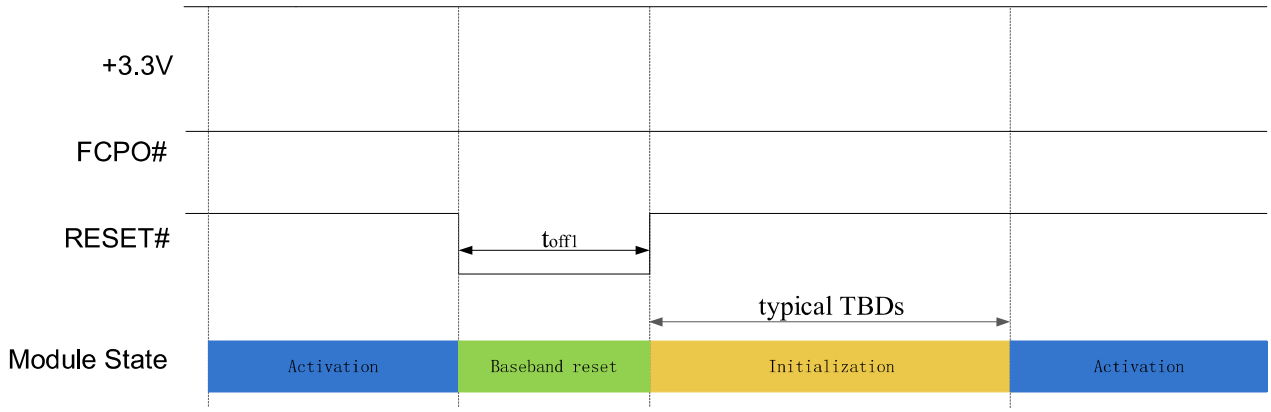

Figure 10. Reset timing 1st

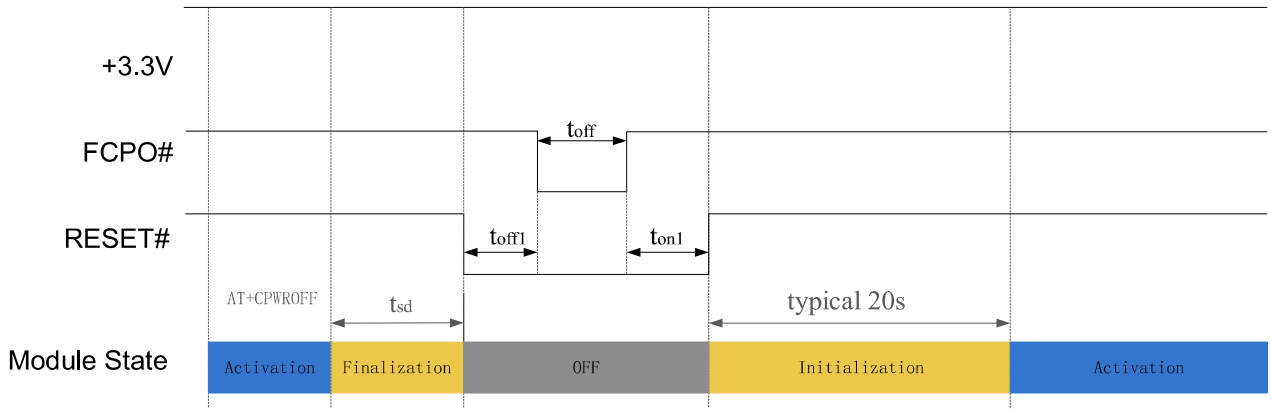

Figure 11. Reset timing 2nd

Index	Min.	Recommended	Max.	Comment
t_{off1}	20ms	20ms	-	FCPO# should be asserted after RESET#, refer section 3.3.2
t_{off}	500ms	500ms	-	Time to allow the WWAN module to fully discharge any residual voltages before the pin could be de-asserted again. This is required for both Pre-OS as well as Runtime flow
t_{on1}	8ms	20ms	-	RESET# should be de-asserted after FCPO# assert to high, refer section 3.3.1.2

RESET# is a sensitive signal, it's recommended to add a filter capacitor close to the module. In case of PCB layout, the RESET# signal lines should keep away from the RF interference and protected by GND. Also, the RESET# signal lines shall neither near the PCB edge nor route on the surface planes to avoid module from reset caused by ESD problems.

3.4 USIM Interface

The FM101 module has Dual SIM (one embedded eSIM and USIM interface)., USIM interface

supports 1.8V/3V SIM card.

3.4.1 USIM Pins

The USIM pins description is shown in the following table:

Pin	Pin Name	I/O	Reset Value	Description	Type
36	UIM1_PWR	PO	-	USIM power supply	1.8V/3V
30	UIM1_RESET	O	-	USIM reset	1.8V/3V
32	UIM1_CLK	O	-	USIM clock	1.8V/3V
34	UIM1_DATA	I/O	-	USIM data, internal pull up(4.7KΩ)	1.8V/3V
66	SIM1_DETECT	I	PD	USIM card detect, internal 390 KΩ pull-up. Active high, and high level indicates SIM card is inserted; and low level indicates SIM card is detached.	1.8V

3.4.2 USIM Interface Circuit

3.4.2.1 N.C. SIM Card Slot

The reference circuit design for N.C. (Normally Closed) SIM card slot is shown in Figure 12:

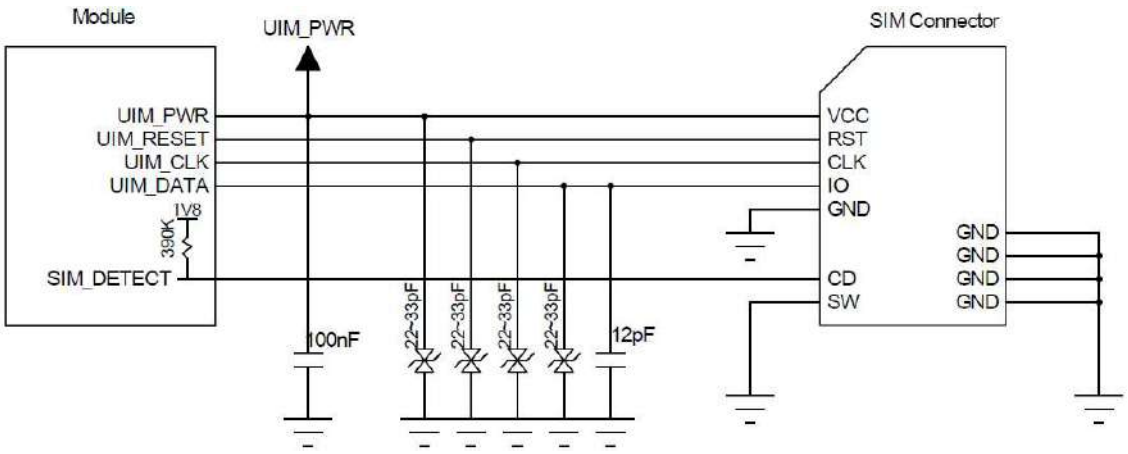

Figure 12. Reference circuit for N.C. SIM card slot

The principles of the N.C.SIM card slot are described as follows:

- When the SIM card is detached, it connects the short circuit between CD and SW pins, and drives the SIM1_DETECT pin low.
- When the SIM card is inserted, it connects an open circuit between CD and SW pins, and drives the SIM1_DETECT pin high.

3.4.2.2 N.O. SIM Card Slot

The reference circuit design for N.O. (Normally Open) SIM card slot is shown in Figure 13:

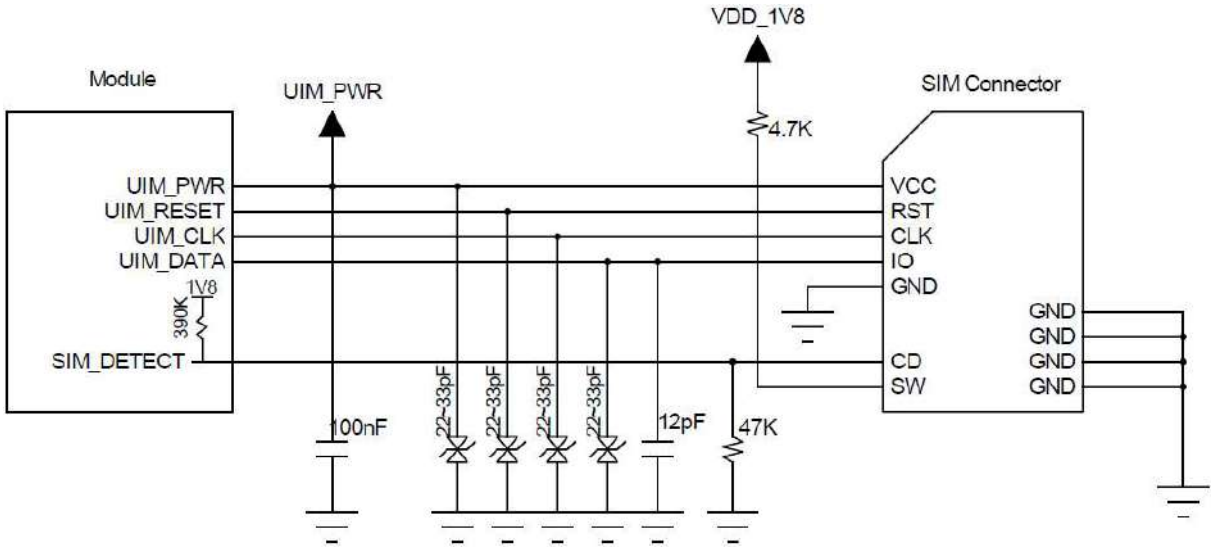

Figure 13. Reference circuit for N.O. SIM card slot

The principles of the N.O.SIM card slot are described as follows:

- When the SIM card is detached, it connects an open circuit between CD and SW pins, and drives the SIM_DETECT pin low.
- When the SIM card is inserted, it connects the short circuit between CD and SW pins, and drives the SIM_DETECT pin high.

3.4.3 USIM Hot-Plug

The FM101 module supports the SIM card hot-plug function, which determines whether the SIM

card is inserted or detached by detecting the SIM_DETECT pin state of the SIM card slot.

The SIM card hot-plugging function can be configured by AT+MSMPD command, and the description for AT command is shown in the following table:

AT Command	Hot-plug Detection	Function Description
AT+MSMPD=1	Enable	Default value, the SIM card hot-plug detection function is enabled. The module can detect whether the SIM card is inserted or not through the SIM_DETECT pin state.
AT+MSMPD=0	Disable	The SIM card hot-plug detect function is disabled. The module reads the SIM card when starting up, and the SIM_DETECT status will not be detected.

After the SIM card hot-plugging detection function is enabled, the module detects that the SIM card is inserted when the SIM_DETECT pin is high, then executes the initialization program and finish the network registration after reading the SIM card information. When the SIM_DETECT pin is low, the module determines that the SIM card is detached and does not read the SIM card.

SIM_DETECT is active high. It can be swapped to active low by AT CMD.

3.4.4 USIM Design

The SIM card circuit design should meet the EMC standards and ESD requirements with the improved capability to resist interference, to ensure that the SIM card can work stably. The following guidelines should be noted in design:

- The SIM card slot should be placed as close as possible to the module, and away from the RF antenna, DC/DC power supply, clock signal lines, and other strong interference sources.
- The SIM card slot with a metal shielding housing can improve the anti-interference ability.

- The trace length between the SIM card slot and the module should not exceed 100mm, or it could reduce the signal quality.
- The UIM_CLK and UIM_DATA signal lines should be isolated by GND to avoid crosstalk interference. If it is difficult for the layout, the whole SIM signal lines should be wrapped with GND as a group at least.
- The filter capacitors and ESD devices for SIM card signals should be placed near to the SIM card slot, and the ESD devices with 22~33pF capacitance should be used.

3.4.5 USB 3.0 Interface Application

The reference circuit is shown in Figure 14:

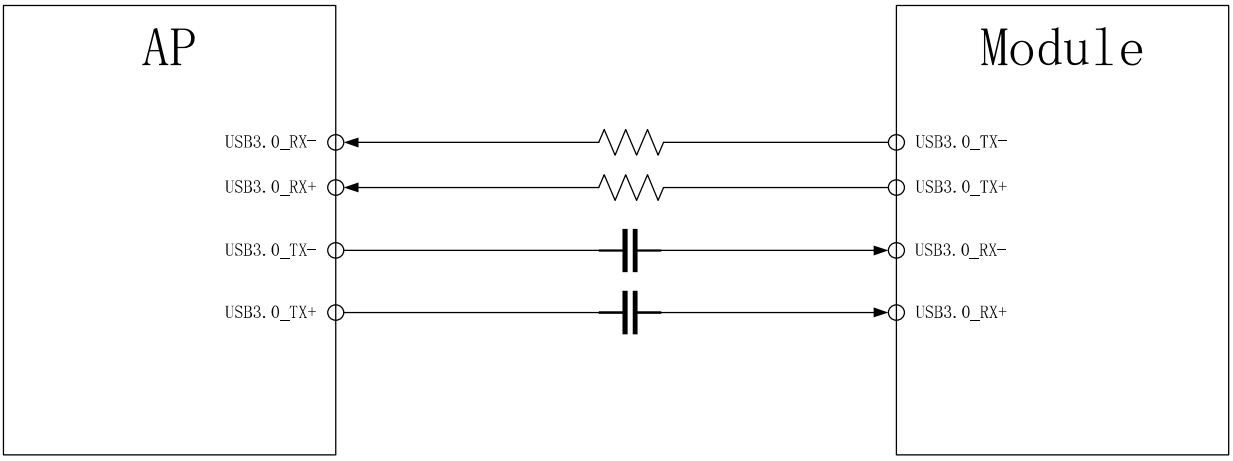

Figure 14. Reference circuit for USB 3.0 interface

USB 3.0 signals are super speed differential signal lines with the maximum transfer rate of 5Gbps. So the following rules should be followed carefully in the case of PCB layout:

- USB 3.0_TX-/USB 3.0_TX+ and USB 3.0_RX-/ USB 3.0_RX+ are two pairs differential signal lines. The differential impedance should be controlled as 90Ω.
- The two pairs differential signal lines should be parallel and have the equal length. The right angle routing should be avoided.
- The two pairs differential signal lines should be routed on the layer that is adjacent to the ground layer, and wrapped with GND vertically and horizontally.

3.5 Status Indicator

The FM101 module provides two signals to indicate the operating status of the module, and the status indicator pins is shown in the following table:

Pin	Pin Name	I/O	Reset Value	Pin Description	Level
10	LED1#	OD	T	System status LED, drain output.	3.3V
23	WOWWAN#	DO	PD	Wake up host, default low, Reserved	1.8V

3.5.1 LED#1 Signal

The LED#1 signal is used to indicate the operating status of the module, and the detailed description is shown in the following table:

Module Status	LED1# Signal
RF function ON	Low level (LED on)
RF function OFF	High level (LED off)

The LED driving circuit is shown in figure 15:

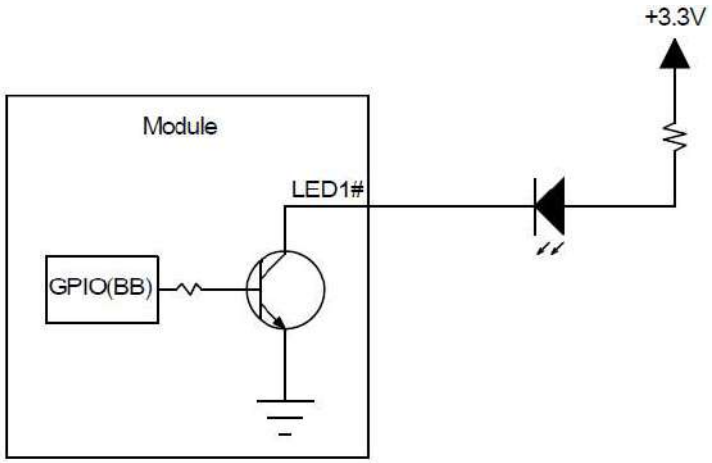

Figure 15. LED driving circuit

The resistance of LED current-limiting resistor is selected according to the driving voltage and the driving current.

3.6 Interrupt Control

The FM101 module provides two interrupt signals, and the pin definitions are as follows:

Pin	Pin Name	I/O	Reset Value	Pin Description	Type
8	W_DISABLE1#	I	PU	WWAN disable, default high, active low	3.3/1.8V
25	DPR	I	PD	Dynamic power reduction detect, default high, active low	3.3/1.8V

3.6.1 W_DISABLE1#

The module provides a hardware pin to enable/disable WWAN RF function, need AT+GTFMODE=1 to enable this function and the function can also be controlled by the AT command. The module enters into flight mode after the RF function is disabled. The definition of W_DISABLE1# signal is as follows:

W_DISABLE1# signal	Function
High/Floating	WWAN function is enabled, the module exits the flight mode.
Low	WWAN function is disabled, the module enters into flight mode.

The function of W_DISABLE1# is disabled in default. It can be enabled by customer's request.

3.6.2 DPR

The FM101 module supports BodySAR function by detecting the DPR pin. The voltage level of DPR is high by default, and when the SAR sensor detects the closing human body, the DPR signal will be pulled down. As the result, the module then lowers down its emission power to its default threshold value, thus reducing the RF radiation on the human body. The threshold of emission power can be set by the AT Commands. The definition of DPR signal is shown in the following table:

DPR Signal	Function
High/Floating	The module keeps the default emission power
Low	Lower the maximum emission power to the threshold value of the module.

3.7 ANT Tunable Interface

The module supports ANT Tunable interfaces with two different control modes, i.e. MIPI interface and 4bit GPO interface. Through cooperating with external antenna adapter switch via ANT tunable, it can flexibly configure the bands of WCDMA and LTE antenna to improve the antenna's working efficiency and save space for the antenna. Module also support 1.8V output for antenna tuner. The pin definition is as below table:

Pin	Pin Name	I/O	Reset Value	Pin Description	Level
24	ANT_TUNER_1V8	PO	PD	1.8V power output for antenna tuner, reserved	1.8V
56	RFFE_SCLK	O	PD	Tunable ANT control, MIPI Interface, RFFE clock	1.8V
58	RFFE_SDATA	I/O	PD	Tunable ANT control, MIPI Interface, RFFE data	1.8V
59	ANTCTL0	O	PD	Tunable ANT CTRL0, default low	1.8V