TOSHIBA BIPOLAR LINEAR INTEGRATED CIRCUIT SILICON MONOLITHIC

TA31136F, TA31136FN

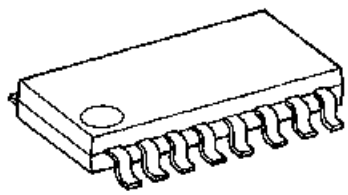
FM IF DETECTOR IC FOR CORDLESS TELEPHONE

Low operation voltage FM IF detector IC. This IC is suitable for cordless telephone.

FEATURES

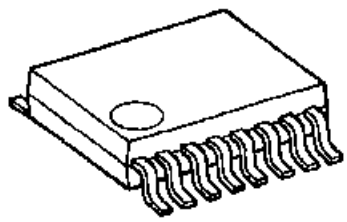
- Low operating voltage : V_{CC} = 1.8~5.5V
- Excellent temperature characteristics
- High sensitivity
  12dB sensitivity : 11dBμV EMF (Input 50Ω)
- High intercept point : 96dBμV (Input 50Ω)
- Quadrature detector, both ceramic and coil discriminators are usable
- Built-in 2nd MIX
  Operating frequency : 10~100MHz
- Built-in noise detection circuit
- RSSI function
- Very small package

TA31136F



SSOP16-P-225-1.00A

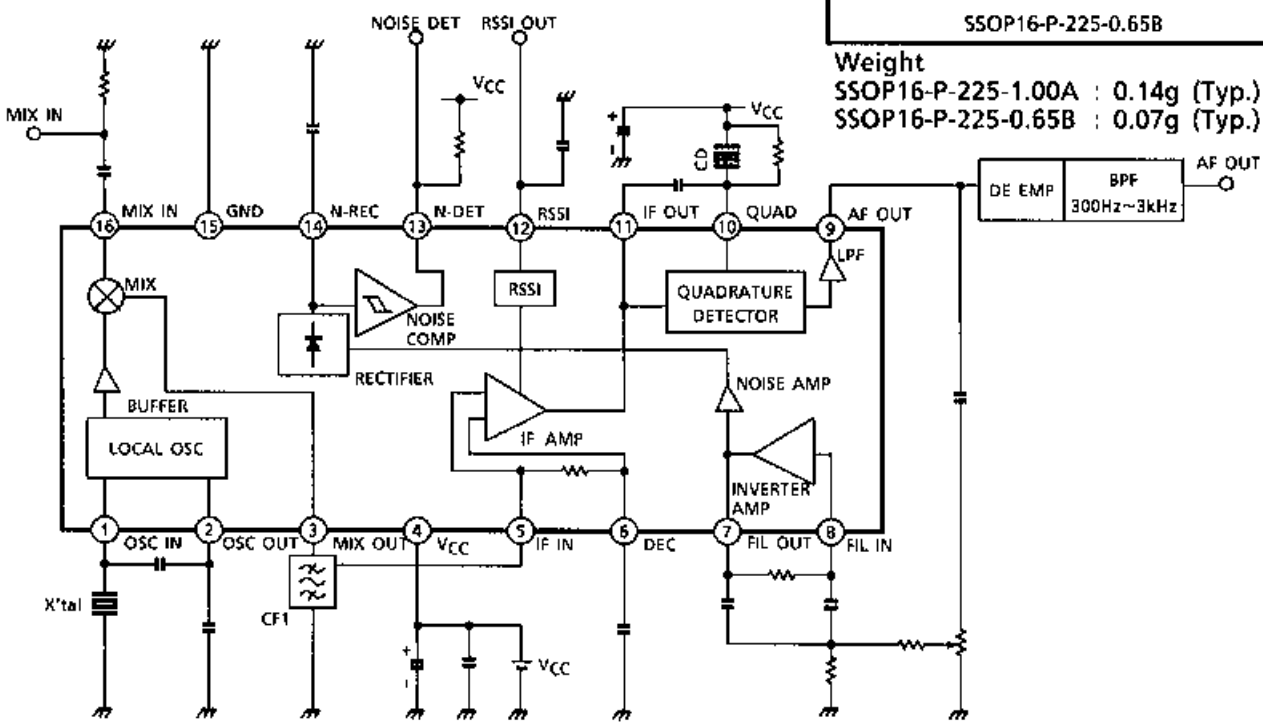
TA31136FN



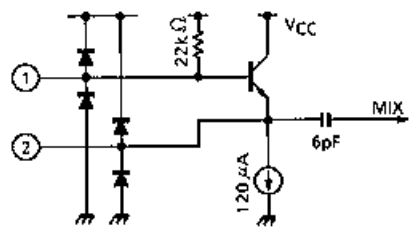
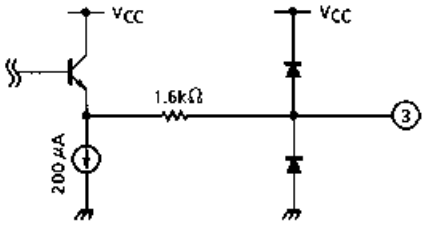
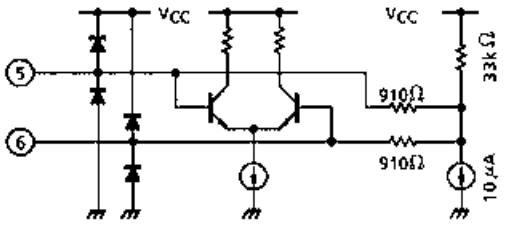
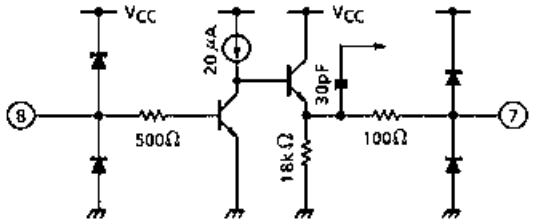
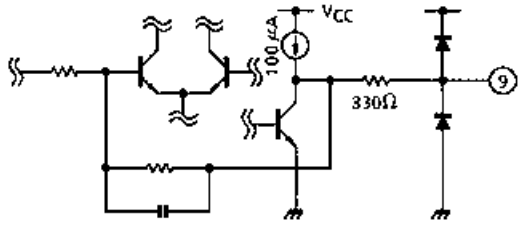
SSOP16-P-225-0.65B

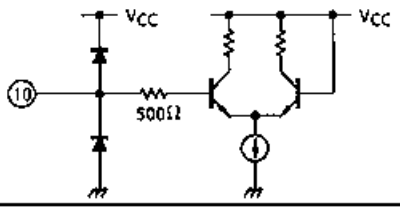
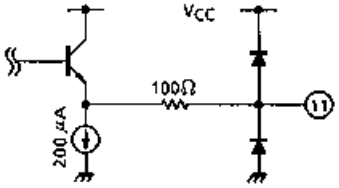
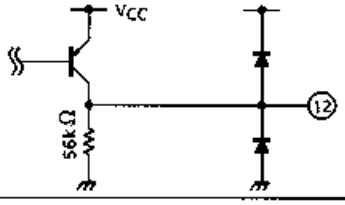
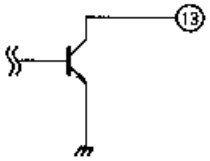
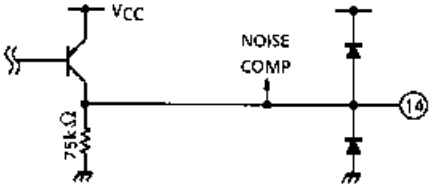
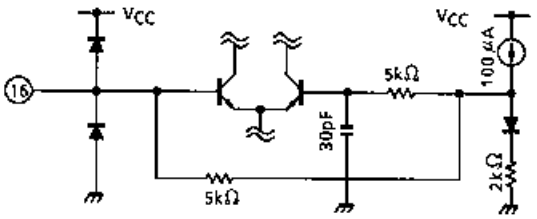
Weight
SSOP16-P-225-1.00A : 0.14g (Typ.)
SSOP16-P-225-0.65B : 0.07g (Typ.)

BLOCK DIAGRAM



PIN FUNCTION (The values of resistor and capacitor are typical.)

PIN No.	PIN NAME	FUNCTION	INTERNAL EQUIVALENT CIRCUIT
1	OSC IN	Local oscillator input and output terminals. Colpitts oscillator is formed by internal emitter follower and external X'tal. And external injection is possible from pin 2 or pin 1.	
2	OSC OUT		
3	MIX OUT	MIX output terminal. Output impedance is around 1.8kΩ.	
4	V_{CC}	Power supply	—
5	IF IN	2nd IF input and decoupling for bias. Input impedance is around 1.8kΩ.	
6	DEC		
7	FIL OUT	INVERTER AMP input and output terminals. BPF is composed of external capacitors and resistors. Connected internally to rectifier circuit by coupling capacitor.	
8	FIL IN		
9	AF OUT	Demodulate signal output terminal. Carrier leak is small as LPF is built-in. Output impedance is around 360Ω.	

PIN No.	PIN NAME	FUNCTION	INTERNAL EQUIVALENT CIRCUIT
10	QUAD	Phase shift signal input terminal of FM demodulator.	
11	IF OUT	Output terminal of IF AMP.	
12	RSSI	This terminal outputs DC level according to input signal level to IF AMP. Dynamic range is around 70dB.	
13	N-DET	The result of noise detection is output by comparing output voltage of N-REC terminal with internal refrence. Hysteresis range is about 100mV and output is open collector.	
14	N-REC	After output of INVERTER AMP amplified around 20dB, noise signal is rectified by external capacitor.	
15	GND	GND terminal.	—
16	MIX IN	1st IF signal input terminal. Input impedance is around 4kΩ at 21.7MHz.	

DESCRIPTION

1. Local oscillator external injection method

Inject as shown in Figure 1, setting the injection level between 95dBμV and 100dBμV. A built-in BUFFER amp. minimizes leakage from the mixer.
Input from pin 1 is possible as shown in Figure 2. However, when the input frequency is high, the level at pin 2 may not be sufficient, causing a decrease in sensitivity.
In such a case, add resistor R_{51} and set the input signal so that signal level at pin 2 is 95~100dBμV.
The input capacitance of pins 1 and 2 is respectively 1.5pF (typ.) and 4.6pF (typ.).

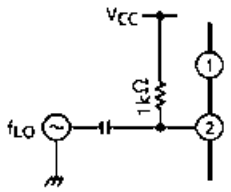


Figure 1

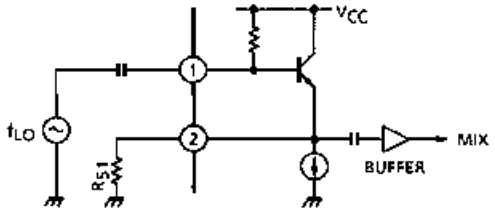


Figure 2

2. Overtone oscillation

Figure 3 shows the basic configuration of the local oscillation circuit using overtone oscillation. The C_{51} and L_1 tuning circuits prevent crystal fundamental oscillation. Therefore, set C_{51} and L_1 to inductive at the fundamental frequency and capacitive at the overtone frequency.
Since the level at pin 2 may decrease and the sensitivity may fall at high frequency as with external injection, adjust the oscillation level using R_{51}.

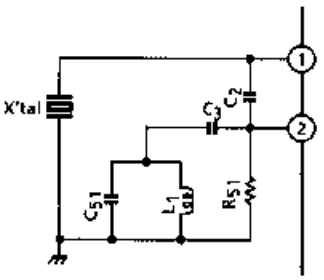
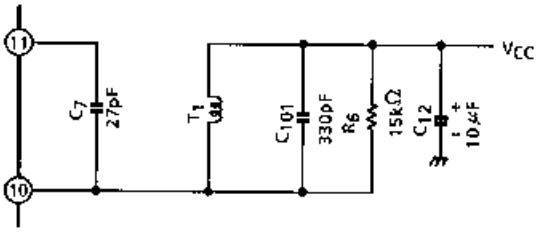


Figure 3

3. Detection circuit

Detection stage is quadrature method.
Oscillator is ceramic discriminator on reference application. In case of using coil, connect as shown in Figure 4. In this case, demodulation output V_{OD} is about 80mV_{rms}. Demodulation output can be increased by raising damping resistance R_3. However, be careful because the temperature dependency of the modulation output also increases.
Center frequency f_0 and demodulation output depends largely on phase shifter and C_7. For C_7, use a capacitor with good temperature characteristics.
In case of coil, especially C_{101}, use a capacitor with good temperature characteristics.



T_1 : 5114-JPS-010
(SUMIDA)

Figure 4

4. Demodulation output distortion factor

Demodulation output distortion factor is about −43dB when ceramic discriminator CDB450C24 used, is about −50dB when coil 5114-JPS-010 used. (IF 100dBμV EMF input, measured pin 9 before when input from MIX demodulation output distortion factor depends largely on a ceramic filter band and a group delay characteristic. Select ceramic filter adequately.

5. INVERTER AMP usage

The INVERTER AMP can be used to form a band pass filter as shown in Figure 4.
Set constants as in equations (1) to (3). However, because a low pass filter and a high pass filter are built in, it is recommended that center frequency f_0 be about 30kHz.

(1) $f_0 = \dfrac{1}{2\pi\sqrt{R_3 (R_4 // R_5) C^2}}$

(2) $G_V = R_3 / 2R_4$

(3) $Q^2 = \dfrac{R_3}{4 (R_4 // R_5)}$

at $R_4 \gg Rp$

Example R_3 = 150kΩ, R_4 = 330kΩ,
R_5 = 3.3kΩ, Rp = 20kΩ (VR)
C = 220pF provide ;
$f_0 \simeq$ 31kHz, $G_V \simeq$ −13dB
Q ≃ 12

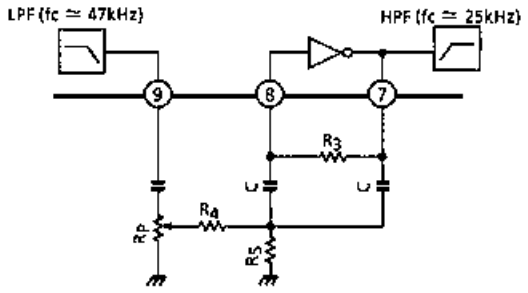


Figure 5

6. Noise detection rise time

The rise time is a proportion of time constant 7.5ms of the smoothing capacitor C_9 = 0.1μF of the noise rectifier and internal resistor 75kΩ. Although decreasing the capacitance of C_9 can shorten the rise time, note that the noise detection output fluctuation may increase. This should be taken into account before use.

7. RSSI function

A DC voltage corresponding to the input level of IF input pins (pin 5) is output to the RSSI pin (P21). While the linear range is about 80dB when V_{CC} = 2V, the range can be expanded to 80dB as in Figure 6.
However, in such a case, note that the temperature characteristics of the RSSI output may alter due to a disparity between the temperature coefficient of the external resistor and the internal resistance of the IC.

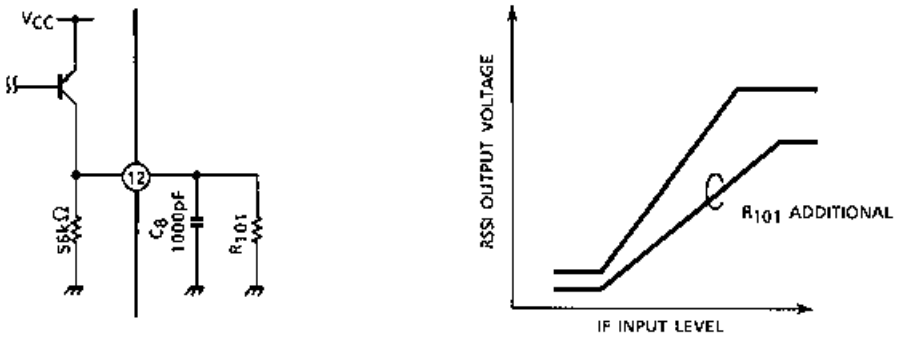


Figure 6

8. DC voltages for pins (Typical values for reference)

V_{CC} = 2.0V

PIN No.	PIN NAME	VOLTAGE	PIN No.	PIN NAME	VOLTAGE
1	OCS IN	1.98	9	AF OUT	—
2	OSC OUT	1.33	10	QUAD	2.0
3	MIX OUT	0.74	11	IF OUT	1.14
4	V_{CC}	2.0	12	RSSI	—
5	IF IN	1.67	13	N-DET	—
6	DEC	1.67	14	N-REC	—
7	FIL OUT	0.67	15	GND	0.0
8	FIL IN	0.65	16	MIX IN	0.94

(UNIT : V)

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Supply Voltage		V_{CC}	7	V
Power Dissipation	TA31136F	P_D	370	mW
	TA31136FN		560	
Operating Temperature		T_{opr}	−30~85	°C
Storage Temperature		T_{stg}	−50~150	°C

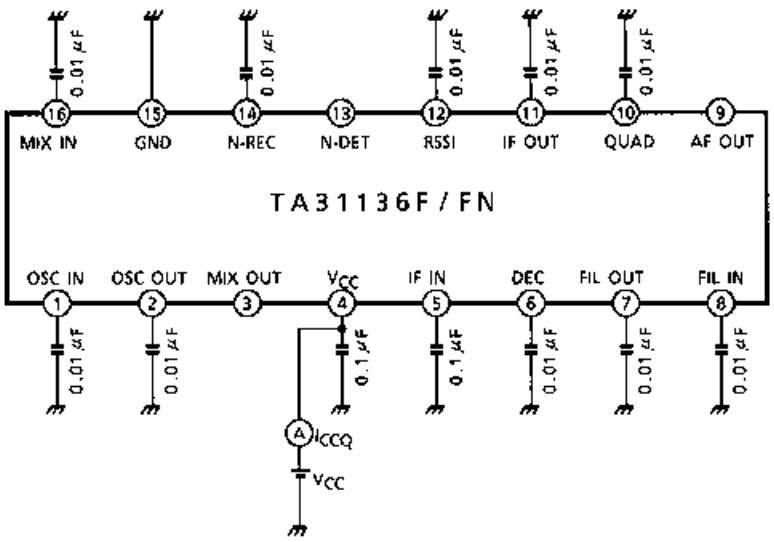
ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, V_{CC} = 2.0V, $f_{IN\ (MIX)}$ = 21.7MHz, $f_{IN\ (IF)}$ = 450kHz, Δf = ± 1.5kHz, f_{MOD} = 1kHz, Ta = 25°C)

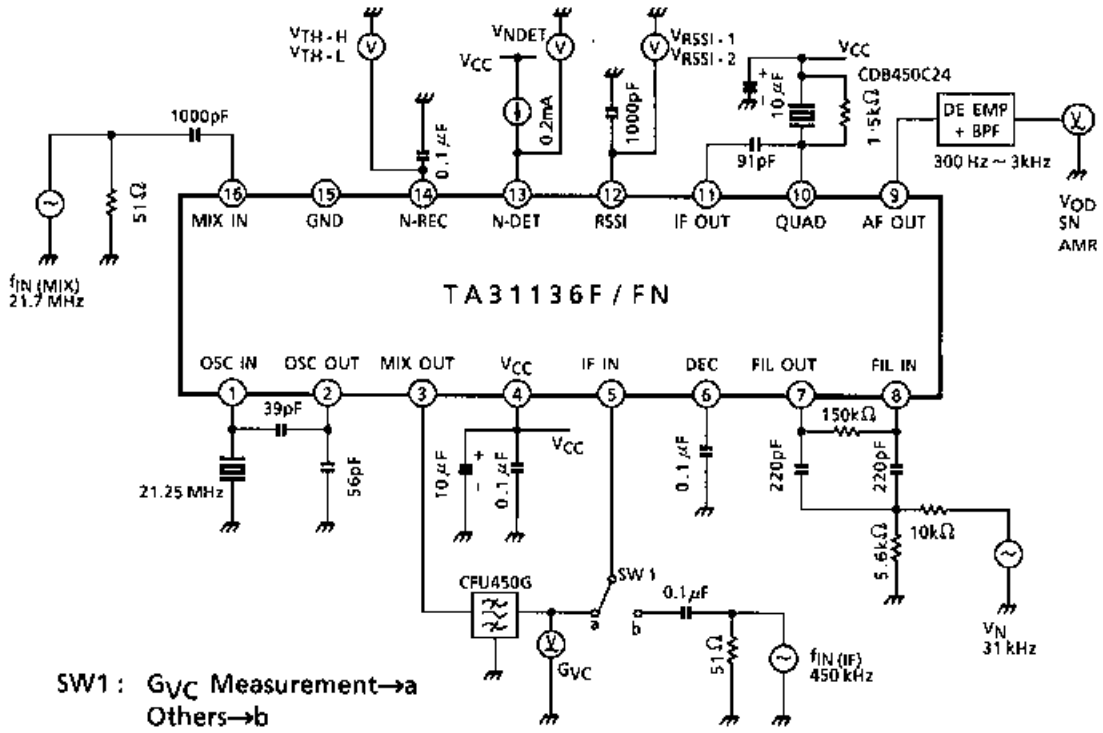
CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION		MIN.	TYP.	MAX.	UNIT
Power Supply Voltage		V_{CC}	—	—		1.8	2.0	5.5	V
Current Consumption		I_{CCQ}	1	—		—	3.2	4.6	mA
Mixer Conversion Gain		G_{VC}	2	Measured through ceramic filter. $V_{IN\ (MIX)}$ = 46dBμV		15	18	21	dB
Mixer Intercept Point		P_{IM}	—	Input 50Ω		—	96	—	dBμV
Mixer Input Impedance		$R_{IN\ (MIX)}$	—	—		—	5.5	—	kΩ
		$C_{IN\ (MIX)}$	—			—	2.8	—	pF
Mixer Output Resistance		$R_{O\ (MIX)}$	—	—		1.2	1.8	2.4	kΩ
12dB Sensitivity		12dB SN	—	—		—	11	—	dBμV
Demodulation Output Level		V_{OD}	2	$V_{IN\ (IF)}$ = 80dBμV		70	100	130	mV_{rms}
SN Ratio		SN	2	$V_{IN\ (IF)}$ = 80dBμV		43	65	—	dB
AM Rejection Ratio		AMR	2	$V_{IN\ (IF)}$ = 80dBμV, AM = 30%		—	40	—	dB
IF AMP. Input Resistance		$R_{IN\ (IF)}$	—	—		1.2	1.8	2.4	kΩ
RSSI Output Voltage		V_{RSSI-1}	2	V_{CC} = 3V	$V_{IN\ (IF)}$ = 30dBμV	200	360	520	mV
		V_{RSSI-2}	2		$V_{IN\ (IF)}$ = 100dBμV	1.4	2.0	2.6	V
Noise Detection Output Voltage		V_{NDET}	2	I SINK = 0.2mA		—	0.1	0.5	V
Noise Detection Output Leak Current		I_{LEAK}	—	V_{NREC} = 0.6V, V_{NDET} = 2V		—	0	5	μA
Noise Detection Level	"H" Level	V_{TH-H}	2	—		—	0.5	0.7	V
	"L" Level	V_{TH-L}				0.3	0.4	—	

All AC levels are indicated by open level (EMF).

TEST CIRCUIT 1

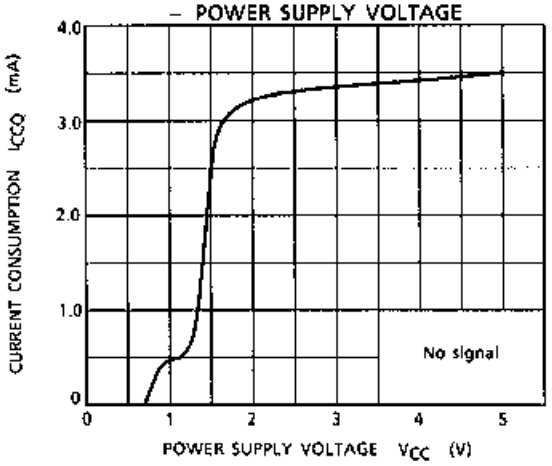


TEST CIRCUIT 2

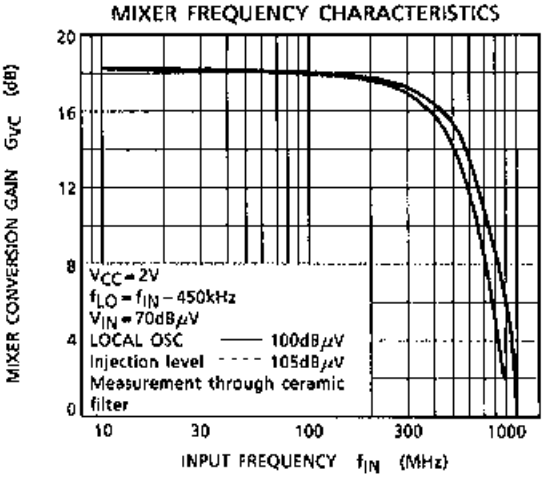


SW1 : G_{VC} Measurement→a
Others→b

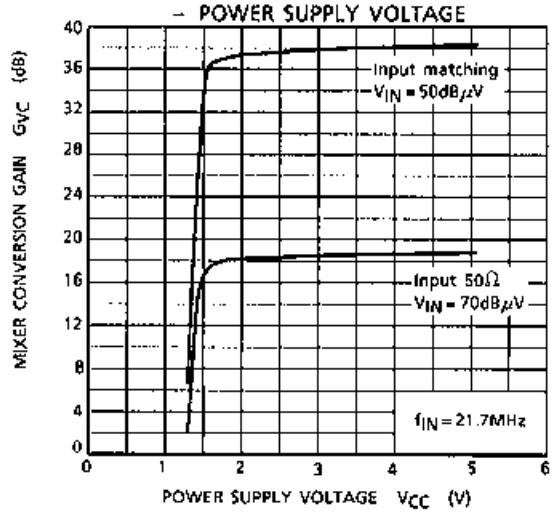
CURRENT CONSUMPTION – POWER SUPPLY VOLTAGE



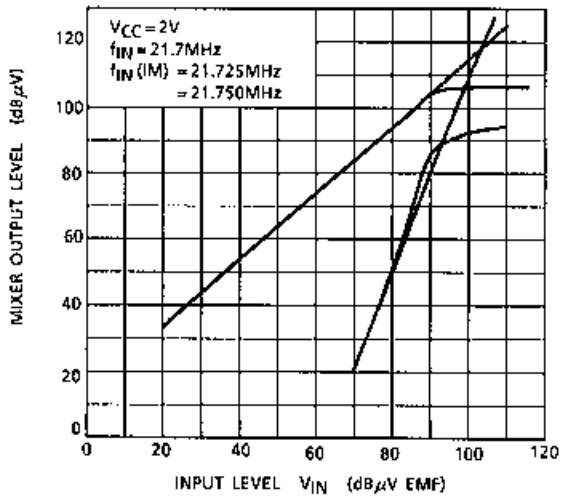
MIXER FREQUENCY CHARACTERISTICS



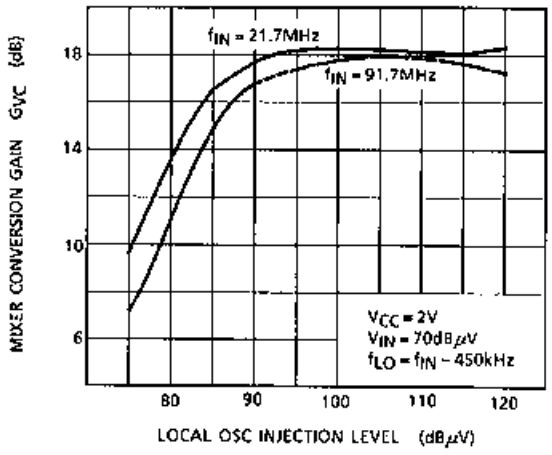
MIXER CONVERSION GAIN – POWER SUPPLY VOLTAGE



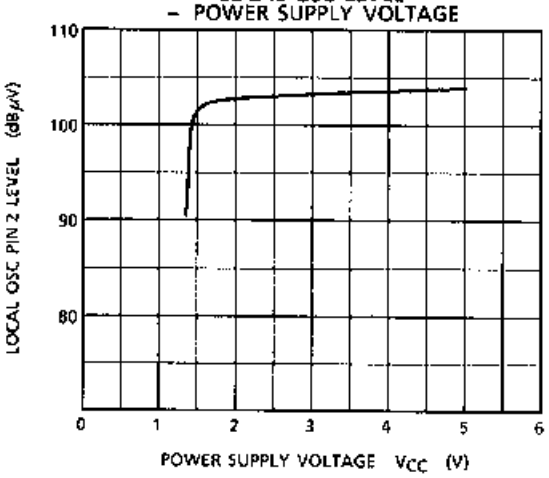
MIXER INTERCEPT POINT CHARACTERISTICS



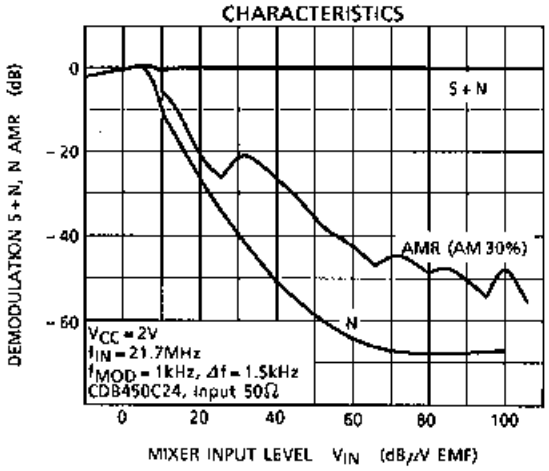
MIXER CONVERSION GAIN – LOCAL OSC INJECTION LEVEL



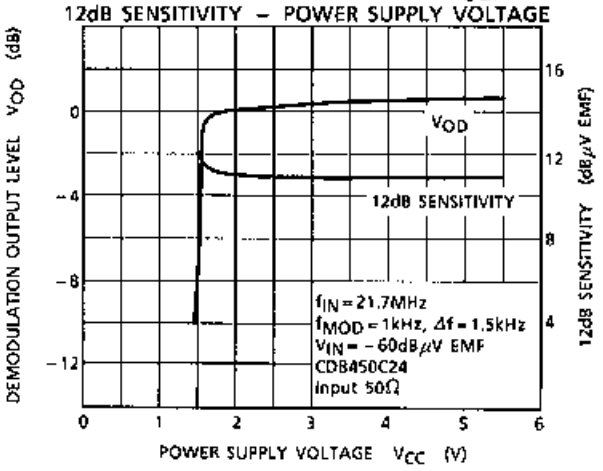
LOCAL OSC LEVEL – POWER SUPPLY VOLTAGE



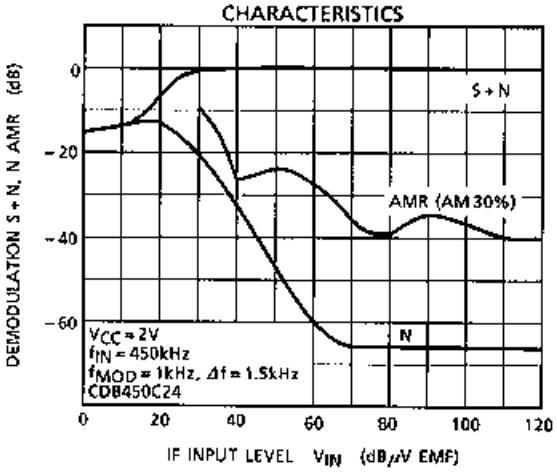
MIXER INPUT DEMODULATION CHARACTERISTICS



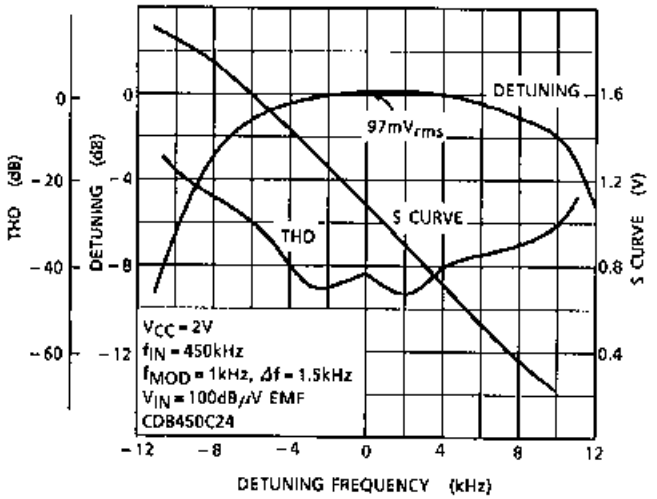
DEMODULATION OUTPUT LEVEL V_{OD}, 12dB SENSITIVITY – POWER SUPPLY VOLTAGE



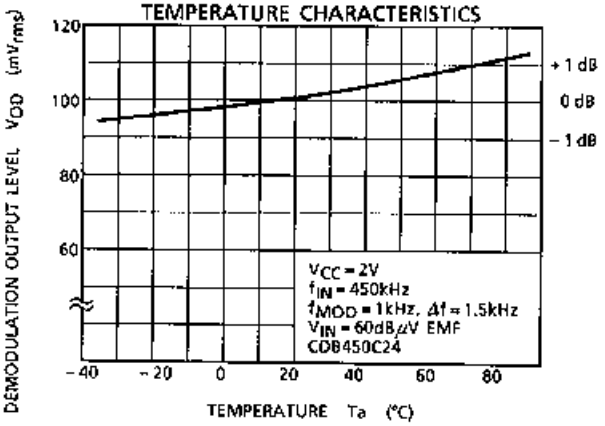
IF INPUT DEMODULATION CHARACTERISTICS



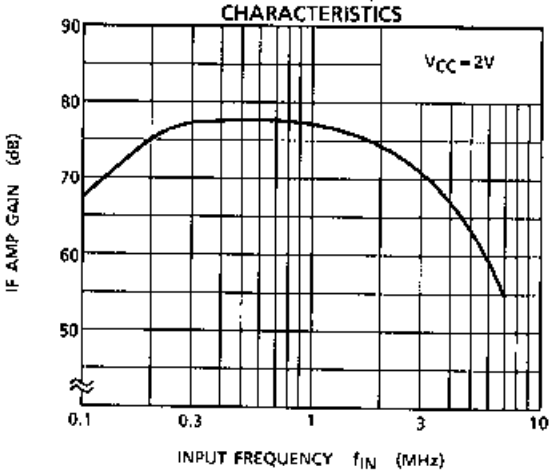
IF INPUT DETUNING CHARACTERISTICS



DEMODULATION OUTPUT LEVEL TEMPERATURE CHARACTERISTICS

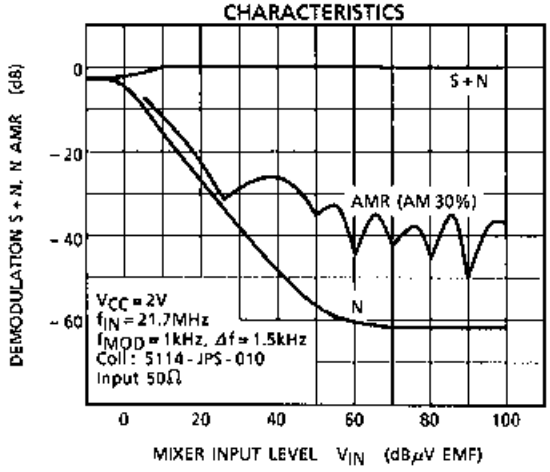


IF AMP GAIN FREQUENCY CHARACTERISTICS

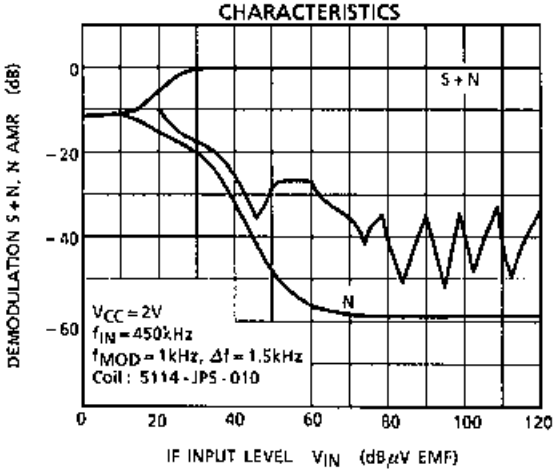


IN COIL DISCRIMINATER USED

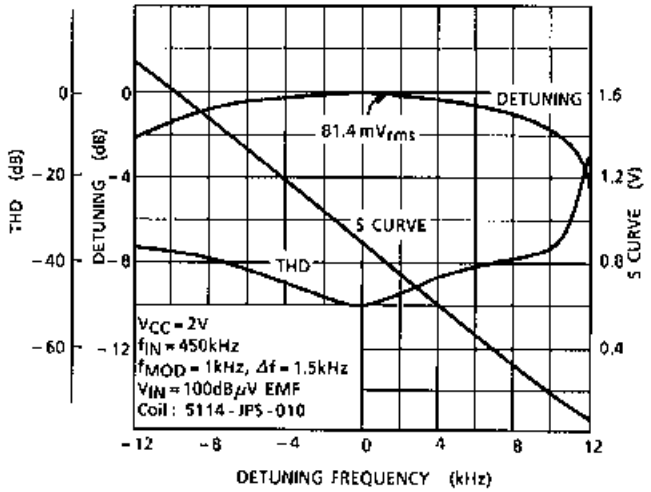
MIXER INPUT DEMODULATION CHARACTERISTICS



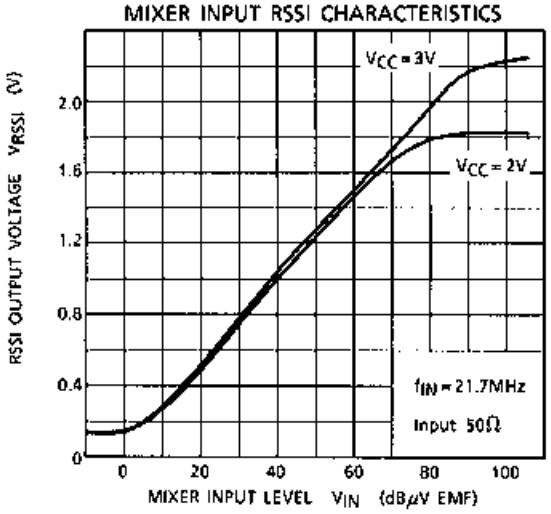
IF INPUT DEMODULATION CHARACTERISTICS



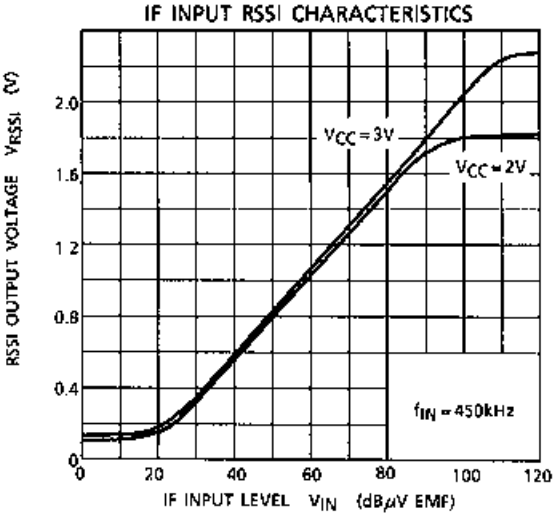
IF DETUNING CHARACTERISTICS



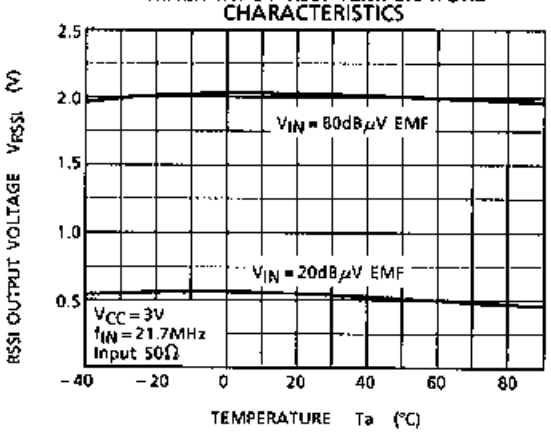
MIXER INPUT RSSI CHARACTERISTICS



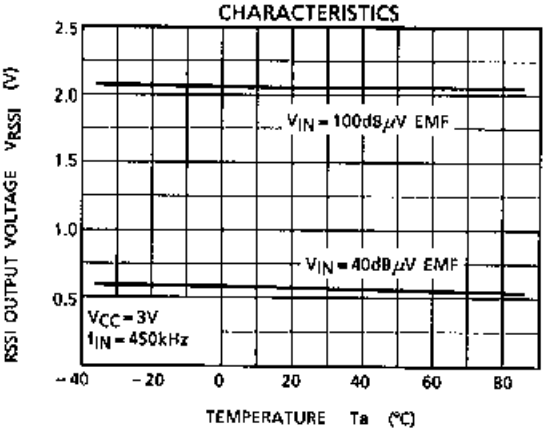
IF INPUT RSSI CHARACTERISTICS



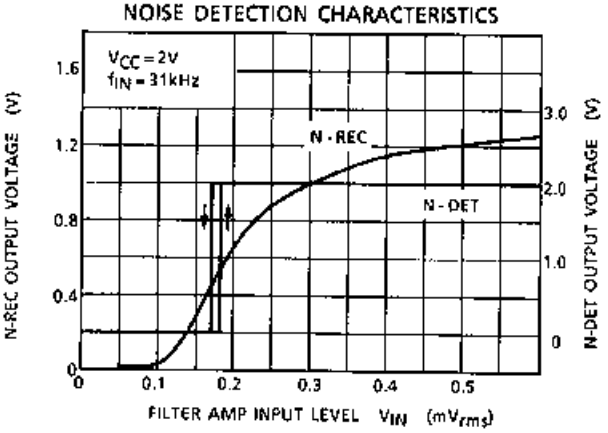
MIXER INPUT RSSI TEMPERATURE CHARACTERISTICS



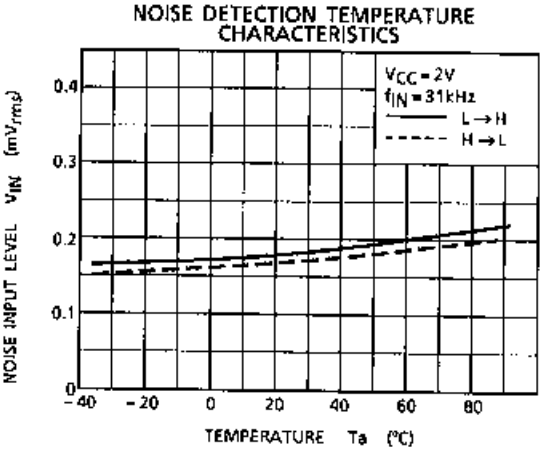
IF INPUT RSSI TEMPERATURE CHARACTERISTICS



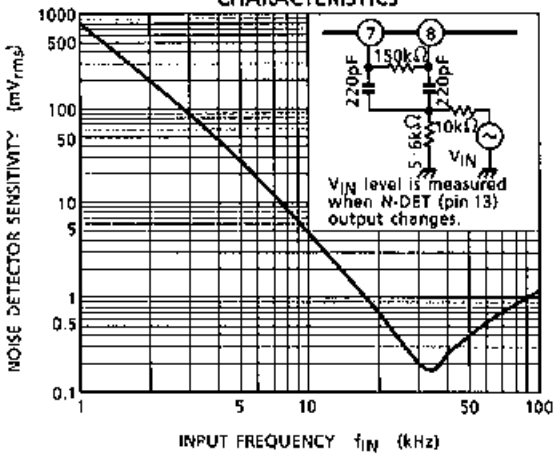
NOISE DETECTION CHARACTERISTICS



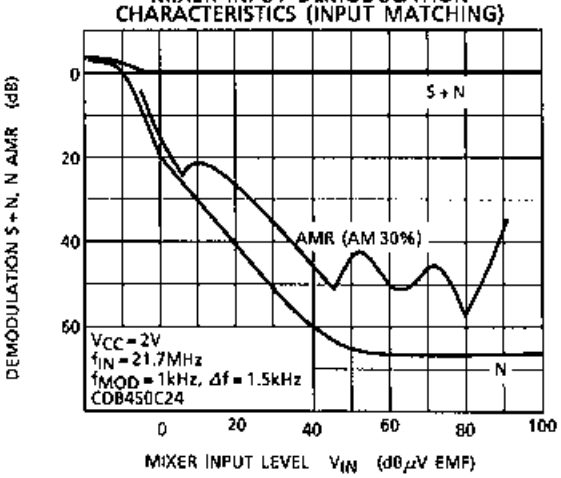
NOISE DETECTION TEMPERATURE CHARACTERISTICS



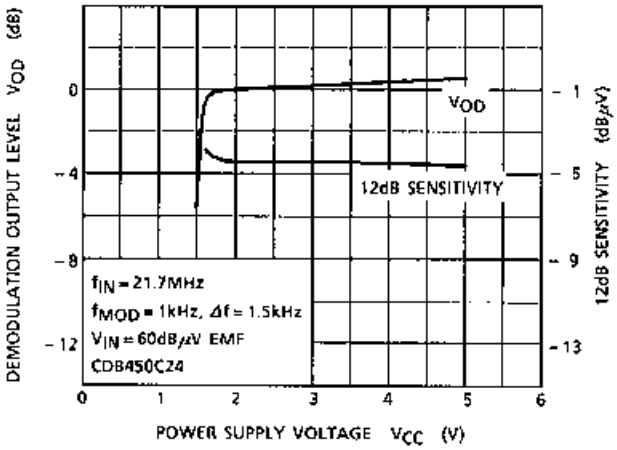
NOISE DETECTION FREQUENCY CHARACTERISTICS



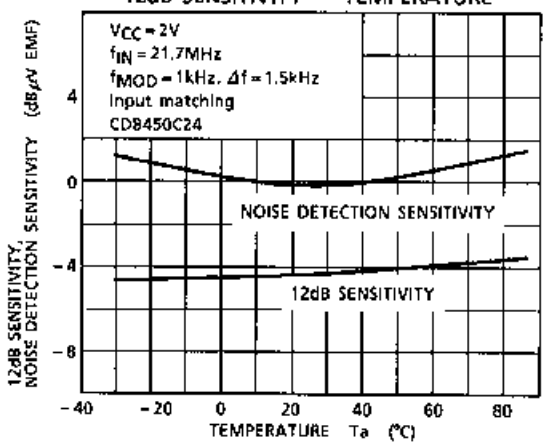
MIXER INPUT DEMODULATION CHARACTERISTICS (INPUT MATCHING)



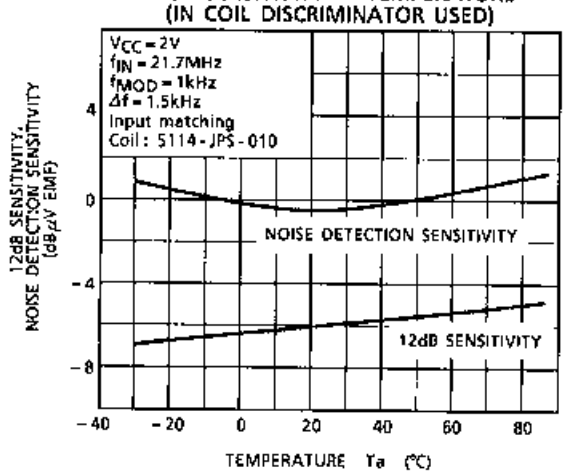
DEMODULATED OUTPUT 12dB SENSITIVITY – POWER SUPPLY VOLTAGE



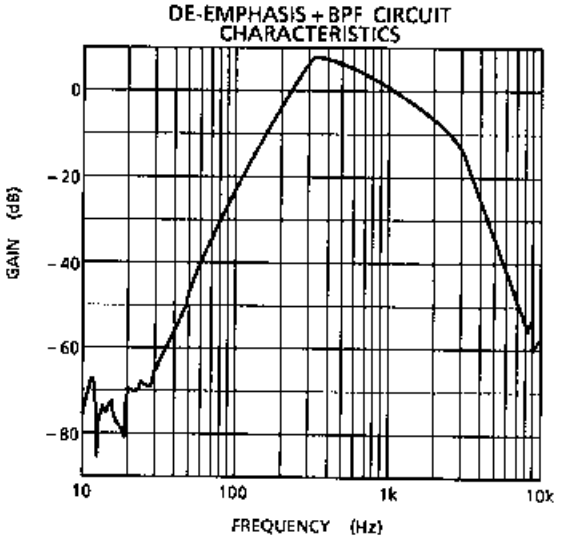
NOISE DETECTION SENSITIVITY, 12dB SENSITIVITY – TEMPERATURE



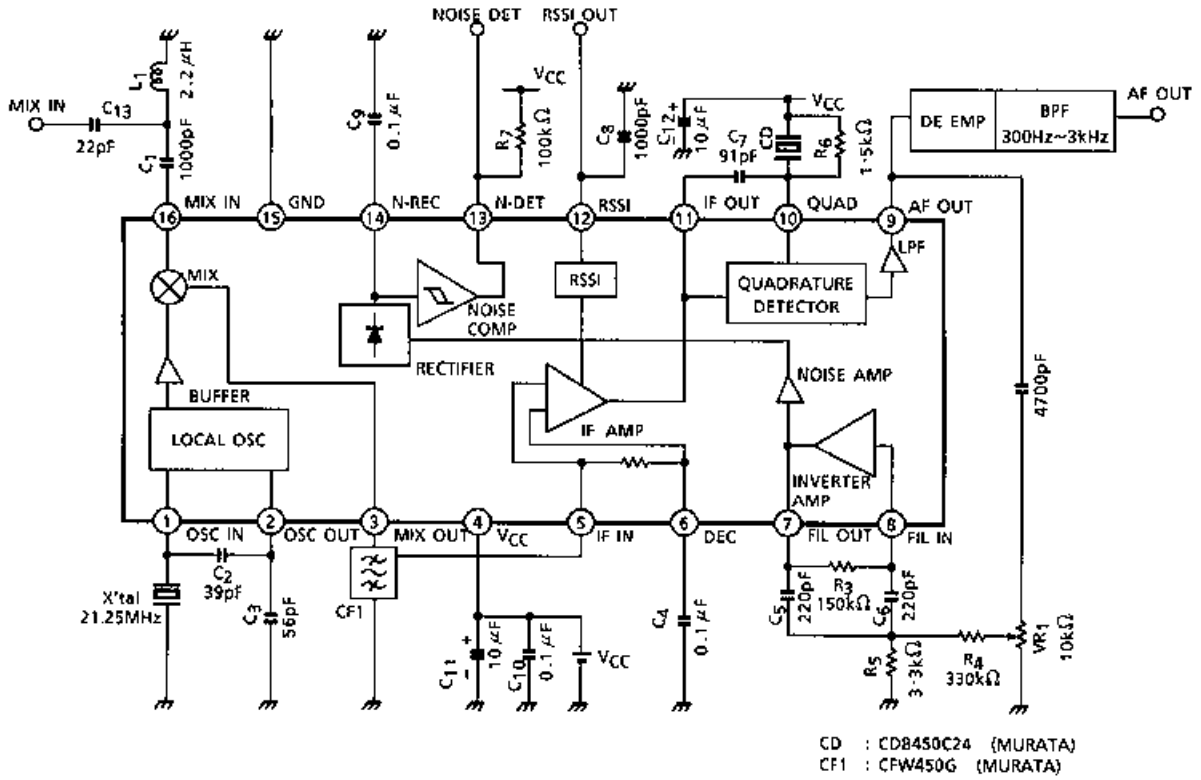
NOISE DETECTION SENSITIVITY, 12dB SENSITIVITY – TEMPERATURE (IN COIL DISCRIMINATOR USED)



DE-EMPHASIS + BPF CIRCUIT CHARACTERISTICS



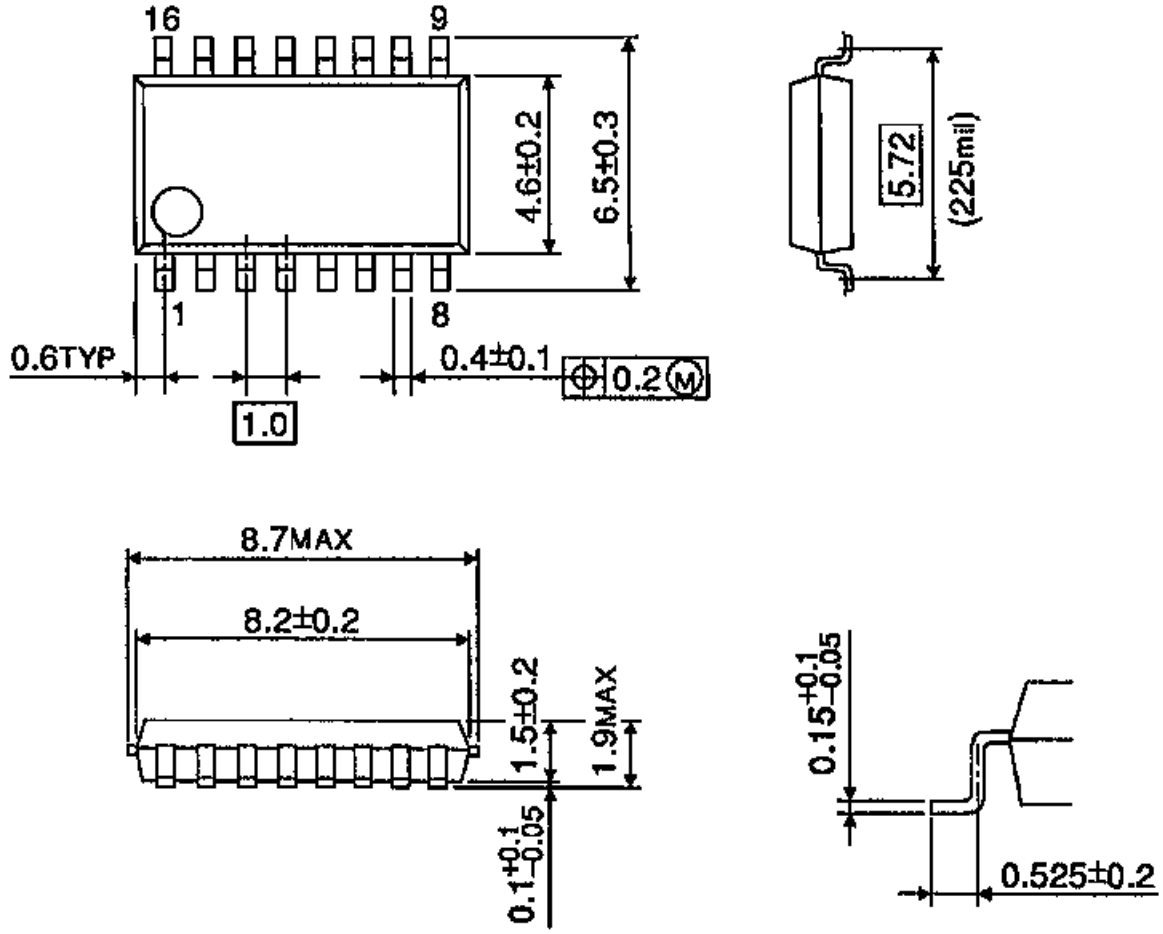
APPLICATION CIRCUIT



PACKAGE DIMENSIONS

SSOP16-P-225-1.00A

Unit : mm

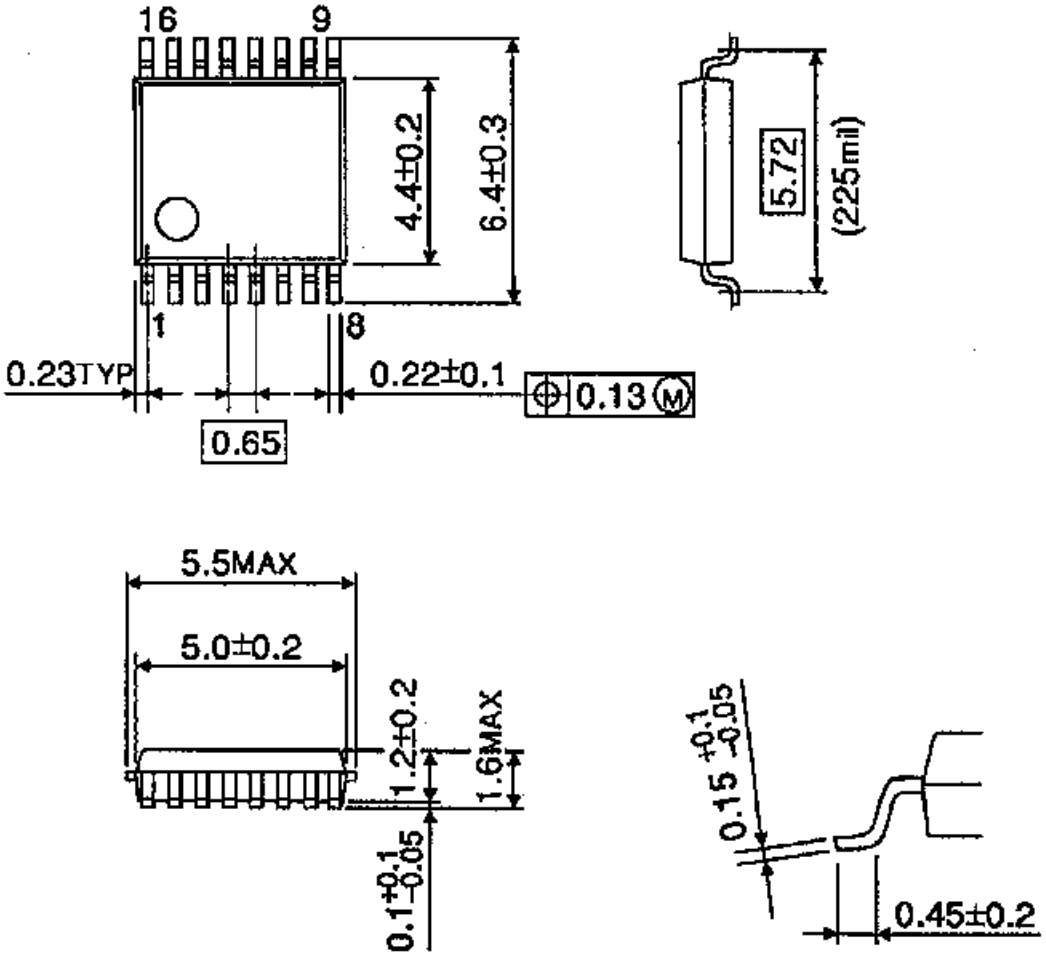


Weight : 0.14g (Typ.)

PACKAGE DIMENSIONS

SSOP16-P-225-0.65B

Unit : mm



Weight : 0.07g (Typ.)

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000707EBA

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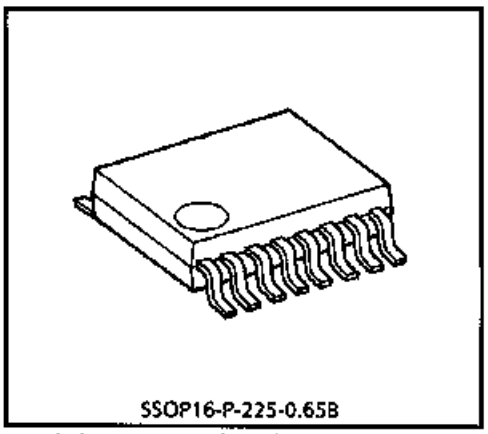
- The information contained herein is subject to change without notice.

TOSHIBA Bi-CMOS INTEGRATED CIRCUIT SILICON MONOLITHIC

TB31202FN

PLL FREQUENCY SYNTHESIZER



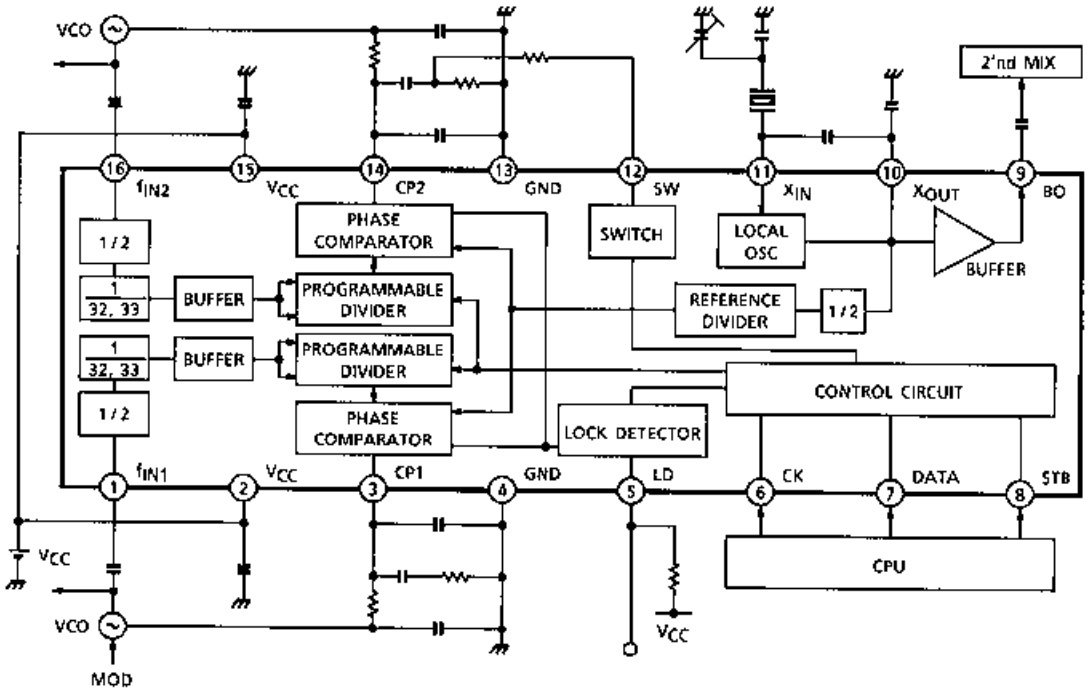
SSOP16-P-225-0.65B

Weight : 0.07g (Typ.)

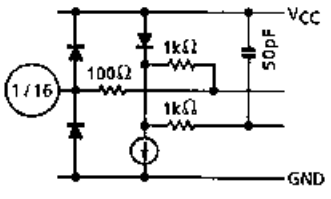
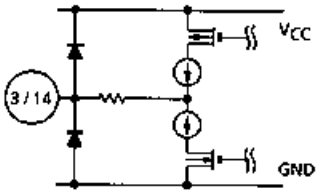
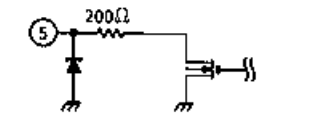
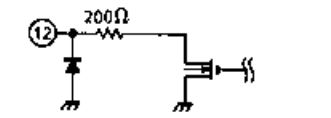
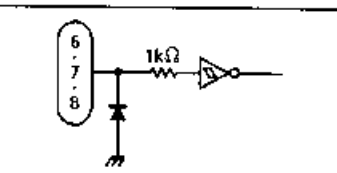
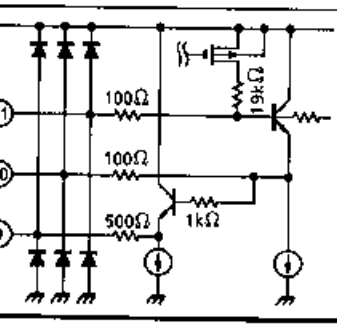
FEATURES

- One packaging two systems prescaler and PLL for receiver and transmitter
- Low operating power supply voltage : V_{CC} = 2.0~5.5V
  (Temperature ≧ − 10°C : V_{CC} = 1.9~5.5V)
- Low current consumption : I_{CC} = 8mA (Typ.)
- Input frequency : f_{IN} = 200~520MHz
- High input sensitivity : V_{IN} = 93~107dBμV
- Charge pump is constant current type, and is able to change output current by serial data
- Reference oscillation circuit is adopted circuit of bipolar, so getting the stable X'tal oscillation circuit
- Available standby control for receiver and transmitter independent of each other
- The very small package : SSOP16pin (0.65mm pitch)

BLOCK DIAGRAM



PIN FUNCTION (The values of resistor and capacitor are typical.)

PIN No.	PIN NAME	FUNCTION	INTERNAL EQUIVALENT CIRCUIT
1	f_{IN1}	Input terminal of RF oscillation signal.	
16	f_{IN2}		
2	V_{CC}	Terminal of power supply. Pin 2 and pin 15 are cannected in IC.	
15	V_{CC}		
3	CP1	Output terminal of charge pump. Charge pump is constant current output circuit, and output current is varied by input serial data.	
14	CP2		
4	GND	Terminal of GND. Pin 4 and pin 13 are cannected in IC.	
13	GND		
5	LD	Output terminal of lock detection. It is the open drain output.	
12	SW	Switchover terminal for constant of loop filter. It is the open drain output. When don't switch constant of loop filter, available general output.	
6	CK	Input terminal of clock.	
7	DATA	Input terminal of serial data.	
8	STB	Input terminal of strobe signal.	
9	BO	Output terminal of buffer amplifier. The signal of local oscillation is output through the buffer amplifier.	
10	X_{OUT}	Output terminal of local oscillation signal.	
11	X_{IN}	Input terminal of local oscillation signal. In case of external input, connecting it to this terminal.	

DESCRIPTION OF FUNCTION AND OPERATION

1. Entry of serial data

- Serial data used to control the IC is input through three terminals, CK, DATA and STB.

  ① During the rise of a clock pulse, data is fed to the shift register in the IC in order from the LSB.

  ② Upon the reception of all data, the strobe signal (STB) is made "H".

  ③ After the reception of a strobe signal (STB) of the "H" level, the data stored in the shift register is transferred to the latch in the block selected by the group code, whereby the IC is controlled.

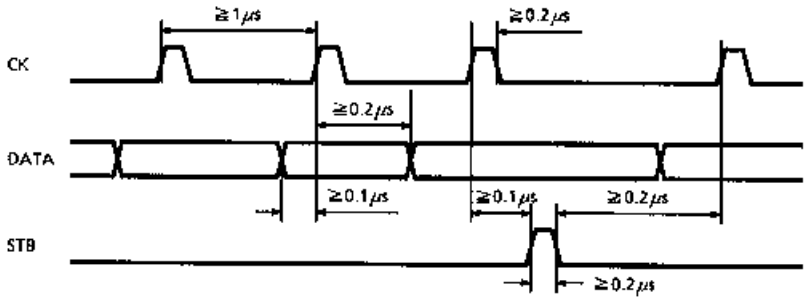
- The three terminal, CK, DATA and STB, contains Schmitt trigger circuits to prevent the data errors by noise, etc.

○ Serial data group and group code

- The IC has control divided into four groups so that they may be controlled independent of one another. Each group is identified by a 2bit group code attached at the data end.

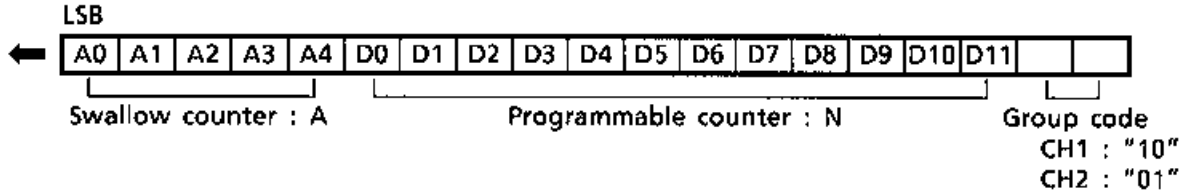
CODE	ITEM
10	Number of divisions by CH1 programmable divider (f_{IN1})
01	Number of divisions by CH2 programmable divider (f_{IN2})
11	Number of divisions by reference divider (X_{IN})
00	Optional control

○ Serial data input timing



2. Programmable dividers (CH1, CH2)

- These programmable dividers are composed of a 5bit swallow counter (5bit programmable divider), a 12bit programmable counter, and a two-modulars prescaler providing 64 and 66 divisions.
- The strategy of a swallow counter is used to set high reference frequency.
- Sending certain data to the swallow counter and the programmable counter allows the setting of any of 2048 to 262142 divisions (multiple of two).
- The programmable counter and swallow counter are set by each channel. Each channel is specified by a group code.



$A = A0 + A1 \times 2^1 + \cdots + A4 \times 2^4$
$N = D0 + D1 \times 2^1 + \cdots\cdots + D11 \times 2^{11}$
Number of divisions = 2 (32N + A)
$2048 \leqq$ Number of divisions $\leqq 262142$

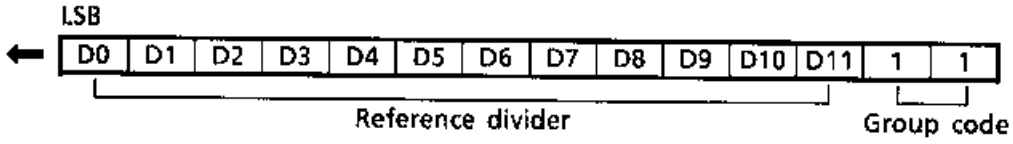
N : Value of N counter
A : Value of A counter

(EX) A Signal of 380MHz is entered into f_{IN1}, being divided into 12.5MHz step. (Reference frequency is 6.25kHz)

$380 \times 10^6 + (12.5 \times 10^3 \div 2) = 60800$
$60800 = 2\ (32N + A)$
$\therefore N = 950,\ A = 0$

3. Reference divider

- This block generates the reference frequency for the PLL.
- The reference divider is composed of a 12bit reference divider and a half fixed divider.
- Sending certain data to the reference divider allows the setting of any of 16 to 8190 divisions (multiple of two).



$D = D0 + D1 \times 2^1 + \cdots\cdots D10 \times 2^{10} + D11 \times 2^{11}$
Number of divisions = 2D
$16 \leqq$ Number of divisions $\leqq 8190$

(EX) With a 21.25MHz X'tal oscillator connected, being divided into 12.5kHz step. (Reference frequency is 6.25kHz)

$21.25 \times 10^6 + (12.5 \times 10^3 \div 2) = 3400$
$3400 = 2D$
$\therefore D = 1700$

4. Optional control

- The optional control below is available.

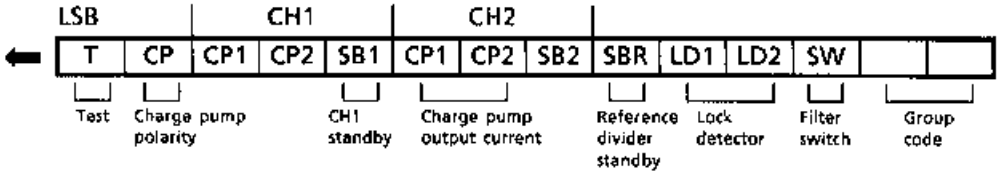
① Test mode (Usually set up T = "0").

② Control and polarity control of the charge pump output current for each channel.

③ Output terminal for Lock detector.

④ Standby control of each channel and reference divider.

⑤ Control of filter switch.



T : Bit for test mode
CP : Switchover bit for charge pump output polarity
CP1, 2 : Switchover bit for charge pump output current
SB1, 2 : Standby control bit for CH1, CH2
SBR : Standby control bit for reference divider
LD1, 2 : Control bit for lock detector output
SW : Control bit for filter switch

- Description of options including their control

① Test mode (T)

Bit "T" is for test mode. In other than the test mode, set this bit at "0".

② Control of charge pump output current (CP1, CP2)

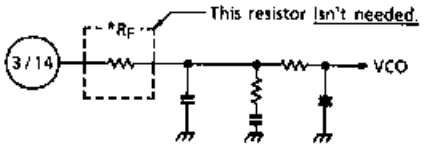
This IC uses a constant current output type charge pump circuit. Output current is varied by controlling "CP1" and "CP2".

CHARGE PUMP OUTPUT CURRENT

CONTROL BIT		CHARGE PUMP OUTPUT CURRENT
CP1	CP2	
0	0	±100μA
0	1	±200μA
1	0	±400μA
1	1	±800μA

High speed lock up is possible by switching charge pump output current.

(Note)



Charge pump output polarity (CP)

Bit "CP" can be reversed charge pump output polarity.

CHARGE PUMP OUTPUT POLARITY

CP	OUTPUT POLARITY
0	Normal
1	Reverse

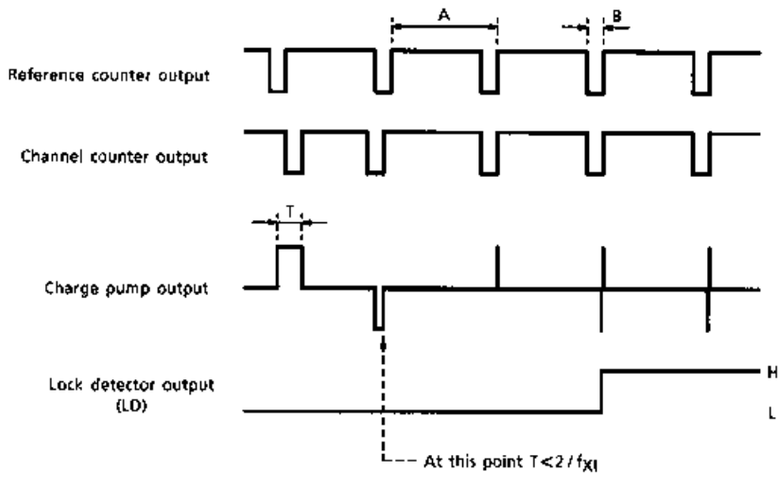
③ Lock detector output

When phase comparator detects phase difference, LD terminal (pin 5) outputs "L". When phase comparator locks, LD terminal outputs "H". On standby, outputs "H".
LD terminal output is controlled by "SB1", "SB2", "LD1" and "LD2".

CONTROL BIT				LOCK DETECTOR OUTPUT STATE
SB1	SB2	LD1	LD2	
0	0	0	0	L
		0	1	CH2 only detect
		1	0	CH1 only detect
		1	1	CH1 * CH2
0	1	0	0	L
		0	1	H
		1	0	CH1 only detect
		1	1	CH1 only detect
1	0	0	0	L
		0	1	CH2 only detect
		1	0	H
		1	1	CH2 only detect
1	1	0	0	L
		0	1	H
		1	0	H
		1	1	H

→ Logical multiply (AND) of CH1, CH2

About SB1, SB2 bit
- 0 : Normal operation
- 1 : Standby



f_{XI} : X_{IN} operating frequency (LOCAL OSC)

T : The time difference of the pulse between reference counter output and channel counter output.

$$A = \frac{\text{Number of divisions by reference divider}}{f_{XI}} \quad (s)$$

$$B = 2 / f_{XI} \quad (s)$$

When the situation that T is less than $2 / f_{XI}$ ($T < 2 / f_{XI}$) continues more than three cycles of reference counter output, lock detector outputs "H".

④ Standby control (SB1, SB2, SBR)

Standby control by three bits (SB1, SB2, SBR).
Bits "SB1" and "SB2" do standby control of CH1, CH2. Bit "SBR" does standby control of reference divider.

CONTROL BIT			STATE			
SB1	SB2	SBR	CH1	CH2	REF	
0	0	*	ON	ON	ON	Interlocking mode
0	1	*	ON	OFF	ON	
1	0	*	OFF	ON	ON	
1	1	0	OFF	OFF	ON	REF ON mode
1	1	1	OFF	OFF	OFF	

⑤ Filter switch control (SW)

Control of SW terminal by bit "SW".
This terminal is for switching constant of loop filter.
Output type of this terminal is open drain output. Switching the register of loop filter by this terminal with switching charge pump output current, high mode and normal mode can operate PLL by ideal braking factor.
When constant of loop filter don't change switch, available general output.

FILTER SWITCH CONTROL

SW	OUTPUT
0	OFF
1	ON

5. Reference frequency oscillation circuit and buffer amplifier

This IC has a stable oscillation circuit composed of bipolar.
In case of inputting the external reference frequency directly, use X_{IN} terminal (pin 11).
For the common use of X'tal of the reference frequency oscillation circuit for the PLL and X'tal of local oscillation to 2'nd MIX, output terminal of local oscillation signal with buffer amplifier (pin 9) may be used.
This terminal (pin 9) is provied with a buffer amplifier.

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{CC}	6	V
Power Dissipation	P_D	560	mW
Operating Temperature	T_{opr}	−30~85	°C
Storage Temperature	T_{stg}	−55~150	°C

ELECTRICAL CHARACTERISTIC
(Unless otherwise specified, V_{CC} = 2.2V, Ta = 25°C)

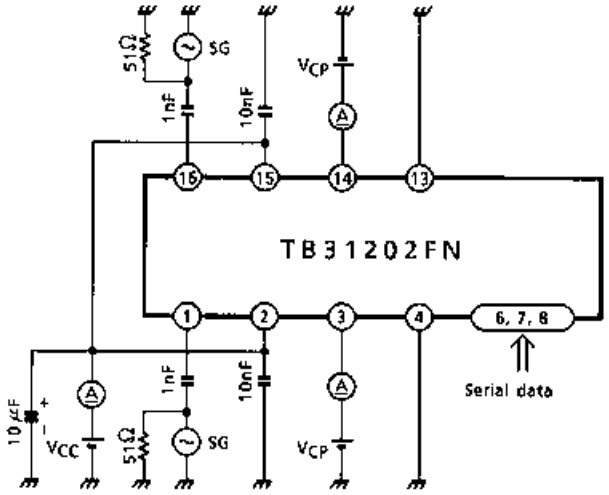
CHARACTERISTIC	SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Power Supply Voltage	V_{CC}		Ta = −30~85°C	2.0	2.2	5.5	V
			Ta = −10~85°C	1.9	2.2	5.5	
Operating Current Consumption	I_{CCO}		CH1 = CH2 = 300MHz, 107dBμV input	5.0	8.0	11.0	mA
Current Consumption	I_{CCQ}		At standby mode	—	0	10	μA
f_{IN} Operating Frequency	f_{IN1}		V_{IN1} = 93dBμV	200	—	520	MHz
	f_{IN2}		V_{IN2} = 93dBμV	200	—	520	
f_{IN} Input Sensitivity	V_{IN1}		f_{IN1} = 200~520MHz	93	—	107	dBμV
	V_{IN2}		f_{IN2} = 200~520MHz	93	—	107	
X_{IN} Operating Frequency	f_{XI}		V_X = 0.5V_{p-p}, Sin-wave	5	21.25	25	MHz
X_{IN} Input Voltage	V_{XI}		f_{XI} = 21.25MHz	102	107	112	dBμV
Input Voltage	V_{IH}		STB, DATA, CK	V_{CC} × 0.8	V_{CC}	5.7	V
	V_{IL}		STB, DATA, CK	−0.2	0	V_{CC} × 0.2	
CK Input Frequency	f_{CK}		CK	—	—	1	MHz
Charge Pump Output Current	I_{CP1}		"CP1" = 0, "CP2" = 0, V_{CP} = 1.1V	—	± 100	—	μA
	I_{CP2}		"CP1" = 0, "CP2" = 1, V_{CP} = 1.1V	—	± 200	—	
	I_{CP3}		"CP1" = 1, "CP2" = 0, V_{CP} = 1.1V	—	± 400	—	
	I_{CP4}		"CP1" = 1, "CP2" = 1, V_{CP} = 1.1V	—	± 800	—	
Charge Pump OFF Leak Current	CP_{OFF}		Standby mode, V_{CP} = 1.1V	—	—	± 1.0	μA
SW Terminal ON Resistance	R_{SW}		SW_{ON}	—	500	—	Ω
LD Terminal ON Resistance	R_{LD}		LD_{ON}	—	500	—	Ω
SW Terminal OFF Leak Current	SW_{OFF}		SW_{OFF}	—	—	± 1.0	μA
LD Terminal OFF Leak Current	LD_{OFF}		LD_{OFF}	—	—	± 1.0	μA

REFERENCE DATA (Typ.)

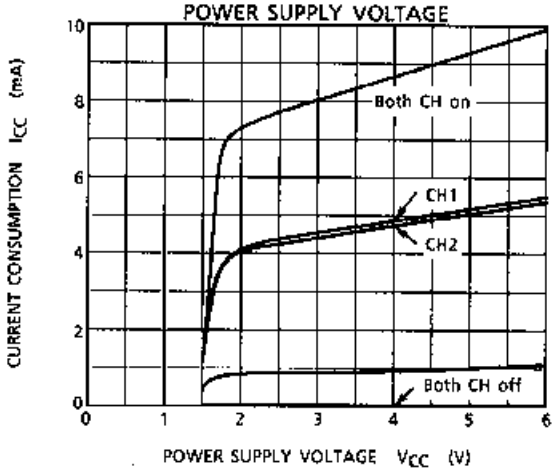
CH1	CH2	REFERENCE DIVIDER	CURRENT CONSUMPTION	UNIT
N	N	ON	8.0	mA
N	S	ON	4.5	mA
S	N	ON	4.5	mA
S	S	ON	800	μA
S	S	OFF	0	μA

A : Normal operation
S : Srandby state

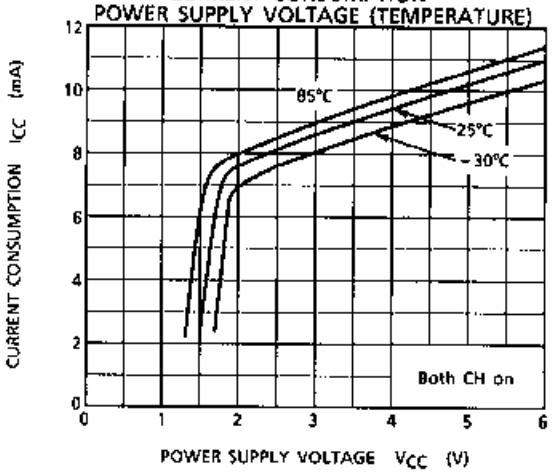
TEST CIRCUIT



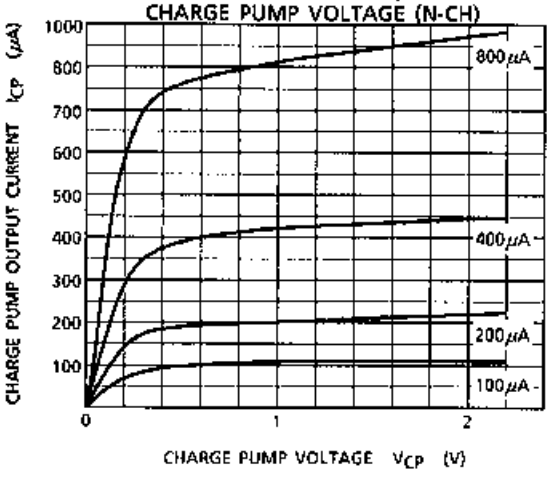
CURRENT CONSUMPTION – POWER SUPPLY VOLTAGE



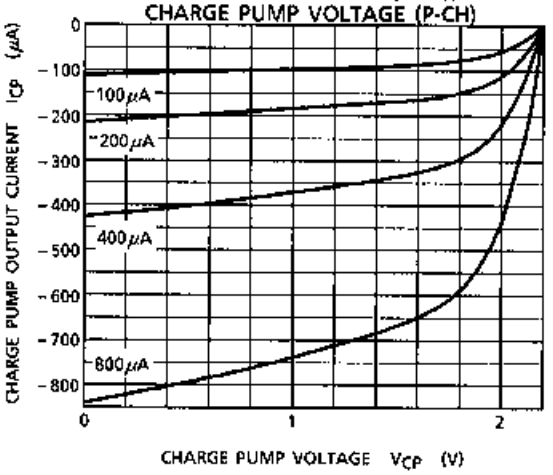
CURRENT CONSUMPTION – POWER SUPPLY VOLTAGE (TEMPERATURE)



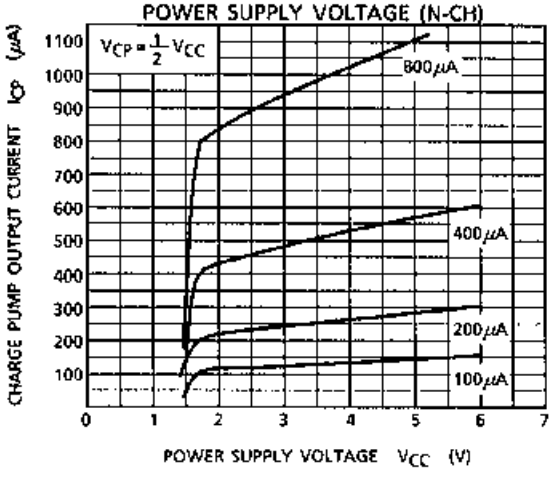
CHARGE PUMP OUTPUT CURRENT – CHARGE PUMP VOLTAGE (N-CH)



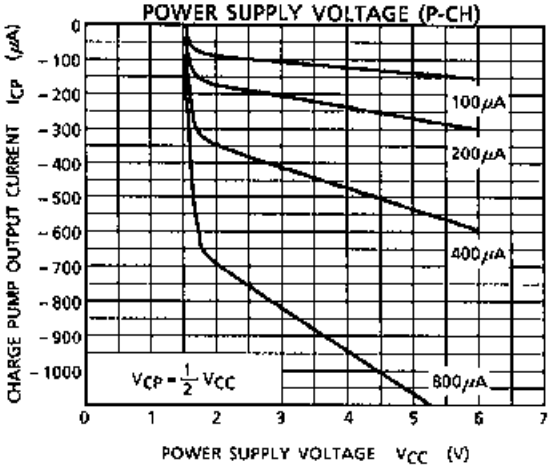
CHARGE PUMP OUTPUT CURRENT – CHARGE PUMP VOLTAGE (P-CH)



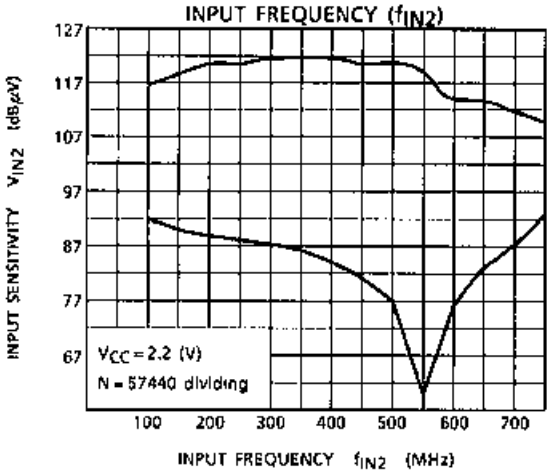
CHARGE PUMP OUTPUT CURRENT – POWER SUPPLY VOLTAGE (N-CH)



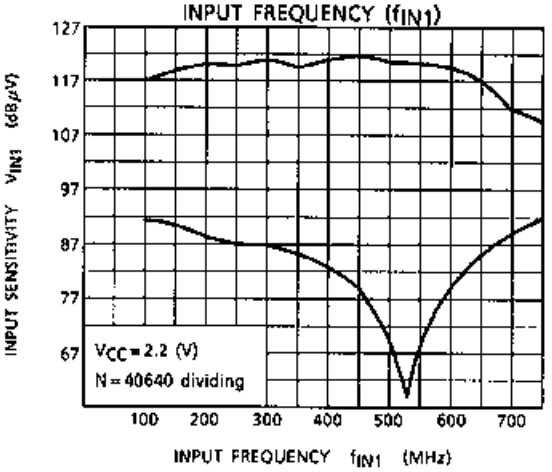
CHARGE PUMP OUTPUT CURRENT – POWER SUPPLY VOLTAGE (P-CH)



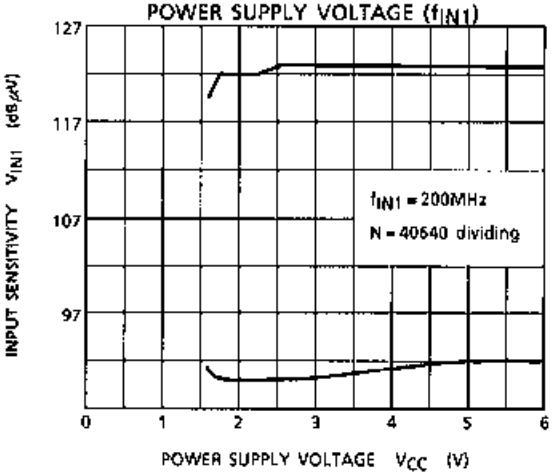
INPUT SENSITIVITY – INPUT FREQUENCY (f_{IN2})



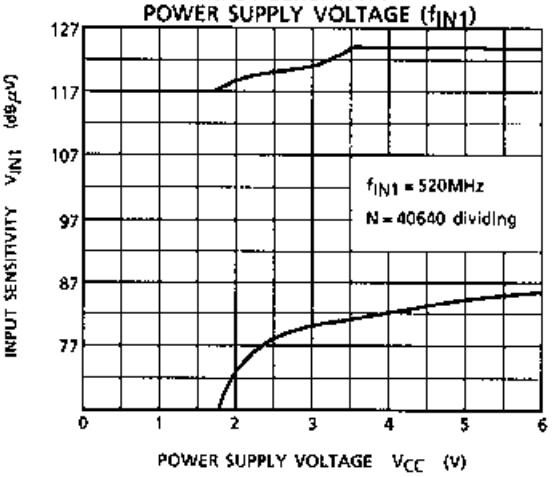
INPUT SENSITIVITY – INPUT FREQUENCY (f_{IN1})



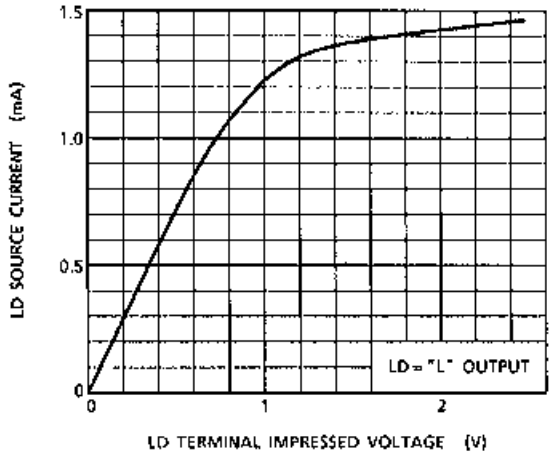
INPUT SENSITIVITY – POWER SUPPLY VOLTAGE (f_{IN1})



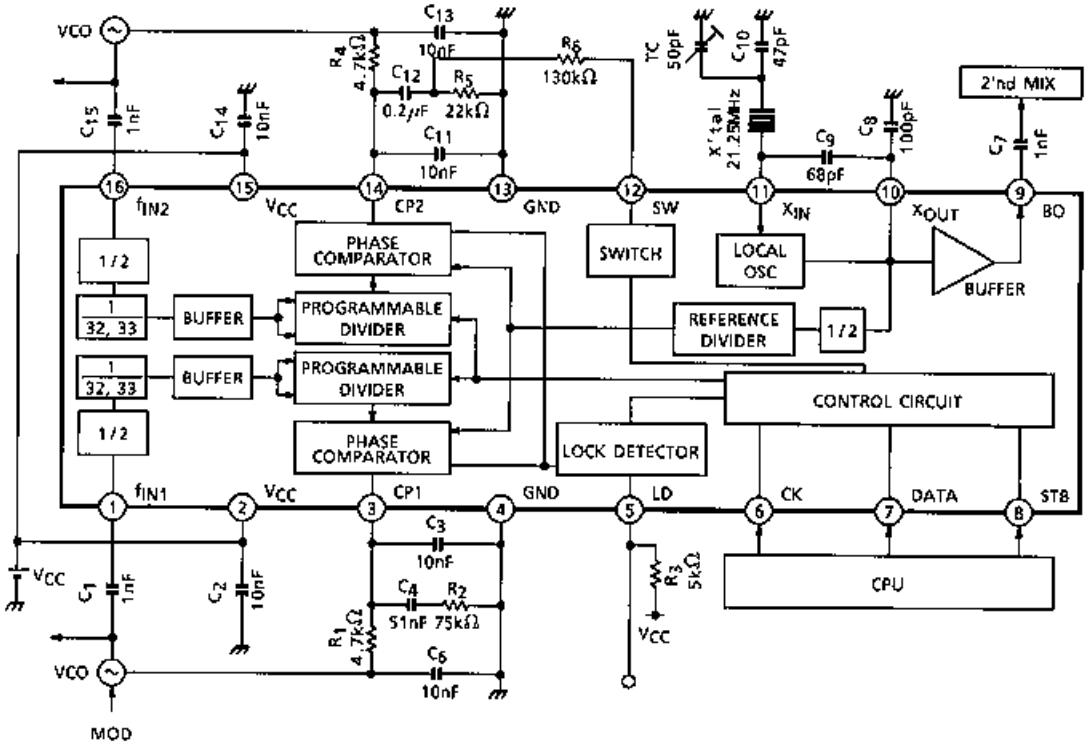
INPUT SENSITIVITY – POWER SUPPLY VOLTAGE (f_{IN1})



LD TERMINAL OUTPUT



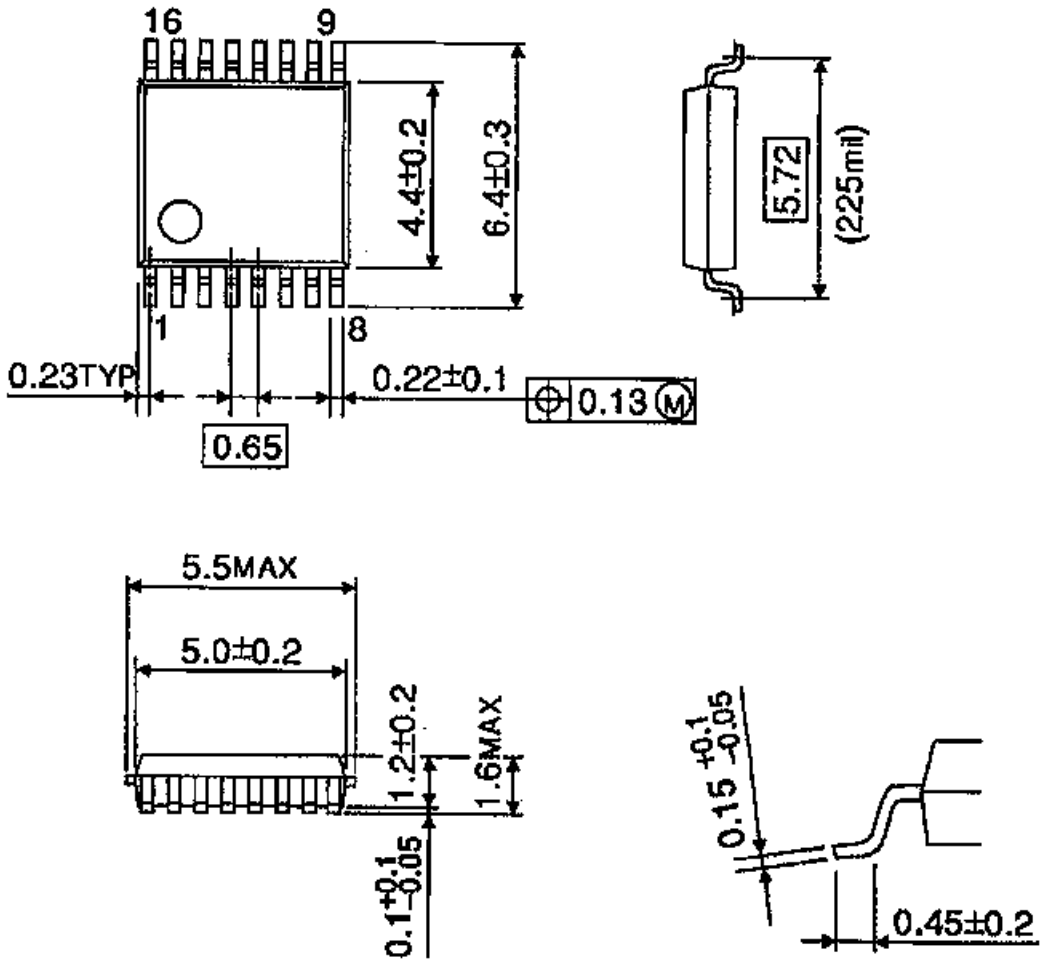
APPLICATION CIRCUIT



PACKAGE DIMENSIONS

SSOP16-P-225-0.65B

Unit : mm



Weight : 0.07g (Typ.)

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000707EBA

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  In developing your designs, please ensure that TOSHIBA products are used within specified operating ranges as set forth in the most recent TOSHIBA products specifications. Also, please keep in mind the precautions and conditions set forth in the "Handling Guide for Semiconductor Devices," or "TOSHIBA Semiconductor Reliability Handbook" etc..
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SP5055

2.6GHz Bidirectional I²C BUS Controlled Synthesiser

DS2361 ISSUE 4.5 November 2001

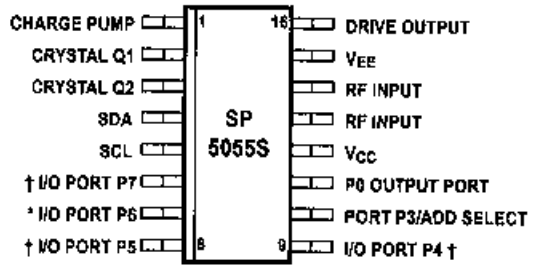
The SP5055 is a single chip frequency synthesiser designed for TV tuning systems. Control data is entered in the standard I²C BUS format. The device contains 4 addressable current limited outputs and 4 addressable Bi-Directional open collector ports one of which is a 3 bit ADC. The information on these ports can be read via the I²C BUS. The device has one fixed I²C BUS address and 3 programmable addresses, programmed by applying a specific input voltage to one of the current limited outputs. This enables 2 or more synthesisers to be used in a system.

FEATURES

- Complete 2.6GHz Single Chip System
- Programmable via I²C BUS
- Low power consumption (5V 65mA)
- Low Radiation
- Phase Lock Detector
- Varactor Drive Amp Disable
- 6 Controllable Outputs, 4 Bi-Directional
- 5 Level ADC
- Variable I²C BUS Address For Multi Tuner Applications
- Full ESD Protection*

* Normal ESD handling procedures should be observed.

Ordering Information
SP5055GS/KG/MPAS (Tubes)
SP5055GS/KG/MPAD (Tape & Reel)
16lead minature plastic package



† = Logic level I/O
* = 3-bit ADC input

MP16

Fig. 1 Pin connections – top view

APPLICATIONS

- Satellite TV
- High IF Cable Tuning Systems

ELECTRICAL CHARACTERISTICS

T_{amb} = -20°C to +80°C, V_{CC} = +4.7V to 5.3V.
These Characteristics are guaranteed by either production test or design. They apply within the specified ambient temperature and supply voltage unless otherwise stated. Reference frequency = 4MHz unless otherwise stated.

Characteristic	Pin	Value			Units	Conditions
		Min.	Typ.	Max.		
Supply current	12		65	80	mA	V_{CC} = 5V
Prescaler input voltage	13, 14	50		300	mV_{RMS}	500MHz to 2.6GHz Sinewave
Prescaler input voltage	13, 14	100		300	mV_{RMS}	120MHz, see Fig. 5
Prescaler input impedance	13, 14		50		Ω	
Prescaler input capacitance			2		pF	
SDA, SCL						
Input high voltage	4, 5	3		5.5	V	
Input low voltage	4, 5	0		1.5	V	
Input high current	4, 5			10	µA	Input voltage = V_{CC}
Input low current	4, 5			-10	µA	Input voltage = 0V
Leakage current	4, 5			10	µA	When V_{CC} = 0V
SDA						
Output voltage	4			0.4	V	I_{sink} = 3mA
Charge pump current low	1		±50		µA	Byte 4, bit 2 = 0, pin 1 = 2V
Charge pump current high	1		±170		µA	Byte 4, bit 2 = 1, pin 1 = 2V
Charge pump output leakage current	1			±5	nA	Byte 4, bit 4 = 1, pin 1 = 2V
Charge pump drive output current	16	500			µA	$V_{pin\ 16}$ = 0·7V
Charge pump amplifier gain			6400			
Recommended crystal series resistance		10		200	Ω	
Crystal oscillator drive level	2		80		mVp-p	
Crystal oscillator negative resistance	2	750			Ω	
Output Ports						
P0, P3 sink current	10, 11	0.7	1	1.5	mA	V_{OUT} = 12V
P0, P3 leakage current	10, 11			10	µA	V_{OUT} = 13·2V
P4-P7 sink current	9-6	10			mA	V_{OUT} = 0.7V
P4-P7 leakage current	9-6			10	µA	V_{OUT} = 13·2V
Input Ports						
P3 input current high	10			+10	µA	$V_{pin\ 10}$ = 13.2V
P3 input current low	10			-10	µA	$V_{pin\ 10}$ = 0V
P4,P5,P7 input voltage low	9,8,6			0.8	V	
P4,P5,P7 input voltage high	9,8,6	2.7			V	
P6 Input current high	7			+10	µA	See Table 3 for ADC Levels
P6 input current low	7			-10	µA	

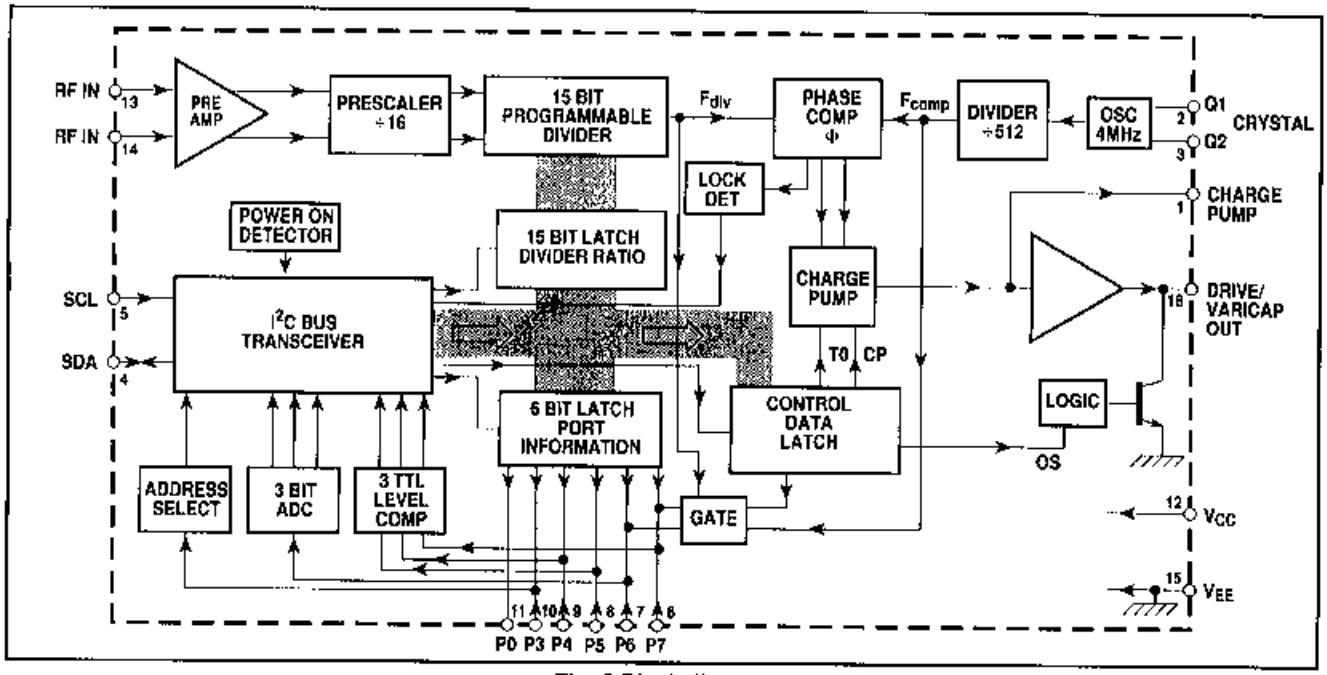


Fig. 2 Block diagram

FUNCTIONAL DESCRIPTION

The SP5055 is programmed from an I²C BUS. Data and Clock are fed in on the SDA and SCL lines respectively as defined by the I²C BUS format. The synthesiser can either accept new data (write mode) or send data (read mode). The Tables in Fig. 3 illustrate the format of the data. The device can be programmed to respond to several addresses, which enables the use of more than one synthesiser in an I²C Bus system. Table 4 shows how the address is selected by applying a voltage to P3. The last bit of the address byte (R/W) sets the device into read mode if it is high and write mode if it is low. When the SP5055 receives a correct address byte it pulls the SDA line low during the acknowledge period and during following acknowledge periods after further data bytes are programmed. When the SP5055 is programmed into the read mode the controlling device accepting the data must pull down the SDA line during the following acknowledge period to read another status byte.

WRITE MODE (FREQUENCY SYNTHESIS)

When the device is in the write mode Bytes 2 + 3 select the synthesised frequency while bytes 4 + 5 select the output port states and charge pump information.

Once the correct address is received and acknowledged, the first Bit of the next Byte determines whether that byte is interpreted as byte 2 or 4, a logic 0 for frequency information and a logic 1 for charge pump and output port information. Additional data bytes can be entered without the need to re-address the device until an I²C stop condition is recognised. This allows a smooth frequency sweep for fine tuning or AFC purposes.

If the transmission of data is stopped mid-byte (i.e., by another device on the bus) then the previously programmed byte is maintained.

Frequency data from bytes 2 and 3 is stored in a 15-bit shift register and is used to control the division ratio of the 15-bit programmable divider which is preceded by a divide-by-16 prescaler and amplifier to give excellent sensitivity at the local oscillator input; see Fig 5. The input impedance is shown in Fig 7.

The programmed frequency can be calculated by multiplying the programmed division ratio by 16 times the comparison frequency F_{comp}.

When frequency data is entered, the phase comparator, via the charge pump and varactor drive amplifier, adjusts the local oscillator control voltage until the output of the programmable divider is frequency and phase locked to the comparison frequency.

The reference frequency may be generated by an external source capacitively coupled into pin 2 or provided by an on-board 4MHz crystal controlled oscillator.

Note that the comparison frequency is 7·8125kHz when a 4MHz reference is used.

Bit 2 of byte 4 of the programming data (CP) controls the current in the charge pump circuit, a logic 1 for ±170μA and a logic 0 for ±50μA, allowing compensation for the variable tuning slope of the tuner and also to enable fast channel changes over the full band. Bit 4 of byte 4 (T0) disables the charge pump if set to a logic 1. Bit 8 of byte 4 (OS) switches the charge pump drive amplifier's output off when it is set to a logic 1. Bit 3 of Byte 4 (T1) selects a test mode where the phase comparator inputs are available on P6 and P7, a logic 1 connects F_{comp} to P6 and F_{div} to P7.

Byte 5 programs the output ports P0 to P7; on a logic 0 for a high impedance output, logic 1 for low impedance (on).

READ MODE

When the device is in the read mode the status data read from the device on the SDA line takes the form shown in Table 2.

Bit 1 (POR) is the power-on reset indicator and is set to a logic 1 if the power supply to the device has dropped below 3V and the programmed information lost (e.g., when the device is initially turned on). The POR is set to 0 when the read sequence is terminated by a stop command. The outputs are all set to high impedance when the device is initially powered up. Bit 2 (FL) indicates whether the device is phase locked, a logic 1 is present if the device is locked and a logic 0 if the device is unlocked.

Bits 3, 4 and 5 (I2,I1,I0) show the status of the I/O Ports P7, P5 and P4 respectively. A logic 0 indicates a low level and a logic 1 a high level. If the ports are to be used as inputs they should be programmed to a high impedance state (logic 1). These inputs will then respond to data complying with TTL type voltage levels. Bits 6, 7 and 8 (A2,A1,A0) combine to give the output of the 5 level ADC.

The 5 level ADC can be used to feed AFC information to the microprocessor from the IF section of the receiver, as illustrated in the typical application circuit.

APPLICATION

A typical Application is shown in Fig. 4. All input/output interface circuits are shown in Fig. 6.

	MSB							LSB		
Address	1	1	0	0	0	MA1	MA0	0	A	**Byte 1**
Programmable divider	0	2^{14}	2^{13}	2^{12}	2^{11}	2^{10}	2^{9}	2^{8}	A	**Byte 2**
Programmable divider	2^{7}	2^{6}	2^{5}	2^{4}	2^{3}	2^{2}	2^{1}	2^{0}	A	**Byte 3**
Charge pump and test bits	1	CP	T1	T0	1	1	1	OS	A	**Byte 4**
I/O port control bits	P7	P6	P5	P4	P3	X	X	P0	A	**Byte 5**

Table 1 Write data format (MSB transmitted first)

Address	1	1	0	0	0	MA1	MA0	1	A	**Byte 1**
Status byte	POR	FL	I2	I1	I0	A2	A1	A0	A	**Byte 2**

Table 2 Read data format (MSB is transmitted first)

A	:	Acknowledge bit
MA1, MA0	:	Variable address bits (see Table 4)
CP	:	Charge Pump current select
T1	:	Test mode selection
T0	:	Charge pump disable
OS	:	Varactor drive Output disable Switch
P7, P6, P5, P4, P3, P0	:	Control output states
POR	:	Power On Reset indicator
FL	:	Phase lock detect flag
I2, I1, I0	:	Digital information from Ports P7, P5 and P4, respectively
A2, A1, A0	:	5 Level ADC data from P6 (see Table 3)
X	:	Don't care

A2	A1	A0	Voltage input to P6
1	0	0	$0.6V_{CC}$ to 13.2V
0	1	1	$0{\cdot}45V_{CC}$ to $0{\cdot}6V_{CC}$
0	1	0	$0{\cdot}3V_{CC}$ to $0{\cdot}45V_{CC}$
0	0	1	$0{\cdot}15V_{CC}$ to $0{\cdot}3V_{CC}$
0	0	0	0 to $0.15V_{CC}$

Table 3 ADC levels

MA1	MA0	Voltage input to P3
0	0	0V to $0{\cdot}2V_{CC}$
0	1	Always valid
1	0	$0{\cdot}3V_{CC}$ to $0{\cdot}7V_{CC}$
1	1	$0{\cdot}8V_{CC}$ -13.2V

Table 4 Address selection

Fig. 3 Data formats

APPLICATION

A typical application is shown in Fig. 4. All input/output interface circuits are shown in Fig. 6.

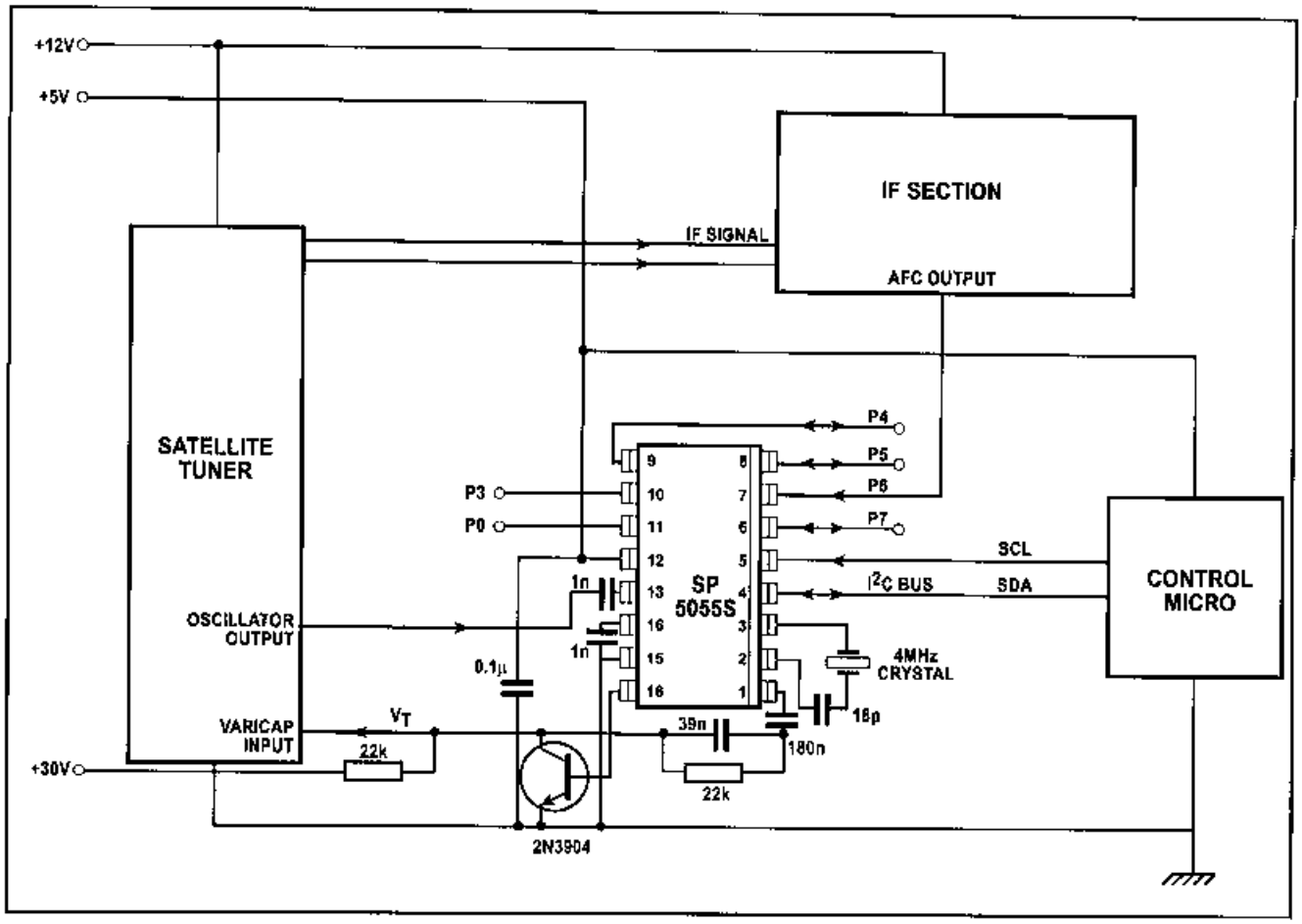


Fig. 4 Typical application

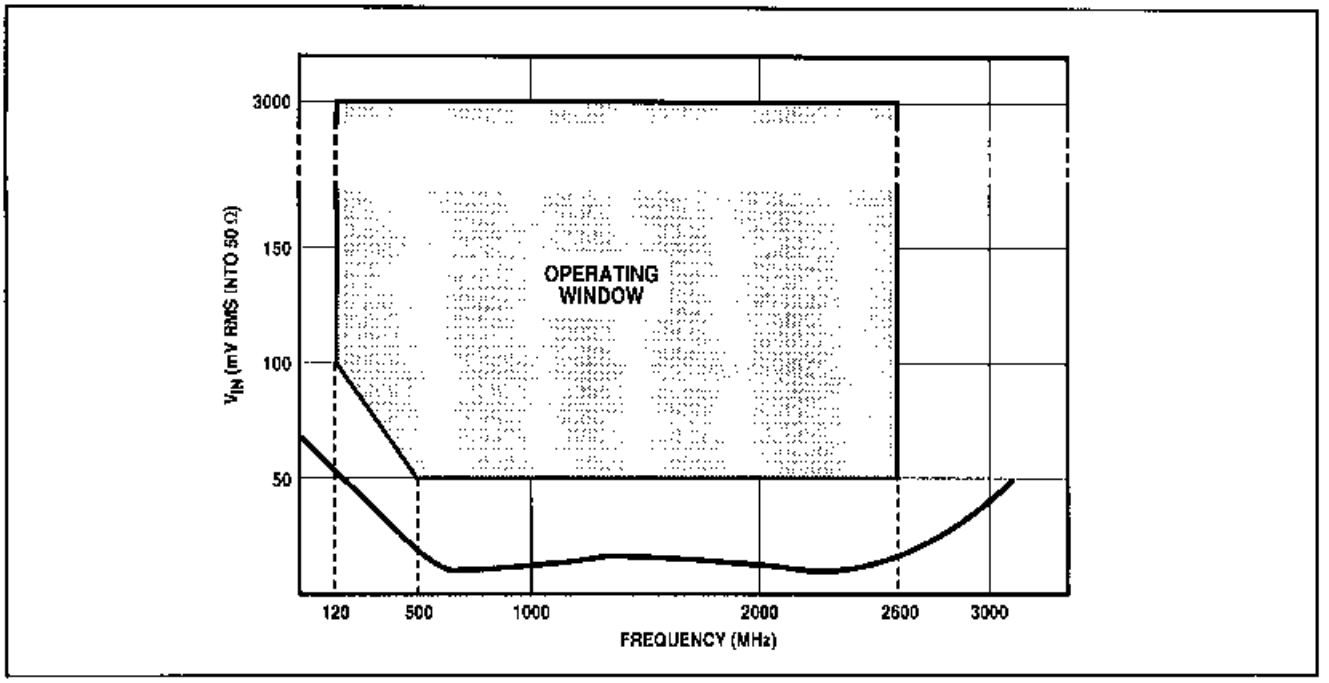


Fig. 5 Typical input sensitivity

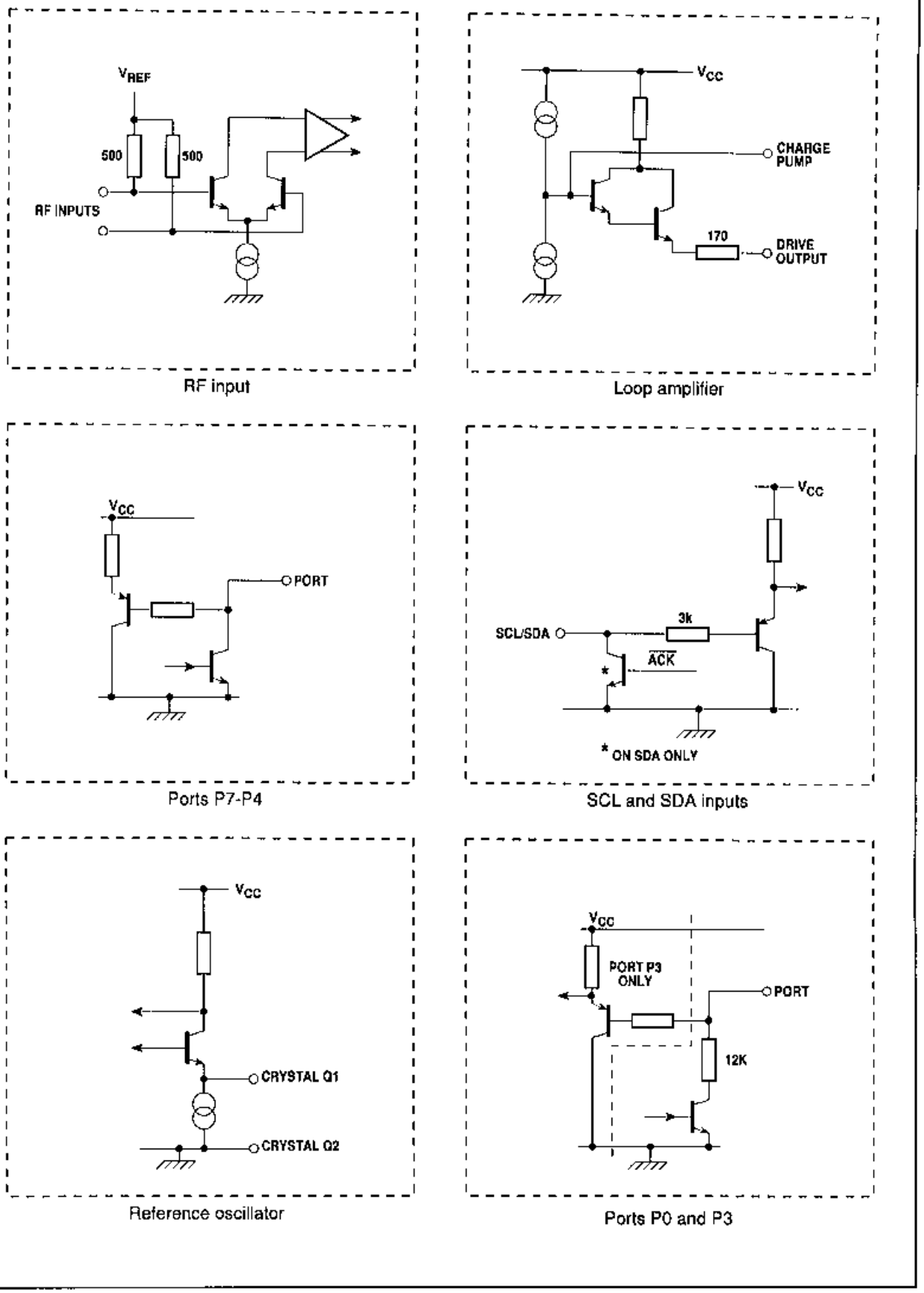


Fig. 6 SP5055 Input/output interface circuits

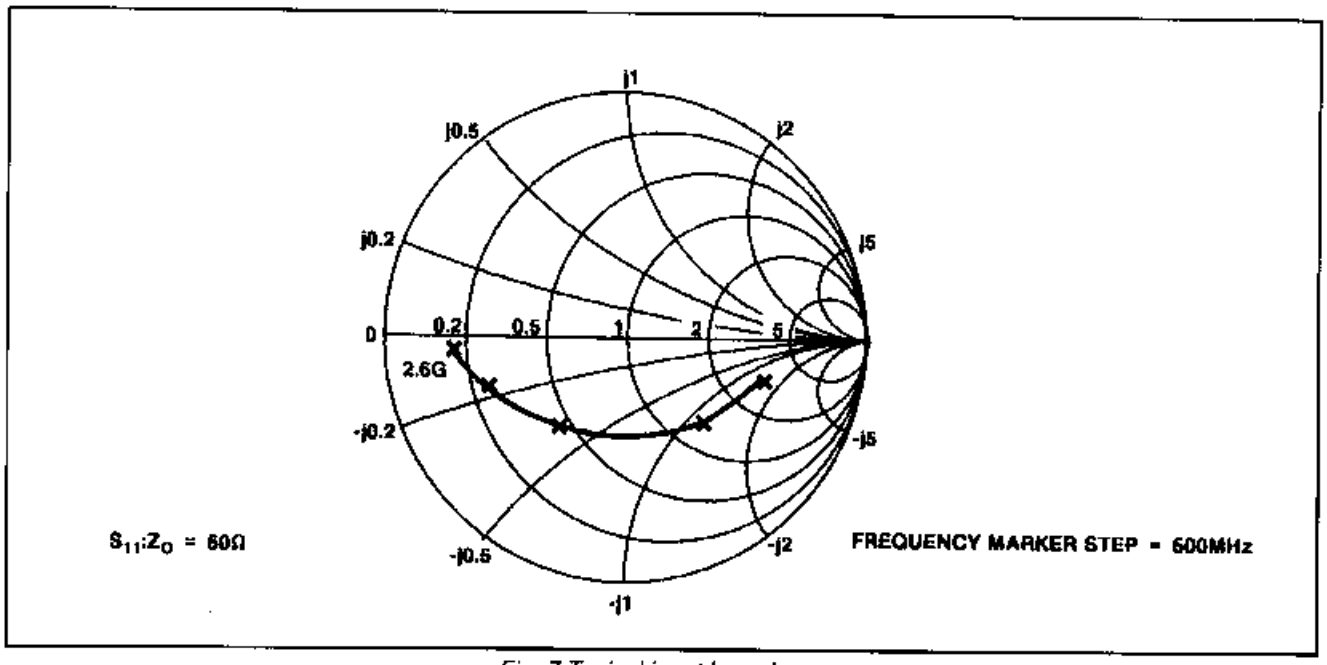


Fig. 7 Typical input impedance

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to V_{EE} and pin 3 at 0V

Parameter	Pin	Value		Units	Conditions
		Min.	Max.		
Supply voltage	12	-0.3	7	V	
RF input voltage	13, 14		2.5	Vp-p	
Port voltage	6-11	-0.3	14	V	Port in off state
	6-9	-0.3	6	V	Port in on state
	10, 11	-0.3	14	V	Port in on state
Total port output current	6-11		50	mA	
RF input DC offset	13, 14	-0.3	V_{CC}+0.3	V	
Charge pump DC offset	1	-0.3	V_{CC}+0.3	V	
Drive DC offset	16	-0.3	V_{CC}+0.3	V	
Crystal oscillator DC offset	2	-0.3	V_{CC}+0.3	V	
SDA, SCL input voltage	4, 5	-0.3	V_{CC}+0.3	V	With V_{CC} applied
		-0.3	5.5	V	V_{CC} not applied
Storage temperature		-55	+125	°C	
Junction temperature			+150	°C	
MP 16 Thermal resistance, chip-to-ambient			111	°C/W	
MP 16 Thermal resistance, chip-to-case			41	°C/W	
Power consumption at 5.5V			440	mW	All ports off

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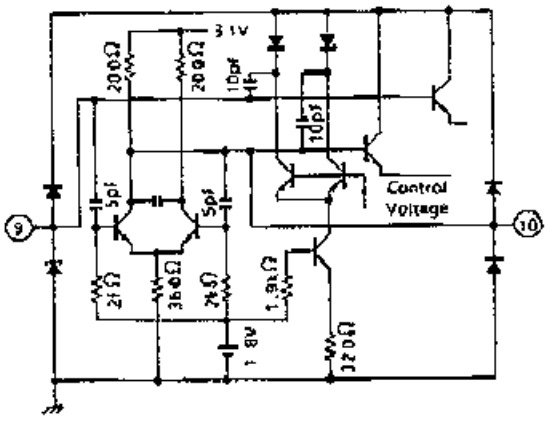
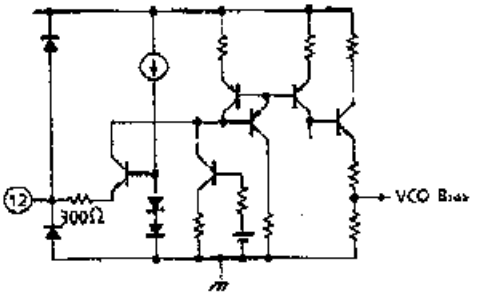
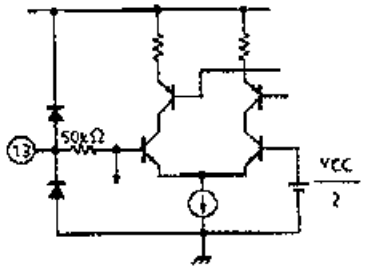
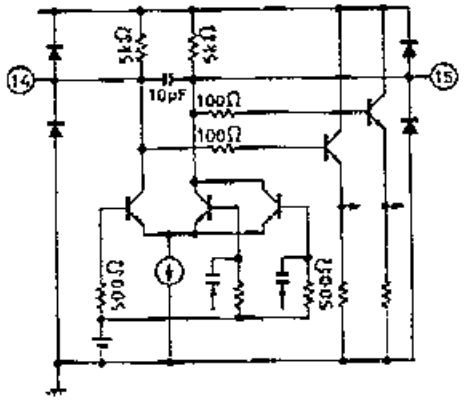
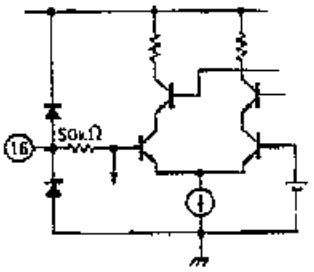
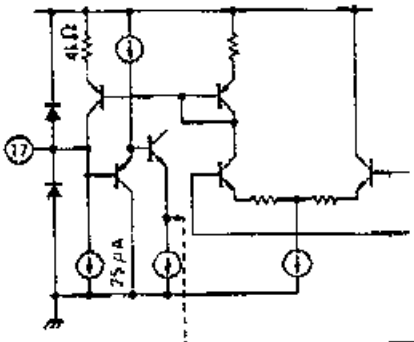
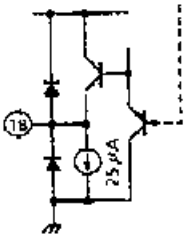
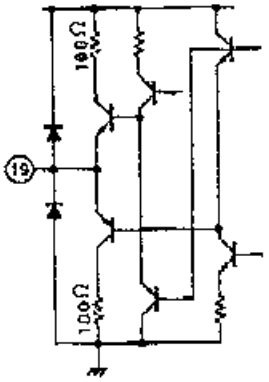
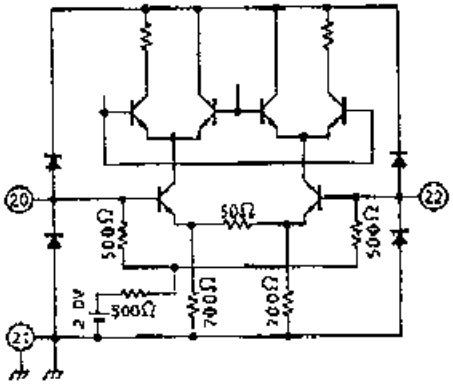
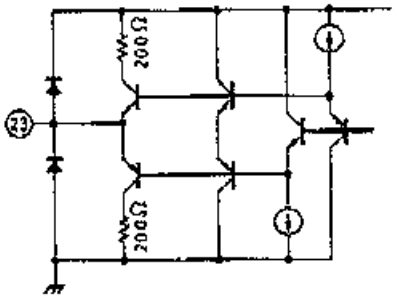
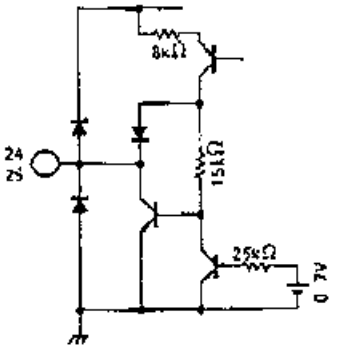
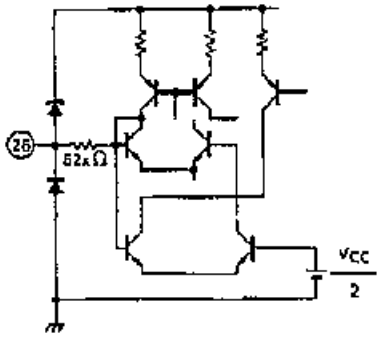
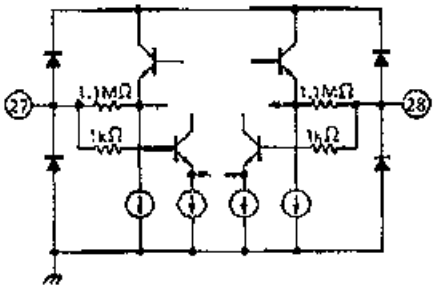
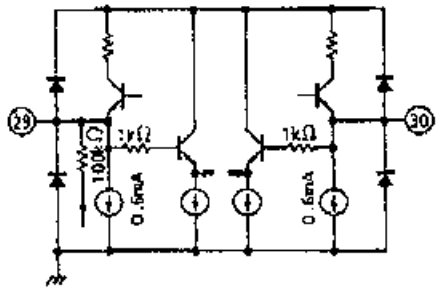
PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
8	GND1	It is the GND of VCO circuit blocks that are VCO (pins 9, 10, 12), loop filter (pins 6, 7), video amplifier (pins 4, 5) AFT system (pins 1, 23, 24, 25, 26, 27, 28) and S/H (pins 29, 30).	—
9 10	VCO Coil	It is the VCO using variations in internal impedance of diode for control voltage from mixer. Use a UJ characteristic for the capacitor of the external tank circuit to correct the internal temperature drift.	
12	VCO Temperature Compensate Bias	The VCO bias is composed of a synthesis of bias in proportion to V_{BE} and V_T of transistor, and this terminal generates a bias proportioned to the V_{BE}. If the external resistance reduced, the VCO sensitivity will rise.	
13	2nd AGC Adjustment	It changes the input level for a AGC detector. It adjusts by adding the direct current offset to pins 14 and 15. The variation width of about 8dB can be added. Internal bias is 2.5V.	

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
14 15	2nd AGC Filter	It generates the AGC voltage by filtering the 402.78MHz (479.5MHz) IF signal by means of an internal resistance and an external condenser. If applying the V_{CC} to pin 15, the AGC will be minimum gain and the VCO oscillates at free-running frequency.	
16	1st AGC Slice Adjustment	It sets the input level threshold for generating the control signal to lower gain from the IC to the 2nd converter of front stage when excessive input. Even if the 2nd AGC adjustment varies, the 1st AGC adjustment point hardly changes. The internal bias is 2.5V.	
17	1st AGC Filter	It outputs by comparating with the AGC and 1st AGC slice level adjustment voltages. This comparator is constructed by the active load type high gain amplifier and determines its response by a capacitor connected to this terminal.	
18	1st AGC Control	It outputs the control voltage using an emitter follower (active low level). The internal current sink has only 25μA.	

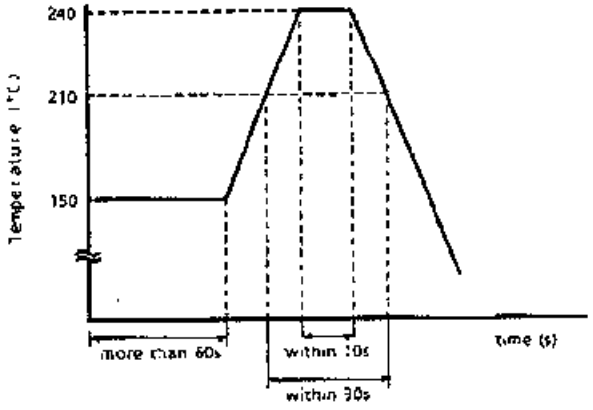
PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
19	Signal Level Out	It outputs the AGC voltage by doing logarithm <-> linear conversion. In the TA8804F the level detection can be carried out even after the 1st AGC is effective and input is reduced using the 1st AGC output.	
20 22	2nd IF In	The IF amplifier constructed by the 3-step series connection of variable gm type gain control, of which the maximum gain is 47dB and minimum gain −8dB. In order to prevent a sneak of radio frequency all the circuits are balance-connected. Therefore, the differential combination is also desirable for the IC input. The internal bias is 2.0V and input impedance 1kΩ.	
23	AFT Output (Analog)	It outputs by integrating the detection output by means of pin 27 and 28 filters, doing center adjustment and multiplying about five times as much.	

PIN No.	PIN NAME	FUNCTION	INTERFACE CIRCUIT
24 25	AFT Output (Digital)	It outputs by converting the analog AFT output to binary with a comparator. In the case of center detection, the each output will be high level. The width of dead gone is determined by the internal threshold and VCO sensitivity, that cannot be adjusted externally.	
26	AFT Center Adjustment	It moves the AFT center frequency in the width of 10MHz and absorbs the center gap caused by dispersion of each AFT circuit.	
27 28	AFT Filter	It constructs a filter whose cut off frequency is less than 1Hz (capacitor : 0.7Hz at 0.1μF) with an internal 1.1MΩ resistance and external condenser.	
29 30	Hold Capacitor	Sample and hold by charge / discharging the condenser using the switching signal regenerated by keyed pulse.	

MAXIMUM RATINGS (Ta = 25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Power Supply Voltage	V_{CC} MAX	6.0	V
Power Dissipation	P_D MAX	1000	mW
Operation Temperature	T_{opr}	−20~75	°C
Storage Temperature	T_{stg}	−55~150	°C
Lead Temperature	—	260°C, 10s	

Recommended assembly method : Recommended temperature profile of reflow soldering of far and medium infrared rays



RECOMMENDED POWER SUPPLY VOLTAGE

PIN No.	PIN NAME	MIN.	TYP.	MAX.	UNIT
11	V_{CC}	4.5	5.0	5.5	V

ELECTRICAL CHARACTERISTICS

DC CHARACTERISTICS (Unless otherwise specified, V_{CC} = 5.0V, Ta = 25°C)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Current		I_{CC}	1	—	55	80	105	mA
Terminal Voltage	Pin 1	V_1	1	—	2.0	2.5	3.0	V
	Pin 2	V_2		—	1.9	2.4	2.9	
	Pin 3	V_3		—	1.9	2.4	2.9	
	Pin 4	V_4		—	0.8	1.3	1.8	
	Pin 5	V_5		—	0.8	1.3	1.8	
	Pin 6	V_6		—	1.7	2.1	2.5	
	Pin 7	V_7		—	1.7	2.1	2.5	
	Pin 9	V_9		—	2.4	2.8	3.2	
	Pin 10	V_{10}		—	2.4	2.8	3.2	
	Pin 12	V_{12}		—	0.4	0.7	1.0	
	Pin 13	V_{13}		—	2.3	2.5	2.7	
	Pin 14	V_{14}		—	—	3.6	—	
	Pin 15	V_{15}		—	—	3.6	—	
	Pin 16	V_{16}		—	2.1	2.5	2.9	
	Pin 18	V_{18h}		Pin 17 : 1kΩ-GND	—	1.0	1.3	
		V_{18l}		Pin 17 : V_{CC}	3.9	4.3	4.7	
	Pin 20	V_{20}		—	1.5	2.0	2.5	
	Pin 22	V_{22}		—	1.5	2.0	2.5	
	Pin 27	V_{27}		—	—	2.3	2.8	
	Pin 28	V_{28}		—	—	2.3	2.8	
	Pin 29	V_{29}		—	1.8	2.3	2.8	
	Pin 30	V_{30}		—	1.8	2.3	2.8	
Pin 2, 3 Acceptable Output Current		I_2, I_3	1	—	−1.0	—	6.0	mA
1'st AGC Output Current		I_{18}	1	—	−0.02	—	6.0	mA

AC CHARACTERISTICS

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
IF Input Frequency Range	f_{in}	—	—	350	400	550	MHz
IF Input Level Range	v_{in}	—	—	−60	—	−10	dBmW (50Ω)
1st AGC Shoulder Level Range	AGC_{MAX}	2	(Note 1)	—	−20	−10	dBmW (50Ω)
1st AGC Control Sensitivity	ΔAGC	2	(Note 2)	1.0	3.5	6.0	V/dB
Signal Level Sensitivity	ΔV/Δv	2	(Note 3)	10	35	60	mV/dB
VCO Conversion Sensitivity	β	2	Converting to output rate Pin 4, 5 : open / (Note 4)	—	110	130	MHz/V
VCO Temperature Drift	Δf_{Ta}	2	Ta = −10~65°C / (Note 5)	—	±1.0	±2.5	MHz
PLL Lock Range	f_L	2	(Note 6)	±25	±30	—	MHz
PLL Capture Range	fca	2	(Note 6)	±25	±30	—	MHz
Demodulation Output Level	V_{out}	2	$\Delta f = 10MHz_{p-p}$ / (Note 7)	0.15	0.26	0.40	V_{p-p}
Video Amplifier Variable Width	$V_{outS/5}$	2	Pin 4, 5 : short, 5kΩ / (Note 8)	10	14	—	dB
Demodulation Output Amplitude Frequency Characteristics 1	V_{outA1}	2	f = 0.2~4MHz / (Note 9)	—	—	±0.5	dB
Demodulation Output Amplitude Frequency Characteristics 2	V_{outA2}	2	f = 4~9MHz / (Note 9)	—	—	±2	dB
Group Delay Characteristics 1	τpd1	2	f = 0.2~4MHz / (Note 9)	—	—	±10	ns
Group Delay Characteristics 2	τpd2	2	f = 4~9MHz / (Note 9)	—	—	±40	ns
AFT Sensitivity	Δf/ΔV	2	(Note 12)	2.4	3.2	4.0	MHz/V
S/H Sample Speed	Δf_{spl}	2	Converting to input frequency rate / (Note 10)	0.1	0.2	—	MHz/μs
Keyed AFT Input Range	V_1	2	—	0.35	0.5	0.65	V_{p-p}
Keyed AFT Input Frequency	T_1	2	(Note 11)	8.0	16.7	50	ms
AFT Width of Dead Zone	V_{DEAD}	2	(Note 13)	250	340	400	kHz
Digital AFT Voltage Low Level	V_{20L}	2	(Note 13)	—	0.3	0.5	V
DG	DG	application circuit	APL 90% / (Note 14)	—	±2.0	±5.0	%

CHARACTERISTIC	SYMBOL	TEST CIRCUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
DP	DP	application circuit	APL 90% / (Note 14)	—	±2.0	±5.0	°
Inter-Modulation 2	IM2	application circuit	2.15MHz beat level / (Note 15)	40	45	—	dB
Inter-Modulation 3	IM3	application circuit	1.43MHz beat level / (Note 15)	40	50	—	dB
Video Output S/N	S/N_{SAT}	application circuit	C/N = ∞	48	51	—	dB

MEASUREMENT CONDITION

(Note 1) 1st AGC Shoulder Level Range : AGC_{MAX}

F = 402.78MHz input level v_{in} = 0 to −40dBmW (50Ω) to pin 20. Measure v_{in} that pin 18 voltage is lower than 4V by opening pin 16 and raising v_{in}.

(Note 2) 1st AGC Control Sensitivity : ΔAGC

Input f = 402.78MHz v_{in} = 0 ~ −40dBmW (50Ω) to pin 20. Calculate v_{in} that pin 18 voltage is 4V / 1V (as v_{in1}, v_{in2}), using the equation below.

$$\Delta AGC = -3/(v_{in1} - v_{in2}) \quad V/dB$$

(Note 3) Signal Level Sensitivity : ΔV/ΔV

Measure each output voltage of pin 19 at v_{in} = −40, −60dBmW (50Ω)

$$\Delta V/\Delta V = (V_{-60} - V_{-40})/20 \quad mV/dB$$

(Note 4) VCO Conversion Sensitivity : β

Input mainly f = 402.78MHz and sweep ±5MHz, v_{in} = −30dBmW (50Ω) to pin 20. Calculate $\beta = 10/(Vdet_{+5} - Vdet_{-5})$ and multiply the gain portion (2.66) of video amplifier when outputting a direct current voltage to pin 3 at 407.78MHz, 397.78MHz as $Vdet_{+5}$ and $Vdet_{-5}$ each.

(Note 5) VCO Temperature Drift : Δf_{Ta}

Short pin 6 and 7, and connect pin 14 to GND.
Measure the VCO frequency at ambient temperature Ta = 25°C, −10°C +65°C and calculate how much changes from 25°C. (read out the VCO leakage output by spectrum analyzer.)

(Note 6) PLL Lock Range : f_L, Capture Range : fca

Measure the range that synchronizes with VCO by putting pin 20 input frequency away from the free-running frequency.

(Note 7) Demodulation Output Level : V_{out}

Input pin 20 f = 402.78MHz, f_m = 100kHz, Δf = 10MHz$_{p-p}$, v_{in} = −30dBmW (50Ω)
Open pin 4 and 5 and measure the output level of pin 3.

(Note 8) Video Amplifier Variable Width : V_{out5}, V_{out5}

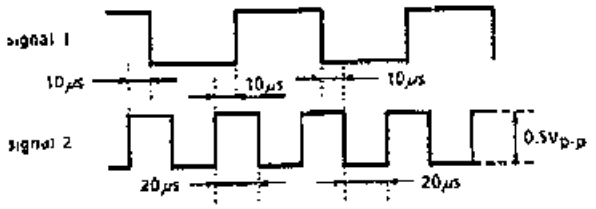
Input pin 20 f = 402.78MHz, f_m = 100kHz, Δf = 10MHz$_{p-p}$, v_{in} = −30dBmW (50Ω)
Measure the variation of video output by shorting between pin 4 and 5 and connecting a 5kΩ resistance.

(Note 9) Demodulation Output level Width, Group Delay Characteristics : V_{outA}, τpd

Input pin 20 f = 402.78MHz, f_m = 100kHz, 60Hz to 4MHz to 9MHz, Δf = 5MHz$_{p-p}$, v_{in} = −30dBmW (50Ω)
Compare to the value at 100kHz by opening pin 4 and 5, and measuring the output level and group delay of pin 3.

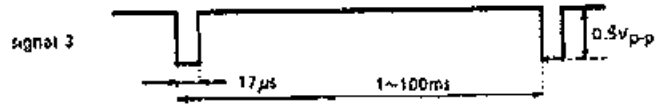
(Note 10) S/H Sample Speed : Δf_{spl}

Input the signal 1 below for a modulation signal. Input the signal 2 below to pin 1. Observe the differential voltage waveform between pin 29 and 30, and measure the slew rate in the sampling period.



(Note 11) Keyed Pulse Allowable Period : T_1

Input the signal below to pin 1 and open pin 27 and 28. Observe the pin 23 output and change f so as to be 2.5V voltage.



Measure the frequency range in which a 2kHz sine wave does not output to pin 23, by changing the signal 3 period.
If the sample-hold circuit malfunctions, the 2kHz sine wave will be outputted from pin 23.

(Note 12) AFT Sensitivity : $\Delta f / \Delta V_{23}$

Input pin 20 f = 402.78MHz ± 1MHz, v_{in} = −30dBmW (50Ω)
Adjust f so that pin 23 output will be 2.5V. By moving f up. and down, calculate each frequency as f_H, f_L when pin 23 voltage varies 0.5V using the following equation.

$$\Delta f / \Delta V_{23} = f_H - f_L \ (MHz/V)$$

(Note 13) AFT Digital Output Width of Blind Sector : f_{DEAD}

Input pin 20 f = 402.78MHz ± 5MHz, v_{in} = −30dBmW (50Ω)
Measure the input frequency range in which both pin 24 and 25 become high level, by sweeping f.

(Note 14) DG, DP

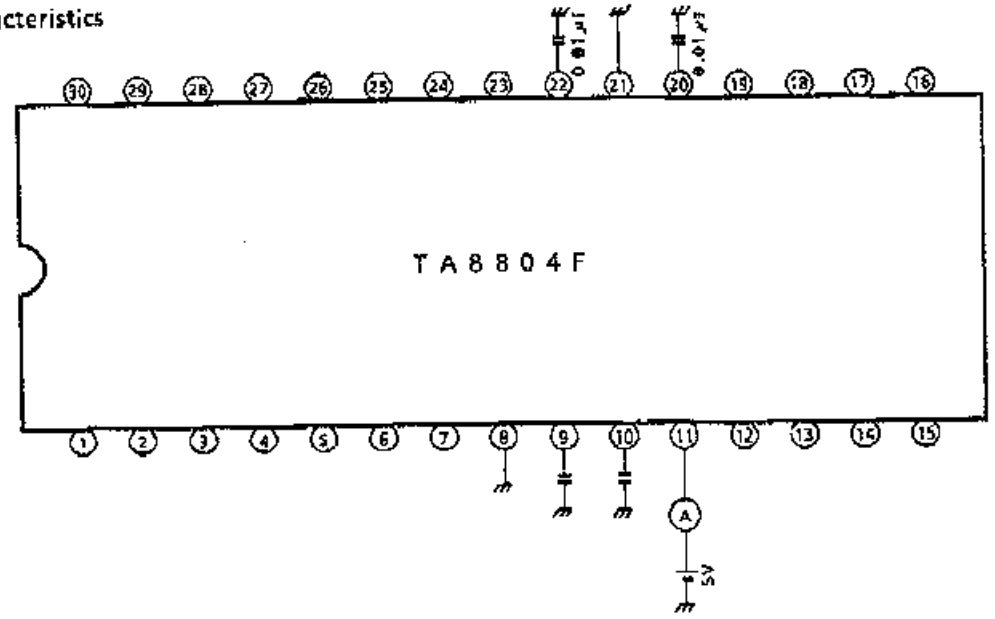
Input pin 20 f = 402.78MHz ± 5MHz, v_{in} = −30dBmW (50Ω), Δf = 17MHz$_{p-p}$, Gray level video signal (APL : 10~90%)···Pre-emphasis-on

(Note 15) IM2, IM3

Input pin 20 f = 402.78MHz ± 5MHz, v_{in} = −30dBmW (50Ω), Δf = 17MHz$_{p-p}$. Color subcarrier (3.579MHz), Sound subcarrier (5.7272MHz) ···
Observe the frequency component outputting to the screen output pin (pin 3) through the video gate of a video noise meter by spectrum analyzer, and measure the level difference between 3.579MHz component and 2.15MHz, 1.43MHz components.

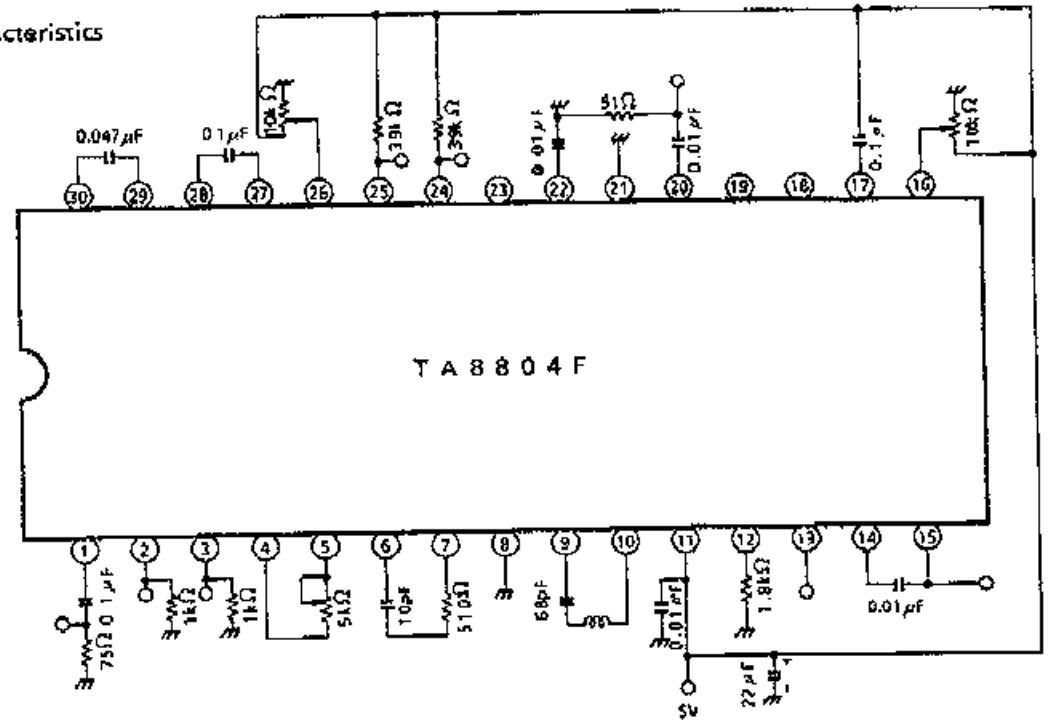
TEST CIRCUIT 1

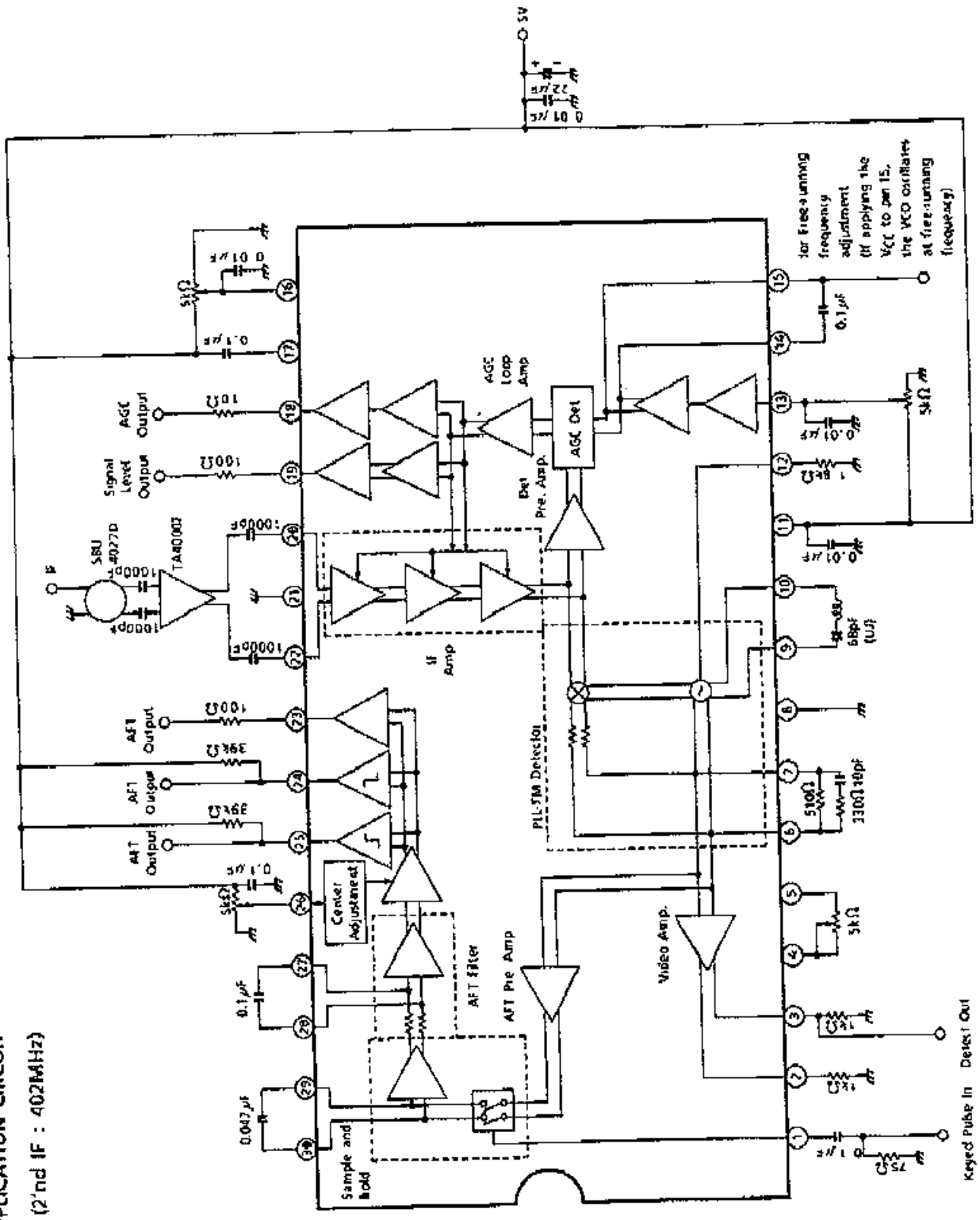
DC characteristics



TEST CIRCUIT 2

AC characteristics





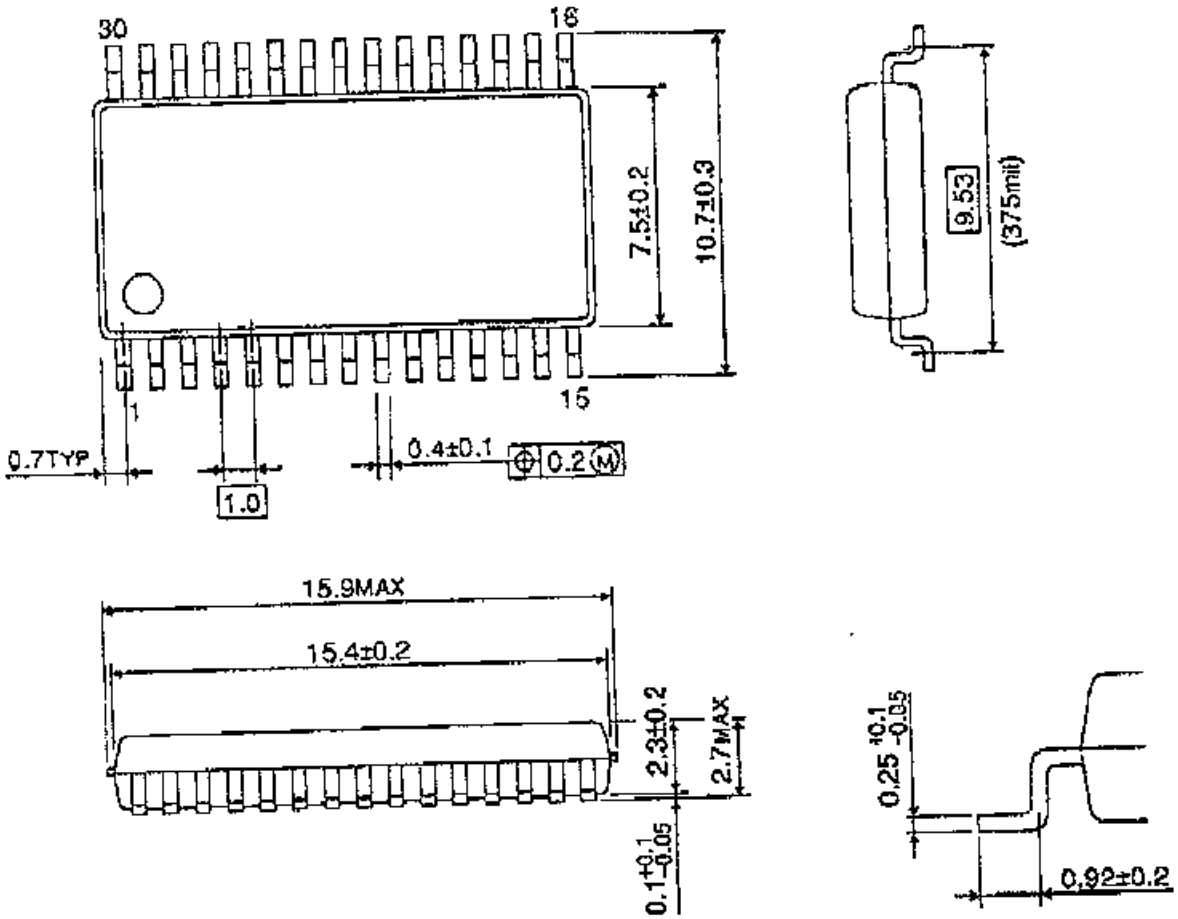
APPLICATION CIRCUIT

(2'nd IF : 402MHz)

TA8804F-15

OUTLINE DRAWING
SSOP30-P-375

Unit : mm



Weight : 0.63g (Typ.)

Si983 TECHNICAL DESCRIPTION

A. CIRCUIT OPERATION :

1. USB interface communicates with PC.
2. 900MHz channel for data/voice transmit and receive.
3. 2.4G channel for video and voice receive.

B. COMPONENT DESCRIPTION:

CATEGORY	NUMBER	NAME	DESCRIPTION
Integated circuit	MC68HC908JB8	Microcontroller	Communicates with PC. Process all date input and output.
Integated circuit	ST16C550CJ44	UART with 16-byte FIFO's	UART interface to Tx and Rx the data
Integated circuit	LM324	Operation Amplifier	Audio signal amplifier
Integated circuit	CD4053	Analog Mutiplexer	Analog switches to turn on/off the audio/data signal
Integated circuit	74HC132	NAND GATES	Reshape data signal, Invertor
Integated circuit	HT7533	3.3V Regulator	Power supply
Integated circuit	AIC1563	DC/DC Converter	Convert 5V to 10V
Transistor	2N3906	Small signal transistor	900MHz module power on/off
Transistor	2N3904	Small signal transistor	Automatic gain contol
Transistor	PN2222A	NPN silicon transistor	Automatic gain contol
Transistor	8550D	NPN silicon transistor	Video power on/off
Diode	1N5817	Schottky rectifier	Rectifier for the DC/DC Converter
Crystal	6.000MHz	Crystal 30ppm	Microcontroller operation
Crystal	1.8432MHz	Crystal 30ppm	ST16C550CJ44 operation
Integated circuit	TA31136FN	FM IF DETECTOR	900mhZ FM IF DETECT operation
Integated circuit	TB31202FN	PLL FREQUENCY SYNTHESIZER	Control Tx & RX VCO frequency operation
Integated circuit	SP5055	2.6GHz SYNTHESIZER	Control 2.4GHz RX VCO frequency operation
Integated circuit	TA8804F	FM DEMODULATION	2.4GHz FM Demodulation operation
Crystal	10.25MHz	Crystal 20ppm	TB31202FN operation
Crystal	4.000MHz	Crystal 20ppm	SP5055 operation