1. Hardware

1.1. About the A840

The A840 is a low power gateway intended primarily as base station for the Adcon Telemetry's networks. The device is capable of controlling a telemetry network via an external wireless communicator (e.g. an A440 wireless modem), store the data on its flash memory based local file system and provides access to/from a TCP/IP network.

To withstand power failure conditions, the A840 is equipped with a 7 cell NiMH rechargeable battery. The battery is managed by the integrated charger unit. An A840 can typically run for one day on the built-in battery.

With Linux as the operating system, the A840 is open for many different applications and interfaces.

1.2. Description

The complete electronics is situated on the main board (A840MB) except for the optional modem board, which can be installed if desired (most systems are however

delivered with a modem pre-installed). For additional details, please refer to the attached schematic diagrams.

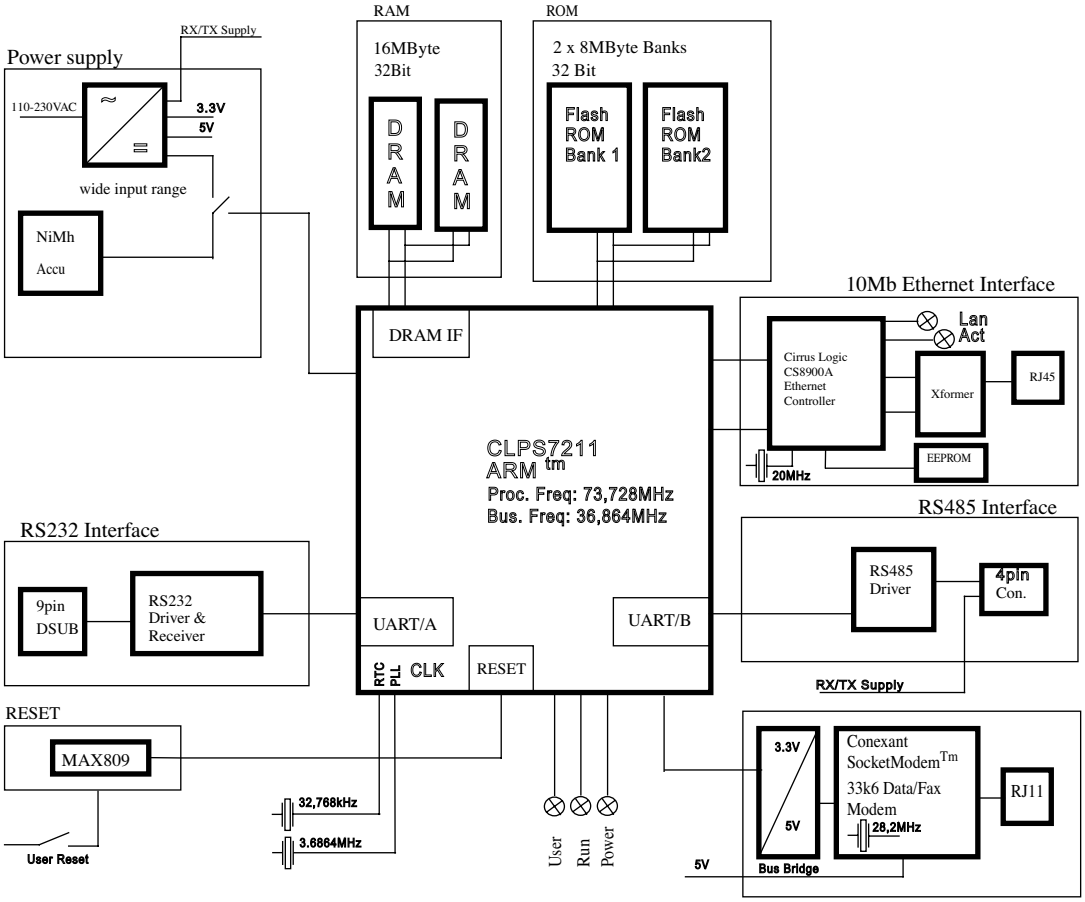

Figure 1. A840 Telemetry Gateway Block Diagram

1.2.1. Power Supply

The mains voltage (100-240V~) is converted to 12V/0.42ADC via the AC/DC converter PS1 (see also the Figure 4 on page 14). The 12V supply is used to charge the NiMH battery via Q1 and R2 in standard charge mode and via R1 and R2 in trickle charge mode. The battery voltage is measured via ADC U1. To prevent deep discharging of the battery, the power supply can be completely shut down via PORT PD7. Also the external communication unit can be shut off via PORT PD3. Once a complete shutdown has occurred, the system wakes up only when the mains input voltage is re-applied.

The DC/DC converter U3 is used to provide the 3.3V system voltage. The CPU core voltage is provided by U9, a 2.5V low drop-out series voltage regulator. The 3.3V supply is monitored by U4, which releases the POR line at least 140ms after Vcc is

above 3.08V. The 12V supply is monitored by Q4 and enables the system to recognize power failures.

A special reset circuitry is used to wake up the CPU after a USER RESET or POR. This unit is build around U10, U19 and Q5.

1.2.2. CPU

A low power high performance ARM CPU from Cirrus Logic (EP7211) is the heart of the A840 (see also the Figure 5 on page 15). The core-logic functionality of the EP7211 is build around an ARM720T processor.

1.2.2.1. Booting

Two operating modes are used. These modes are BOOT mode and NORMAL mode. Jumper JP1 must be set to enable the BOOT mode. In BOOT mode, after RESET, the CPU waits for code to be downloaded via the serial interface (RS232). After finishing the transmission, the CPU executes this code. After this procedure, the jumper JP1 has to be removed to enable the NORMAL mode.

Note: A complete POWER OFF/ON cycle is required after changing the mode, otherwise the mode change will not be recognized by the CPU.

1.2.2.2. Boot Options

The desired Boot Option can be configured via R32/R33 and R35/36, see "DS352PP1 Functional Description" for further details. The 32-bit Boot option is used on the A840MB.

1.2.2.3. User Reset Button

The User Reset Button is located on the back of the unit. Pushing the button resets and wakes up the CPU. The DRAM refresh will not be disturbed. If the unit is jumpered for NORMAL mode, booting the operating system will occur next.

1.2.3. Clock oscillators

Two clock oscillators are used for the CPU. The 32.768kHz oscillator, based on X1, is used for the RTC. The 3.6864MHz oscillator is the reference input of the on-chip PLL clock generator. The PLL clock generator provides all BUS and CPU clocks. For complete details on the Cirrus Logic CLPS7211 CPU refer to "DS352PP1 Functional description". The on-chip PLL mode is used on the A840MB, R34 must therefore be populated. The 20MHz crystal X3 provides the system clock for the ethernet controller U11.

1.2.4. Memory

The A840 includes 16 MB Flash, 16 MB RAM and an small 128 bytes serial EEPROM.

1.2.4.1. FLASH

16MB (mega byte) FLASH, organized in 2 banks of 2MB x 32 bits each is available on the A840MB. R13, R14, R39 and R40 must be populated to accommodate four Intel® TE28F320C3 chips. CS0 and CS1 are the related chip select signals. According to the "flexible block locking feature" of the flashes, some or all blocks can be locked down and the signal WP is used to protect these blocks. Non locked down blocks are protected by software commands only.

1.2.4.2. EDO-DRAM

16MB EDO-DRAM, organized in 1 Bank of 4MB x 32, are available on the A840MB. RAS0 is the related chip select signal. Low power self-refreshing is supported by the DRAM chips, that means, even if the CPU is in "STANDBY-MODE", the content of the DRAM is preserved. Due to the internal organization of the chips, the bank is split into 2 section of 8MB each.

1.2.4.3. SERIAL EEPROM

128 Bytes (64x16) of serial EEPROM (U2) are accessible via the ethernet controller U11. The first 8 words contains the MAC address, ethernet controller setup and a checksum. The remaining words can be used for other non-volatile data of the A840. For details of accessing this memory please consult the CS8900 Manual.

1.2.4.4. Memory Map

Memories and peripherals are mapped according to the following table:

CSn	Device	Remarks
CS0	FLASH, 8MB	U12, U13, 1st FLASH bank
CS1	FLASH, 8MB	U14, U15, 2nd FLASH bank
RAS0	DRAM, 16MB	U5, U6
CS2	ETHERNET	U11, CS8900A
CS3	Modem	U17, SF336D/SP

1.2.5. Ethernet controller

The CS8900 U11 incorporates the complete 10-BaseT interface, including BUS IF, MAC, ENC and PHY (see also the Figure 6 on page 16). The 10-BaseT line is connected via P2 and T2 to the controller. R18 – R20 and C24 are used for line impedance matching and EMC purposes. The serial EEPROM U2 is used to store configuration data and the MAC-address. The line condition can be observed via D2 (ACT) and D3 (LAN) which are visible on the front panel of the A840. The ACT led lights up when valid link pulses are present. The LAN led lights up when a packet is received, a packet is sent or a collision is detected. The CS2 line is used to select U11, A2 to A4 are used to address the internal registers. For power saving purposes, it is possible to switch the controller into the hardware sleep mode via PB7 ($\overline{\text{ETH-SLEEP}}$) in conjunction with the desired control word written to it.

1.2.6. RS232, Serial Interface, UART1

The 15kV ESD protected RS-232 driver U7, a MAX3243, is used to convert the 3.3V signals to RS-232 compatible signals (see also the Figure 7 on page 17). The signal FORCEOFF (PB4) can be used to force the device to the power down state. Even in power down state of U7, the external signal RXD can wake up the CPU. Note that the first received character is lost when the CPU wakes up from standby. The existence of an external serial device can be checked via the INVALID signal (PB5). This bit is "0" when no external device is attached. The 16C550-like UART supports the handshaking signals DCD & CTS directly, RI, DTR and RTS via GPIO. This signals are connected to PB2, PD4 and PB1.

1.2.7. RS485, Serial Interface, UART 2

The 15kV ESD protected RS-485 driver U16 is used to communicate with the external RX/TX modem unit A440. Similar to the RS-232 Interface, any activity on the RS-485 line can wake up the CPU; as with the other serial line, some steps must be taken in the software driver due to the first received character that is lost. For power saving purposes, the RX and the TX driver can be switched off via the signals RS485RXEN and RS485TXEN. The RS-485 line is held in a known, so called *inactive* state, to prevent false start bit detection of the UARTs.

1.2.8. Analog Modem, 33.6kbps

The Conexant SocketModem contains a complete data/fax subsystem. As a V.34 data modem, the SocketModem operates at line speeds up to 33.6kbps. Error correction and compression (V.42bis/MNP 5) maximize data transfer integrity and boost average data troughput up to 230 kbps. In the V.32bis mode, the SocketModem operates at line speeds up to 14.4kbps.

In FAX mode, the modem supports V.17 fax (Class I/II) send and receive rates up to 14.4 kbps and T.30 protocol.

The SocketModem can be installed on the A840MB via the 64pin connector U17. A RJ-11 connector, placed on the back of the A840, is used for connection to the analog telephone line.

One 5V voltage regulator (U22) and two bus voltage translators (U18/U20) are used to connect the SocketModem (which operates at 5V) to the 3.3V system bus.

The modem can be powered down completely for power saving purpose. PORT PB0 is used to switch on and off the 5V regulator and the bus translators. A delay of approx. 2sec is required after the modem is powered on. Accessing the modem registers in the startup phase will fail. The modem will also enter a low-power sleep mode, if register S24 is configured accordingly. See also the document "1131(RCxxxDATCommandManual)".

The CPU communicates via an 16550 style interface with the SocketModem. The Modem CS input is connected to CS3 of the CPU. CS3 also enables the bus translator U18, which translates the 3.3V data bus to the 5V data bus and vice versa. The direction of the dataflow is controlled by the signal MOE. The other bus translator is always enabled and translates the signals $\overline{\text{MOE}}$, $\overline{\text{MWE}}$, $\overline{\text{CS3}}$, $\overline{\text{URST}}$ and $\overline{\text{A5..A3}}$. The interrupt output of the modem is translated via Q9 and is connected to $\overline{\text{EINT2}}$ of the CPU.

For complete details on the register set see "SocketModem SF336D/SP Series Designer's Guide" and "MCU Technical Reference Manual".

1.2.9. LED indicators

To examine the status of the A840, three LED indicators are mounted on the front plate of the device. The LEDs D4, D8 and D9 can be switched on/off individually via the ports PD0-PD2 respectively. LED D2 and D3 are connected to the Ethernet chip. LED D9 normally reflects the power supply status, this is done by the software.

Mains	LED9 (PWR)
Power o.k.	ON
Failure	BLINKING

For power saving purpose LEDs D2 and D3 can be forced off via PB6 ($\overline{\text{LEDSON}}$).

1.2.10. Connectors

All user accessible connectors are located on the back of the A840. See the table below for an explanation of their purpose.

Connector	Purpose	Type
P2	Network connector (10BaseT)	RJ45, CAT-5
P3	Appliance inlet	IEC 60320 -1/C14
P4	RS-485, connection to A440 or equivalent	Binder 763
P5	RS-232, serial port 1	D-SUB 9, male
P6	Telephone Line	RJ11