2 Device Pinout Diagram

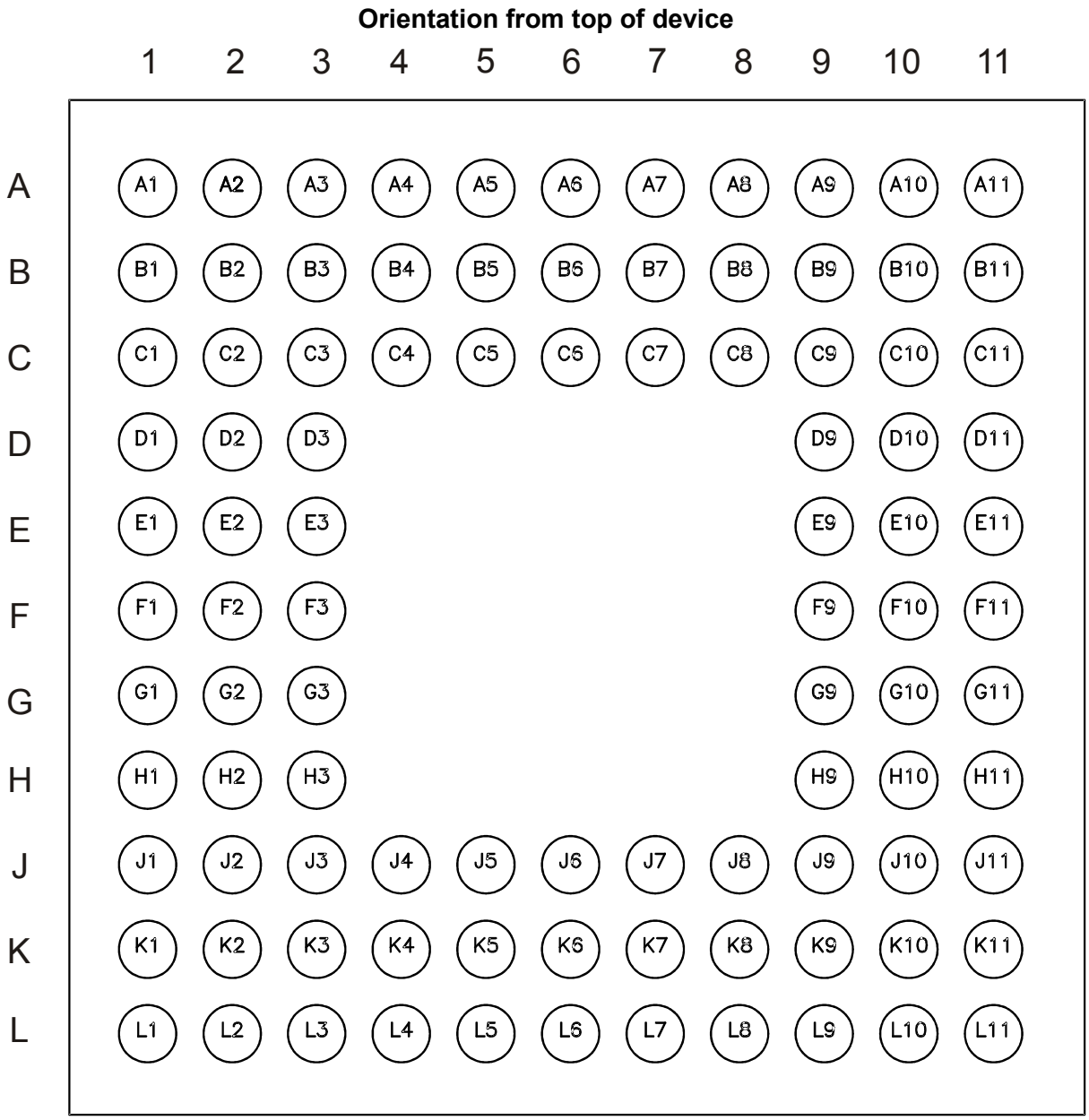

Figure 2.1: BlueCore2-External Device Pinout Diagram

Notes:

Device pinout diagram is the same for:

10x10mm LFBGA (BN)

8x8x1mm VFBGA package (DN)

6x6x1mm VFBGA package (EN)

6x6x0.6mm LGA package (LN)

3 Device Terminal Functions

Radio	Ball	Pad Type	Description
RF_IN	E1	Analogue	Single ended receiver input
PIO[0]/RXEN	C1	Bi-directional with weak internal pull-up/down	Control output for external LNA (if fitted)
PIO[1]/TXEN	C2	Bi-directional with weak internal pull-up/down	Control output for external PA Class 1 applications only
TX_A	G1	Analogue	Transmitter output/Switched Receiver input
TX_B	F1	Analogue	Complement of TX_A
AUX_DAC	D2	Analogue	Voltage DAC output

Synthesiser and Oscillator	Ball	Pad Type	Description
XTAL_IN	L1	Analogue	For crystal or external clock input
XTAL_OUT	L2	Analogue	Drive for crystal
LOOP_FILTER	J1	Analogue	Connection to external PLL loop filter

External Memory Port	Ball	Pad Type	Description
REB	D10	CMOS output, tristatable with internal weak pull-up	Read enable for external memory (active low)
WEB	E10	CMOS output, tristatable with internal weak pull-up	Write enable for external memory (active low)
CSB	C10	CMOS output, tristatable with internal weak pull-up	Chip select for external memory (active low)

Address Lines	Ball	Pad Type	Description
A[0]	D9	CMOS output, tristatable	Address line
A[1]	E9	CMOS output, tristatable	Address line
A[2]	E11	CMOS output, tristatable	Address line
A[3]	F9	CMOS output, tristatable	Address line
A[4]	F10	CMOS output, tristatable	Address line
A[5]	F11	CMOS output, tristatable	Address line
A[6]	G9	CMOS output, tristatable	Address line
A[7]	G10	CMOS output, tristatable	Address line
A[8]	G11	CMOS output, tristatable	Address line
A[9]	H9	CMOS output, tristatable	Address line
A[10]	H10	CMOS output, tristatable	Address line
A[11]	H11	CMOS output, tristatable	Address line
A[12]	J8	CMOS output, tristatable	Address line
A[13]	J9	CMOS output, tristatable	Address line
A[14]	J10	CMOS output, tristatable	Address line
A[15]	J11	CMOS output, tristatable	Address line
A[16]	K9	CMOS output, tristatable	Address line
A[17]	K10	CMOS output, tristatable	Address line
A[18]	K11	CMOS output, tristatable	Address line

Data Bus	Ball	Pad Type	Description
D[0]	K8	Bi-directional with weak internal pull-down	Data line
D[1]	L9	Bi-directional with weak internal pull-down	Data line
D[2]	L10	Bi-directional with weak internal pull-down	Data line
D[3]	L11	Bi-directional with weak internal pull-down	Data line
D[4]	L8	Bi-directional with weak internal pull-down	Data line
D[5]	J7	Bi-directional with weak internal pull-down	Data line
D[6]	K7	Bi-directional with weak internal pull-down	Data line
D[7]	L7	Bi-directional with weak internal pull-down	Data line
D[8]	J6	Bi-directional with weak internal pull-down	Data line
D[9]	K6	Bi-directional with weak internal pull-down	Data line
D[10]	L6	Bi-directional with weak internal pull-down	Data line
D[11]	J5	Bi-directional with weak internal pull-down	Data line
D[12]	K5	Bi-directional with weak internal pull-down	Data line
D[13]	L5	Bi-directional with weak internal pull-down	Data line
D[14]	J4	Bi-directional with weak internal pull-down	Data line
D[15]	K4	Bi-directional with weak internal pull-down	Data line

PCM Interface	Ball	Pad Type	Description
PCM_OUT	B9	CMOS output, tristatable with internal weak pull-down	Synchronous data output
PCM_IN	B10	CMOS input, with internal weak pull-down	Synchronous data input
PCM_SYNC	B11	Bi-directional with weak internal pull-down	Synchronous data SYNC
PCM_CLK	B8	Bi-directional with weak internal pull-down	Synchronous data clock

USB and UART	Ball	Pad Type	Description
UART_TX	C8	CMOS output	UART data output active high
UART_RX	C9	CMOS input with weak internal pull-down	UART data input active high
UART_RTS	B7	CMOS output, tristatable with internal pull-up	UART request to send active low
UART_CTS	B6	CMOS input with weak internal pull-down	UART clear to send active low
USB_D+ (1)	A7	Bi-directional	USB data plus
USB_D- (1)	A6	Bi-directional	USB data minus

Test and Debug	Ball	Pad Type	Description
RESET	F3	CMOS input with weak internal pull-down	Reset if high. Input debounced so must be high for >5ms to cause a reset
SPI_CSB	A4	CMOS input with weak internal pull-up	Chip select for Synchronous Serial Interface active low
SPI_CLK	B5	CMOS input with weak internal pull-down	Serial Peripheral Interface clock
SPI_MOSI	A5	CMOS input with weak internal pull-down	Serial Peripheral Interface data input
SPI_MISO	B4	CMOS output, tristatable with weak internal pull-down	Serial Peripheral Interface data output
TEST_EN	G3	CMOS input with strong internal pull-down	For test purposes only (leave unconnected)

PIO Port[3]	Ball	Pad Type	Description
PIO[2]/ USB_PULL_UP [1] [2]	B3	Bi-directional with programmable weak internal pull-up/down	PIO or USB pull-up (via 1.5kΩ resistor to USB_D+)
PIO[3]/USB_WAKE_ UP/RAM_CSB [1] [2]	B2	Bi-directional with programmable weak internal pull-up/down	PIO or output goes high to wake up PC when in USB mode or external RAM chip select
PIO[4]/USB_ON [1] [2]	B1	Bi-directional with programmable weak internal pull-up/down	PIO or USB on (input senses when VBUS is high, wakes BlueCore2-External)
PIO[5]/USB_DETACH [1] [2]	A3	Bi-directional with programmable weak internal pull-up/down	PIO line or chip detaches from USB when this input is high
PIO[6]/CLK_REQ	C3	Bi-directional with programmable weak internal pull-up/down	PIO line or clock request output to enable external clock for external clock line
PIO[7]	E3	Bi-directional with programmable weak internal pull-up/down	Programmable input/output line
PIO[8]	D3	Bi-directional with programmable weak internal pull-up/down	Programmable input/output line
PIO[9]	C4	Bi-directional with programmable weak internal pull-up/down	Programmable input/output line
PIO[10]	C5	Bi-directional with programmable weak internal pull-up/down	Programmable input/output line
PIO[11]	C6	Bi-directional with programmable weak internal pull-up/down	Programmable input/output line
AIO[0]	K3	Bi-directional	Programmable input/output line
AIO[1]	L4	Bi-directional	Programmable input/output line
AIO[2]	J3	Bi-directional	Programmable input/output line

Notes:

[1] USB functions are available on BC212015 only.

[2] USB functions can be software mapped to any PIO terminal.

[3] All PIO's are configured as inputs with weak pull-downs at reset.

Power Supplies and Control	Ball	Pad Type	Description
VDD_RADIO	D1 H3	VDD	Positive supply connection for RF circuitry
VDD_VCO	H1	VDD	Positive supply for VCO and synthesiser circuitry
VDD_ANA	K1	VDD	Positive supply for analogue circuitry
VDD_CORE	A8	VDD	Positive supply for internal digital circuitry
VDD_PIO	A1	VDD	Positive supply for PIO and AUX DAC
VDD_PADS	A10	VDD	Positive supply for all other input/output
VDD_MEM	D11	VDD	Positive supply for external memory port and AIO
VSS_RADIO	E2 F2 G2	VSS	Ground connections for RF circuitry
VSS_VCO	J2 H2	VSS	Ground connections for VCO and synthesiser
VSS_ANA	L3 K2	VSS	Ground connections for analogue circuitry
VSS_CORE	A9	VSS	Ground connection for internal digital circuitry
VSS_PIO	A2	VSS	Ground connection for PIO and AUX DAC
VSS_PADS	A11	VSS	Ground connection for input/output except memory port
VSS_MEM	C11	VSS	Ground connection for external memory port
VSS	C7	VSS	Ground connection for internal package shield

4 Electrical Characteristics

Absolute Maximum Ratings		
Rating	**Min**	**Max**
Storage Temperature	-40°C	+150°C
Supply Voltage: VDD_RADIO, VDD_VCO, VDD_ANA, VDD_CORE	-0.40V	1.90V
Supply Voltage: VDD_PADS, VDD_PIO, VDD_MEM	-0.40V	3.60V

Recommended Operating Conditions		
Operating Condition	**Min**	**Max**
Operating Temperature Range[1]	-40°C	105°C
Supply Voltage: VDD_RADIO, VDD_VCO, VDD_ANA, VDD_CORE	1.70V	1.90V
Supply Voltage: VDD_PADS, VDD_PIO, VDD_MEM	1.70V	3.60V

Note:

[1] The device functions across this range. See long form data book for guaranteed performance over temperature.

Input/Output Terminal Characteristics				
Digital Terminals	**Min**	**Typ**	**Max**	**Unit**
Input Voltage				
V_{IL} input logic level low (VDD=3.0V)	-0.4	-	+0.8	V
(VDD=1.8V)	-0.4	-	+0.4	V
V_{IH} input logic level high	0.7VDD	-	VDD+0.4	V
Output Voltage				
V_{OL} output logic level low, (I_O = 4.0mA), VDD=3.0V	-	-	0.2	V
V_{OL} output logic level low, (I_O = 4.0mA), VDD=1.8V	-	-	0.4	V
V_{OH} output logic level high, (I_O = -4.0mA), VDD=3.0V	VDD-0.2	-	-	V
V_{OH} output logic level high, (I_O = -4.0mA), VDD=1.8V	VDD-0.4	-	-	V
Input and Tristate Current with:				
Strong pull-up	-100	-20	-10	µA
Strong pull-down	+10	+20	+100	µA
Weak pull-up	-5	-1	0	µA
Weak pull-down	0	+1	+5	µA
I/O pad leakage current	-1	0	+1	µA
C_I Input Capacitance	2.5	-	10	pF

Input/Output Terminal Characteristics (Continued)				
USB Terminals	**Min**	**Typ**	**Max**	**Unit**
Input threshold				
V_{IL} input logic level low	-	-	0.3VDD_PADS	V
V_{IH} input logic level high	0.7VDD_PADS	-	-	V
Input leakage current				
VSS_PADS< VIN< VDD_PADS[1]	-1	-	1	µA
C_I Input capacitance	2.5	-	10	pF
Output levels to correctly terminated USB Cable				
V_{OL} input logic level low	0	-	0.2	V
V_{OH} input logic level high	2.8	-	VDD_PADS	V

Notes:

VDD_CORE, VDD_RADIO, VDD_VCO and VDD_ANA are at 1.8V unless shown otherwise

VDD_PADS, VDD_PIO and VDD_MEM are at 3.0V unless shown otherwise

Current drawn into a pin is defined as positive; current supplied out of a pin is defined as negative.

(1) Internal USB pull-up disabled

Input/Output Terminal Characteristics (Continued)				
Auxiliary DAC, 8-Bit Resolution	**Min**	**Typ**	**Max**	**Unit**
Resolution	-	-	8	Bits
Average output step size[1]	12.5	14.5	17	mV
Output Voltage		monotonic[1]		
Voltage range (I_O=0)	VSS_PIO	-	VDD_PIO	V
Current range	-10	-	+0.1	mA
Minimum output voltage (I_O=100µA)	0	-	0.2	V
Maximum output voltage (I_O=10mA)	VDD_PIO-0.3	-	VDD_PIO	V
High Impedance leakage current	-1	-	+1	µA
Offset	-220	-	+120	mV
Integral non-linearity[1]	-2	-	+2	LSB
Starting time (50pF load)	-	-	10	µs
Settling time (50pF load)	-	-	5	µs

Input/Output Terminal Characteristics (Continued)				
Crystal Oscillator	**Min**	**Typ**	**Max**	**Unit**
Crystal frequency [2]	8.0	-	32.0	MHz
Digital trim range [3]	5	6.2	8	pF
Trim step size [3]	-	0.1	-	pF
Transconductance	2.0	-	-	mS
Negative resistance [4]	870	1500	2400	Ω

Input/Output Terminal Characteristics (Continued)				
Power-on reset	**Min**	**Typ**	**Max**	**Unit**
VDD falling threshold	1.40	1.50	1.60	V
VDD rising threshold	1.50	1.60	1.70	V
Hysteresis	0.05	0.10	0.15	V

Notes:

VDD_CORE, VDD_RADIO, VDD_VCO and VDD_ANA are at 1.8V unless shown otherwise

VDD_PADS, VDD_PIO and VDD_MEM are at 3.0V unless shown otherwise

The same setting of the digital trim is applied to both XTAL_IN and XTAL_OUT.

Current drawn into a pin is defined as positive, current supplied out of a pin is defined as negative.

[1] Specified for an output voltage between 0.2V and VDD_PIO -0.2V

[2] Integer multiple of 250kHz.

[3] The difference between the internal capacitance at minimum and maximum settings of the internal digital trim.

[4] XTAL frequency = 16MHz; XTAL C_0 = 0.75pF; XTAL load capacitance = 8.5pF

Radio Characteristics, VDD = 1.8V Temperature = +20°C						
	Frequency (GHz)	**Min**	**Typ**	**Max**	**Bluetooth Specification**	**Unit**
Sensitivity at 0.1% BER	2.402	-	-83	-	≤-70	dBm
	2.441	-	-85	-		dBm
	2.480	-	-85	-		dBm
Maximum received signal at 0.1% BER	2.402	-	-	-	≥-20	dBm
	2.441	-	-	-		dBm
	2.480	-	-	-		dBm
RF transmit power [1]	2.402	-	6.0	-	-6 to +4[2]	dBm
	2.441	-	6.0	-		dBm
	2.480	-	6.0	-		dBm
Initial carrier frequency tolerance	2.402	-	12	-	±75	kHz
	2.441	-	10	-		kHz
	2.480	-	9	-		kHz
20dB bandwidth for modulated carrier	2.402	-	879	-	≤1000	kHz
	2.441	-	816	-		kHz
	2.480	-	819	-		kHz
RF power control range		-	35	-	≥16	dB
RF power range control resolution		-	1.8	-	-	dB

Notes:

[1] BlueCore2-External firmware maintains the transmit power to be within the Bluetooth specification v1.1 limits.

[2] Class 2 RF transmit power range, Bluetooth specification v1.1

Average Current Consumption [1]		
VDD=1.8V Temperature = 20°C		
Mode	**Avg**	**Unit**
SCO connection HV3 (40ms interval Sniff Mode) (Slave)	26.0	mA
SCO connection HV3 (40ms interval Sniff Mode) (Master)	26.0	mA
SCO connection HV1 (Slave)	53.0	mA
SCO connection HV1 (Master)	53.0	mA
ACL data transfer 115.2kbps UART (Master)	15.5	mA
ACL data transfer 720kbps USB (Slave)	53.0	mA
ACL data transfer 720kbps USB (Master)	53.0	mA
ACL connection, Sniff Mode 40ms interval, 38.4kbps UART	4.0	mA
ACL connection, Sniff Mode 1.28s interval, 38.4kbps UART	0.5	mA
Parked Slave, 1.28s beacon interval, 38.4kbps UART	0.6	mA
Standby Mode (Connected to host, no RF activity)	0.047	mA
Deep Sleep Mode[2]	20.0	µA

Notes:

[1] Current consumption is the sum of both BC212013B or BC212015B and the flash.

[2] Current consumption is for the BC212013B and BC212015B devices only.

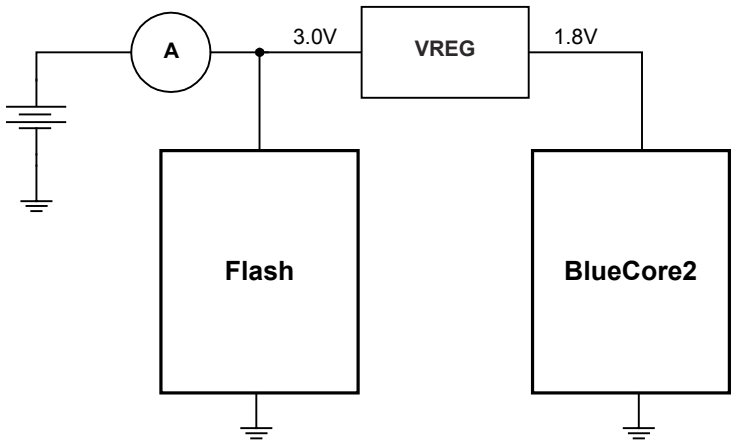

Figure 4.1: Current Measurement Circuit

5 Device Diagram

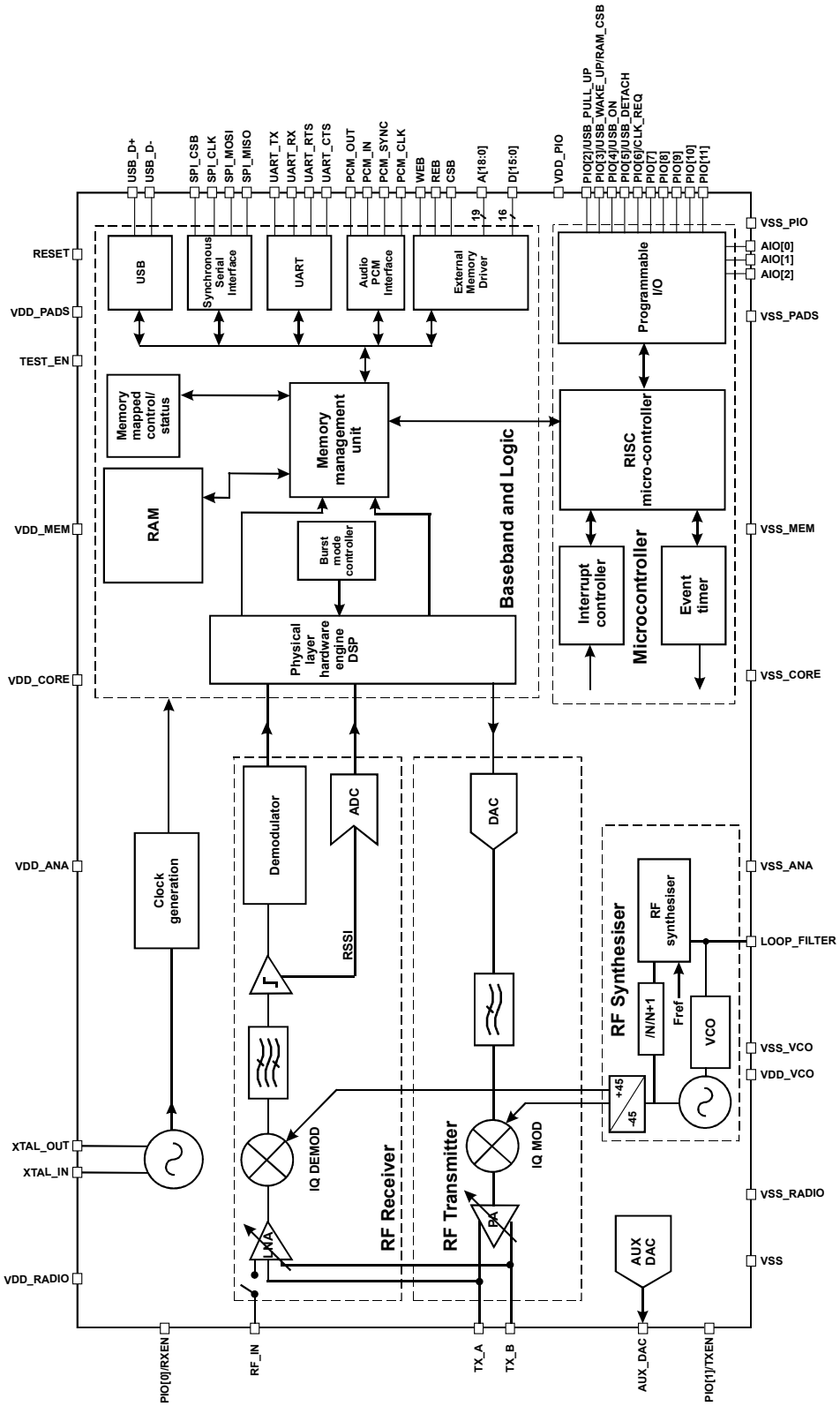

Figure 5.1: BlueCore2-External Device Diagram