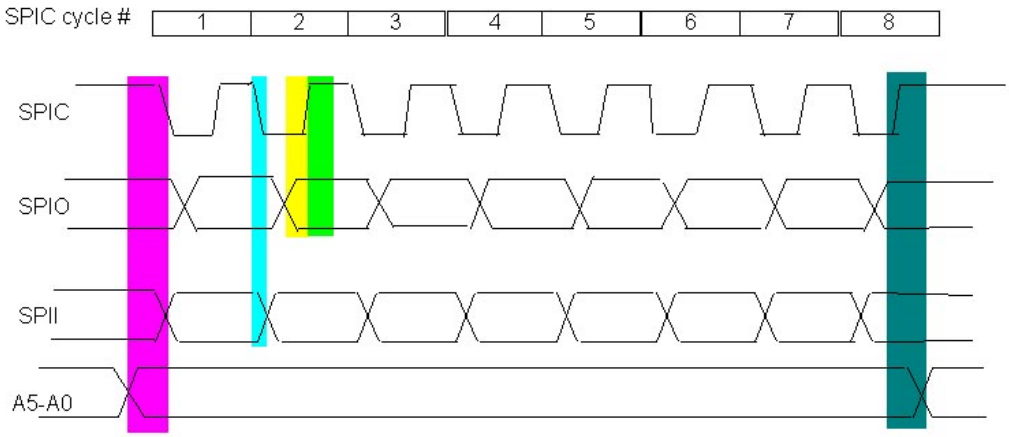


	Min	Max	Unit
1st SPIC Low after A5-A0 stable	200 ~~100~~	-	uS
SPIC Low to SPII valid	-	100	ns
SPIO valid to SPIC High (setup)	20	-	ns
SPIC High to SPIO change (hold)	0	-	ns
SPI Clock High to A5-A0 invalid	1/2 Tclk	-	

Tclk refers to the SPIC cycle. If SPIC cycle is 500kHz, 1/2 Tclk is equal to 1 us

0Figure 3-2

The Power Amplifier must be able to support a SPIC cycle of between 0kHz and 800kHz. The design of the interface should not assume that the time intervals between edges of signals during a transfer will necessarily be regular, i.e. there may be some jitter and delay during clocking, although all maximum and minimum timings given above will be adhered to.

Minimum time interval between SPI transfers to an individual PA is 500uS.

Whenever the SPI address does not match a device's SPI ID, the SPIO line must go high-impedance (<20uA output current).

3.7.1 Power Amplifier DeviceID 0 transfer protocol

DeviceID 0 is a 5 byte transfer with the following order:

Byte 1:Temperature

Byte 2: Forward Power

Byte 3: Reflected Power

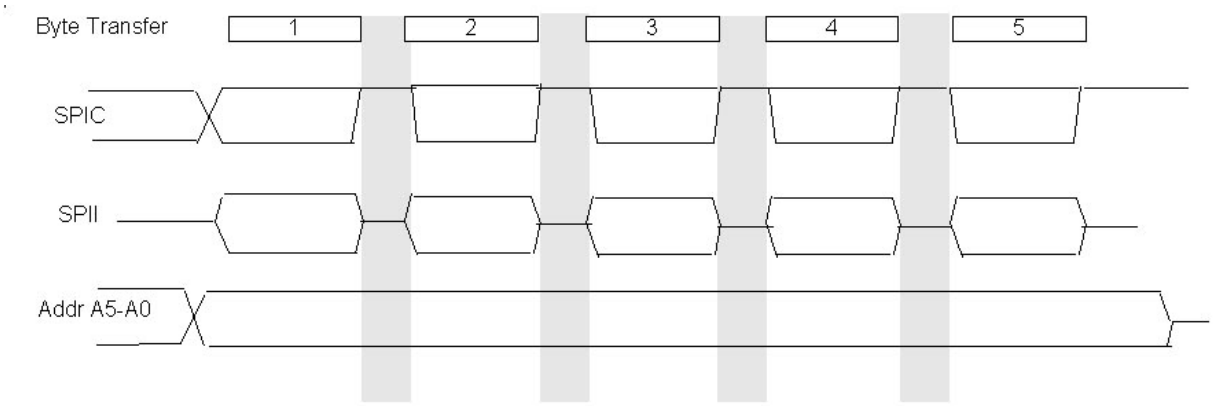
Byte 4: DC Supply Voltage

Byte 5: DC Supply Current

During the 5 byte transfer, A5-A0 will not normally change.

If prior to the completion of the 5 byte transfer, the SPI address A5..A0 changes, for example due to a host reset or error, the transfer will be halted by the PA. The next time the device ID on the addressed PA is active, the transfer begins again starting with byte 1.

The timing diagram is shown in Figure 3-3:



	Min	Max	Unit
SPIC High between bytes	300 ~~50~~	-	uS

0Figure 3-3

3.7.2 Power Amplifier DeviceID 1 transfer protocol

DeviceID 1 is a 1 byte transfer. The timing diagram for this transfer is shown in Figure 3-2.

3.7.3 Power Amplifier DeviceID 2 transfer protocol

DeviceID 2 is a 1 byte transfer. The timing diagram for this transfer is shown in Figure 3-2.

3.7.4 Power Amplifier DeviceID 3 transfer protocol

DeviceID 3 is a 1 byte transfer. The timing diagram for this transfer is shown in Figure 3-2.

3.7.5 Power Amplifier DeviceID 4 transfer protocol

3.7.5.1 Read

A read of DeviceID 4 is a 6 byte transfer with the following order:

Byte 1: 0x03 (this is the READ instruction byte for the EEPROM)

Byte 2: target EEPROM page number (0-63) shifted left two bits (e.g page 3 = 00001100b)

Byte 3: byte 1

Byte 4: byte 2

Byte 5: byte 3

Byte 6: byte 4

The timing diagram for this transfer is approximately shown in Figure 3-3, with the addition of a byte.

3.7.5.2 Write

A write to DeviceID 4 is an 8 byte transfer with the following order:

Byte 1: 0x06 (this is the WRITE ENABLE instruction byte for the EEPROM)

Byte 2: 0x02 (this is the WRITE instruction byte for the EEPROM)

Byte 3: target EEPROM page number (0-63) shifted left two bits (e.g page 63 = 11111100b)

Byte 4: byte 1

Byte 5: byte 2

Byte 6: byte 3

Byte 7: byte 4

Byte 8: 0x04 (this is the WRITE DISABLE instruction byte for the EEPROM)

The timing diagram for this transfer is approximately shown in Figure 3-3, with the addition of 3 bytes.