ALIGNMENT PROCEDURES

RECEIVER

1) Pre-selector and Post selector
Both selectors have been pre-tuned at the factory, so no alignment is required.

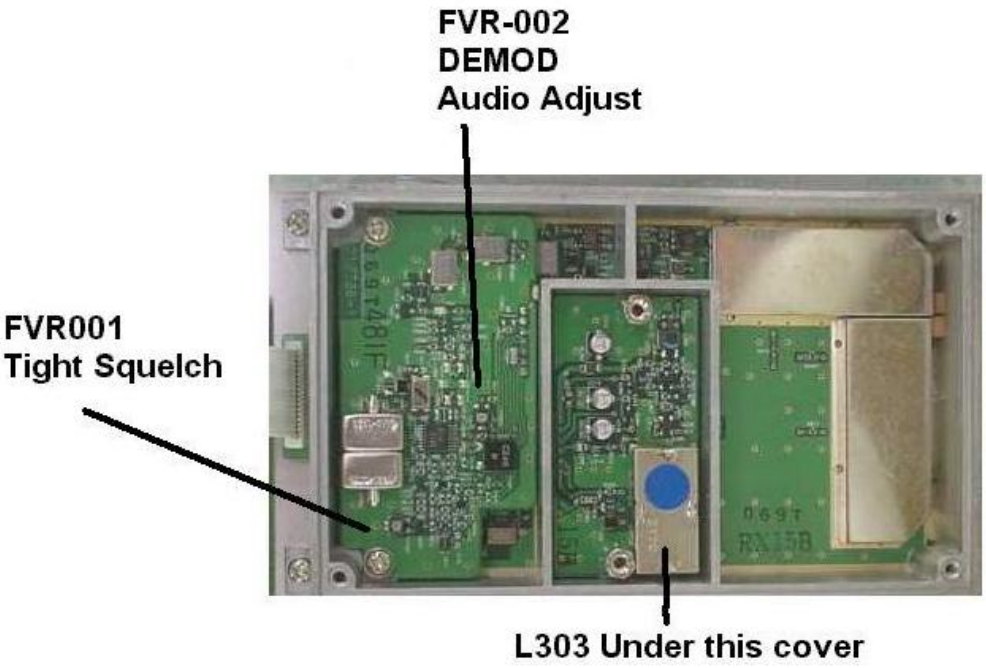
2) FVR001 Alignment
This is to adjust Tight Squelch level.

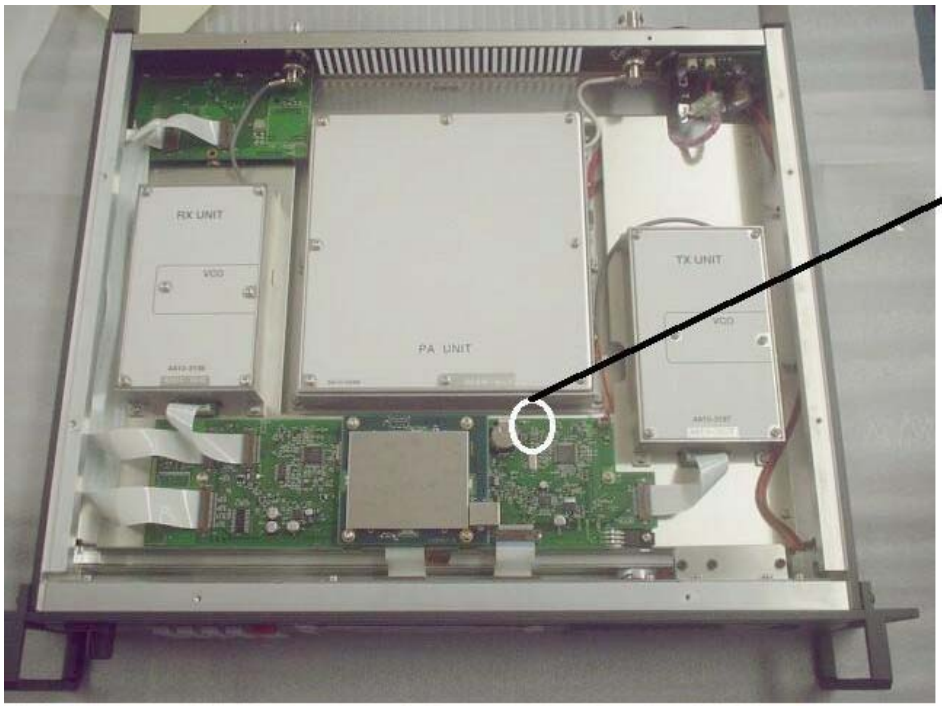
3) VCO Alignment
The VCO has been aligned at the factory to cover full sub-band. However, if you need to re-adjust VCO when you repair, set the VCO voltage at 10.5V by L303 at the high end of the sub band. The VCO cover must be removed for access.

4) RX 0 dBm Adjustment
This is 600 ohm audio available on pins 20 and 21 of the EXT Option port. It is electronically adjusted.
Ground TP-2 on Logic PCB and power up Radio. Station is now in Adjust Mode.
Release TP-2 from ground. See figure on next page
The display should look as follows:

```
      <Adjust Mode>
TXN   RX 0dbm Out
C0001      2 0 /  3 1
```

Use the “A” and “B” keys to adjust the level up or down. Pressing the “#” key will change the mode you are adjusting. “A” will increase level and “B” will decrease level. You will be able to monitor the output if the station is receiving valid carrier and signaling. Turn off Power and turn on power to return to normal operation.
The other ADJUST Modes are: RX FX828 MOD-1 (Repeated Deviation Analog; Currently Disabled) ; “DIGITAL DEVI” and “ANALOG DEVI”





TP-2
Ground to enter
"ADJUST MODE"

TRANSMITTER

1) FVR201 Alignment
   This potentiometer determines modulation balance below 300 Hz. Carefully align this potentiometer to obtain flat deviation from the lowest to the highest frequency programmed in the transmitter.

2) FVR202 Alignment
   This potentiometer determines low frequency (below 300Hz) deviation.
   When POCSAG, CTCSS and DCS are used, it may be necessary to readjust to have enough deviation at low frequency.

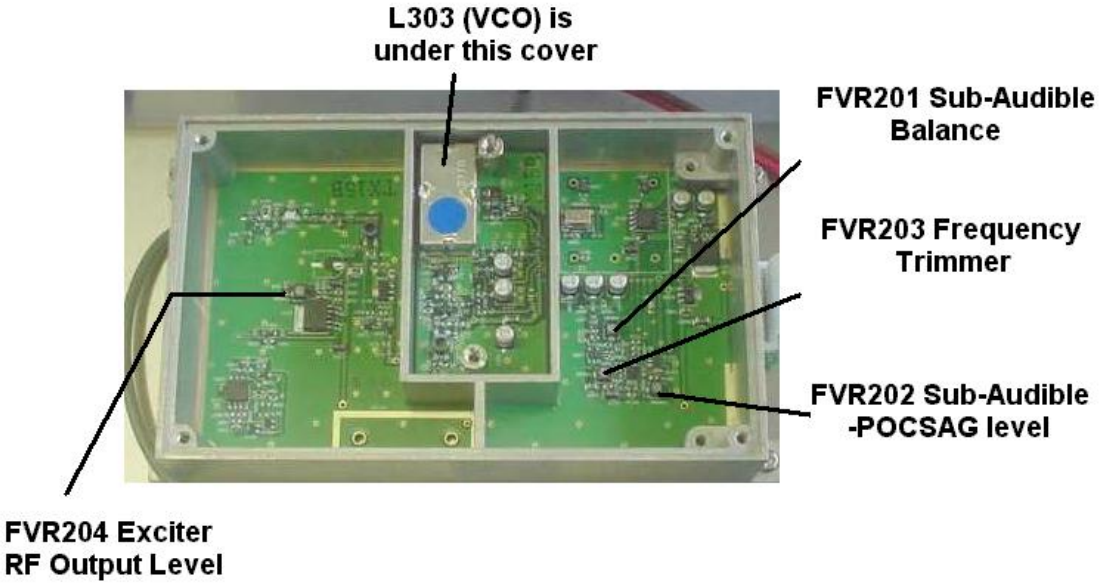
3) FVR203 Alignment
   This is to determine the carrier frequency tolerance. It will adjust deviation +/- 200Hz.

4) FVR204 Alignment
   This is to adjust transmitter output power. Approximately 80mW.

5) VCO alignment
   The VCO has already been aligned at the factory, however, if you need to re-adjust, set the VCO voltage at 10.5V at the highest sub band frequency with L303. L303 is beneath the cover (see below)

6) Maximum Deviation Alignment
   Max deviation is accomplished electronically. The station must be put into the “Adjust Mode”. Ground TP-2 on Logic PCB and cycle power, release TP-2 from ground. See figure on previous page.
   Press “#” key to Change to Display “DIGITAL DEVI” this will adjust Digital TX MAX Deviation. Key the PTT. This will place a 1200 Hz tone on the carrier Adjust the “A” to increase and “B” to decrease the level for ~2.8KHz deviation. Release PTT.

   Press the “#” to display “ANALOG DEVIATION” Key the PTT. Adjust “A” & “B” to get proper Deviation. 12.5/15 kHz channels should be less than 2.5 kHz with Sub-Audible Tone and 25/30 kHz channels should be less than 5 kHz with Sub-Audible Tone. Recycle power to return to normal operation



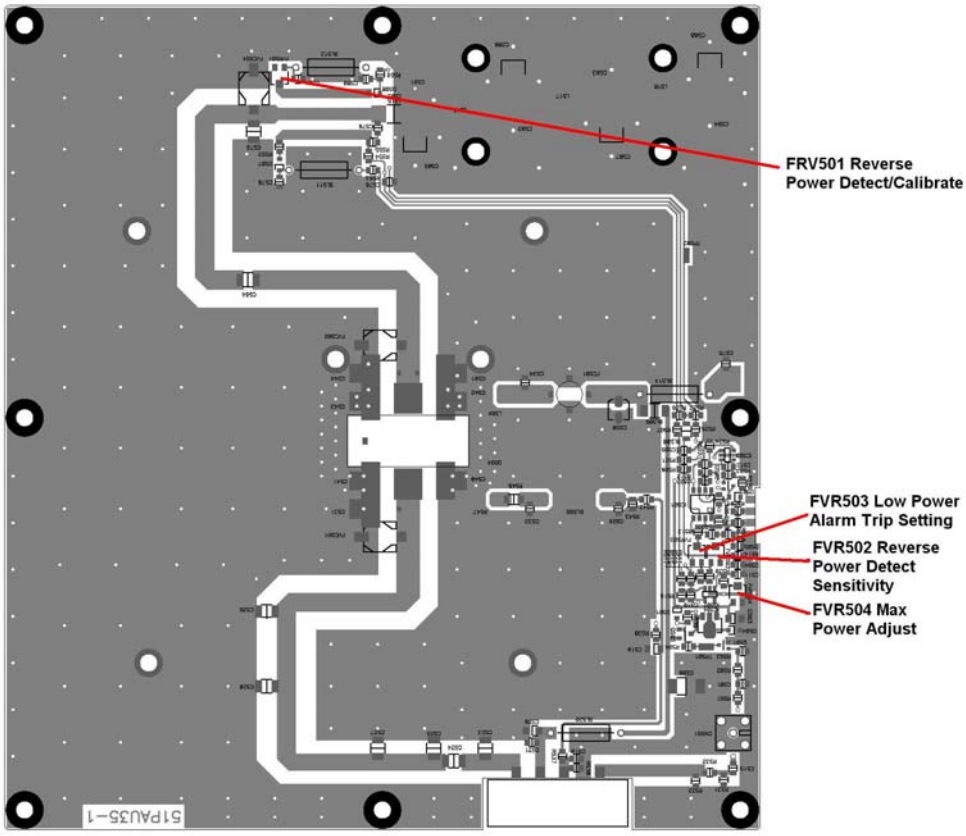
POWER AMPLIFIER 25-50 Watt

1) FVR501 Reverse Power Calibration
   a. Connect 50Ω resistive load
   b. Monitor TP502
   c. Key the transmitter.
   c. Adjust FVR501 for minimum DC voltage when terminated into a 50 Ω load.

2) FVR502
FVR502 sets the point where reverse power is detected. This should only be adjusted if parts have been replaced or FVR502 has been disturbed. Radio must be operating at 460.000 MHz for this adjustment.
   a. Connect 50Ω load
   b. Key the transmitter and measure the station total DC current .
   c. Disconnect 50Ω load at N connector on rear of transceiver housing and key the transmitter.
   d. Adjust FVR502 for DC current level not exceeding the above measurement in step-3b.

3) FVR503
   FVR503 sets the point where a low-power-alarm is triggered.

4) FVR504
   FVR504 sets the maximum power from the power module, however, do not exceed 70 watts.
5) The Front Panel Pots (Marked H and L; through the front panel) Adjust High and Low Output power respectively. (See Analog Alignment)



POWER AMPLIFIER 50-100W

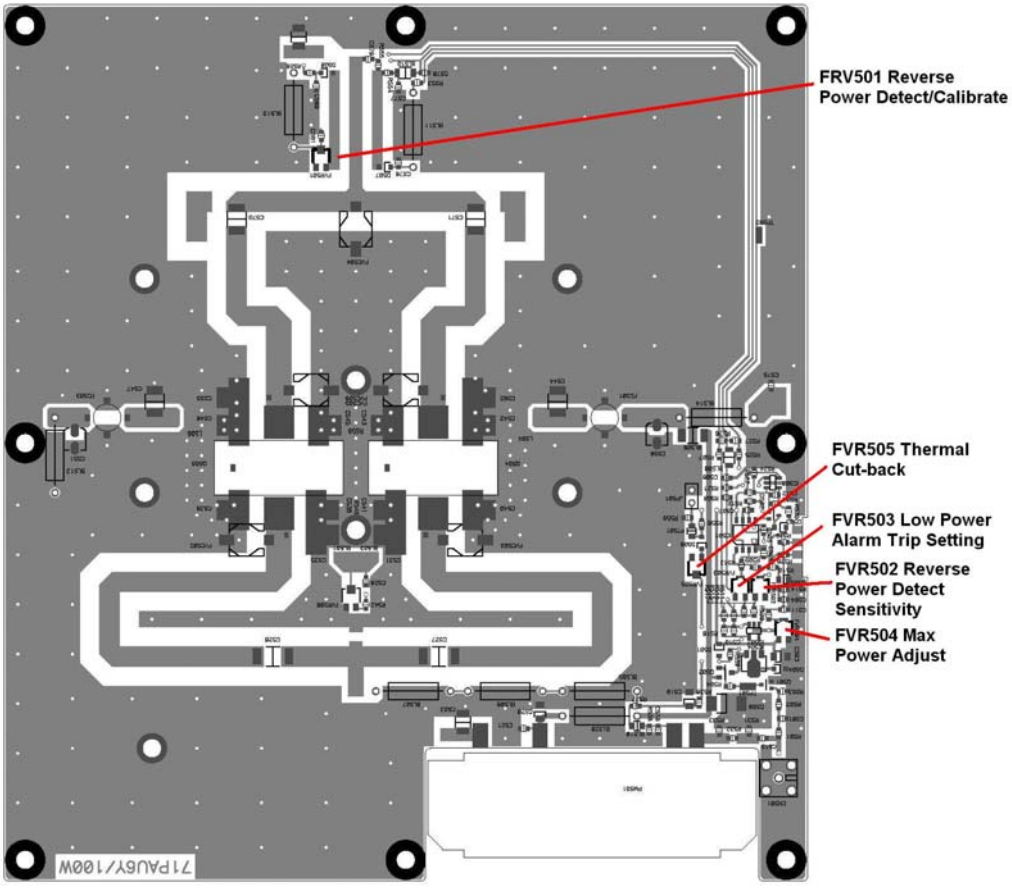
1) FVR501 Reverse Power Calibration
   a. Connect 50Ω resistive load
   b. Monitor TP502
   c. Key the transmitter.
   d. Adjust FVR501 for minimum dc voltage when terminated into a 50Ω load.

2) FVR502
FVR502 sets the point where reverse power is detected. This should only be adjusted if parts have been replaced or FVR502 has been disturbed. Radio must be operating at 460.000 MHz for this adjustment.
   a. Connect 50Ω load
   b. Key the transmitter and measure the station total DC current .
   c. Disconnect 50Ω load at N connector on rear of transceiver housing and key the transmitter.
   d. Adjust FVR502 for DC current level not exceeding the above measurement in step-3b.

3) FVR503
   FVR503 sets the point where a low-power-alarm is triggered.

4) FVR504
   FVR504 sets the maximum power from the power module, however, do not exceed 120 watts.

5) The Front Panel Pots (Marked H and L; through the front panel) Adjust High and Low Output power respectively (See Analog Alignment)



ANALOG LOGIC

1) VR401 Alignment
   This is to set volume level by pulse code switch. Press again and Noise Squelch can be set, press once again and then Display lighting level can be set.

2) FVR401 Alignment
   This is to set the Hi-Power-Level of the transmitter output power. Station will indicate ▶ ▶ in the right side of the display when in High power Mode. Press “SHIFT” + “2” to toggle Power Mode.

3) FVR402 Alignment
   This is to set the Low-Power-Level of the transmitter output power. The station must be on a low power channel or the station must be placed in the Low Power Mode.
   Press “SHIFT” + “2” to toggle Power Mode.

DIGITAL LOGIC

The digital logic section has no physical points to adjust or tune.

DESCRIPTION OF CIRCUITS TO STABILIZE TX AND RX FREQUENCY

The transmitter and receiver each use a TCVXO (Temperature and Voltage Controlled Crystal Oscillator) to generate 12.00MHz reference frequency for the respective PLL and VCO circuits. The accuracy of the TCVXO is less than +/- 0.00015% over the range of –30 degree C and +60 degree C.

DESCRIPTION OF CIRCUIT TO SUPPRESS SPURIOUS EMMISSIONS AND MODULATION LIMITING

A multiple pole Low Pass Filter is used after the final power amplifier stage.
It is designed to sharply attenuate spurious and harmonics frequencies above the highest frequency in the sub-band of the radio.

Modulation limiting is performed by TX audio processor AK2344 located in the analog logic part. Internal limiting/compression amplifier provides excellent limiting with minimum distortion.

In addition to modulation limiting, this device contains all circuitry to perform Pre-emphasis, band pass shaping and CTCSS encoder.

CIRCUIT DESCRIPTION

RECEIVER

1) RF Section
   An incoming signal is fed to pre-selector, and amplified by Q861, then fed to post-selector. The balanced mixer, consisting of IC811produces 73.35MHz by injection from the 1st local signal provided by RX VCO.
2) IF Section
   The output signal from the mixer is fed to the crystal filter (XF801), then amplified by Q810. Again, this signal is fed to the 4-pole crystal filters and amplified by Q001. After amplified by Q001, signal is fed to the 2nd IF processor (IC001). The 2nd local crystal signal is fed to IC001 to produce the 2nd local signal (455KHz). IC001 amplifies the 2nd local signal and becomes an audio signal by detector circuit inclusive within IC001. Then, the audio signal is fed to the low-pass-filter inclusive in IC002, and fed to audio processor IC3.

3) VCO section
   The oscillator circuit produces the 1st local signal (Rx frequency – 73.35MHz).
   The 1st local signal is amplified by buffer (Q302), and again amplified by pre-amplifier (IC301) and post amplifier Q303. The amplified signal is fed to the balanced mixer.

4) PLL Section
   PLL IC inclusive with pre-scaler IC806 compares the phase between the VCO frequency and reference oscillator frequency (12.00MHz) by method of dividing the frequency, and produces VCO control signal. Then, this control signal is fed to the charge pump and fed to the low-pass-filter. The supply voltage of charge pump is multiplied by IC807 (to approx. 13V) to achieve greater S/N ratio.

TRANSMITTER

1) VCO Section
   The oscillator circuit generates transmitter frequency. Then this signal is fed to the 3-stage of amplifier, buffer amplifier Q302, pre-amplifier IC301 and post amplifier Q303 and lead to the final amplifier, and lead to the final amplifier.

2) PLL section
   Basically, the circuit description is the same as RX. The PLL IC inclusive with prescaler (IC208) compares the phase between VCO signal and reference oscillator frequency (12.00MHz) by method of dividing the frequency, and produces VCO control signal. Then this VCO control signal is fed to the charge pump, and fed to the low-pass-filter. The supply voltage of charge pump is amplified by IC210 (to approx. 13V) to achieve greater S/N ratio.

3) Modulation Section
   The modulation signal is fed to both VCO and the reference oscillator (TCVXO 12.00MHz), this permits very flat modulation characteristics against low frequency (DC). This is an advantage when BASE TECH III is used as a POCSAG transmitter.

4) TX Exciter Section
   The VCO signal is amplified by Q211 to achieve 80mW.

5) 100W PA Section

The 80 mW signal from TX Exciter stage is fed to PM501 to produce 10W output. Then, Q504 and Q505 amplify to 100W. This signal is fed to the Low-Pass- Filter to eliminate the harmonics and spurious frequencies. An APC circuit formed by IC502 stabilizes the output power at the set level. An IC501 protects the final stage transistors from the reverse power caused by a mismatched antenna system

6) 50W PA section

The 80 mW signal from TX Exciter stage is fed to PM501 to produce 10W output. Then, Q504 amplify to 50W.. Then, signal is fed to the LPF to eliminate the harmonics spurious frequencies. An APC circuit formed by IC502 stabilizes the output power at the set level. An IC501 protects the final stage transistors from the reverse power caused by a mismatched antenna system

ANALOG LOGIC

Microcomputer (CPU) Section

CPU IC1, H8S2239 is the 16-bit processor contained 320kb flash memory 6k RAM inside. The CPU controls all functions of BASE TECH III. A flash memory permits on-board-up-grade when new firmware is released.

EEROM Section

IC6 is the 64k bit EEROM. This memory contains all the channel data.

Audio Processor Section

IC2 is for TX and IC3 is for Rx audio processors. IC28 is for CTCSS and IC29 is for DCS processor.

DIGITAL LOGIC

IC1 acts as the DSP control for both incoming digital signal converting it to analog and analog signal to C4FM digital signal. External flash memory within IC2, has 4Mb capacity, contains all data. A memory inclusive with IC1 (256k) has all program data.

FRONT CONTROL PANEL

1) LCD Display Section
   LCD display is constructed by 20 characters x 4 lines. Each characters consist of 7x8 matrix.

2) LED Display Section
   The 5 LED's are indicating each mode of operation BASE TECH III works.

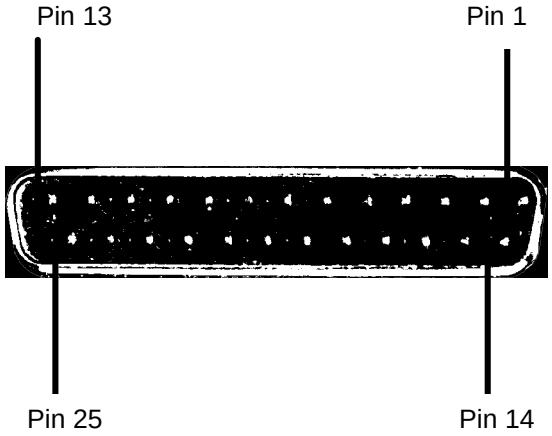
3) Audio Amplifier Section
   IC402 has 5 W power into a 8Ω impedance speaker.

4) Microphone Pre-Amplifier Section
   IC411 is the voice pre-amplifier having –30dBm output to feed TX modulator.

REMOTE CONTROL

25 pin D-sub connector for remote control is provided on the rear panel of Base Tech III. The functions of each pin are as follows:

Pin No.	Name	Description	I/O	Levels	Comments
1	CH0	LSB external binary channel selection	I	0-+3.3VDC	0000 is channel 1
2	CH1	External binary channel selection	I	0-+3.3VDC	
3	CH2	External binary channel selection	I	0-+3.3VDC	
4	CH3	MSB External binary channel selection	I	0-+3.3VDC	1111 is channel 16
5	Unassigned				
6	REM MON	Remote Monitor	I	0-+3.3VDC	+3.3V=Monitor On
7	GND	Ground			
8	Unassigned				
9	Unassigned				
10	DEM OUT	Discriminator audio out	O	≈330mVrms 1KHz @ ±3KHz	C4FM on DIG
11	BUSY	Channel busy indication	O	0-+3.3VDC	+3.3V=busy
12	RSSI	Receive signal strength indicator	O	0-+2.5VDC analog	
13	MOD1	External audio modulation input	I	≈50mVrms 1Khz for ±3KHz	
14	GND	Ground			
15	PTT	Push to talk	I	0-+3.3VDC	0V=transmit
16	MOD2	External modulation input LOW FREQ i.e. CTCSS/DCS IN	I	≈400mVrms 1KHz for ±3KHz	After limiter and filtering
17	SIMP	Simplex mode selected	O	0-+3.3VDC	0V=simplex
18	ERR	Alarm indication	O	0-+3.3VDC	Duty Cycle Determines which alarm
19	DECODE	Decode valid indication	O	0-+3.3VDC	5V=valid signaling
20	RX AUD1	Buffered receive audio	O	≈700mVrms 1KHz @ ±3KHz	1 & 2 Can produce 0 dBm into
21	RX AUD2	Buffered receive audio	O	≈700mVrms 1KHz @ ±3KHz	600 ohm input
22	TX OUT		O		
23	EXT PW/SW	External power switch	I	0-Open source	0V=ONf
24	REMOTE	External channel selection mode	I	0-+3.3VDC	0V=external
25	*+12V*				



Rear Panel View