Necessary Explanations to present to TELEC for certification.

1. **Outline of Design and Development**

We need more explanations in details in writing with describing exact names of parts and numerical values.

1) How "Stability of Frequency" is designed ?

We design and control the frequency stability by Phase-locked-loop control implemented in the Synthesizers contained in the *HFA3683 RF-IF converter IC, U21*, and the *HFA3783 IQ Modulator and demodulator IC, U14*. VCO's (*DMP-VCX2074, U23 for RF, DMP-VCX743, U15 for IF*) feed the LO to the synthesize and their frequencies are compared to reference clock with temperature-guaranteed stability of +/-25ppm with a stabilized power supply.

2) How "Spurious Emissions" is suppressed ?

Components of Spurious are few due to the fact that we design to get the Transmission Frequency directly from the output of VCO, and in addition we suppress the emission from antenna by inserting BPF (SAW filter, FL1 for the IF) and *two* BPF in the RF transmission chain--*FL4* before the PA and *FL3* between the PA and the antenna..

3) How "Frequency Modulation" is controlled and limited ?

We utilized the balanced differential analog signals from the accurate transmit DAC inside the DSS Base Band Processor *HFA3861, U10* .as the input to the IQ modulator inside *HFA3783, U14*. In addition, this signal is dc-coupled and digitally filtered. The combined accuracy in the IQ input and the base-band filtering keeps the spread bandwidth constant.

4) How "Transmit Power" is controlled and limited ?

We design to stabilize the Transmission Power by reading the power level from the voltage of a *detector* integrated with *the Power Amp IC, HFA3983, U24* and then adjust the drive amp gain to maintain a constant transmission power.

5) How "secondarily emitted radio wave from Receiver" is suppressed ?

We implemented automatic gain control (AGC) for the receiving circuit. The AGC works to keep the amplitude of the received signal constant along the receiving chain to minimize spurious signal growth due to the non-linearity of the components of the receiving circuit.

2. **Considerations to environment of use.**

We need more explanations in details with describing exact names of parts and numerical values.

1) Temperature Test : ETSI 300 328 tested at–0°C to +55C

2) Humidity Test ETSI 300 019 tested for 5 days at >92% RH at 50°C

3. **Designed Specifications and Acceptable Technical Reference Specifications**

(1) Transmitter

* Frequency Tolerance
  Designed value : < ±25 ppm
  Technical reference ETS 300 328
* Occupied Frequency Bandwidth Tolerance
  Designed value : Fcenter ± 13MHz at –25dBc points
  Technical reference : FCC part 15.247
* Spreading bandwidth
  Designed value : 11 MHz at –10dB
  Technical reference : FCC part 15.247
* Spreading Factor.
  Value : 11 Mchips/sec at 1.375 Msymbols/sec at 11 mbps datarate.
* Spurious Emission Strength
  Designed value : in compliance with ETS 300328 and FCC part 15.247
  Technical reference: ETS 300328 and FCC part 15.247
* Antenna Power and its tolerance
  Design value : +13.6dBm +1dB, -2dB
  Technical reference : ETS 300 328 and FCC part 15.247
* Emitted power to adjacent channel
  Design value : < -30 dBc
  Technical reference : FCC part 15.247

(2) Receiver

* Secondarily emitted radio wave strength
  Designed value : in compliance with ETS 300328 and FCC part 15.247
  Technical reference: ETS 300328 and FCC part 15.247

4. **Explanations of Operations at every part (section) based on Block Diagram.**

See attached data sheets in pdf format for an example.